ESD/Surge Protection Diode Array

Bi-directional ESD Protection for High-Speed Data Line

SMDA05C Series

The SMDA05C surge protection series is designed to protect equipment attached to up to four high speed communication lines from ESD, EFT and surge.

Features

- SO−8 Package
- Peak Power − 300 W 8 x 20 μs
- ESD Rating:
  IEC 61000−4−2 (ESD) ±15 kV (Air) ±8 kV (Contact)
  IEC 61000−4−4 (EFT) 40 A (5/50 ns)
  IEC 61000−4−5 (Surge) 12 A (8/20 μs)
- UL Flammability Rating of 94 V−0
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Speed Communication Line Protection
- Data and I/O Lines
- Microprocessor Based Equipment
- LAN/WAN Equipment
- Servers
- Notebook and Desktop PC
- Serial and Parallel Ports
- Peripherals

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μs @ T_A = 25°C (Note 1)	P_{pk}	300	W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum 10 Seconds Duration	T_L	260	°C

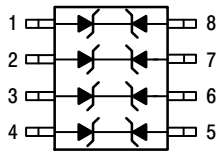
1. Non−repetitive current pulse 8 x 20 μs exponential decay waveform.

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SO−8
ESD AND SURGE PROTECTOR
300 WATTS PEAK POWER

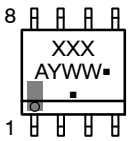
PIN CONFIGURATION AND SCHEMATIC





SO−8
CASE 751−07

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

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SMDA05C ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	–	–	5.0	V
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	6.0	–	–	V
Reverse Leakage Current @ V_{RWM} = 5 Volts	I_R	N/A	–	20	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μs	V_C	N/A	–	9.8	V
Maximum Clamping Voltage @ I_{PP} = 5.0 A, 8 x 20 μs	V_C	N/A	–	11	V
Maximum Peak Pulse Current, 8 x 20 μs	I_{PP}	–	–	17	A
Junction Capacitance @ V_R = 0 V, f = 1 MHz	C_J	–	–	350	pF

SMDA12C ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	–	–	12	V
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	13.3	–	–	V
Reverse Leakage Current @ V_{RWM} = 12 Volts	I_R	N/A	–	1.0	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μs	V_C	N/A	–	19	V
Maximum Clamping Voltage @ I_{PP} = 5.0 A, 8 x 20 μs	V_C	N/A	–	24	V
Maximum Peak Pulse Current, 8 x 20 μs	I_{PP}	–	–	12	A
Junction Capacitance @ V_R = 0 V, f = 1 MHz	C_J	–	–	120	pF

SMDA15C ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	–	–	15	V
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	16.7	–	–	V
Reverse Leakage Current @ V_{RWM} = 15 Volts	I_R	N/A	–	1.0	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μs	V_C	N/A	–	24	V
Maximum Clamping Voltage @ I_{PP} = 5.0 A, 8 x 20 μs	V_C	N/A	–	30	V
Maximum Peak Pulse Current, 8 x 20 μs	I_{PP}	–	–	10	A
Junction Capacitance @ V_R = 0 V, f = 1 MHz	C_J	–	–	75	pF

SMDA24C ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	–	–	24	V
Reverse Breakdown Voltage @ I_t = 1.0 mA	V_{BR}	26.7	–	–	V
Reverse Leakage Current @ V_{RWM} = 24 Volts	I_R	N/A	–	1.0	μA
Maximum Clamping Voltage @ I_{PP} = 1.0 A, 8 x 20 μs	V_C	N/A	–	43	V
Maximum Clamping Voltage @ I_{PP} = 5.0 A, 8 x 20 μs	V_C	N/A	–	55	V
Maximum Peak Pulse Current, 8 x 20 μs	I_{PP}	–	–	5.0	A
Junction Capacitance @ V_R = 0 V, f = 1 MHz	C_J	–	–	50	pF

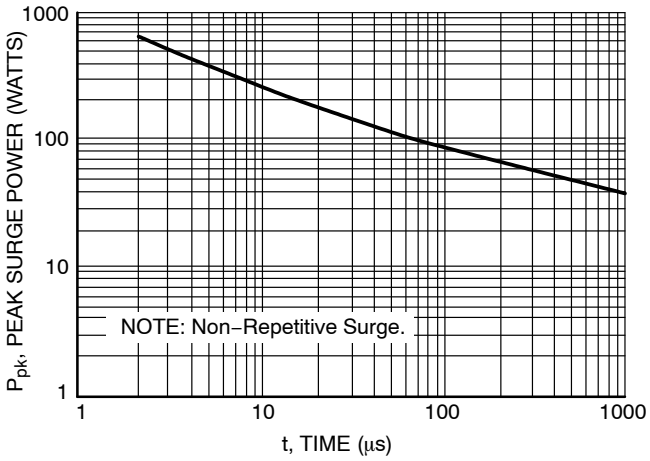


Figure 1. Pulse Width

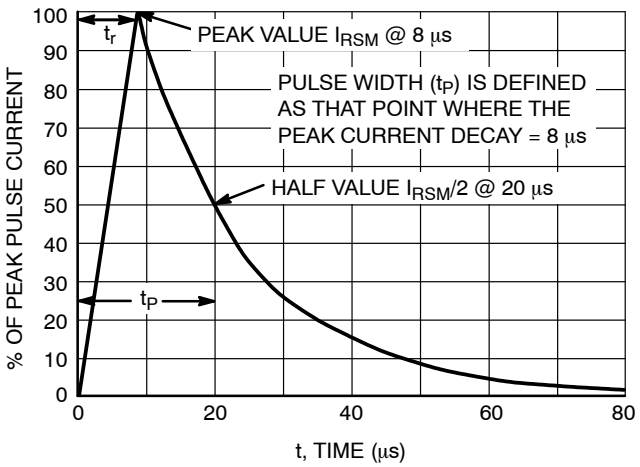


Figure 2. 8 × 20 μs Pulse Waveform

ORDERING INFORMATION

Device	Marking	Package	Shipping†
SMDA05CDR2G	AAA	SO−8 (Pb−Free)	2500 / Tape & Reel
SMDA12CDR2G	AAC	SO−8 (Pb−Free)	2500 / Tape & Reel
SMDA15CDR2G	AAD	SO−8 (Pb−Free)	2500 / Tape & Reel
SMDA24CDR2G	AAE	SO−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

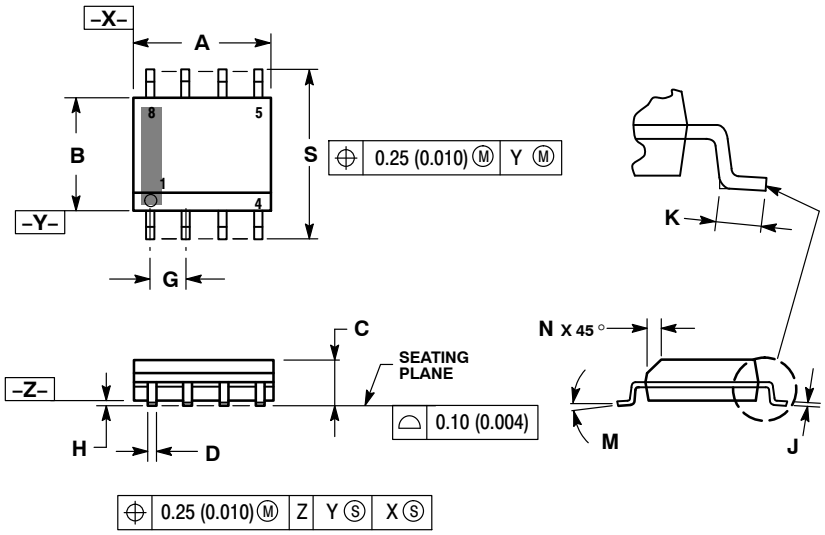
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

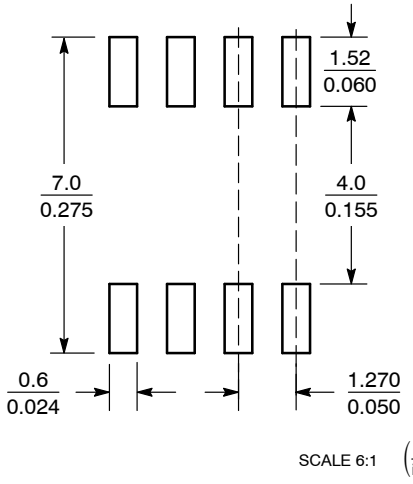
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

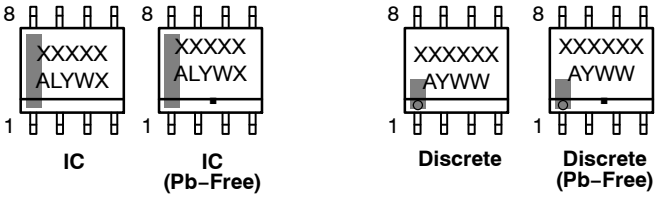
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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