Keywords: sinewave generators, low-distortion signal generators, crystal-stabilized oscillators, ring counters, weighted-resistance networks, lowpass elliptic filters, switched-capacitor filters

APPLICATION NOTE 4547

Low-Cost Circuit Converts Clock to Low-Distortion Sinewave

By: Leo Sahlsten
Dec 21, 2010

Abstract: This circuit derives a pure sinewave from a crystal-controlled clock source by using a ring counter to remove the highest-amplitude unwanted harmonics, and filtering the result with an 8th-order lowpass, switched-capacitor elliptic filter (MAX7400).

A similar version of this article appeared in the October 2007 issue of *PD* magazine.

A simple, low-cost circuit (**Figure 1**) uses the existing clock in a digital system to generate low-distortion audio signals. Because most digital-system clocks are derived from crystal oscillators, those clocks produce stable and accurate sinewaves.

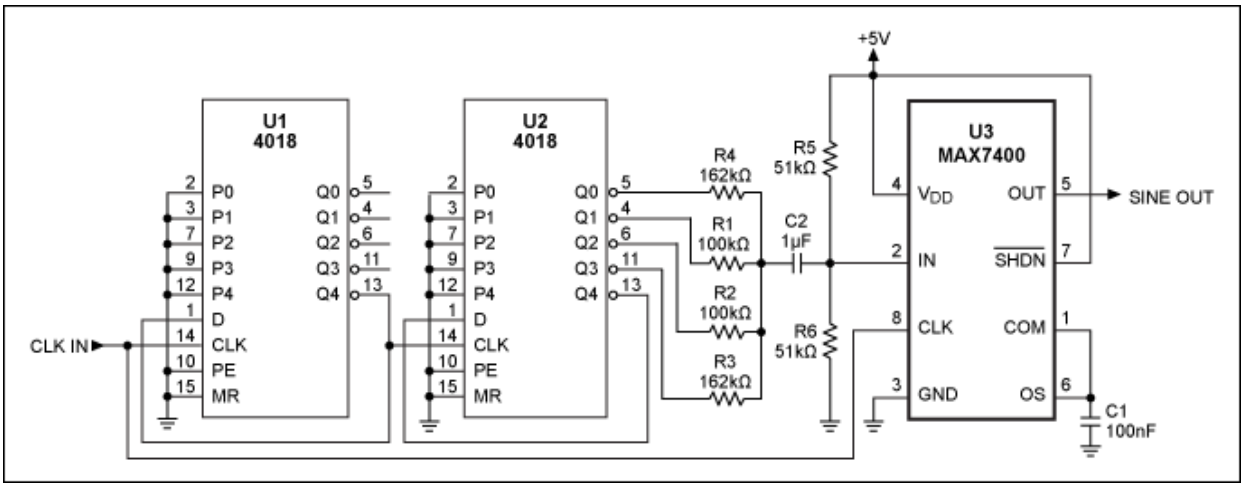

Figure 1. This inexpensive circuit derives a low-distortion sinewave from a 50%-duty-cycle clock signal.

The most obvious approach is to divide the clock frequency down to the required audio frequency, and then filter out the harmonics. A squarewave of 50% duty cycle, for instance, contains only odd harmonics (3rd, 5th, 7th, etc.), and their amplitudes decrease with frequency. The 3rd-harmonic amplitude is 1/3 that of the fundamental, the 5th is 1/5 that of the fundamental, and so on.

Filter circuits give better results if you first attenuate the input signal's highest-amplitude unwanted harmonics. This job is easily accomplished with a ring counter (U2) and a simple weighted-resistance network that attenuates all harmonics below the 9th by at least 70dB (**Figure 2**). An 8th-order lowpass, switched-capacitor elliptic filter (U3, MAX7400) removes most of the remaining harmonics. U3's corner frequency is set by the input clock as

$f_{CLOCK}/100$.

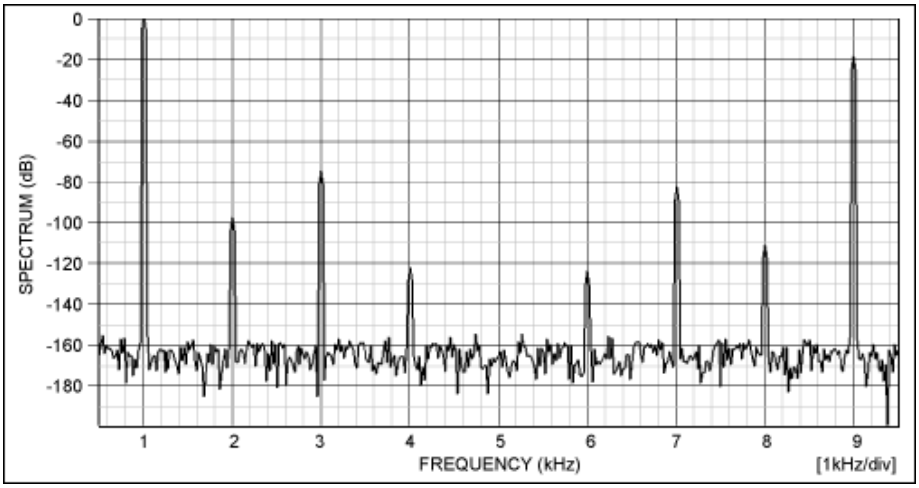

Figure 2. A simple resistance network in the Figure 1 circuit (R1–R4) greatly reduces harmonic distortion below the 9th harmonic.

Ring counter U1 divides the incoming CMOS-level clock signal by ten. The second ring counter (U2) also divides the clock by ten, but its outputs are summed by a weighted-resistance network to produce a 9-step approximation of a sinewave. That waveform is further filtered by U3, which attenuates all harmonics below the noise level. The circuit's input signal (clk in) serves as a clock for U3. To achieve the lowest distortion, U3's input should be biased to $V_{DD}/2$, and its input signal attenuated to 2.2V peak. This attenuation is accomplished with a voltage divider consisting of the weighting network's output resistance and the filter IC's input resistance (R5 and R6 in parallel). Below 10kHz, the circuit shown achieves distortion levels below 0.01%.

Related Parts		
MAX7400	8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters	Free Samples

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