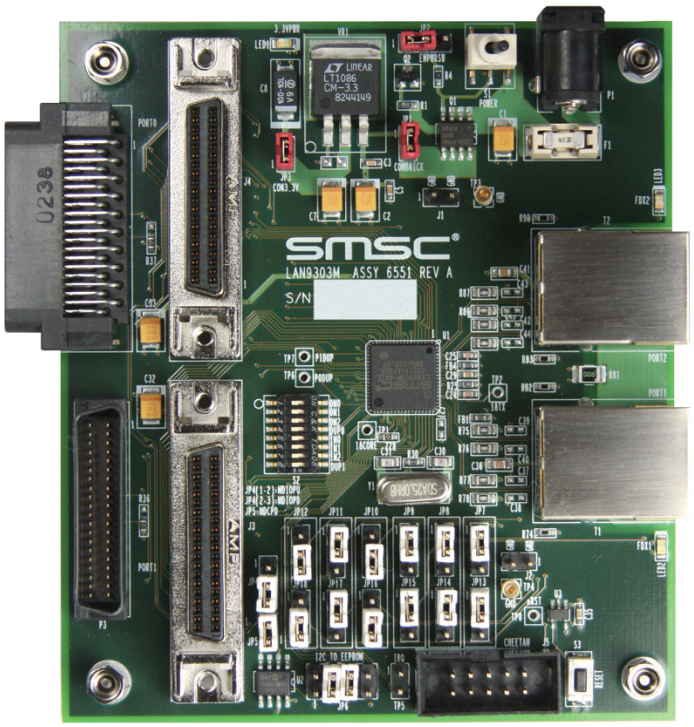
LAN9303M Evaluation Board User Manual



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1 Introduction

The LAN9303M is a full featured, three-port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9303M combines all the functions of a 10/100 Ethernet switch system, including the Switch Fabric, packet buffers, Buffer Manger, MACs, PHY transceivers, and serial management. The LAN9303M complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

The EVB9303M is an Evaluation Board (EVB) that utilizes the LAN9303M to provide a fully functional three-port dual MII/RMII/Turbo MII Ethernet switch. The EVB9303M provides two fully integrated MAC/PHY Ethernet ports (Ports 1 & 2) via on-board RJ45 connectors. Port 0 and Port 1 each provide two MII port connectors (for a total of 4) which support the following:

- An external MII-/RMII-/Turbo MII-capable MAC (with LAN9303M in PHY mode), via the onboard 40-pin male MII connector
- An external MII-/Turbo MII-capable PHY (with LAN9303M in MAC mode), via the onboard 40-pin female MII connector

The Port 0 and Port 1 modes of operation are configured via a single, 8-position, mode-configuration strap switch.

Power is supplied to the board via a +5V external wall-mount power supply. The external supply is not necessary when Port 0 or Port 1 is configured for (and used in) PHY mode. In such cases, the +5V power rail is typically supplied through the MII connector from the MAC side.

The EVB9303M includes a 8Kx8 I^{2}C EEPROM that may be used to automatically load configuration settings from the EEPROM into the device at reset, allowing the device to operate unmanaged. An I^{2}C host adapter interface header (10-pin, 2x5) is provided to simplify I^{2}C based configuration. A simplified block diagram of the EVB9303M can be seen in Figure 1.1.

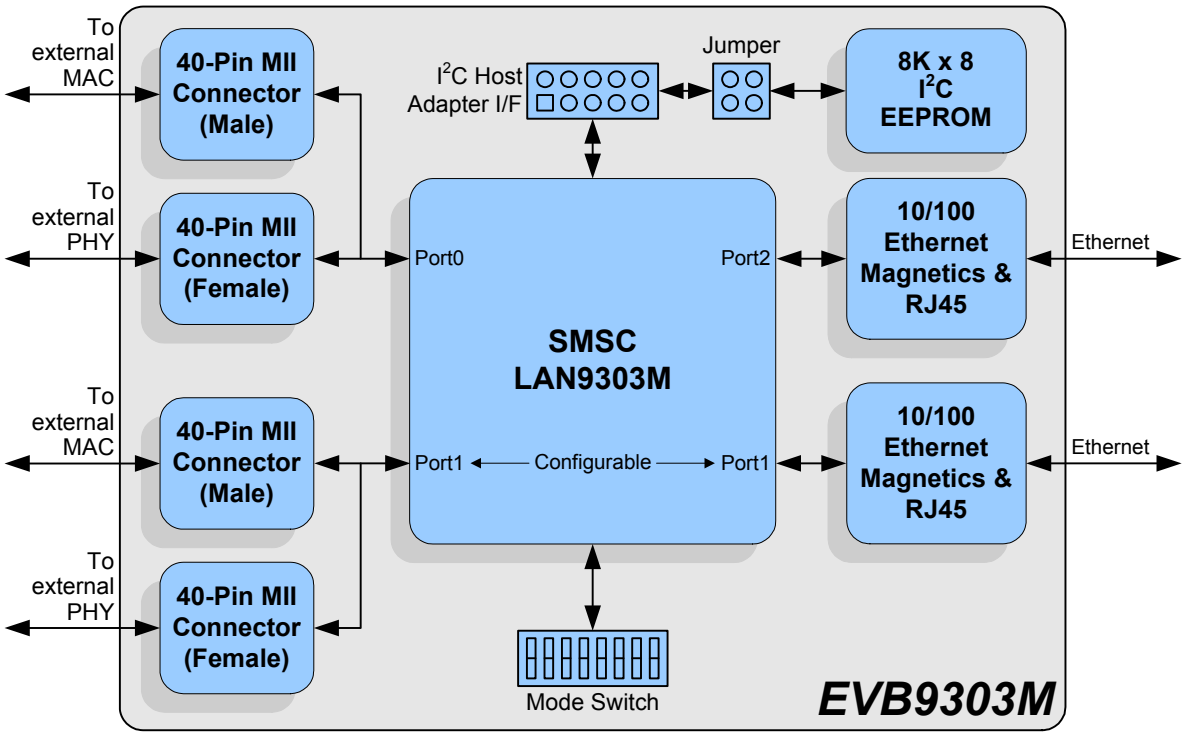


Figure 1.1 EVB9303M Block Diagram

1.1 References

Concepts and material available in the following documents may be helpful when using the EVB9303M.

Table 1.1 References

DOCUMENT	LOCATION
SMSC LAN9303M Datasheet	http://www.smsc.com/main/datasheet.html
AN8-13 Suggested Magnetics	http://www.smsc.com/main/appnotes.html
SMSC EVB9303M Evaluation Board Schematic	http://www.smsc.com/

2 Board Details

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the EVB9303M is shown in Figure 2.1.

Note: The LAN9303M device is RoHS compliant. However, support components on the EVB9303M board are not necessarily RoHS compliant.

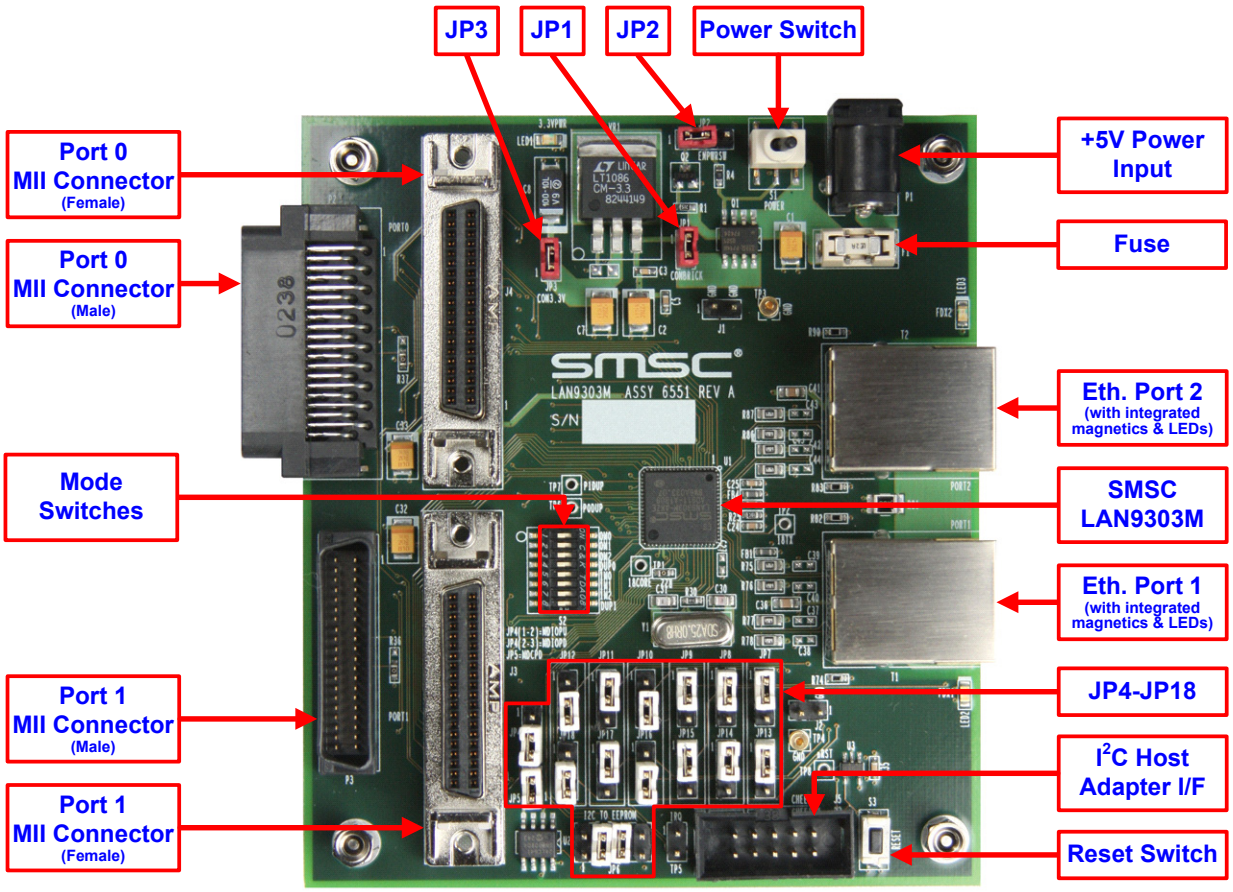


Figure 2.1 EVB9303M Top View

2.1 Jumpers

The following tables describe the default settings and jumper descriptions for the EVB9303M. These defaults are the recommended configurations for evaluation of the LAN9303M. These settings may be changed as needed, however, any deviation from the default settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

Note: A dashed line in the *Settings* column indicates the board's default jumper setting.

2.1.1 JP1 - JP6

Table 2.1 Jumpers JP1 - JP6

JUMPER	DESCRIPTION	SETTINGS	
JP1	Connect +5V DC power supply	1---2	**IN:** Connect +5V brick output to power plane **OUT:** Disconnect +5V brick power
JP2	Power switch enable jumper	1---2	Enable power switch
		2 3	Disable power switch, force power ON always
JP3	Connect +3.3V jumper	1---2	**IN:** Connect +3.3V regulator output to +3.3V power plane **OUT:** Disconnect +3.3V regulator
JP4	MDIO pull-up/down jumper	1---2	Connect MDIO to 1.5K pull-up to +3.3V
		2 3	Connect MDIO to 2.5K pull-down to GND
JP5	MDC pull-down jumper	1---2	**IN:** Connect MDC to 10K pull-down **OUT:** Disconnect MDC from 10K pull-down
JP6	I^2C connect jumper	1 2	Pins 1 and 2 are +3.3V
		3---4	Connect I^2C EEPROM to SDA
		5---6	Connect I^2C EEPROM to SCL
		7---8	Pins 7 and 8 are GND

2.1.2 JP7 - JP18

Jumpers JP7 through JP18 set various functions of the LAN9303M. They can also be used as GPIOs, LED drivers, or interrupts. When used as LED drivers, as they are on the EVB9303M, they are connected a specific way to set the strap value to a "1", and another way to set the strap value to a "0". Figure 2.2 illustrates the schematic connections with the LED1 circuit as a pull-up, and the LED2 circuit as a pull-down. To illuminate LED1, the LAN9303M will drive the cathode of the LED1 low. To illuminated LED2, the LAN9303M will drive the anode of the LED2 high.

The JP7 - JP18 jumpers must be configured in pairs to identical settings in order to realize the LED1 circuit or the LED2 circuit. The pairings are as follows:

- JP7 & JP13
- JP8 & JP14
- JP9 & JP15
- JP10 & JP16

- JP11 & JP17
- JP12 & JP18

The following subsections detail the jumper pair settings, their associated strap settings, and the functional effects of setting the straps. All strap values are read during power-up and on the rising edge of the nRST signal. Once the strap value is set, the LAN9303M will drive the LEDs high or low for illumination according the strap value. For other designs which may use these pins as GPIOs or interrupts, refer to the LAN9303M datasheet for additional information. In those cases, internal default straps must be changed by an I^2C or SMI master or through EEPROM fields.

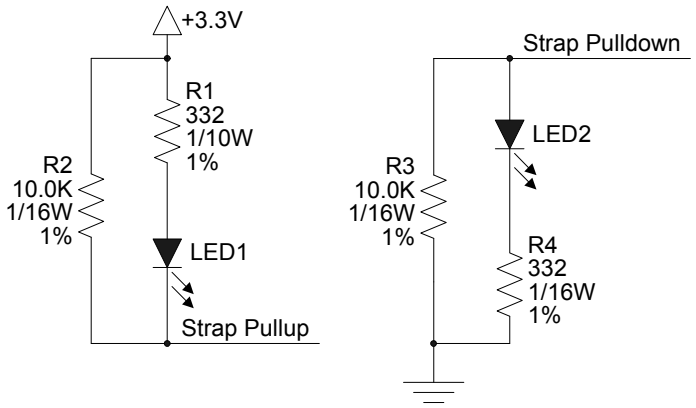


Figure 2.2 LED Strap Circuit

2.1.2.1 Auto-MDIX / EEPROM Jumpers

Table 2.2 Jumpers - Auto-MDIX / EEPROM

JUMPER PAIR	DESCRIPTION	SETTINGS	
JP7, JP13	Port 1 Auto-MDIX enable/disable (Note 2.1)	1---2	Enable Auto-MDIX on Port 1
		2 3	Disable Auto-MDIX on Port 1
JP8, JP14	Port 2 Auto-MDIX enable/disable (Note 2.1)	1---2	Enable Auto-MDIX on Port 2
		2 3	Disable Auto-MDIX on Port 2
JP9, JP15	EEPROM size jumper (Note 2.1, Note 2.2)	1---2	Enable 4Kx8 and larger I^2C EEPROMs
		2 3	Enable 2Kx8 and smaller I^2C EEPROMs

Note 2.1 Paired jumpers *MUST* be set identically.

Note 2.2 The EVB9303M uses an 8Kx8 EEPROM. Therefore, this jumper *MUST* be set to 1-2.

2.1.2.2 Serial Management Jumpers

Table 2.3 Jumpers - Serial Management

JUMPER PAIR	DESCRIPTION	SETTINGS	
JP10, JP16	Serial management MNGT0 jumper (Note 2.3, Note 2.4)	1 2	Set MNGT0 to “1”
		2---3	Set MNGT0 to “0”
JP11, JP17	Serial management MNGT1 jumper (Note 2.3, Note 2.4)	1---2	Set MNGT1 to “1”
		2 3	Set MNGT1 to “0”

Note 2.3 Paired jumpers *MUST* be set identically.

Note 2.4 The MNGT[1:0] settings are defined in Table 2.4:

Table 2.4 MNGT[1:0] Settings

MNGT1	MNGT0	SERIAL MANAGEMENT SETTING
0	0	RESERVED
0	1	SMI
1	0	I^2C (Default)
1	1	RESERVED

2.1.2.3 PHY Port Address Jumpers

Table 2.5 Jumpers - PHY Port Address

JUMPER PAIR	DESCRIPTION	SETTINGS	
JP12, JP18	PHY address jumpers (Note 2.5, Note 2.6)	1 2	Set PHY_ADDR to “1”
		2---3	Set PHY_ADDR to “0”

Note 2.5 Paired jumpers *MUST* be set identically.

Note 2.6 The PHY_ADDR settings are defined in Table 2.6:

Table 2.6 PHY_ADDR Settings

PHY_ADDR STRAP VALUE	VIRTUAL PHY ADDRESS	PORT 1 ADDRESS	PORT 2 ADDRESS
0	0	1	2
1	1	2	3

2.2 LEDs

Table 2.7 LEDs

REFERENCE	COLOR	INDICATION (Note 2.7)
LED1	Green	+3.3V power active
LED2	Green	Full-duplex/Collision Port 1
LED3	Green	Full-duplex/Collision Port 2
T1	Green	Link/Activity Port 1
	Yellow	Speed Port 1
T2	Green	Link/Activity Port 2
	Yellow	Speed Port 2

Note 2.7 Assumes the LED_FUN field of the LED_CFG register is 00b.

2.3 Test Points

Table 2.8 Test Points

TEST POINT	DESCRIPTION	CONNECTION
TP1	Single pin unpopulated VDD18CORE	VDD18CORE
TP2	Single pin unpopulated VDD18TX	VDD18TX
TP3	Single pin populated gold post GND testpoint	GND
TP4	Single pin populated gold post GND testpoint	GND
TP5	2-pin populated IRQ testpoint with GND	**Pin 1:** IRQ **Pin 2:** GND
TP6	Single pin unpopulated P0_DUPLEX	P0_DUPLEX
TP7	Single pin unpopulated P1_DUPLEX	P1_DUPLEX
TP8	Single pin unpopulated nRST	nRST

2.4 System Connections

Table 2.9 System Connections

PLUG/HEADER	DESCRIPTION	PART
J1	2-pin populated GND header	2-pin (1x2) header
J2	2-pin populated GND header	2-pin (1x2) header
J3	MII female connector for external PHY	AMP/Tyco 749069-4
J4	MII female connector for external PHY	AMP/Tyco 749069-4
J5	I^2C host adapter interface connector	Adam Tech BHR-10-V-U-A
P1	+5V DC power connector	Barrel plug, 2.0mm, center positive
P2	MII male connector for external MAC	AMP/Tyco 174218-2
P3	MII male connector for external MAC	AMP/Tyco 5174216-2

2.5 Switches

This section details the various EVB9303M power, mode, and reset switches.

2.5.1 Power

Table 2.10 Power Switch

SWITCH	DESCRIPTION	FUNCTION
S1	SPDT tiny toggle power switch	Connects +5V brick power to board

Note: The EVB9303M includes a 2A fuse (F1) to protect from overcurrrent conditions. If this fuse becomes damaged, it can be replaced with a 2A Littlefuse-154002.

2.5.2 Port 0 Mode

Table 2.11 Port 0 Mode Switches

SWITCH	DESCRIPTION	FUNCTION
S2-1	8-position DIP switch, position 1	Sets P0_MODE0 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.8, Note 2.9)
S2-2	8-position DIP switch, position 2	Sets P0_MODE1 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.8, Note 2.9)
S2-3	8-position DIP switch, position 3	Sets P0_MODE2 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.8, Note 2.9)
S2-4	8-position DIP switch, position 4	Sets P0_MODE3 low when closed (on). Otherwise, the signal is pulled-up internally. This switch selects the duplex polarity strap default for Port 0 as follows: If the strap value is “0”, a “0” on P0_DUPLEX indicates full duplex, while a “1” indicates half-duplex. If the strap value is “1”, a “1” on P0_DUPLEX indicates full duplex, while a “0” indicates half-duplex. The default setting is open.

Note 2.8 There are no default setting for this switch. Customers must choose the appropriate MII mode as dictated by their application.

Note 2.9 The P0_MODE[2:0] settings are defined in Table 2.12:

Table 2.12 P0_MODE[2:0] Settings

S2-3	S2-2	S2-1	PORT 0 MODE SETTINGS
0	0	0	MII MAC Mode
0	0	1	MII PHY Mode
0	1	0	MII PHY Mode / 200Mbps / 12mA clock output
0	1	1	MII PHY Mode / 200Mbps / 16mA clock output
1	0	0	RMII PHY Mode / 12mA clock output
1	0	1	RMII PHY Mode / 16mA clock output
1	1	0	RMII PHY Mode / clock is input
1	1	1	RESERVED

2.5.3 Port 1 Mode

Table 2.13 Port 1 Mode Switches

SWITCH	DESCRIPTION	FUNCTION
S2-5	8-position DIP switch, position 5	Sets P1_MODE0 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.10, Note 2.11)
S2-6	8-position DIP switch, position 6	Sets P1_MODE1 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.10, Note 2.11)
S2-7	8-position DIP switch, position 7	Sets P1_MODE2 low when closed (on). Otherwise, the signal is pulled-up internally. (Note 2.10, Note 2.11)
S2-8	8-position DIP switch, position 8	Sets P1_MODE3 low when closed (on). Otherwise, the signal is pulled-up internally. This switch selects the duplex polarity strap default for Port 1 as follows: If the strap value is “0”, a “0” on P1_DUPLEX indicates full duplex, while a “1” indicates half-duplex. If the strap value is “1”, a “1” on P1_DUPLEX indicates full duplex, while a “0” indicates half-duplex. The default setting is open.

Note 2.10 There are no default setting for this switch. Customers must choose the appropriate MII mode as dictated by their application.

Note 2.11 The P1_MODE[2:0] settings are defined in Table 2.14:

Table 2.14 P1_MODE[2:0] Settings

S2-7	S2-6	S2-5	PORT 1 MODE SETTINGS
0	0	0	MII MAC Mode
0	0	1	MII PHY Mode
0	1	0	MII PHY Mode / 200Mbps / 12mA clock output
0	1	1	MII PHY Mode / 200Mbps / 16mA clock output
1	0	0	RMII PHY Mode / 12mA clock output
1	0	1	RMII PHY Mode / 16mA clock output
1	1	0	RMII PHY Mode / clock is input
1	1	1	Internal PHY Mode

2.5.4 Reset

Table 2.15 Reset Switch

SWITCH	DESCRIPTION	FUNCTION
S3	SW pushbutton	Reset: Generates nRST

2.6 Mechanicals

Figure 2.3 details the EVB9303M mechanical dimensions.

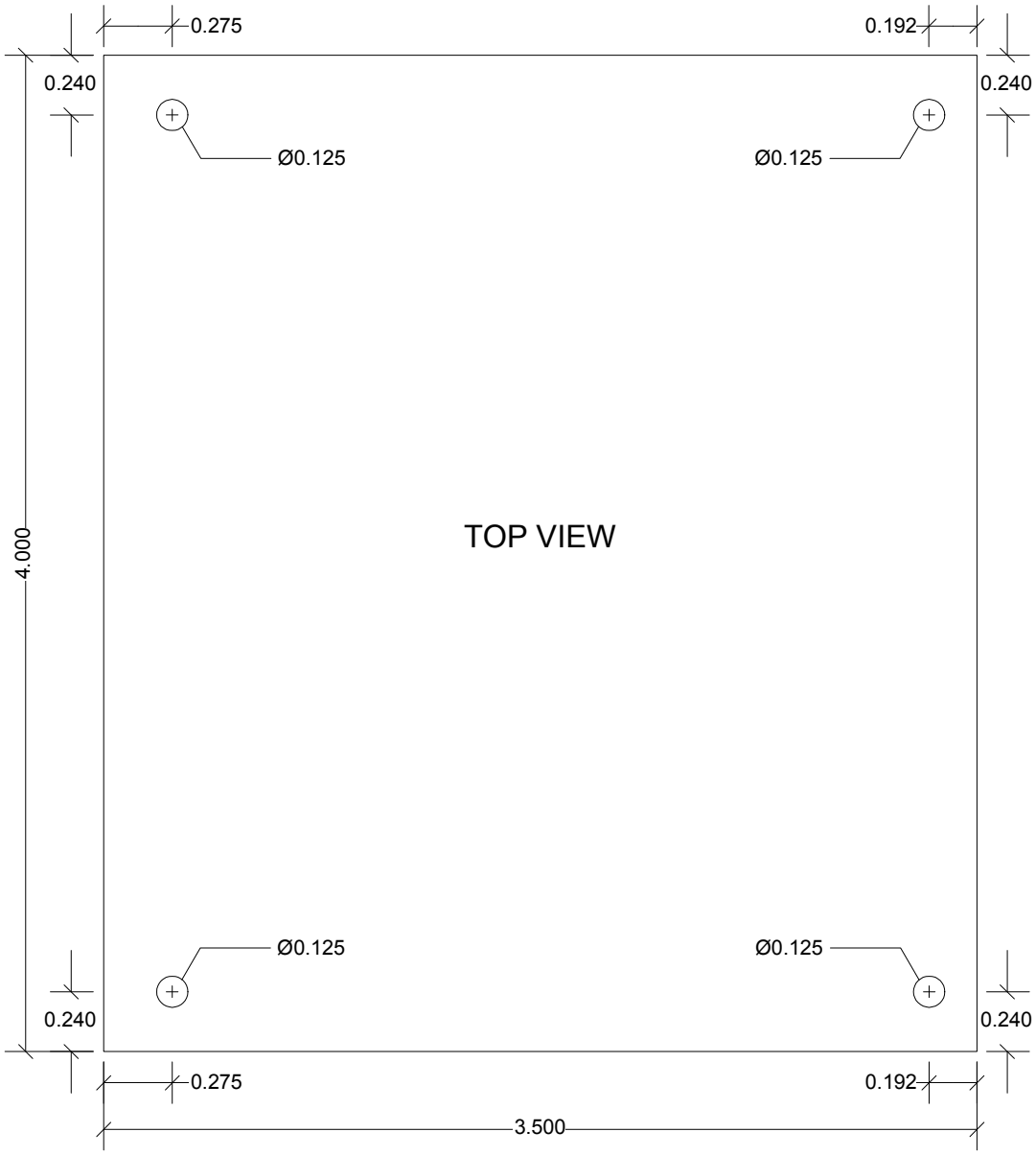


Figure 2.3 EVB9303M Mechanicals