HMC497LP4 / 497LP4E

v04.1108

SiGe WIDEBAND DIRECT MODULATOR RFIC, 100 - 4000 MHz

Typical Applications

The HMC497LP4(E) is ideal for:

- UMTS, GSM or CDMA Basestations
- Fixed Wireless or WLL
- ISM Transceivers, 900 & 2400 MHz
- GMSK, QPSK, QAM, SSB Modulators

Features

Very Low Noise Floor: -161 dBm/Hz

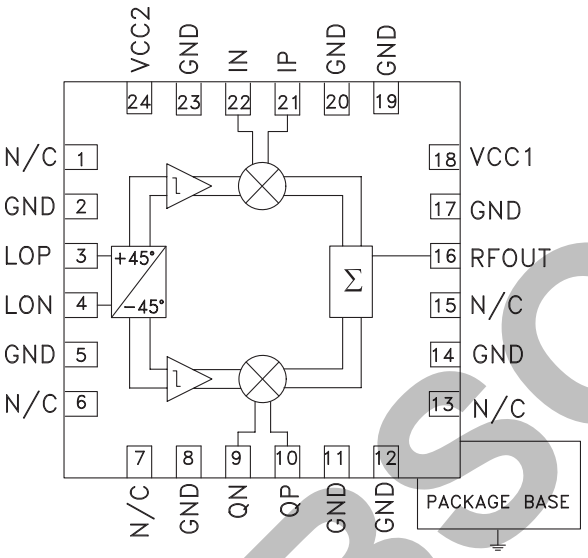
Very High Linearity: +22 dBm OIP3

High Output Power: +9 dBm Output P1dB

High Modulation Accuracy

DC - 700 MHz Baseband Input

Functional Diagram



General Description

The HMC497LP4(E) is a low noise high linearity Direct Quadrature Modulator RFIC which is ideal for digital modulation applications from 100 - 4000 MHz including; Cellular/3G, Broadband Wireless Access & ISM circuits. Housed in a compact 4x4 mm (LP4) SMT QFN package, the RFIC requires minimal external components & provides a low cost alternative to more complicated double upconversion architectures. The RF output port is single-ended and matched to 50 Ohms with no external components. The LO requires -6 to +6 dBm and can be driven in either differential or single-ended mode while the baseband inputs will support modulation inputs from DC - 700 MHz typical. This device is optimized for a supply voltage of +4.5V to +5.5V and consumes 170 mA @ +5V supply.

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Electrical Specifications, See Test Conditions on following page herein.

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF		450 - 960			1700 - 2200			2200 - 2700			3400 - 4000		MHz
Output P1dB		+8			+8			+7			+6		dBm
Output Noise Floor		-161			-159			-157			-150		dBm/Hz
Output IP3		+22			+22			+20			+17		dBm
Output Power	+4	+6		+3	+5		+2	+5		0	+3		dBm
Carrier Feedthrough (uncalibrated)		-38			-36			-32			-30		dBm
Sideband Suppression (uncalibrated)		43			42			33			22		dBc
LO Port Return Loss		25			15			14			13		dB
RF Port Return Loss		11			20			17			11		dB

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Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Output					
RF Frequency Range		100		4000	MHz
RF Return Loss			15		dB
LO Input					
LO Frequency Range		100		4000	MHz
LO Input Power		-6	0	+6	dBm
LO Port Return Loss			15		dB
Baseband Input Port					
Baseband Port Bandwidth	3 dB Bandwidth with 50Ω source.	DC		700	MHz
Baseband Input DC Voltage (Vbbdc)		+1.4	+1.5	+1.6	V
Baseband Input DC Bias Current (Ibbdc)	Single-ended.		90		µA
Single-ended Baseband Input Capacitance	De-embed to the lead of the device.		4.5		pF
DC Power Requirements	See Test Conditions Below				
Supply Voltage (Vcc1, Vcc2)		+4.5	+5.0	+5.5	V
Supply Current (Icc1, Icc2)			168		mA

Test Conditions: Unless Otherwise Specified, the Following Test Conditions Were Used

Parameter	Condition
Temperature	+25 °C
Baseband Input Frequency	200 kHz
Baseband Input DC Voltage (Vbbdc)	+1.5V
Baseband Input AC Voltage (Peak to Peak Differential, I and Q)	1.6V
Baseband Input AC Voltage for OIP3 Measurement (Peak to Peak Differential, I and Q)	800 mV per tone @ 150 & 250 kHz
Frequency Offset for Output Noise Measurements	20 MHz
Supply (Vcc1, Vcc2)	+5.0V
LO Input Power	0 dBm
LO Input Mode	Single-Ended through LON
Mounting Configuration	Refer to HMC497LP4 Application Schematic Herein
Sideband & Carrier Feedthrough	Uncalibrated

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Calibrated vs. Uncalibrated Test Results

During the Uncalibrated Sideband and Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The “Uncalibrated, +25 °C” Sideband and Carrier Suppression plots were measured at room temperature, while the “Uncalibrated, over Temperature” Sideband and Carrier Suppression plots represent the worst case uncalibrated suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

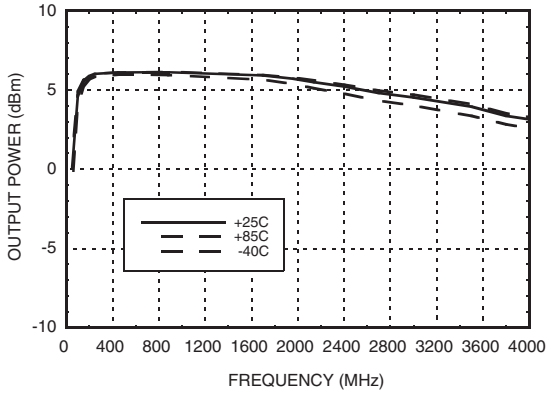
The “Calibrated, + 25 °C” Sideband Suppression data was plotted after a manual adjustment of the I/Q amplitude balance and I/Q phase offset (skew) at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case calibrated Sideband Suppression levels at T= -40 °C, +25 °C, and +85 °C.

The “Calibrated, +25 °C” Carrier Suppression data was plotted after a manual adjustment of the Ip/In & Qp/Qn DC offsets at +25 °C, and at each LO input power level. The +25 °C adjustment settings were held constant during tests over temperature. The “Calibrated, over Temperature” plots represent the worst case Carrier Suppression levels measured at T= -40 °C, +25 °C, and +85 °C.

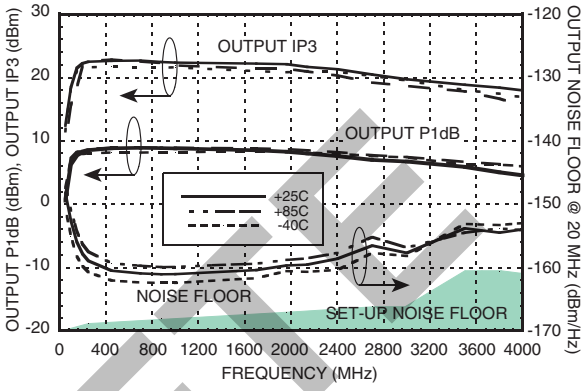
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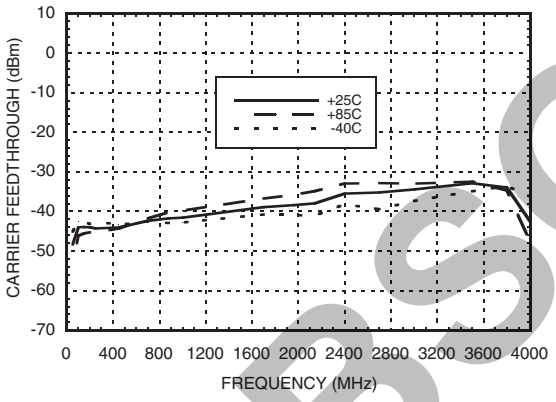
Wideband Performance vs. Frequency



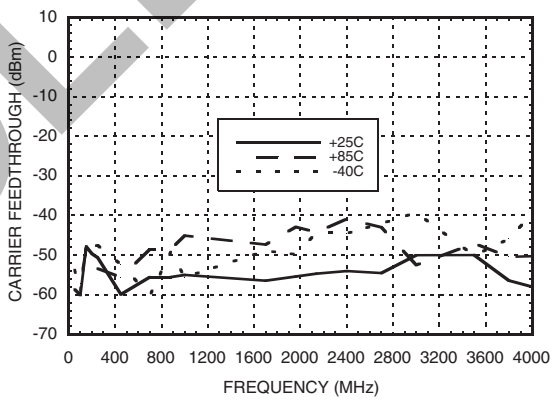
Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency



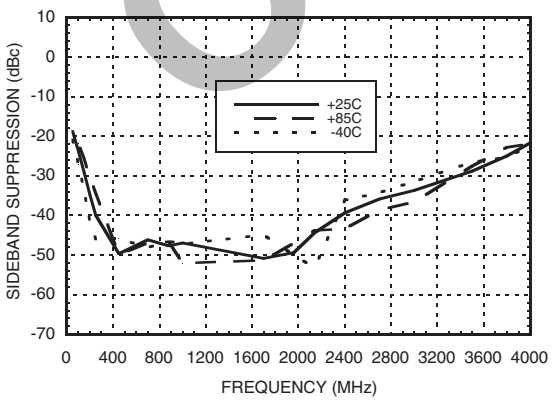
Uncalibrated Carrier Feedthrough [1] vs. Frequency



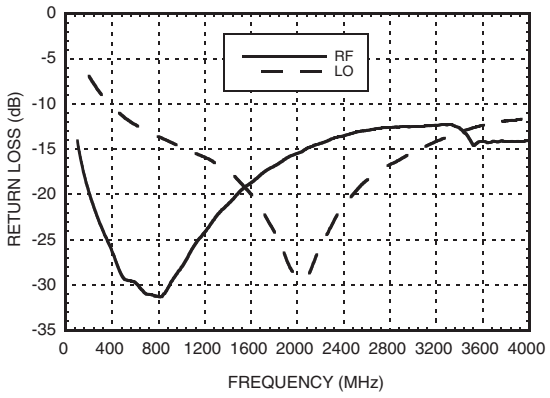
Calibrated Carrier Feedthrough [1] vs. Frequency



Sideband Suppression vs. Frequency



Return Loss vs. Frequency



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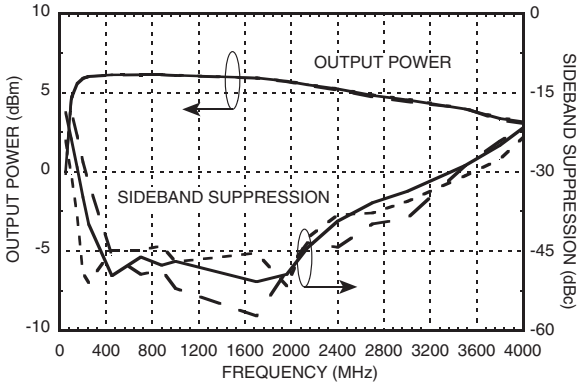
[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

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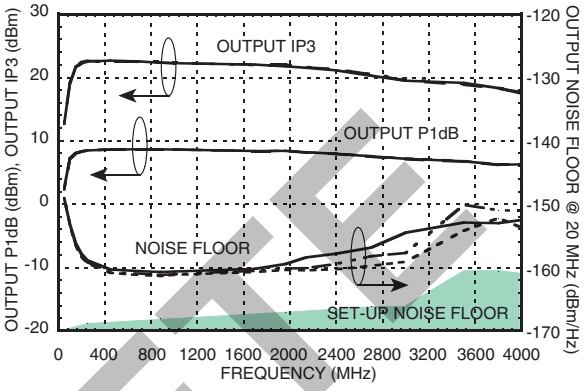
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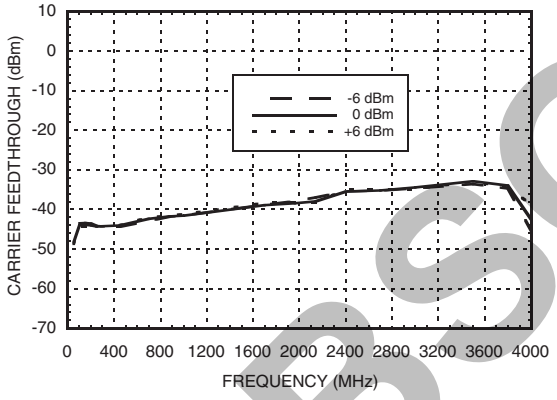
Wideband Performance vs. Frequency Over LO Power [3]



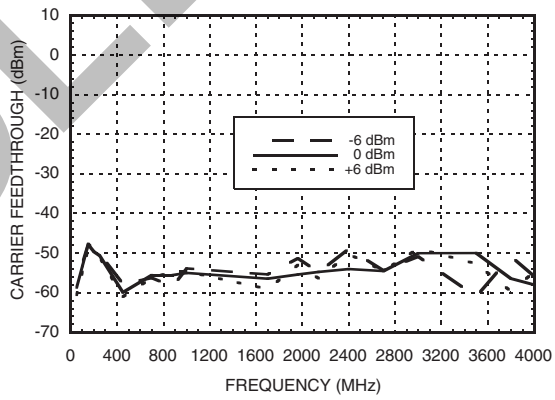
Output IP3, P1dB & Noise Floor @ 20 MHz Offset vs. Frequency Over LO Power [3]



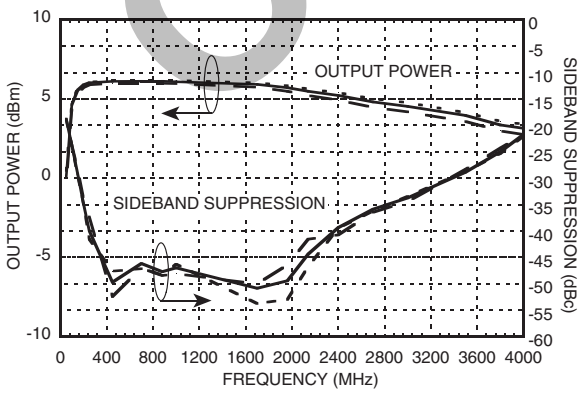
Uncalibrated Carrier Feedthrough [2] vs. Frequency



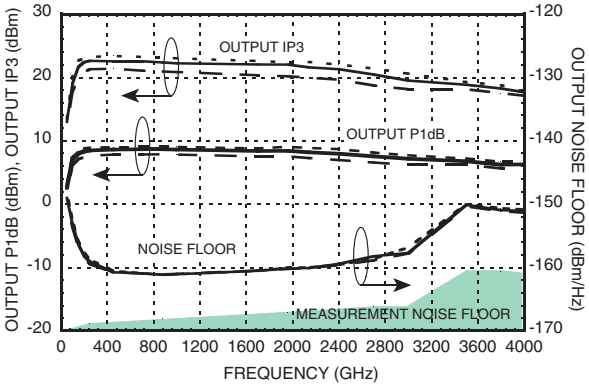
Calibrated Carrier Feedthrough [2] vs. Frequency



Wideband Performance vs. Frequency Over Supply Voltage [1]



Output IP3, P1dB & Noise Floor @ 20 MHz vs. Offset Frequency Over Supply Voltage [1]



[1] See note titled "Calibrated vs. Uncalibrated test results" herein.

[2] Supply voltage from +4.5 to +5.5V.

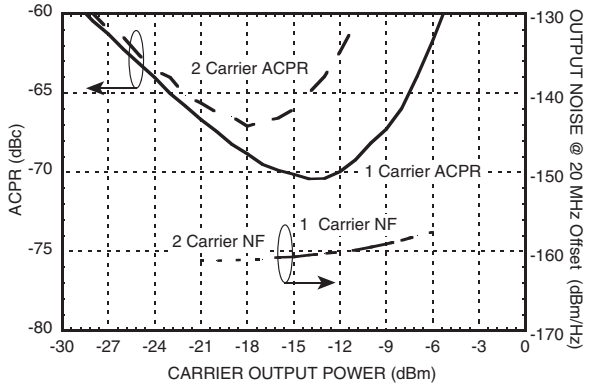
[3] LO Power from -6 dBm to +6 dBm

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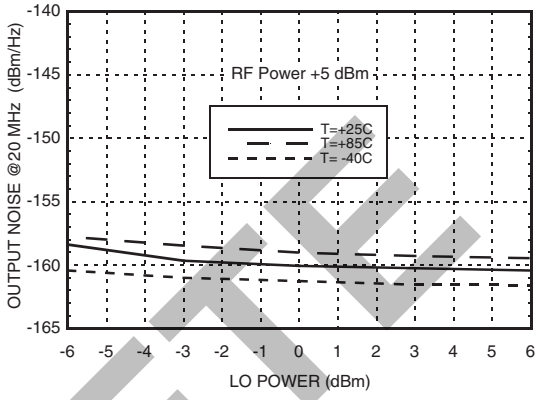
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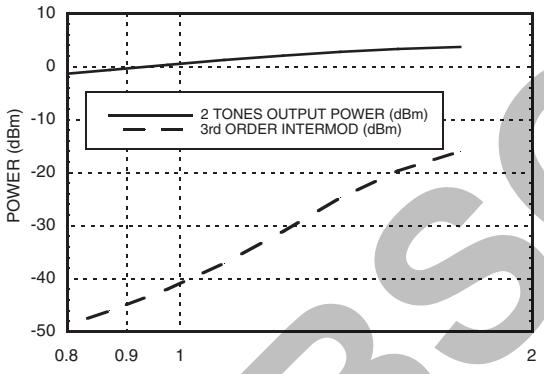
ACPR & Output Noise for W-CDMA @ 2140 MHz



Output Noise @ 20 MHz Offset vs. LO Power Over Temperature

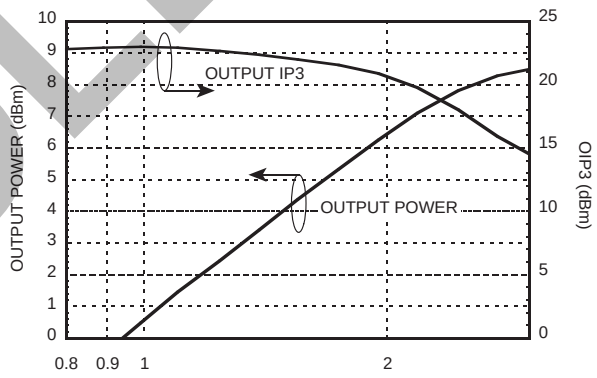


Compression Characteristic @ 2140 MHz



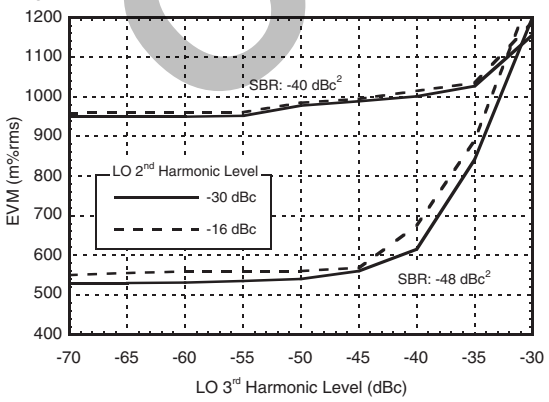
Single Tone

Power & Linearity @ 2140 MHz vs. Baseband Voltage

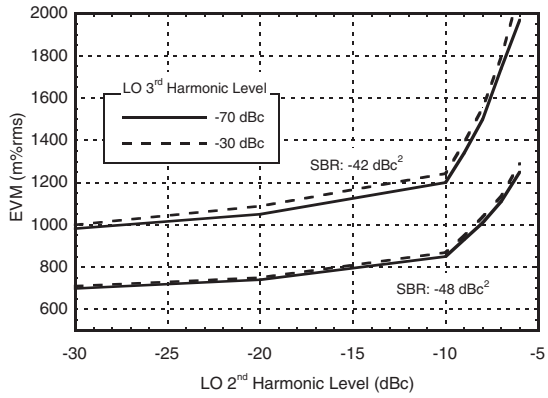


Single Tone

EVM vs. LO Harmonic Level & Sideband Rejection for EDGE @ 900 MHz



EVM vs. LO Harmonic Level & Sideband Rejection for EDGE @ 1900 MHz



Note 1: W-CDMA (Modulation Set-up for ACPR Mode); The Baseband I and Q input signals were generated using "Test Model 1 with 64 channels" settings in the Agilent E3844C.

Note 2: The I/Q baseband amplitude and phase inputs were offset to achieve Sideband Rejection (SBR) levels. LO = +6 dBm, SSB Power = 0 dBm

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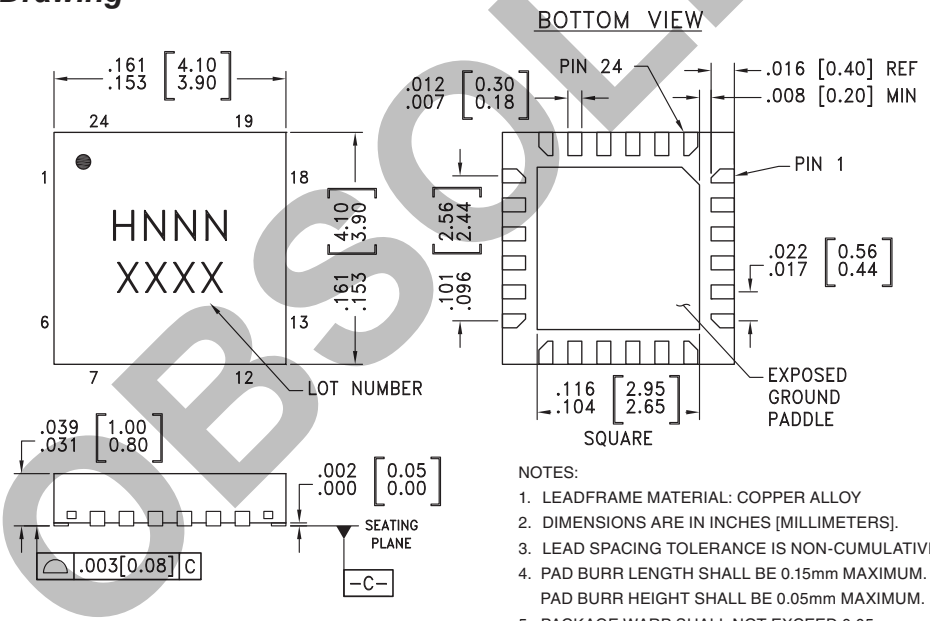
Absolute Maximum Ratings

Vcc1, Vcc2	0V to +6V
LO Input Power	+18 dBm
Baseband Input Voltage (AC + DC) (Reference to GND)	0.0V to +2.8V
Channel Temperature	150 °C
Continuous Pdiss (T = 85°C) (Derate 30 mW/°C above 85°C)	1.8 Watts
Thermal Resistance (R_{th}) (junction to lead)	34 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

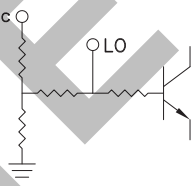
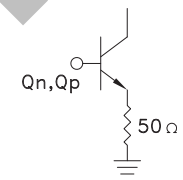
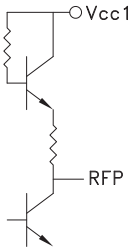
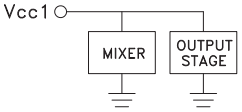
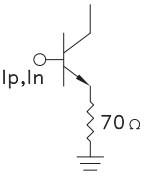
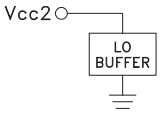
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC497LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H497 XXXX
HMC497LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H497 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1,6, 7, 13, 15	N/C	Not connected.	
2, 5, 8, 11, 12, 14, 17, 19, 20, 23	GND	These pins and the ground paddle should be connected to a high quality RF/DC ground.	
3, 4	LOP, LON	LO inputs. Need DC decoupling capacitors. The ports could be driven single ended or differentially.	
9, 10	QN, QP	Q channel differential baseband input. These high impedance ports should be biased around 1.5V DC. Nominal recommended baseband input is around 1.6V pp differential.	
16	RFOUT	RF output. 50 Ohms. Needs DC blocking capacitor.	
18	Vcc1	Supply voltage for the mixer and output stages 79mA @ +5.0V.	
21, 22	IP, IN	I channel differential baseband input. These high impedance ports should be at the same bias voltage (VbbDC) as Qn & Qp.	
24	Vcc2	Supply voltage for the LO stage 88mA @ +5V.	

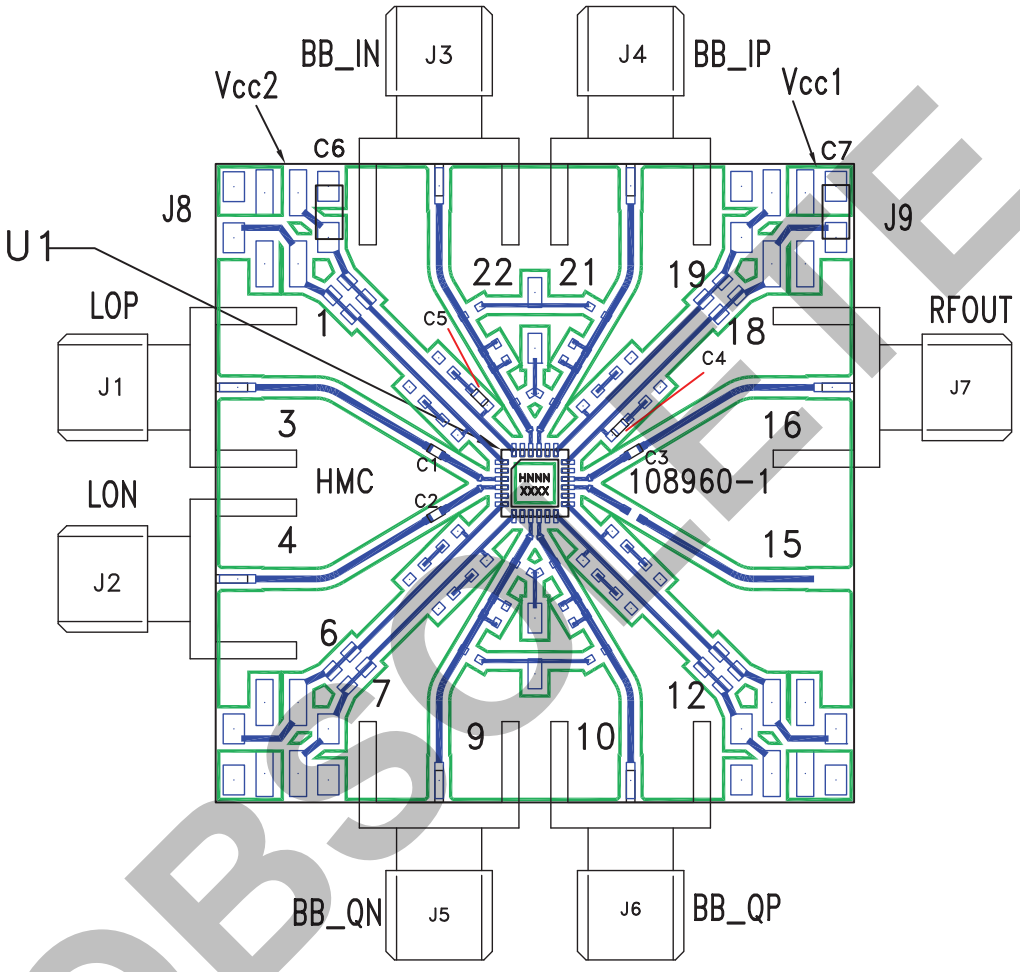
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Evaluation PCB



List of Materials for Evaluation PCB 108962 [1]

Item	Description
J1 - J7	PC Mount SMA Connector
J8, J9	DC Molex Connector
C1 - C3	100 pF Chip Capacitor, 0402 Pkg.
C4, C5	1000 pF Chip Capacitor, 0402 Pkg.
C6, C7	4.7 uF, Case A, Tantulum
U1	HMC497LP4 Modulator
PCB [2]	108960 Eval Board

[1] Reference this number when ordering complete evaluation PCB

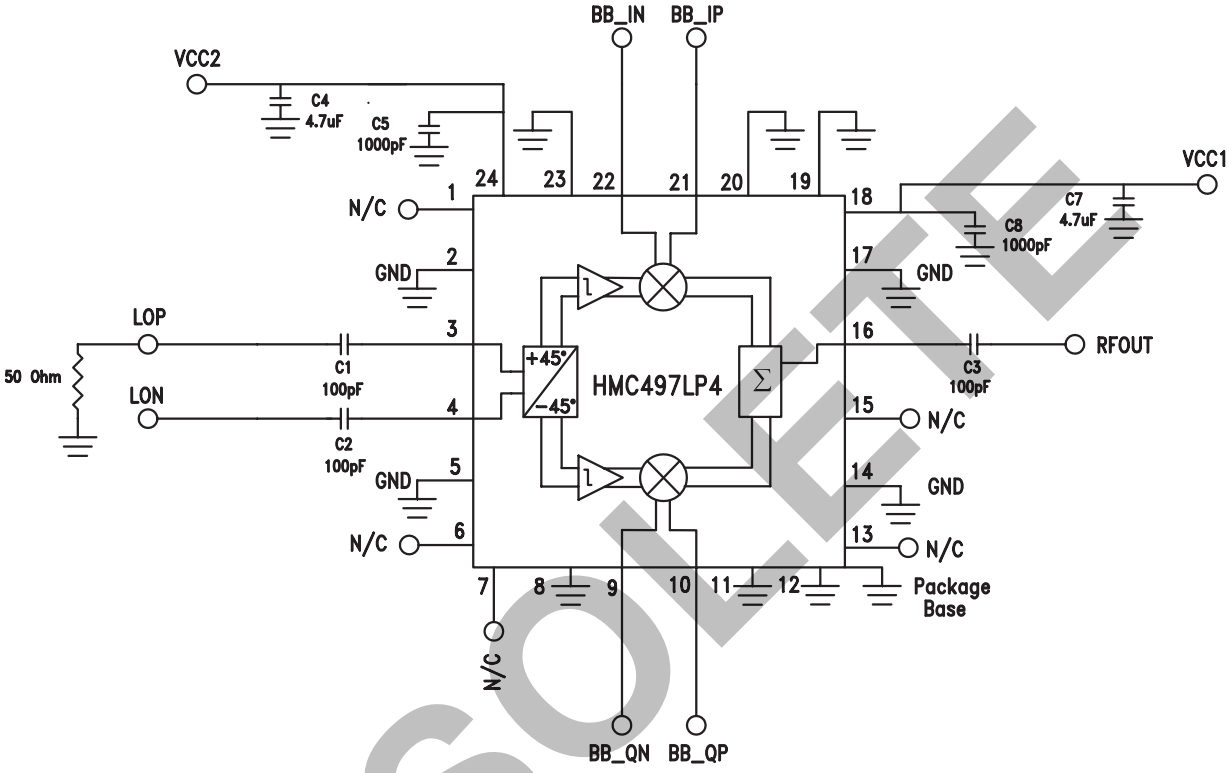
[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

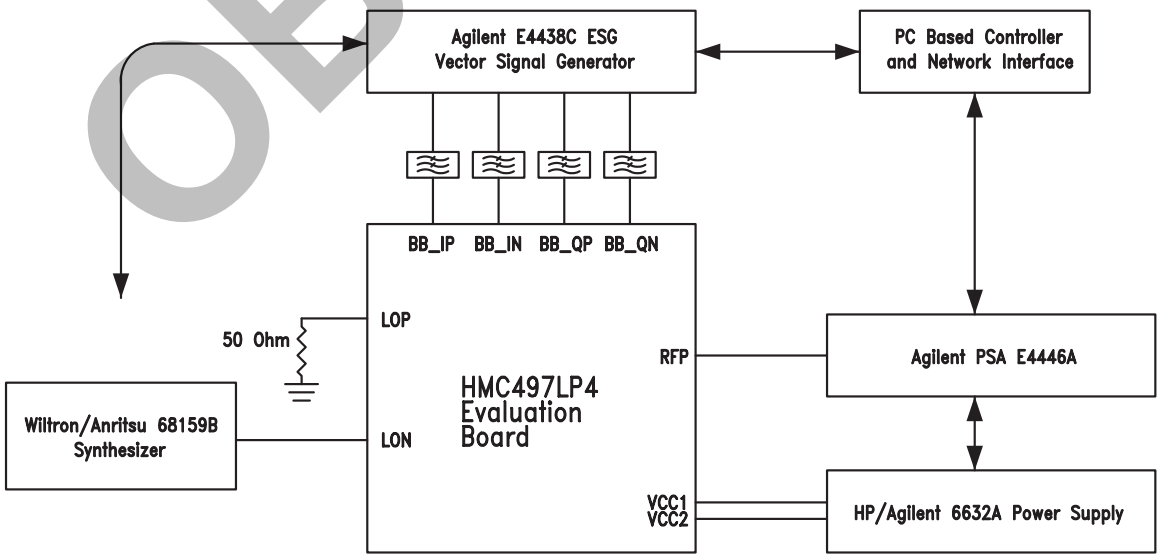
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Application & Evaluation PCB Schematic



Characterization Set-up



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