NCP4686

400 mA, High Accuracy, Low Input Voltage, Low Dropout Regulator

The NCP4686 is CMOS Linear voltage regulators with 400 mA output current capability. The device has very high output voltage accuracy, low supply current and low ON−resistance transistor. The NCP4686 is easy to use and includes output current fold−back protection and a fully integrated constant slope circuit as a soft−start circuit. Due to it inrush current is minimized and no output voltage overshoots are there. A Chip Enable function is included to save power by lowering supply current.

Features

- Operating Input Voltage Range: 1.0 V to 3.6 V
- Output Voltage Range: 0.7 V to 1.8 V (available in 0.1 V steps)
- Output Voltage Accuracy: ±0.8% ($V_{OUT} \geq 1.0$ V, $T_A = 25°C$)
- Supply Current: 48 μA
- Dropout Voltage: 0.22 V ($V_{OUT} = 1.5$ V)
- Line Regulation: 0.1%/V Typ.
- Ripple Rejection: Typ. 60 dB (f = 10 kHz)
- Stable with Ceramic Capacitors: 1 μF or more
- Current Fold Back Protection
- Build−in Constant Slope Circuit
- Available in XDFN6 1.2 x 1.2 mm, SC−70, SOT23 Packages
- These are Pb−Free Devices

Typical Applications

- Battery−powered Equipment
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Home Appliances

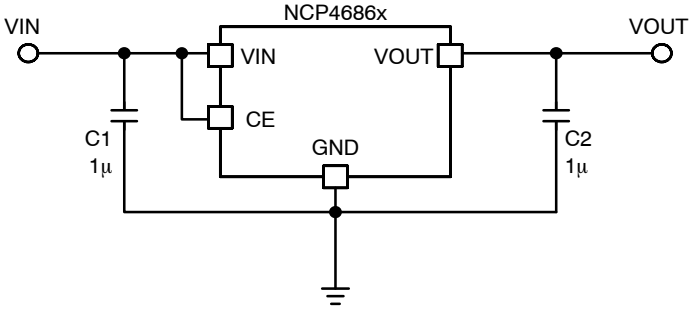


Figure 1. Typical Application Schematics

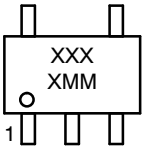
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MARKING DIAGRAMS

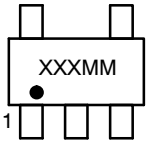


SC−70
CASE 419A



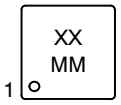


SOT−23−5
CASE 1212





XDFN6
CASE 711AA



XX, XXX, XXXX	= Specific Device Code
M, MM	= Date Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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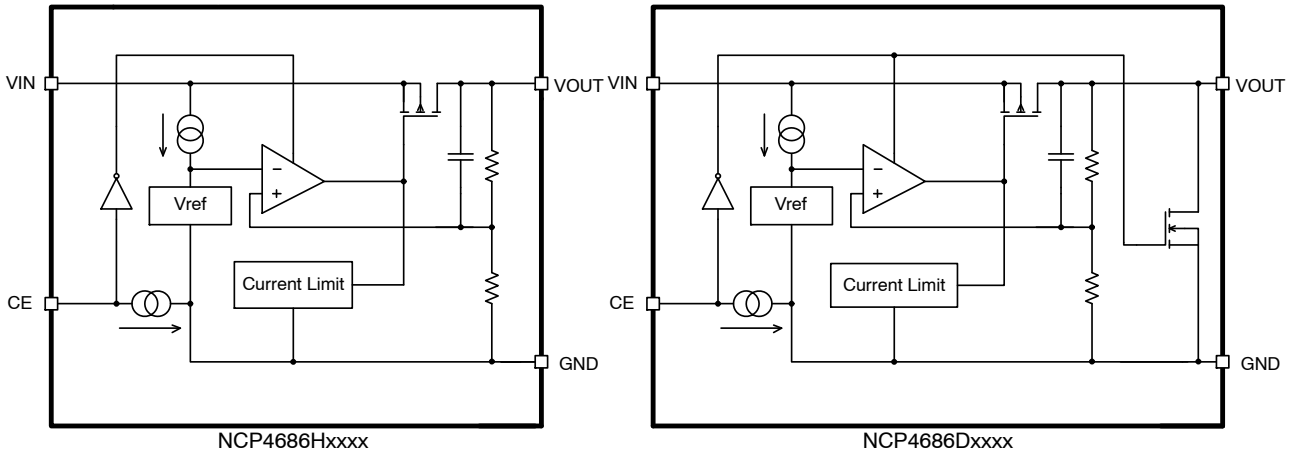


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN6	Pin No. SC−70	Pin No. SOT23	Pin Name	Description
6	4	5	V_{OUT}	Output pin
2	3	2	GND	Ground
3	1	3	CE	Chip enable pin (Active “H”)
4	5	1	V_{IN}	Input pin
1	2	4	NC	No connection
5	–	–	NC	No connection

*Please refer to package dimensions section on Page 15 on this data sheet for pin numbers associated with different package.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	4.0	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	V_{CE}	−0.3 to 4.0	V
Output Current	I_{OUT}	500	mA
Power Dissipation XDFN1212	P_D	400	mW
Power Dissipation SC−70		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 125	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN6 1.2 x 1.2 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W
Thermal Characteristics, SOT23 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	238	°C/W
Thermal Characteristics, SC−70 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	263	°C/W

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V, whichever is greater; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 0.1 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.0		3.6	V
Output Voltage	T_A = +25 °C	$V_{OUT} \ge 1.0$ V	V_{OUT}	x0.992		x1.008	V
		$V_{OUT} < 1.0$ V		−8		8	mV
	$-40°C \le T_A \le 85°C$	$V_{OUT} \ge 1.0$ V		x0.983		x1.017	V
		$V_{OUT} < 1.0$ V		−17		17	mV
Output Voltage Temp. Coefficient	$-40°C \le T_A \le 85°C$		$\Delta V_{OUT} / \Delta T_A$		±60		ppm/°C
Line Regulation	$V_{OUT(NOM)} + 0.5$ V $\le V_{IN} \le 3.6$ V, $V_{IN} \ge 1.3$ V		$Line_{Reg}$		0.10	0.25	%/V
Load Regulation	I_{OUT} = 1 mA to 400 mA		$Load_{Reg}$		25	45	mV
Dropout Voltage	I_{OUT} = 400 mA	0.7 V $\le V_{OUT} <$ 0.8 V	V_{DO}		0.48	0.62	V
		0.8 V $\le V_{OUT} <$ 0.9 V			0.40	0.54	
		0.9 V $\le V_{OUT} <$ 1.0 V			0.36	0.47	
		1.0 V $\le V_{OUT} <$ 1.2 V			0.32	0.45	
		1.2 V $\le V_{OUT} <$ 1.5 V			0.28	0.38	
		1.5 V $\le V_{OUT}$			0.22	0.31	
Output Current			I_{OUT}	400			mA
Short Current Limit	V_{OUT} = 0 V		I_{SC}		110		mA
Quiescent Current			I_Q		48	75	μA
Standby Current	V_{CE} = 0 V, T_A = 25°C		I_{STB}		0.1	8.0	μA
CE Pin Threshold Voltage	CE Input Voltage “H”		V_{CEH}	0.9			V
	CE Input Voltage “L”		V_{CEL}			0.4	
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1.0$ V, $\Delta V_{IN} = 0.2$ V_{pk-pk}, I_{OUT} = 30 mA, f = 10 kHz		PSRR		60		dB
Output Noise Voltage	f = 10 Hz to 100 kHz, V_{OUT} = 0.7 V, I_{OUT} = 30 mA		V_N		30		μV_{rms}
Low Output N−channel Tr. On Resistance	V_{IN} = 2 V, V_{CE} = 0 V, NCP4686D only		R_{LOW}		43		Ω

TYPICAL CHARACTERISTICS

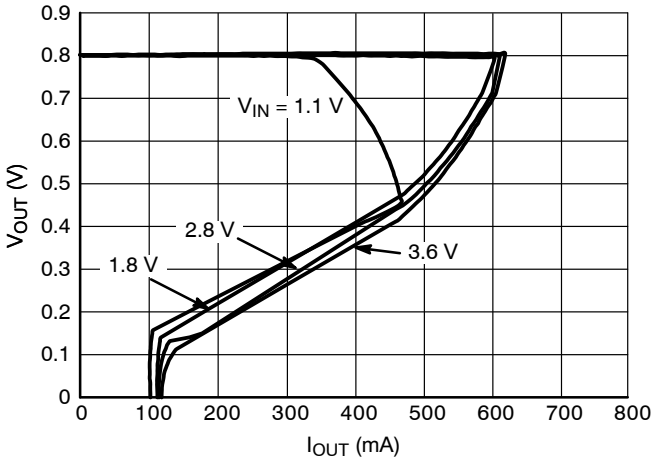


Figure 3. Output Voltage vs. Output Current 0.8 V Version (T_J = 25°C)

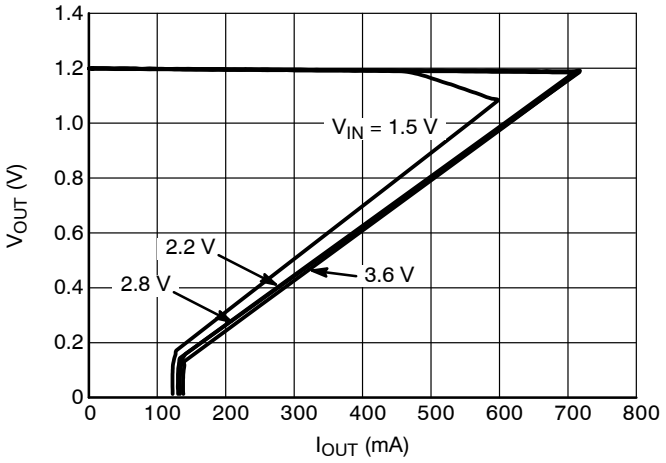


Figure 4. Output Voltage vs. Output Current 1.2 V Version (T_J = 25°C)

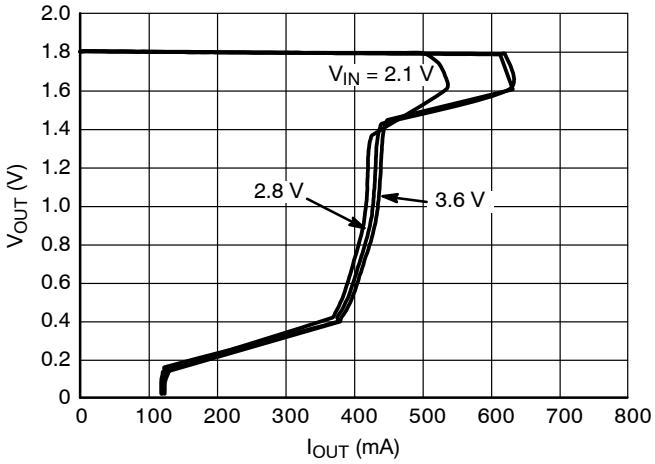


Figure 5. Output Voltage vs. Output Current 1.8 V Version (T_J = 25°C)

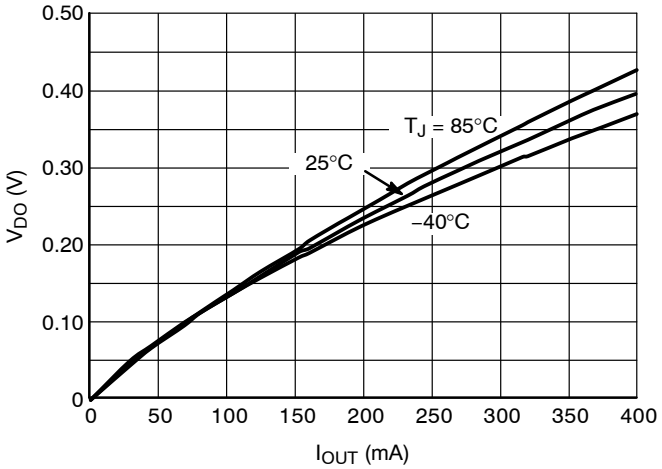


Figure 6. Dropout Voltage vs. Output Current 0.8 V Version

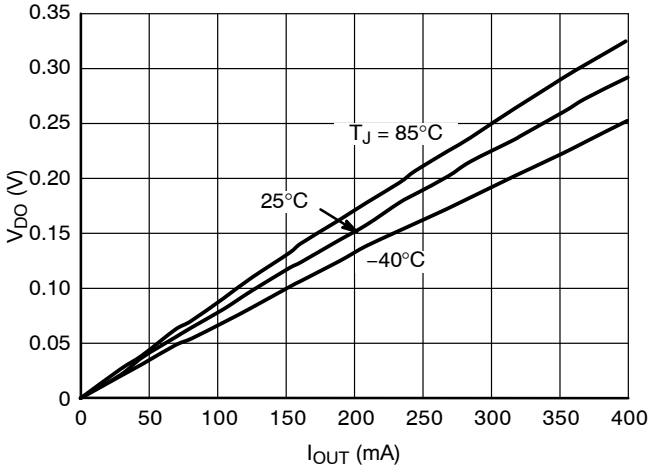


Figure 7. Dropout Voltage vs. Output Current 1.2 V Version

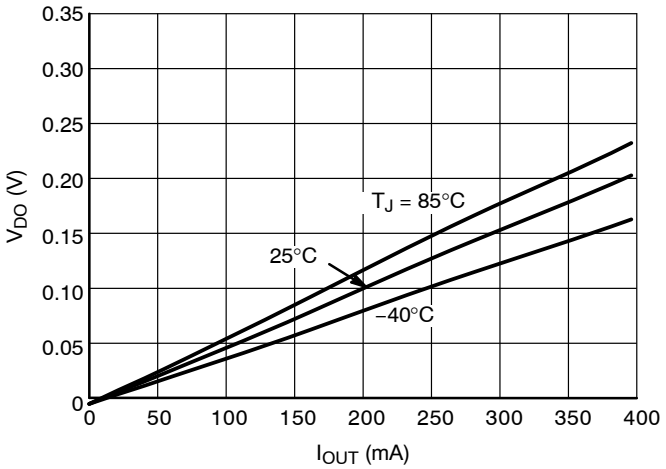


Figure 8. Dropout Voltage vs. Output Current 1.8 V Version

TYPICAL CHARACTERISTICS

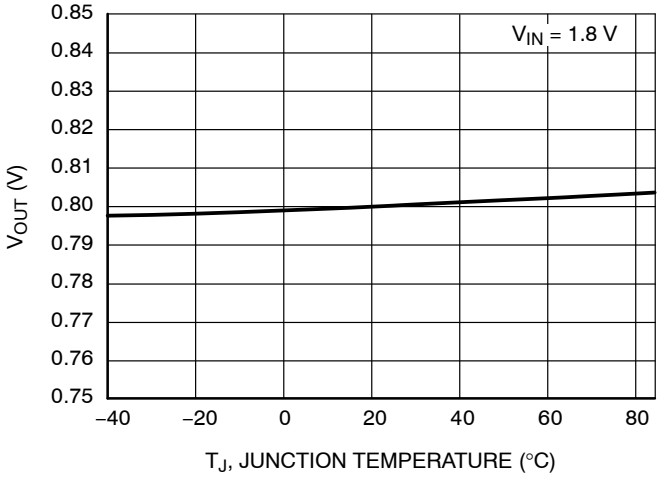


Figure 9. Output Voltage vs. Temperature, 0.8 V Version

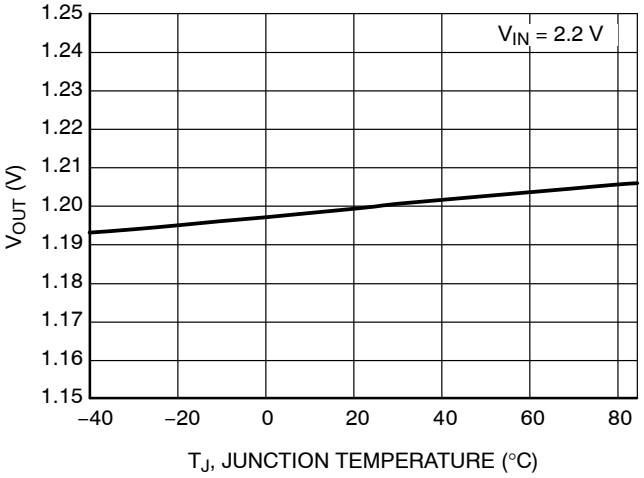


Figure 10. Output Voltage vs. Temperature, 1.2 V Version

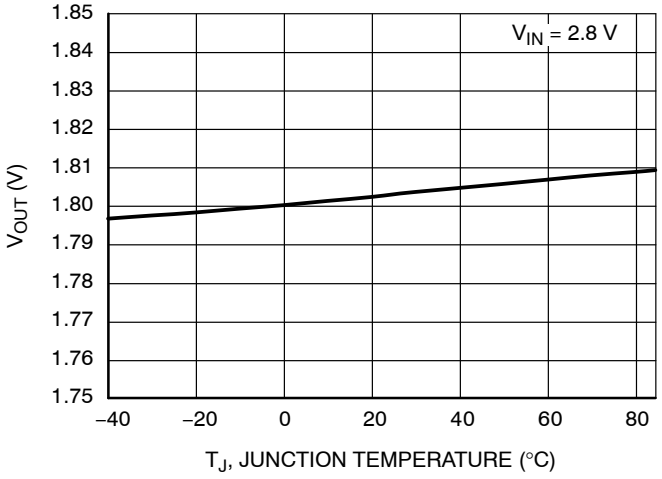


Figure 11. Output Voltage vs. Temperature, 2.8 V Version

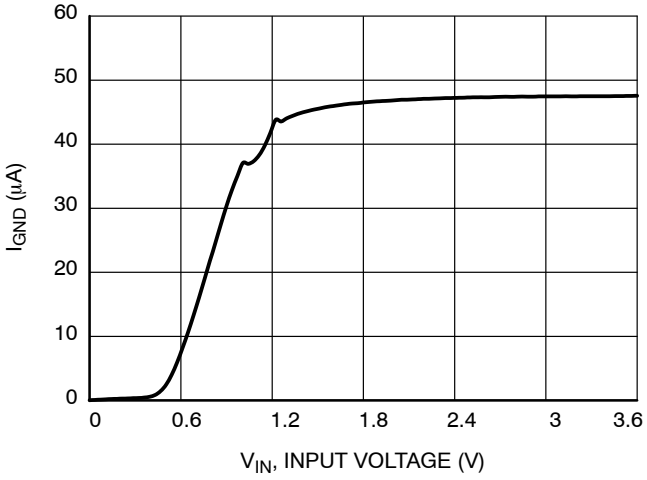


Figure 12. Supply Current vs. Input Voltage, 0.8 V Version

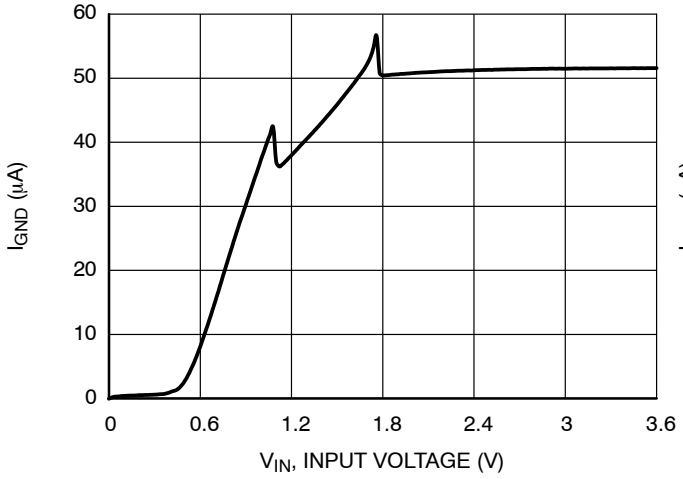


Figure 13. Supply Current vs. Input Voltage, 1.2 V Version

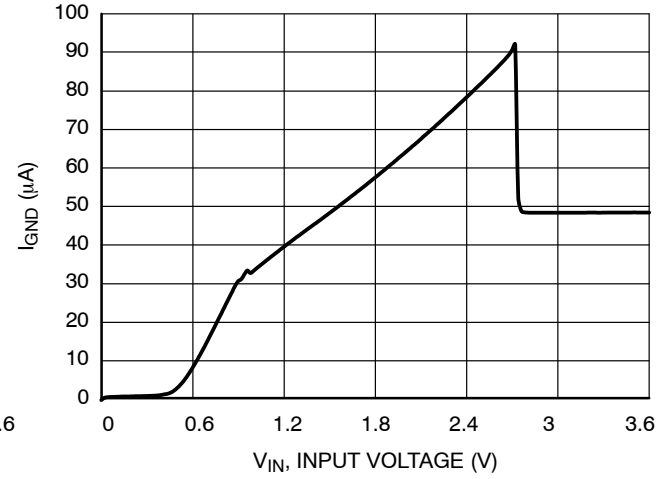


Figure 14. Supply Current vs. Input Voltage, 1.8 V Version

TYPICAL CHARACTERISTICS

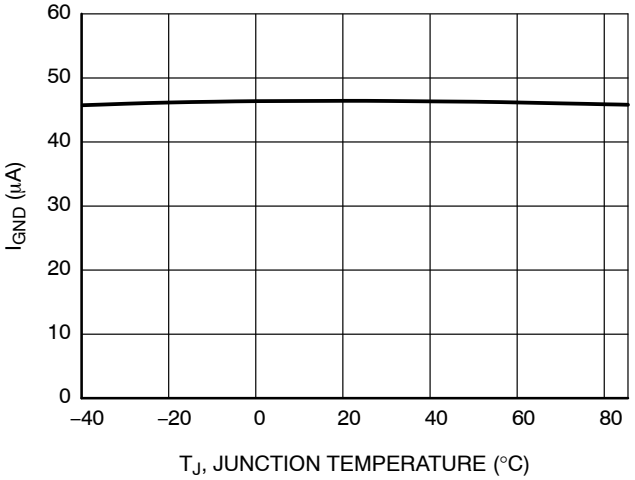


Figure 15. Supply Current vs. Temperature, 0.8 V Version

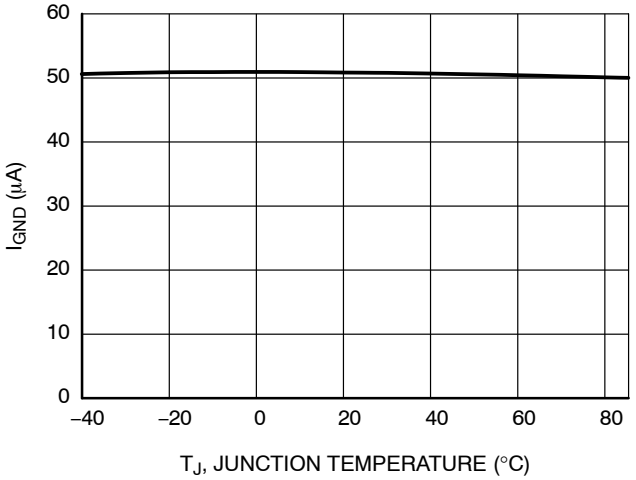


Figure 16. Supply Current vs. Temperature, 1.2 V Version

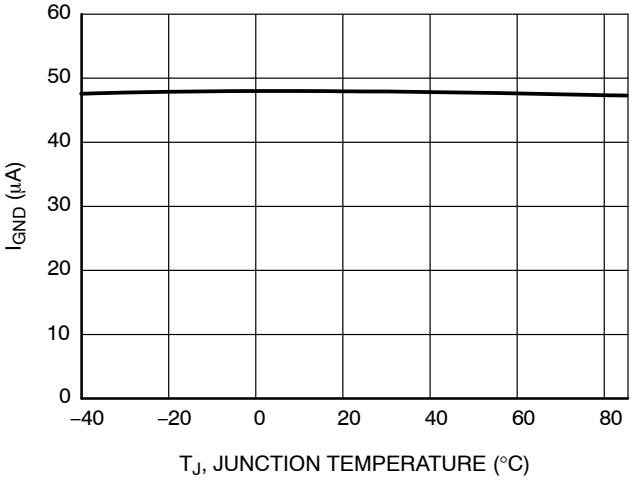


Figure 17. Supply Current vs. Temperature, 1.8 V Version

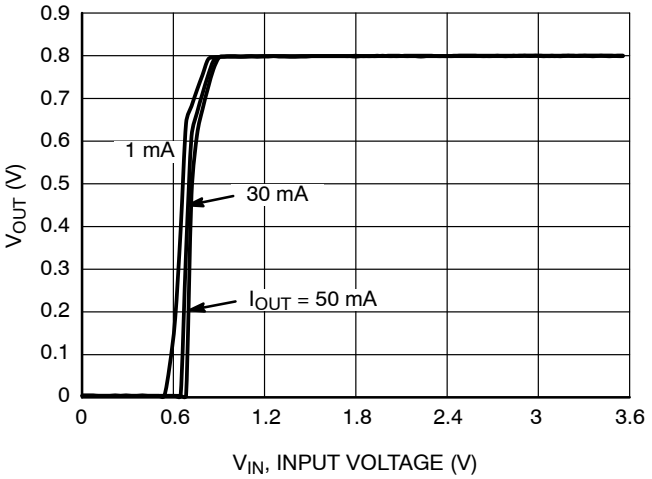


Figure 18. Output Voltage vs. Input Voltage, 0.8 V Version

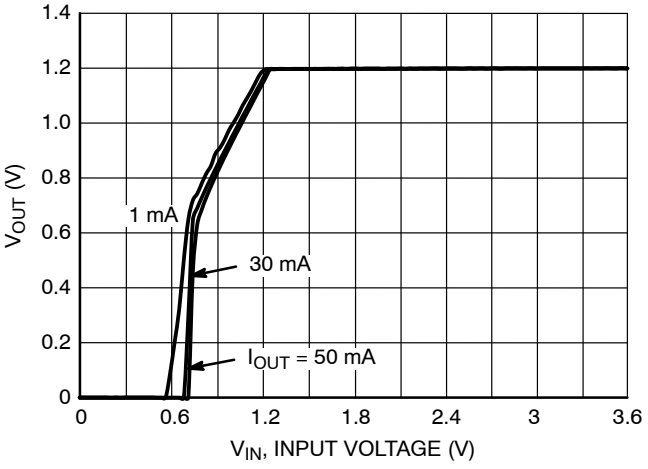


Figure 19. Output Voltage vs. Input Voltage, 1.2 V Version

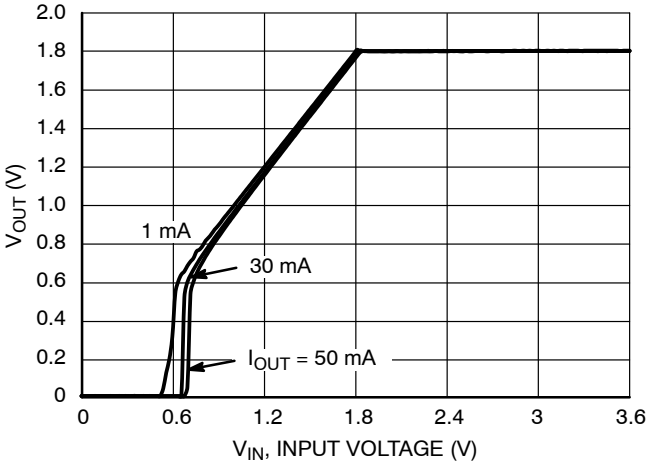


Figure 20. Output Voltage vs. Input Voltage, 1.8 V Version

TYPICAL CHARACTERISTICS

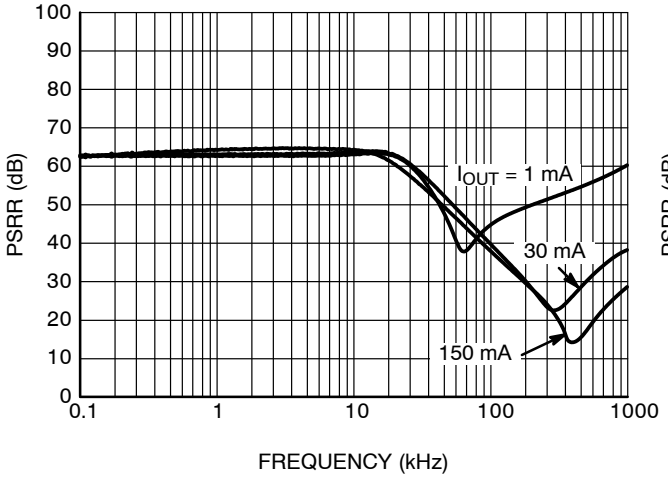


Figure 21. PSRR, 0.8 V Version, V_{IN} = 1.8 V

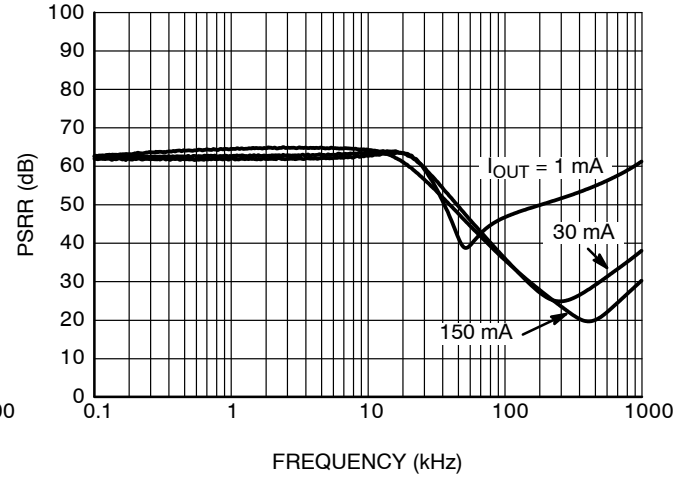


Figure 22. PSRR, 1.2 V Version, V_{IN} = 2.2 V

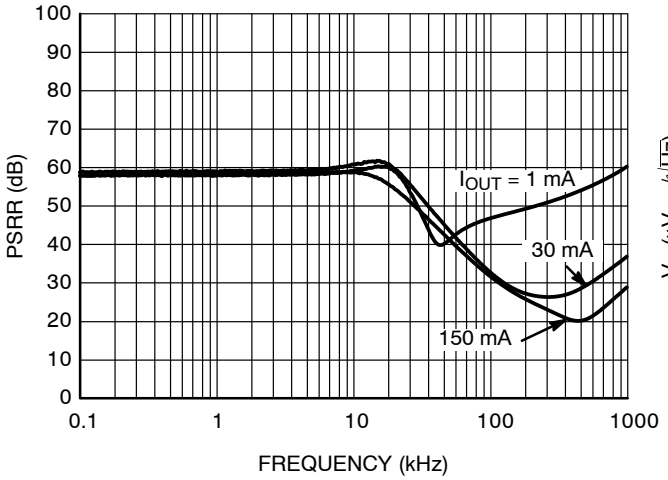


Figure 23. PSRR, 1.8 V Version, V_{IN} = 2.8 V

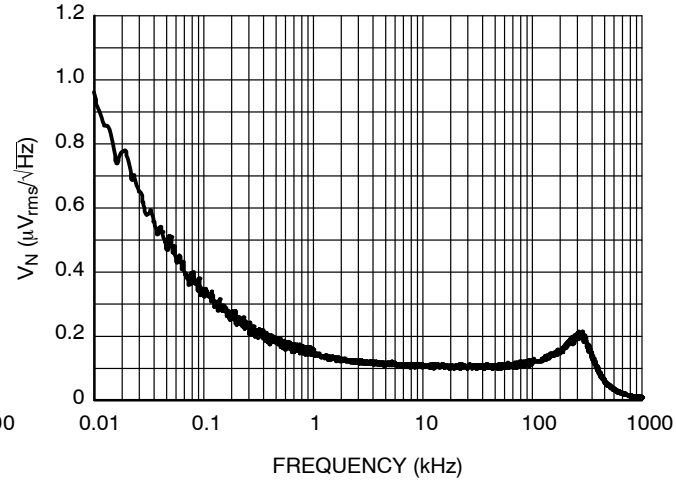


Figure 24. Output Voltage Noise, 0.8 V Version, V_{IN} = 1.8 V, I_{OUT} = 30 mA

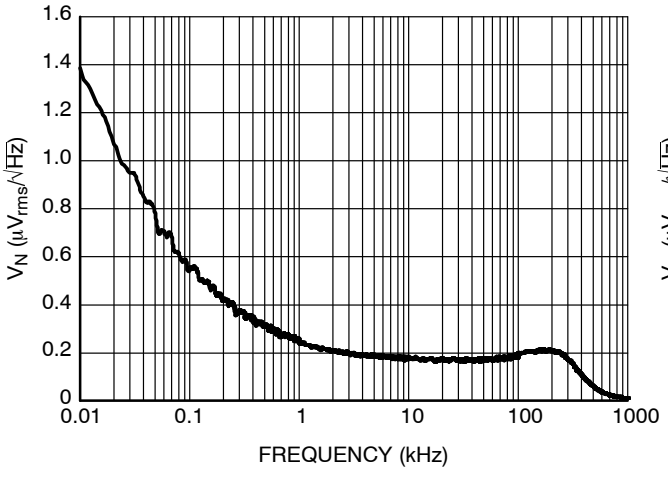


Figure 25. Output Voltage Noise, 1.2 V Version, V_{IN} = 2.2 V, I_{OUT} = 30 mA

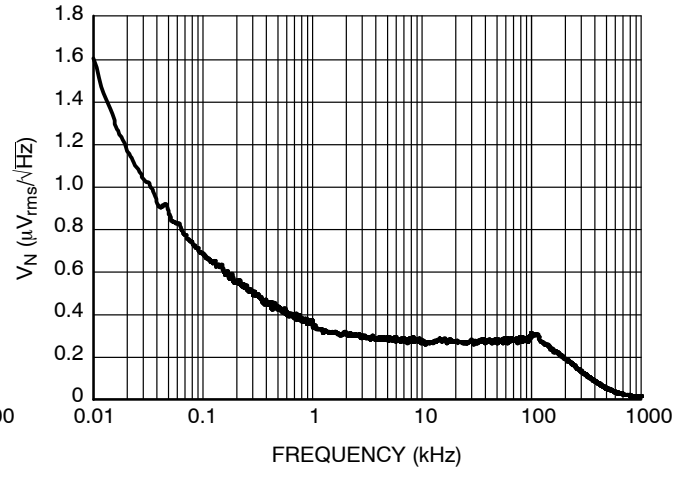


Figure 26. Output Voltage Noise, 1.8 V Version, V_{IN} = 2.8 V, I_{OUT} = 30 mA

TYPICAL CHARACTERISTICS

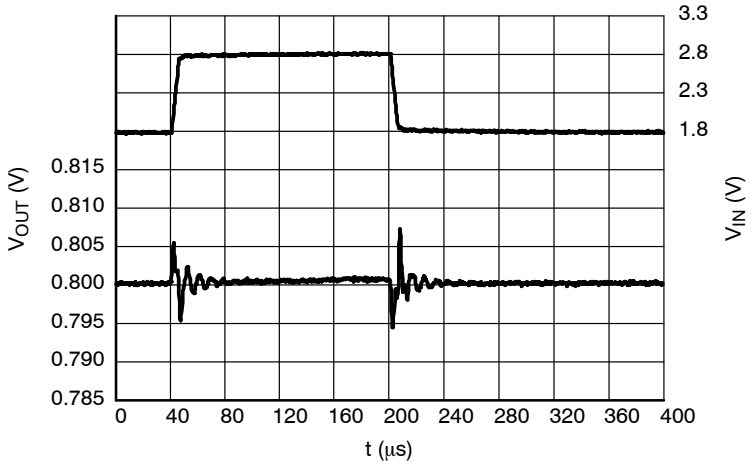


Figure 27. Line Transients, 0.8 V Version, $t_R = t_F = 5$ μs, $I_{OUT} = 30$ mA

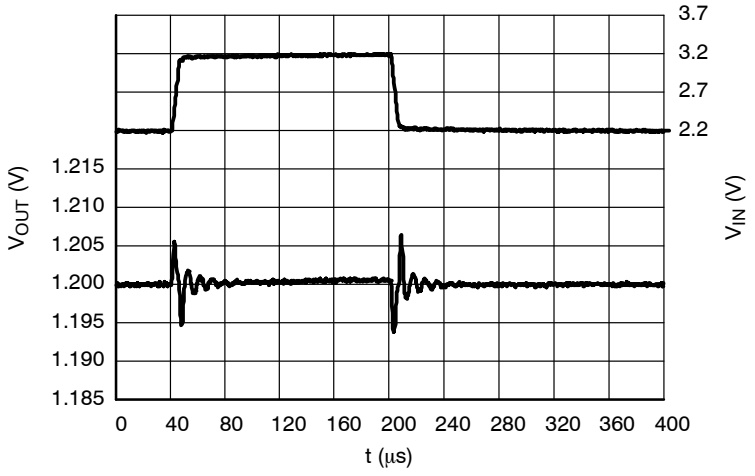


Figure 28. Line Transients, 1.2 V Version, $t_R = t_F = 5$ μs, $I_{OUT} = 30$ mA

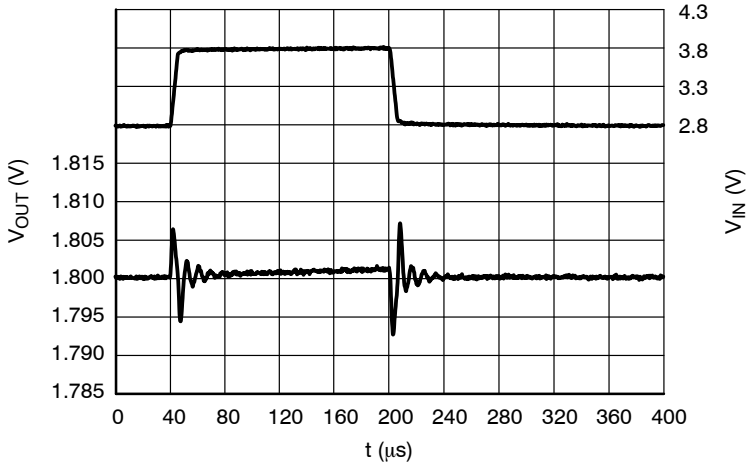


Figure 29. Line Transients, 1.8 V Version, $t_R = t_F = 5$ μs, $I_{OUT} = 30$ mA

TYPICAL CHARACTERISTICS

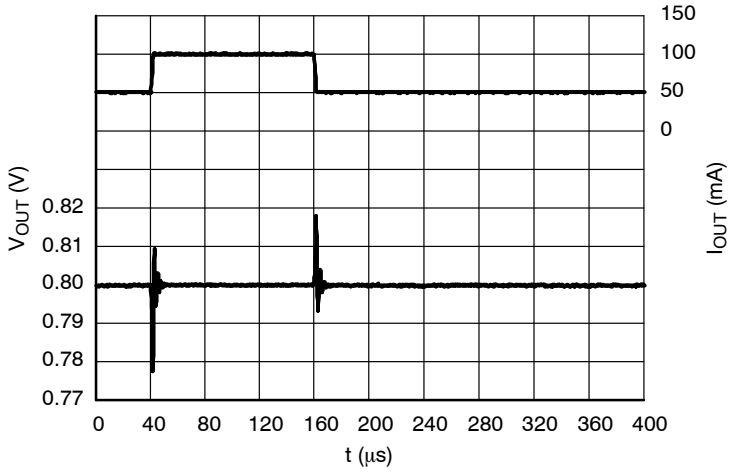


Figure 30. Load Transients, 0.8 V Version, I_{OUT} = 50 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 1.8 V

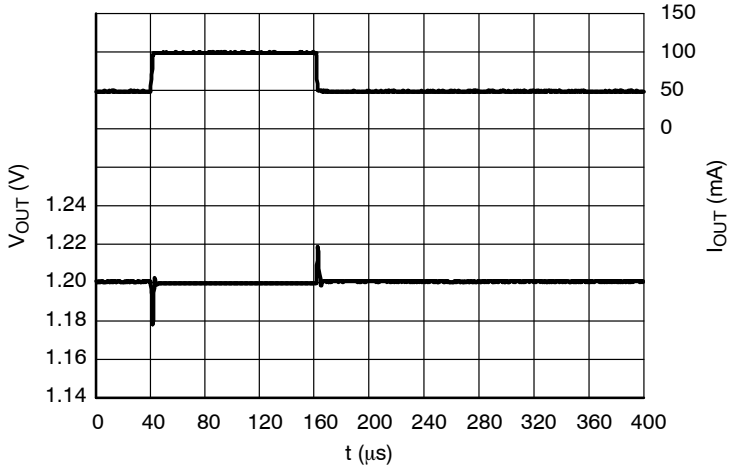


Figure 31. Load Transients, 1.2 V Version, I_{OUT} = 50 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.2 V

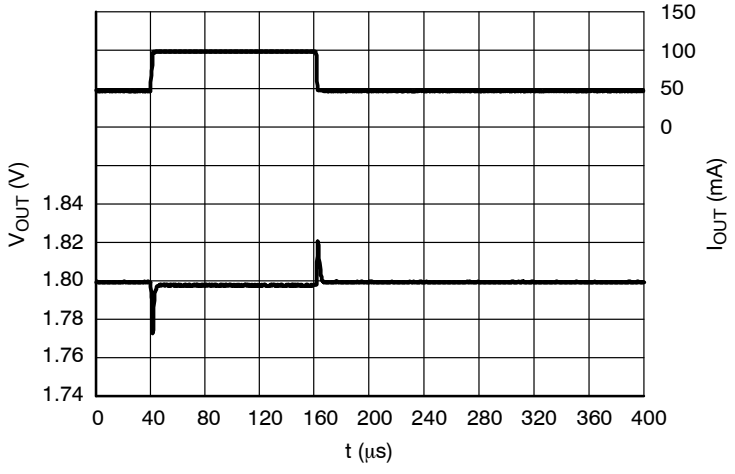


Figure 32. Load Transients, 1.8 V Version, I_{OUT} = 50 – 100 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.8 V

TYPICAL CHARACTERISTICS

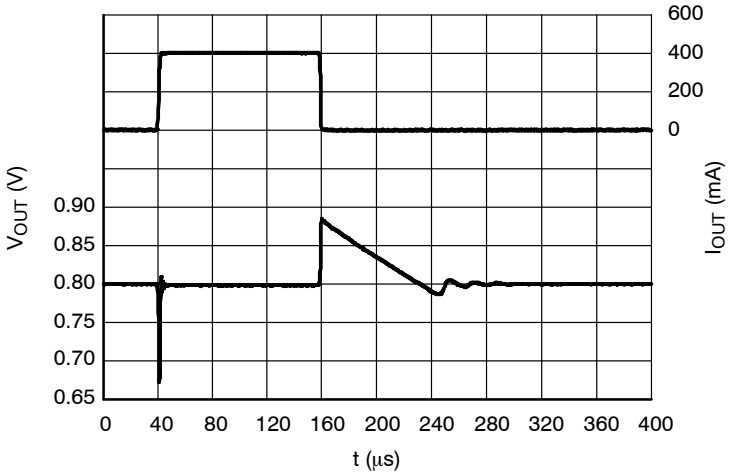


Figure 33. Load Transients, 0.8 V Version, I_{OUT} = 1 – 400 mA, t_R = t_F = 0.5 μs, V_{IN} = 1.8 V

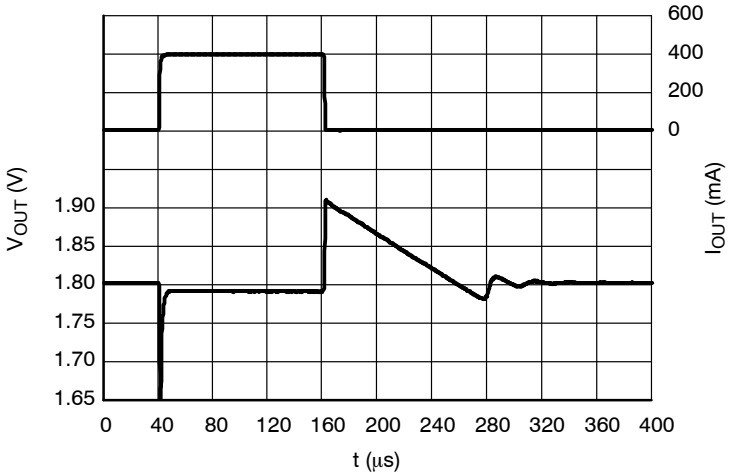


Figure 34. Load Transients, 1.8 V Version, I_{OUT} = 1 – 400 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.8 V

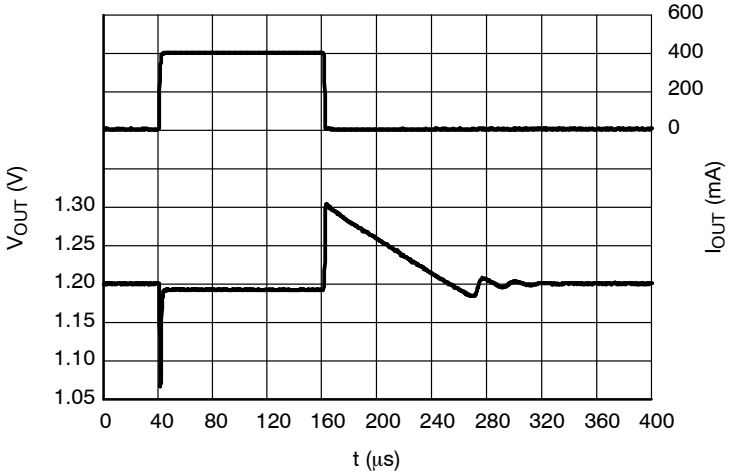


Figure 35. Load transients, 1.2 V version, I_{OUT} = 1 – 400 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.2 V

TYPICAL CHARACTERISTICS

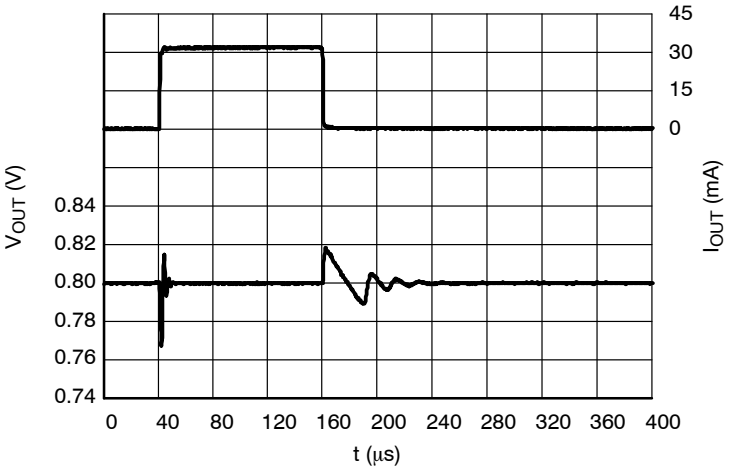


Figure 36. Load Transients, 0.8 V Version, I_{OUT} = 1 – 30 mA, t_R = t_F = 0.5 μs, V_{IN} = 1.8 V

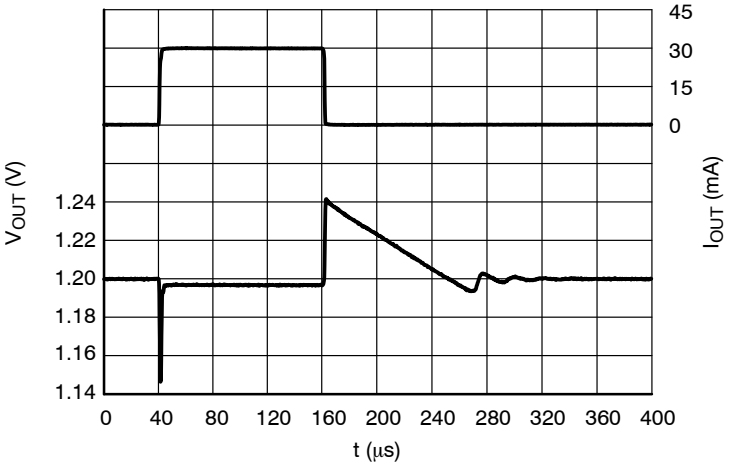


Figure 37. Load Transients, 1.2 V Version, I_{OUT} = 1 – 30 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.2 V

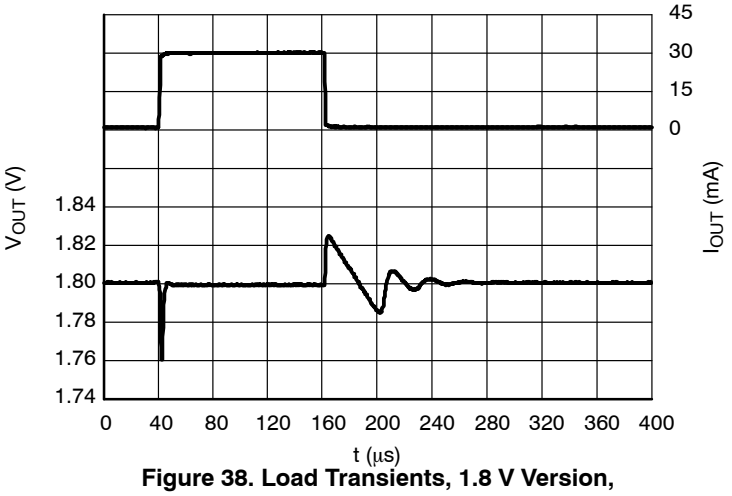


Figure 38. Load Transients, 1.8 V Version, I_{OUT} = 1 – 30 mA, t_R = t_F = 0.5 μs, V_{IN} = 2.8 V

TYPICAL CHARACTERISTICS

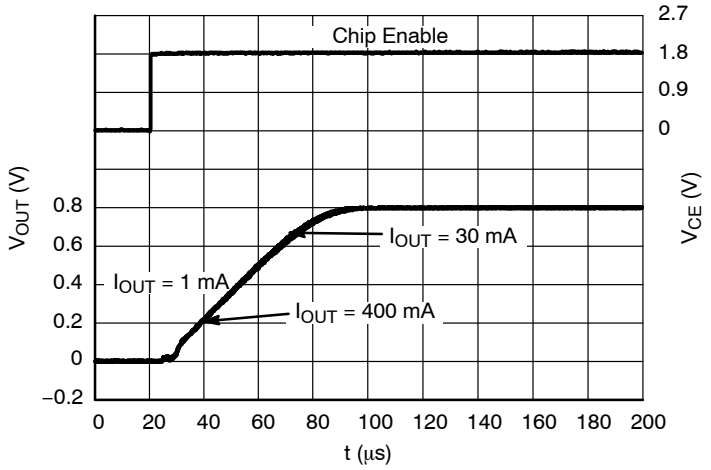


Figure 39. Start−Up, 0.8 V Version, V_{IN} = 1.8 V

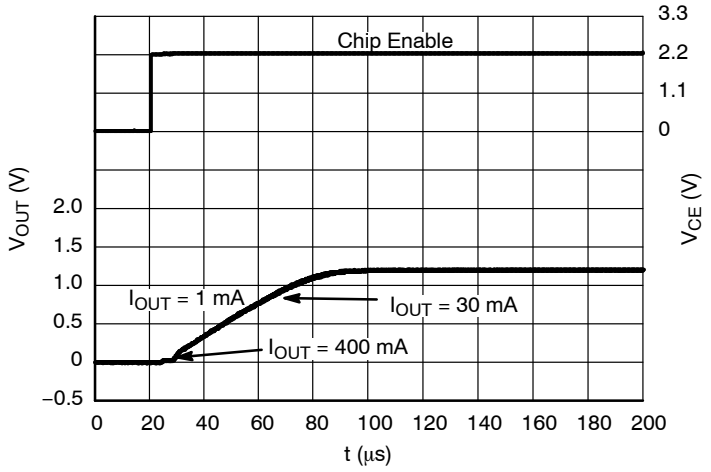


Figure 40. Start−Up, 1.2 V Version, V_{IN} = 2.2 V

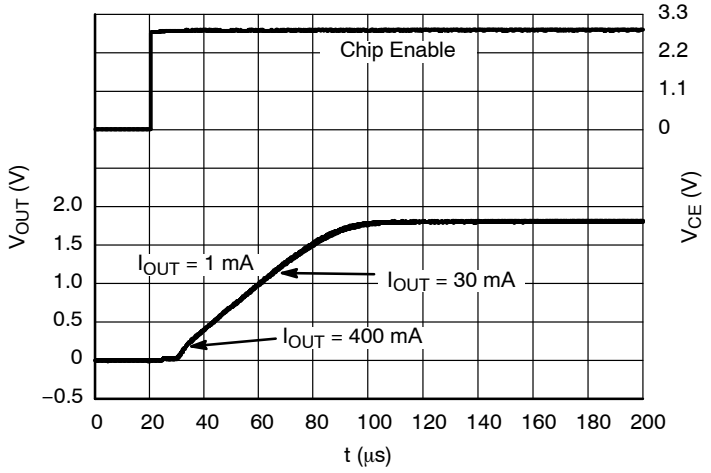


Figure 41. Start−up, 1.8 V Version, V_{IN} = 2.8 V

TYPICAL CHARACTERISTICS

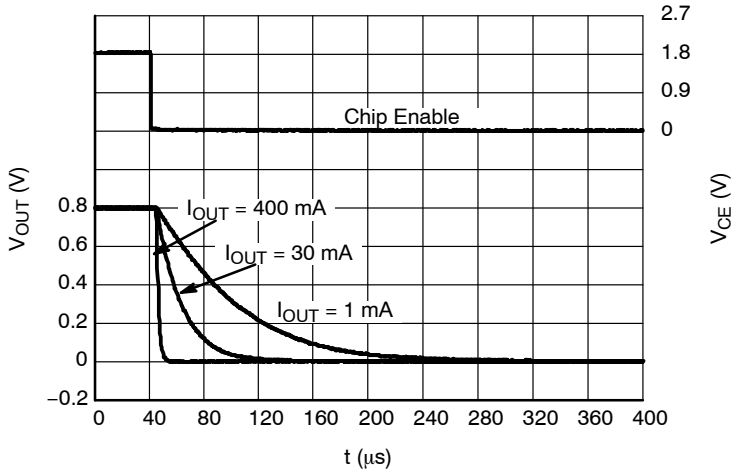


Figure 42. Shutdown, 0.8 V Version, V_{IN} = 1.8 V

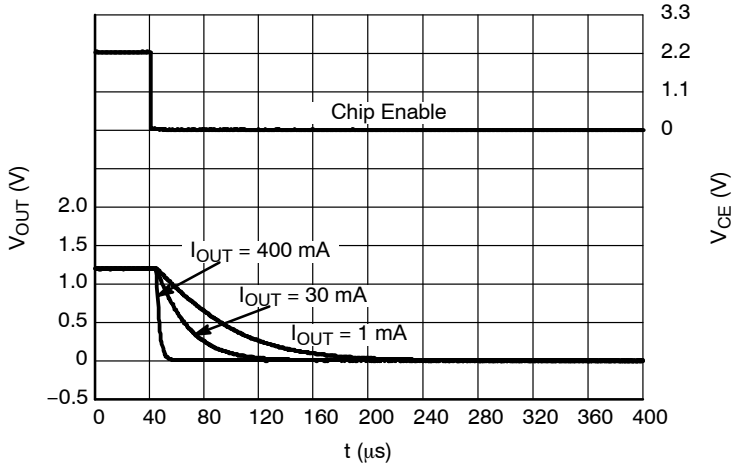


Figure 43. Shutdown, 1.2 V Version, V_{IN} = 2.2 V

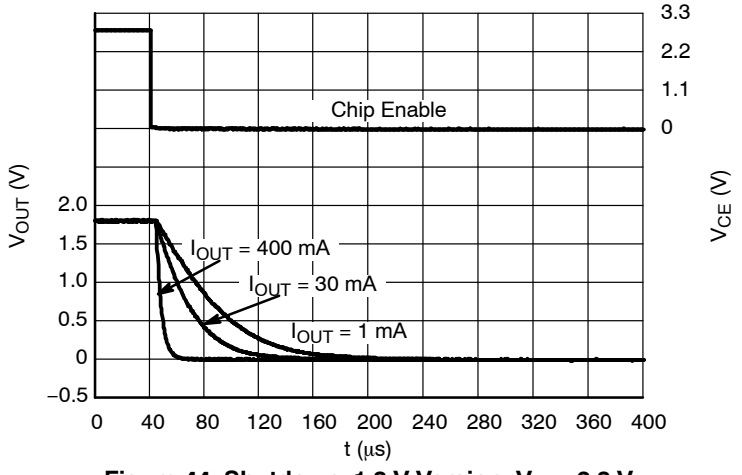


Figure 44. Shutdown, 1.8 V Version, V_{IN} = 2.8 V

APPLICATION INFORMATION

A typical application circuits for NCP4686 series is shown in Figure 45.

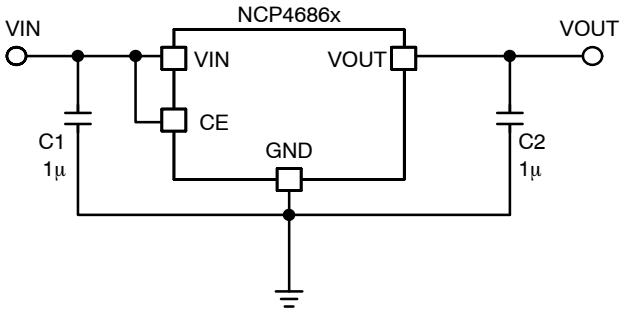


Figure 45. Typical Application Schematics

Input Decoupling Capacitor (C1)

A 1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4686. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Constant Slope Circuit

The constant slope circuit is used as a soft start circuit that allows the output voltage to start up slowly with a defined slope. This circuit minimizes inrush current at start up and also prevents overshoot of the output voltage at start up. The Constant slope circuit is fully built in and no external component is needed. Since the Start up time and output voltage slope is defined internally, there is no way to change it. Starting up into bigger output capacitors doesn't cause problems due to the combination of the constant slope and current limit circuits.

Current Limit

This regulator includes fold−back type current limit circuit. This type of protection doesn't limit current up to current capability in normal operation, but when over current occurs, the output voltage and current decrease until the over current condition ends. Typical characteristics of this protection type can be observed in the Output Voltage versus Output Current graphs shown in the typical characteristics chapter of this datasheet.

Output Discharger

The NCP4686D version includes a transistor between VOUT and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

PCB Layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

ORDERING INFORMATION

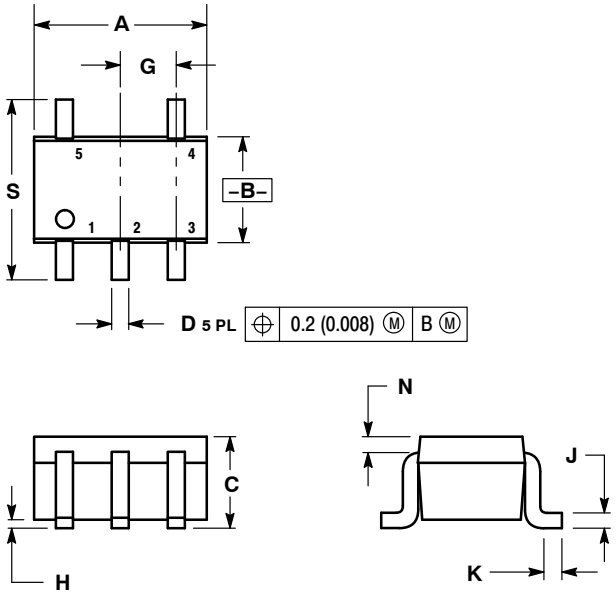
Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP4686DSN08T1G	0.8 V	Auto discharge	CAB	SOT23−5 (Pb−Free)	3000 / Tape & Reel
NCP4686DSN10T1G	1.0 V	Auto discharge	CAD	SOT23−5 (Pb−Free)	3000 / Tape & Reel
NCP4686DSN12T1G	1.2 V	Auto discharge	CAF	SOT23−5 (Pb−Free)	3000 / Tape & Reel
NCP4686DSN18T1G	1.8 V	Auto discharge	CAM	SOT23−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*To order other package and voltage variants, please contact your ON Semiconductor sales representative.

PACKAGE DIMENSIONS

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE K

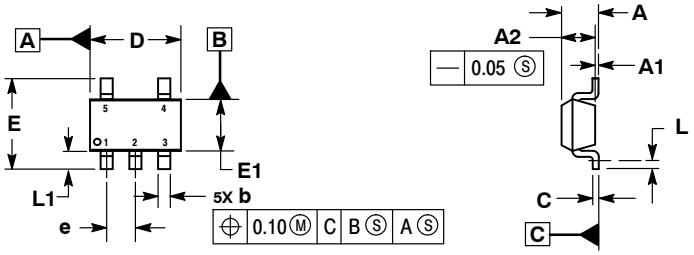


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

PACKAGE DIMENSIONS

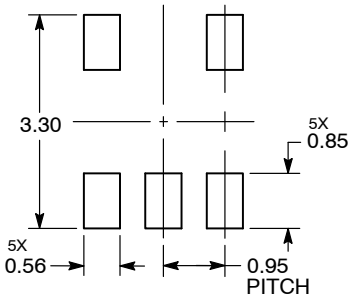
SOT−23 5−LEAD
CASE 1212−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*

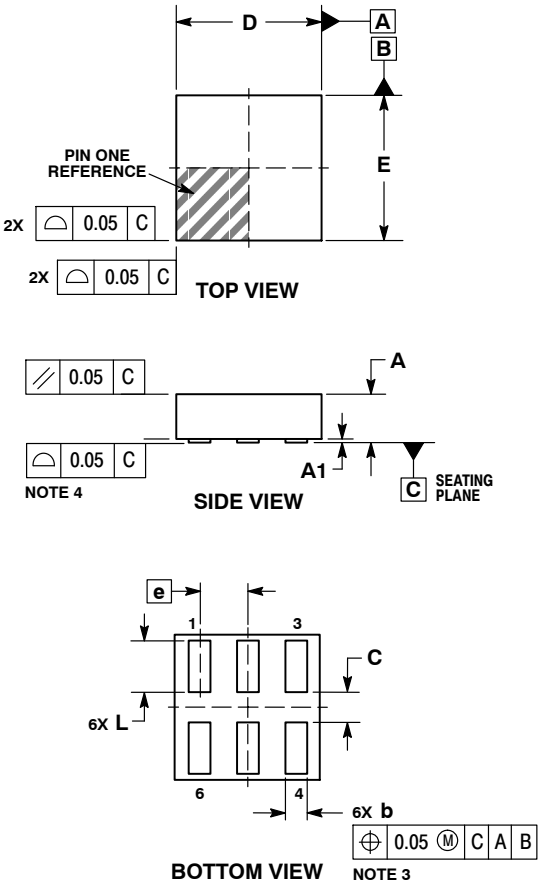


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

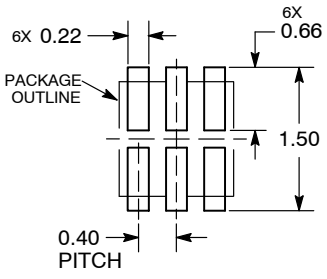
XDFN6 1.2x1.2, 0.4P
CASE 711AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25mm FROM TERMINAL TIPS.
4. COPLANARITY APPLIES TO ALL OF THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.13	0.23
C	0.20	0.30
D	1.20 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.37	0.48

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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