MP92265

18V, 5A, 500kHz, High-Efficiency, Synchronous, Step-Down Converter in 8-Pin TSOT23

DESCRIPTION

The MP92265 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP92265 offers a very compact solution that achieves 5A of output current with excellent load and line regulation over a wide input supply range.

The MP92265 uses synchronous mode operation to achieve high efficiency over the output current load range. Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP92265 requires a minimal number of readily available, standard, external components and is available in a space-saving, 8-pin, TSOT23 package.

FEATURES

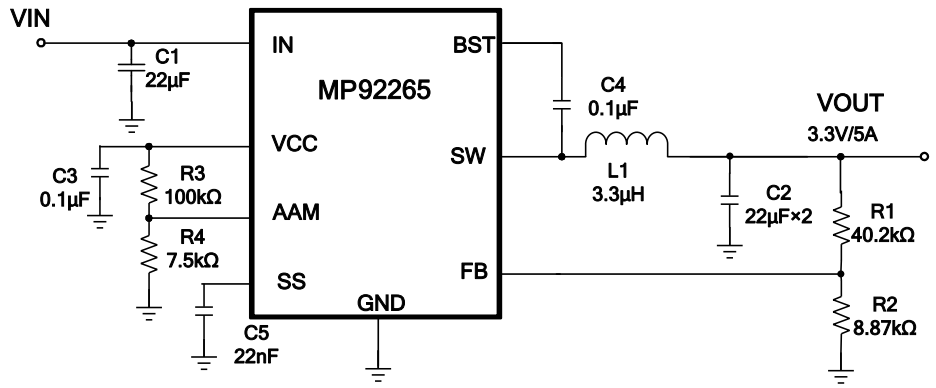
- Wide 6V to 18V Operating Input Range
- Adjustable Output Voltage as Low as 0.6V
- Low 47mΩ/18mΩ $R_{DS(ON)}$ of Internal Power MOSFETs
- High Efficiency up to 97%
- Fixed 500kHz Switching Frequency
- External Programmable Soft-Start Time
- 1% Reference Accuracy at Room Temperature
- External Programmable AAM Power-Save Mode
- Over-Current Protection (OCP) with Hiccup Mode
- Available in a TSOT23-8 Package

APPLICATIONS

- Flat-Panel Televisions and Monitors
- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Distributed Power Systems

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP92265GJ	TSOT23-8	*See Below*

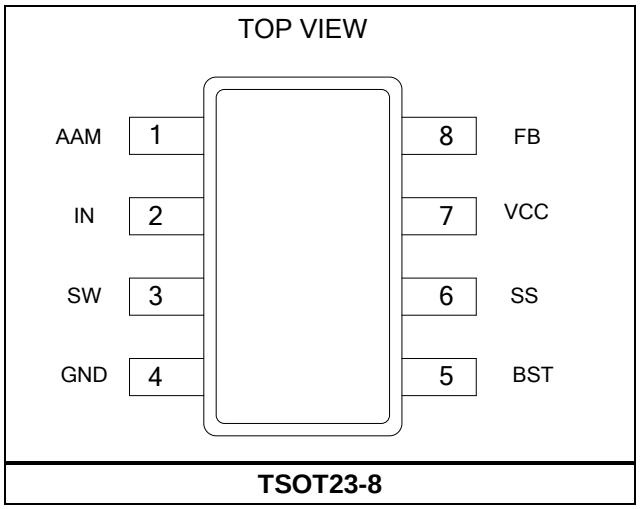
* For Tape & Reel, add suffix –Z (e.g. MP2670GQ–Z)

TOP MARKING

|ATNY

ATN: Product code of MP92265GJ
Y: Year code

PACKAGE REFERENCE



TSOT23-8

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{SW} ..... -0.3V (-5V for <10ns) to V_{IN} + 0.3V (23V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
All other pins ..... -0.3V to 5.5V
Continuous power dissipation (T_A = +25°C) (2)
TSOT23-8 ..... 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 6V to 18V
Output voltage (V_{OUT}) ..... 0.6V to min. of V_{IN} x D_{MAX}
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (quiescent)	I_Q	V_{FB} = 0.7V		320	400	μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		47		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5V		18		mΩ
Switch leakage	SW_{LKG}				2	μA
Current limit	I_{LIMIT}	Under 40% duty cycle	6.5	9.5		A
Oscillator frequency	F_{SW}	V_{FB} = 0.48V	380	500	580	kHz
Foldback frequency	F_{FB}	V_{FB} < 300mV		0.8		F_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	90	95		%
Minimum on time (6)	T_{ON_MIN}			50		ns
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
Feedback voltage	V_{FB}		591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		4.8	5.3	5.8	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			1		V
Soft-start current	I_{SS}	10% to 90% output voltage	8	11	14	μA
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{SD_HYS}			20		°C

NOTES:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by engineering sample characterization.

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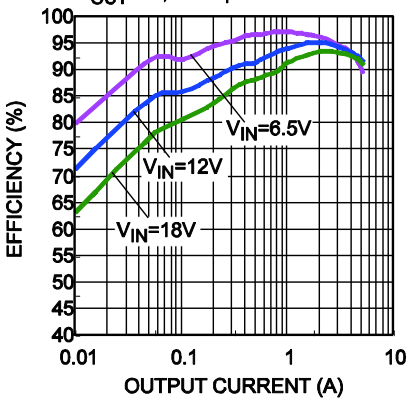
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board described in the Design Example section.

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

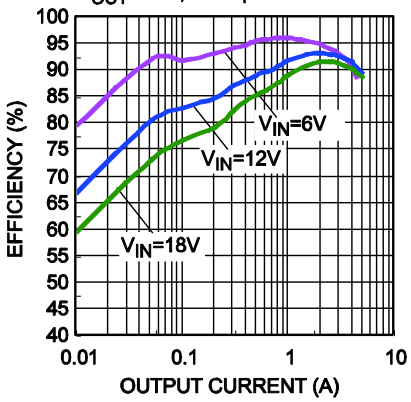
Efficiency vs. Load Current

V_{OUT}=5V, L=4.7µH



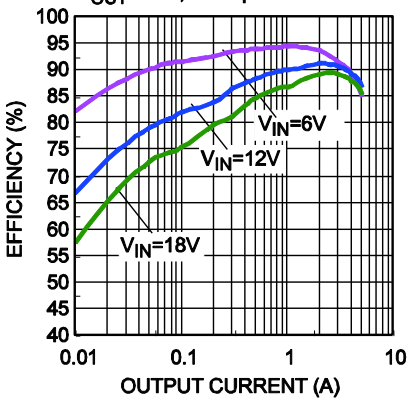
Efficiency vs. Load Current

V_{OUT}=3.3V, L=3.3µH



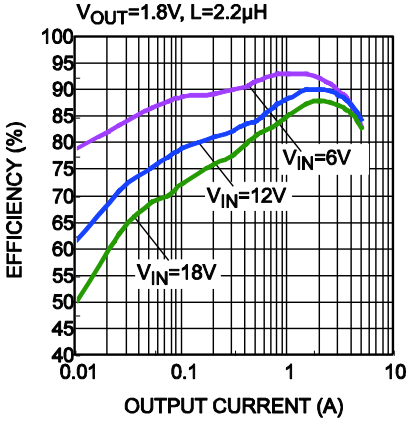
Efficiency vs. Load Current

V_{OUT}=2.5V, L=2.2µH



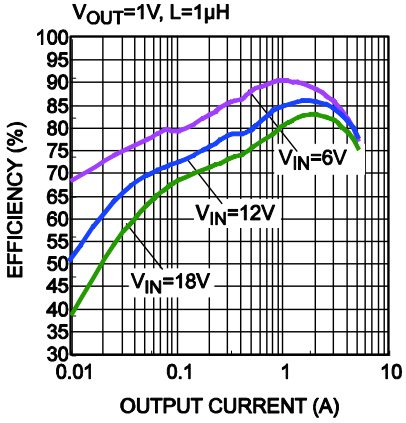
Efficiency vs. Load Current

V_{OUT}=1.8V, L=2.2µH

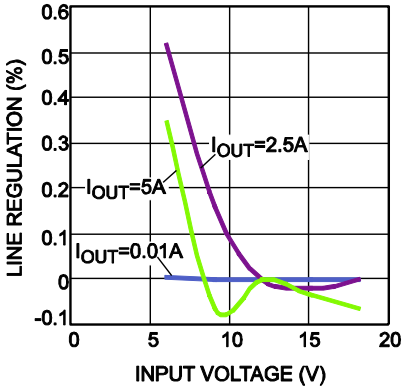


Efficiency vs. Load Current

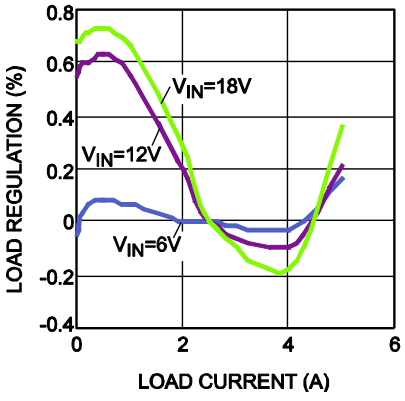
V_{OUT}=1V, L=1µH



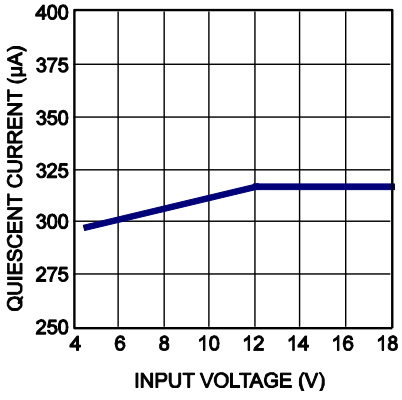
3.3V Line Regulation vs. Input Voltage



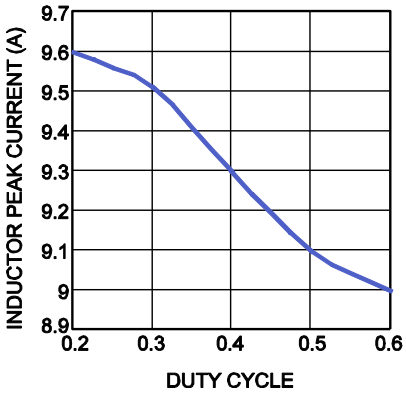
3.3V Load Regulation vs. Load Current



Quiescent Current vs. Input Voltage



IPEAK vs. Duty Cycle



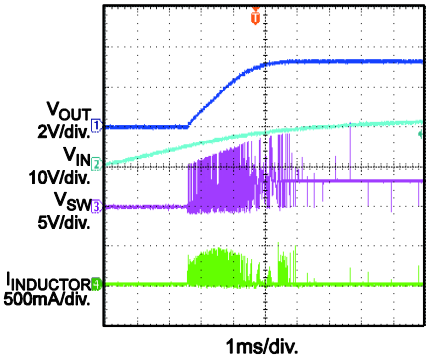
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

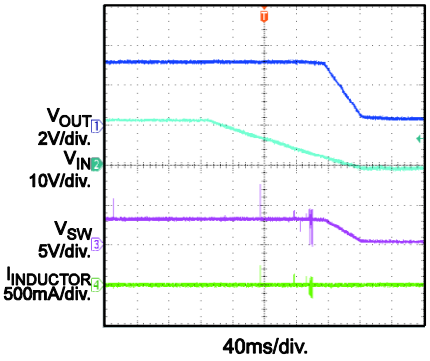
Performance waveforms are tested on the evaluation board described in the Design Example section.

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

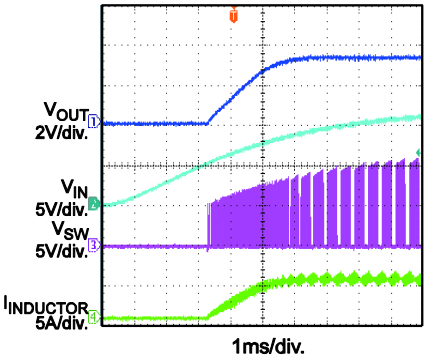
Start-Up through Input Voltage
I_{OUT}=0A



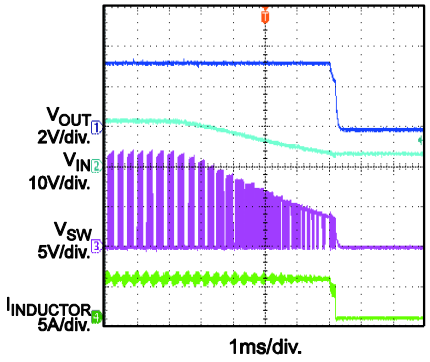
Shutdown through Input Voltage
I_{OUT}=0A



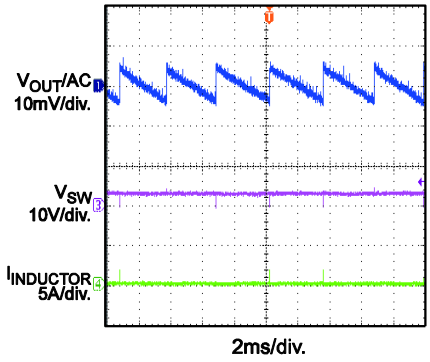
Start-Up through Input Voltage
I_{OUT}=5A



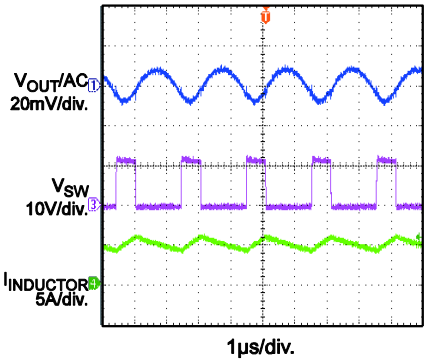
Shutdown through Input Voltage
I_{OUT}=5A



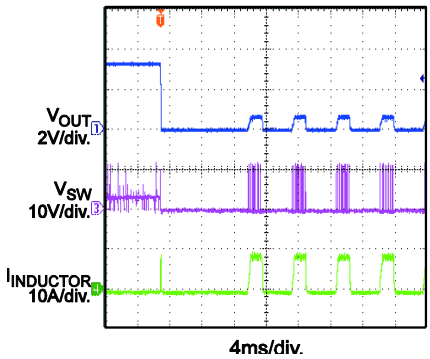
Output Ripple
I_{OUT}=0A



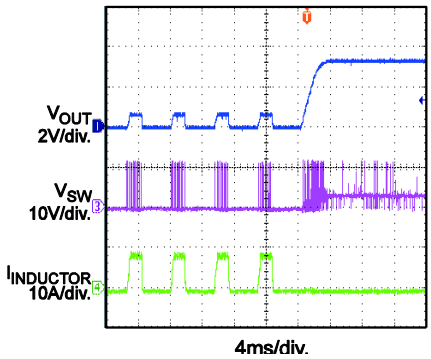
Output Ripple
I_{OUT}=5A



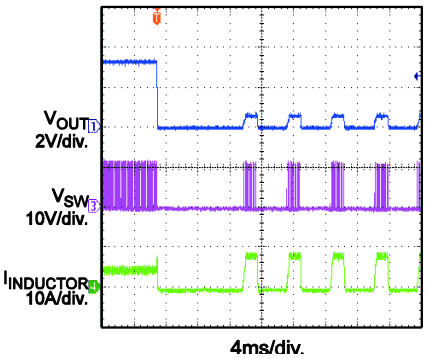
Short-Circuit Entry
I_{OUT}=0A



Short-Circuit Recovery
I_{OUT}=0A



Short-Circuit Entry
I_{OUT}=5A



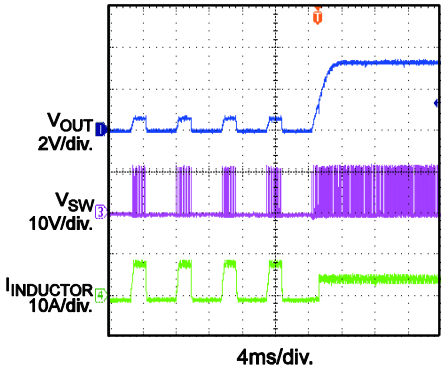
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

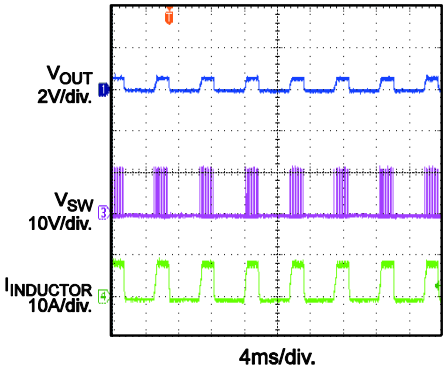
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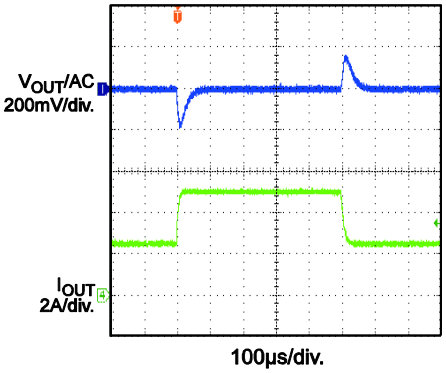
Short-Circuit Recovery
I_{OUT}=5A



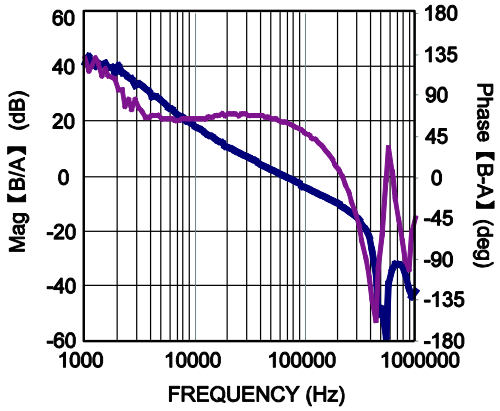
Short-Circuit Steady State



Transient Response
I_{OUT}=2.5A-5A, 2.5A/µs



Bode Plot
I_{OUT}=2.5A



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PIN FUNCTIONS

Pin #	Name	Description
1	AAM	**Advanced asynchronous mode.** Connect to the tap of two resistor dividers from VCC to GND to force the MP92265 into non-synchronous mode under light loads. Drive AAM high (i.e.: connect to VCC) to force the MP92265 into continuous conduction mode (CCM).
2	IN	**Supply voltage.** The MP92265 operates from a 6V to 18V input rail. A capacitor (C1) is required to decouple the input rail. Connect IN using a wide PCB trace.
3	SW	**Switch output.** Connect SW using a wide PCB trace.
4	GND	**Power ground.** GND requires special consideration during PCB layout. Connect GND with copper traces and vias.
5	BST	**Bootstrap.** A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
6	SS	**Soft start.** Connect an external capacitor to SS to program the soft-start time for the switch-mode regulator.
7	VCC	**Bias supply.** Decouple VCC with a 0.1μF to 0.22μF capacitor.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 480mV to prevent current limit runaway during a short-circuit fault condition.

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BLOCK DIAGRAM

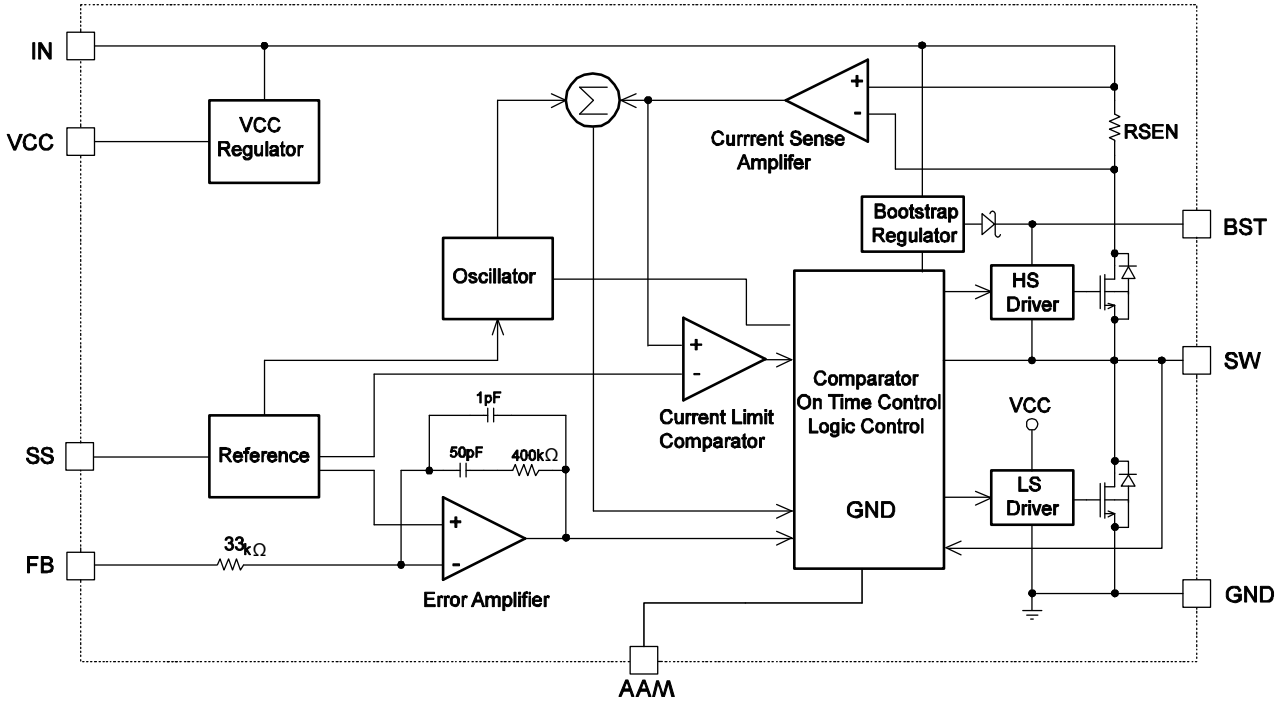


Figure 1: Functional Block Diagram

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OPERATION

The MP92265 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP92265 offers a very compact solution that achieves 5A of output current with excellent load and line regulation over a wide input supply range.

The MP92265 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until the current reaches the value set by the COMP voltage (V_{COMP}). When the power is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the value set by the COMP value in 95% of one PWM period, the power MOSFET is forced off.

VCC Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. The MP92265 requires a 0.1µF ceramic capacitor to decouple noise.

AAM Operation

The MP92265 has advanced asynchronous mode (AAM), which is an internal power-save mode for light-load operation (see Figure 2). Connect AAM to the tap of two resistor dividers from VCC to GND to set the AAM threshold. Under heavy-load condition, V_{COMP} is higher than V_{AAM}. When the clock goes high, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. The internal clock resets whenever V_{COMP} is higher than V_{AAM}.

Under light-load condition, the value of V_{COMP} becomes lower. When V_{COMP} is less than V_{AAM}, and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, so the MP92265 skips some pulses for pulse-frequency modulation (PFM) mode and achieves light-load power save.

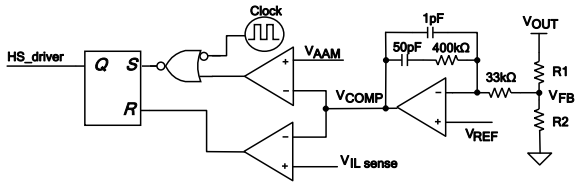


Figure 2: Simplified AAM Control Logic

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal 0.6V reference (REF) and generates a COMP voltage as the output. COMP controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP92265 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 5.3V, while its falling threshold is 4.3V.

Soft Start (SS)

Adjust the soft-start time by connecting a capacitor from SS to ground. When the soft start begins, an internal 11µA current source charges the external capacitor. During soft start, the soft-start capacitor connects to the non-inverting input of the error amplifier. The soft-start period continues until the voltage on the soft-start capacitor exceeds the 0.6V reference. Then the non-inverting amplifier uses the reference voltage as the input. Calculate the soft-start time with Equation (1):

$$T_{SS}(ms) = \frac{0.6V \times C_{SS}(nF)}{11\mu A} \quad (1)$$

Over-Current Protection (OCP) and Hiccup

The MP92265 has a cycle-by-cycle over-current limit, which can limit the inductor current in the event of an output overload or short circuit (SC). If the overload or SC events last long enough, the FB voltage can drop below the under-voltage (UV) threshold (typically 30% of the reference). Once UV is triggered, the MP92265 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is

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reduced greatly to alleviate thermal issues and to protect the regulator. The MP92265 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the temperature of the silicon reaches 150°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.6V with a hysteresis of 350mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 3). If V_{BST} - V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4.

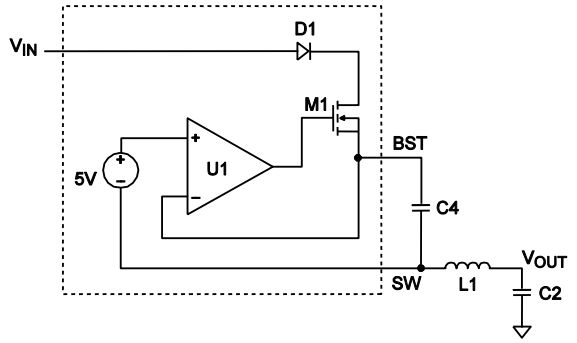


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN} exceeds its thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Two events can shut down the chip: V_{IN} low and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application on page 1). The feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. Choose a value for R1 first, and then calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (2)$$

The feedback network is highly recommended (see Figure 4).

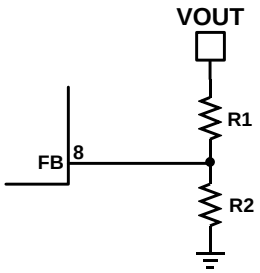


Figure 4: Feedback Network

Table 1 lists recommended resistor and capacitor values for common output voltages.

Table 1: Component Selection for Common Output Voltages (7)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	120	180
1.2	120	120
1.35	100	80.6
1.5	80.6	53.6
1.8	80.6	40.2
2.5	80.6	25.5
3.3	40.2	8.87
5	40.2	5.49

NOTE:

7) The recommended parameters are based on a 500kHz switching frequency. Different output inductors and capacitors can affect the recommended values of R1 and R2. For the other components' parameters, please refer to the Typical Application Circuits on page 15.

Selecting the Inductor

Use a 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current for most applications.

For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can then be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

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The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP92265 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

The BST voltage may become insufficient in some particular conditions. In these cases, an external bootstrap diode can enhance the efficiency of the regulator and help prevent output ripple caused by BST voltage insufficiency during PFM operation at light load. For better efficiency, a diode is needed if the following condition occurs :

- Duty cycle is large: Duty = $\frac{V_{OUT}}{V_{IN}}$ > 75%

To avoid ripple caused by a BST refresh, a diode is needed if the following condition occurs:

- V_{IN} - V_{OUT} < 2.6V

In these cases, it is recommended to add an external BST diode from VCC to BST (see Figure 5).

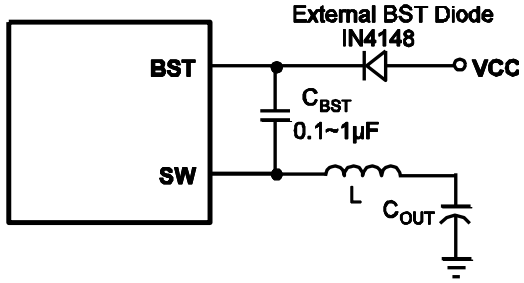


Figure 5: Optional External Bootstrap Diode

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1μF to 1μF.

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PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect the input capacitor to IN using the shortest and widest trace possible.
3. Ensure all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas such as FB.

NOTE:

8) The recommended layout is based on the Typical Application circuit on page 15.

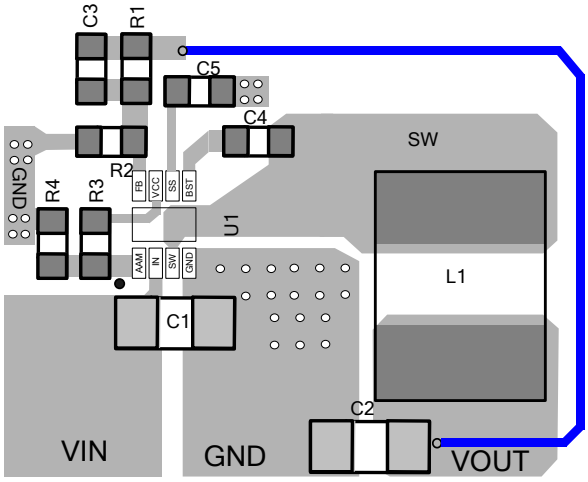


Figure 6: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	5A

The detailed application schematic is shown in Figure 7 through Figure 9. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

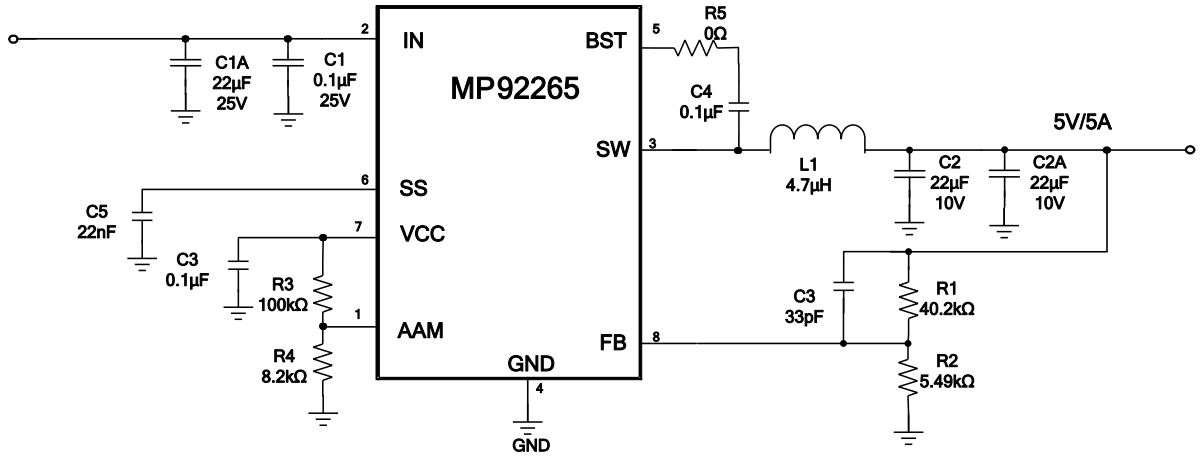


Figure 7: 12 V_{IN}, 5V/5A

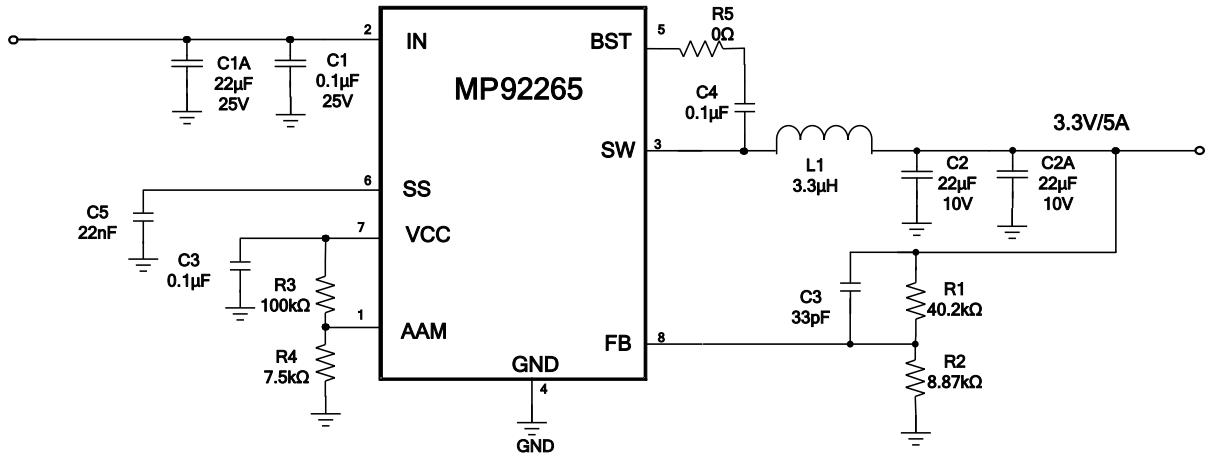


Figure 8: 12 V_{IN}, 3.3V/5A

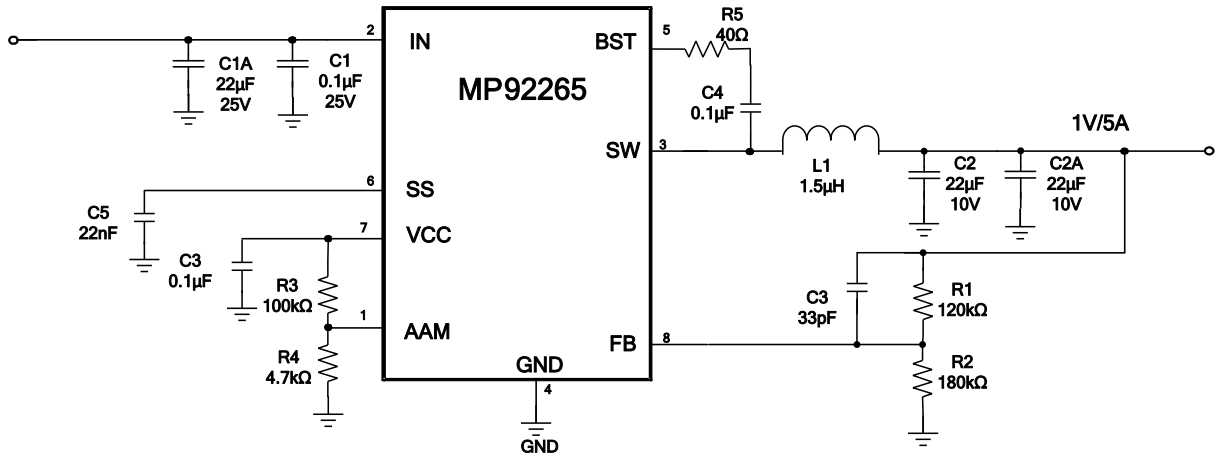


Figure 9: 12 V_{IN}, 1V/5A [9]

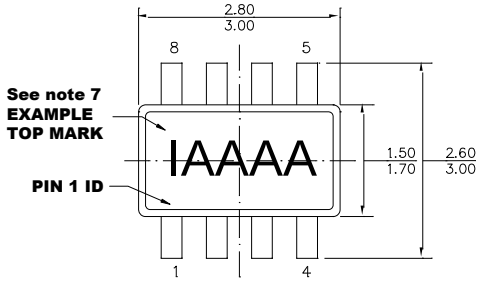
NOTE:

9) It is recommend to use a 400Ω BST resistor for 12V to 1V specs to improve load regulation.

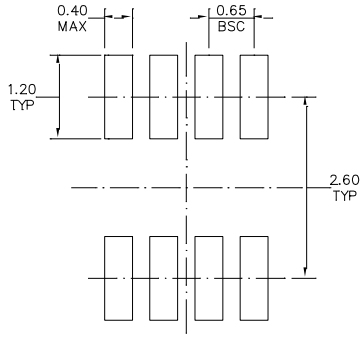
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PACKAGE INFORMATION

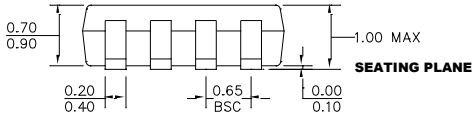
TSOT23-8



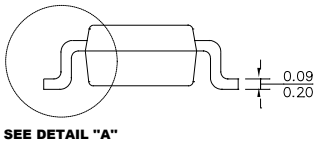
TOP VIEW



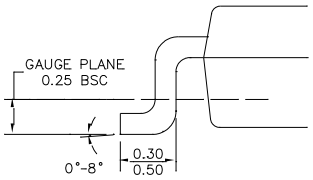
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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