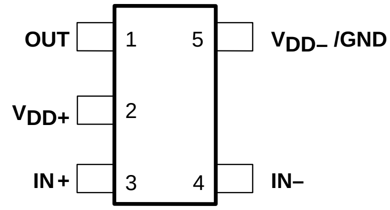
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 15 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High Gain Bandwidth . . . 2 MHz at V_{DD} = 5 V with 600 Ω Load**
- **High Slew Rate . . . 1.6 V/μs at V_{DD} = 5 V**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**

**DBV PACKAGE
(TOP VIEW)**



description

The TLV2731 is a single low-voltage operational amplifier available in the SOT-23 package. It offers 2 MHz of bandwidth and 1.6 V/μs of slew rate for applications requiring good ac performance. The device exhibits rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV2731 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2731, exhibiting high input impedance and low noise, is excellent for small-signal conditioning of high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). The device can also drive 600-Ω loads for telecom applications.

With a total area of 5.6mm^2, the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

AVAILABLE OPTIONS

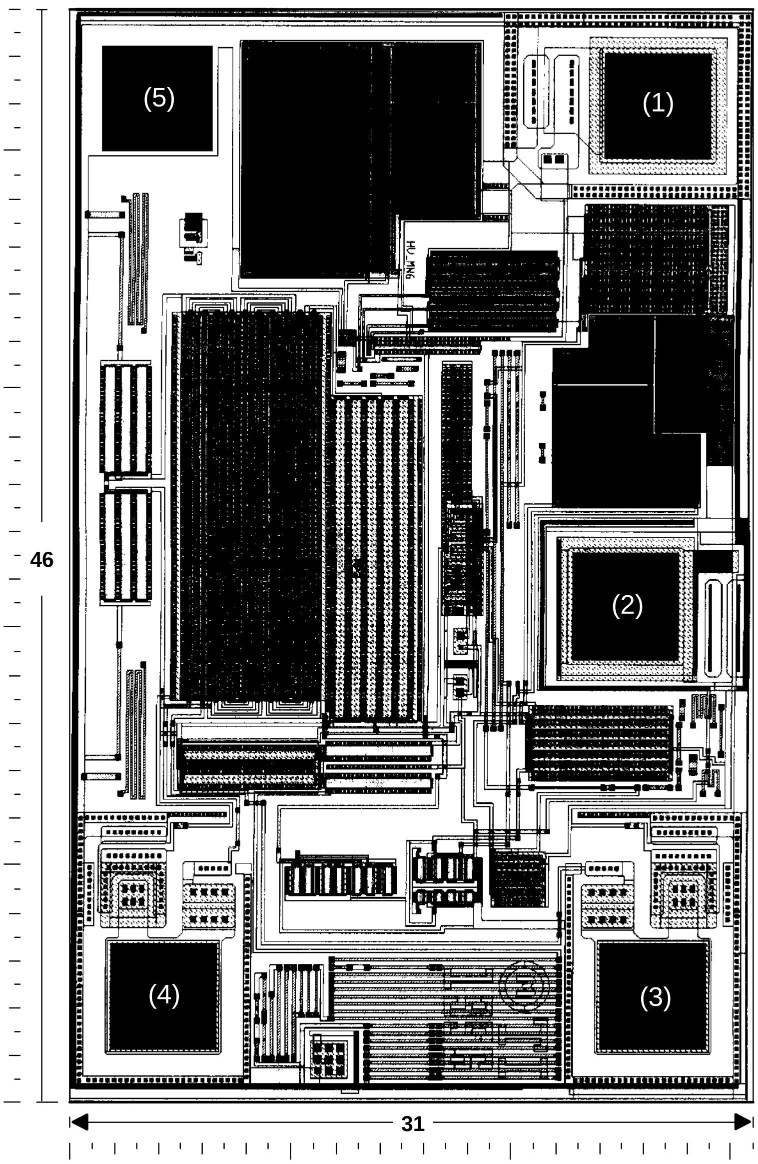
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡ (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2731CDBV	VALC	TLV2731Y
−40°C to 85°C	3 mV	TLV2731IDBV	VALI	

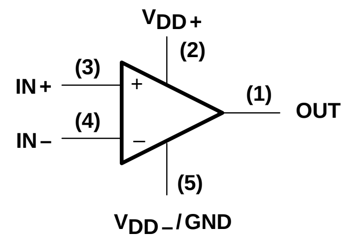
† The DBV package available in tape and reel only.
‡ Chip forms are tested at T_A = 25°C only.

TLV2731Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2731C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

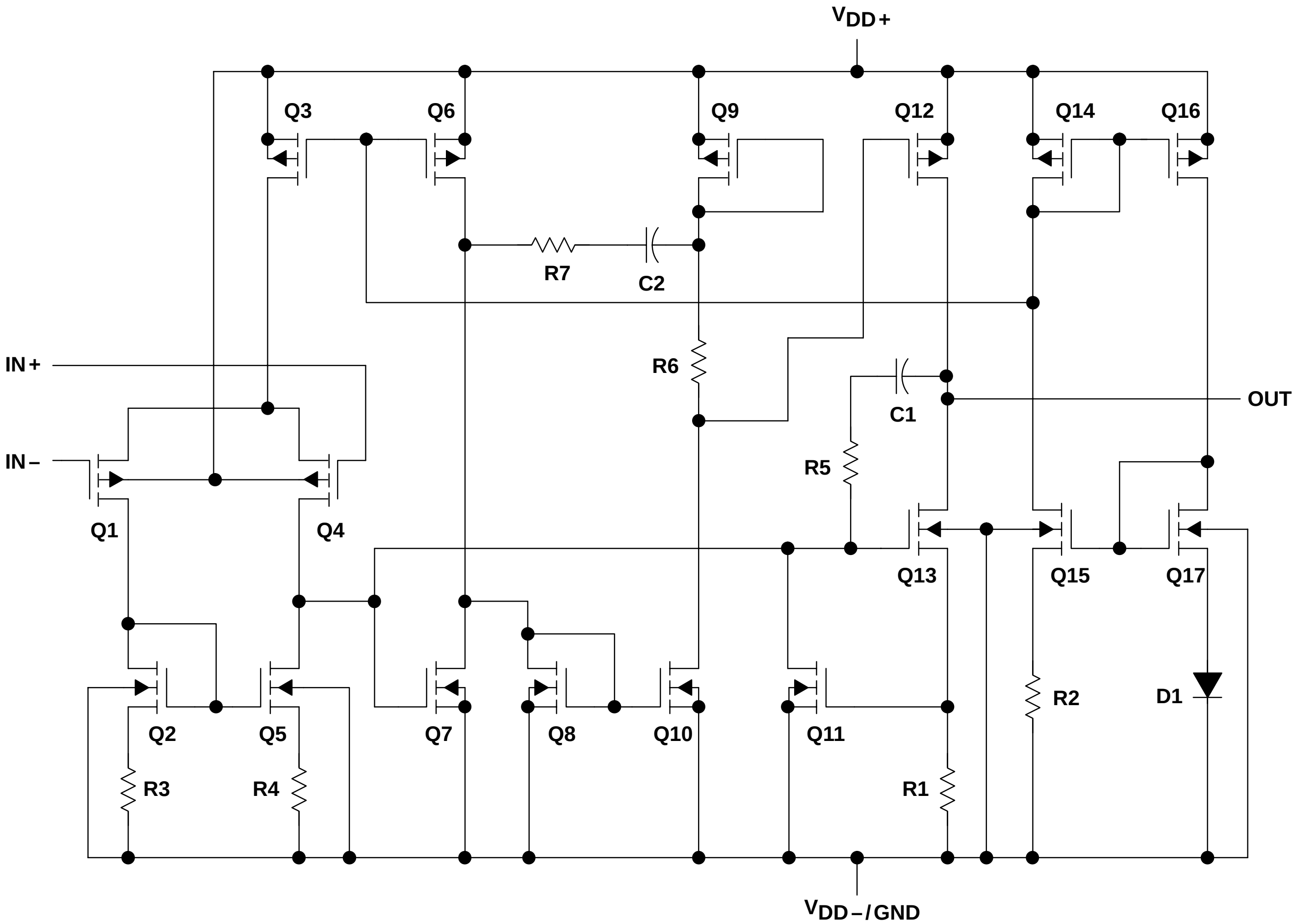
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic



COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . -0.3 V to V_{DD}
Input current, I_I (each input) . . . . ±5 mA
Output current, I_O . . . . ±50 mA
Total current into V_{DD+} . . . . ±50 mA
Total current out of V_{DD-} . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: TLV2731C . . . . 0°C to 70°C
TLV2731I . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2731C		TLV2731I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	–40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2731C MIN	TLV2731C TYP	TLV2731C MAX	TLV2731I MIN	TLV2731I TYP	TLV2731I MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm1.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	Full range		0.7	3		0.7	3	mV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5	60		0.5	60	pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1	60		1	60	pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\lvert V_{IO}\rvert \le 5$ mV	25°C	0 to 2	–0.3 to 2.2		0 to 2	–0.3 to 2.2		V
			Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = –1 mA	25°C		2.87			2.87		V
		I_{OH} = –2 mA	25°C		2.74			2.74		
			Full range	2.3			2.3			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 µA	25°C		100			100		
			Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V, R_L = 600 Ω‡	25°C	1	1.6		1	1.6		V/mV
			Full range	0.3			0.3			
		V_{IC} = 1.5 V, V_O = 1 V to 2 V, R_L = 1 MΩ‡	25°C		250			250		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz	25°C		6			6		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 1	25°C		156			156		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω	25°C	60	70		60	70		dB
			Full range	55			55			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	70	96		70	96		dB
			Full range	70			70			
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		750	1200		750	1200	µA
			Full range			1500			1500	

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is – 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 600 Ω‡,	25°C	0.75	1.25		0.75	1.25		V/µs
				Full range	0.5			0.5			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		105			105		nV/√Hz
		f = 1 kHz		25°C		16			16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.4			1.4		µV
		f = 0.1 Hz to 10 Hz		25°C		1.5			1.5		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 2 V, f = 20 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.285%			0.285%		
			A_V = 10			7.2%			7.2%		
		V_O = 1 V to 2 V, f = 20 kHz, R_L = 600 Ω§	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.098%			0.098%		
			A_V = 100			0.13%			0.13%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 600 Ω‡,	25°C		1.9			1.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω‡,	A_V = 1, C_L = 100 pF‡	25°C		60			60		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		0.9			0.9		µs
			To 0.01%			1.5			1.5		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡,	C_L = 100 pF‡	25°C		50°			50°		
	Gain margin			25°C		8			8		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V
§ Referenced to 0 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C MIN	TLV2731C TYP	TLV2731C MAX	TLV2731I MIN	TLV2731I TYP	TLV2731I MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm 2.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		Full range		0.7	3		0.7	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $\lvert V_{IO}\rvert \le 5$ mV		25°C	0 to 4	–0.3 to 4.2		0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.7			0 to 3.7			
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA		25°C		4.9			4.9		V
		$I_{OH} = -4$ mA		25°C		4.6			4.6		
				Full range	4.3			4.3			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V, $I_{OL} = 500\ \mu A$		25°C		80			80		mV
		$V_{IC} = 2.5$ V, $I_{OL} = 1$ mA		25°C		160			160		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 600\ \Omega$‡	25°C	1	1.5		1	1.5		V/mV
				Full range	0.3			0.3			
			$R_L = 1\ M\Omega$‡	25°C		400			400		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF
z_o	Closed-loop output impedance	f = 1 MHz, $A_V = 1$		25°C		138			138		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V, $R_S = 50\ \Omega$		25°C	60	70		60	70		dB
				Full range	55			55			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	70	96		70	96		dB
				Full range	70			70			
I_{DD}	Supply current	$V_O = 2.5$ V, No load		25°C		850	1300		850	1300	μA
				Full range			1600			1600	

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C MIN	TLV2731C TYP	TLV2731C MAX	TLV2731I MIN	TLV2731I TYP	TLV2731I MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 600 Ω‡,	25°C	1	1.6		1	1.6		V/µs
				Full range	0.7			0.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100			100		nV/√Hz
		f = 1 kHz		25°C		15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.4			1.4		µV
		f = 0.1 Hz to 10 Hz		25°C		1.5			1.5		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 20 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.409%			0.409%		
			A_V = 10			3.68%			3.68%		
		V_O = 1.5 V to 3.5 V, f = 20 kHz, R_L = 600 Ω§	A_V = 1	25°C		0.018%			0.018%		
			A_V = 10			0.045%			0.045%		
			A_V = 100			0.116%			0.116%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 600 Ω‡,	25°C		2			2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω‡,	A_V = 1, C_L = 100 pF‡	25°C		300			300		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		0.95			0.95		µs
			To 0.01%			2.4			2.4		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡,	C_L = 100 pF‡	25°C		48°			48°		
	Gain margin			25°C		8			8		dB

† Full range is –40°C to 85°C.
‡ Referenced to 2.5 V
§ Referenced to 0 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2731Y MIN	TLV2731Y TYP	TLV2731Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD}\pm = \pm 1.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω			750		μV
I_{IO}	Input offset current				0.5	60	pA
I_{IB}	Input bias current				1	60	pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV, R_S = 50 Ω			–0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = –1 mA			2.87		V
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 μA			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 μA			100		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω†		1.6		V/mV
			R_L = 1 MΩ†		250		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			6		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 1			156		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 0, R_S = 50 Ω			70		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = 0, No load			96		dB
I_{DD}	Supply current	V_O = 0, No load			750		μA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TLV2731Y MIN	TLV2731Y TYP	TLV2731Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD}\pm = \pm 1.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω			710		μV
I_{IO}	Input offset current				0.5	60	pA
I_{IB}	Input bias current				1	60	pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le 5$ mV, R_S = 50 Ω			–0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = –1 mA			4.9		V
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 500 μA			80		mV
		V_{IC} = 2.5 V, I_{OL} = 1 mA			160		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω†		15		V/mV
			R_L = 1 MΩ†		400		
r_{id}	Differential input resistance				10^{12}		Ω
r_{ic}	Common-mode input resistance				10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz			6		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 1			138		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 0, R_S = 50 Ω			70		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = 0, No load			96		dB
I_{DD}	Supply current	V_O = 0, No load			850		μA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	1, 2 3, 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5, 6
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	7
V_I	Input voltage	vs Supply voltage vs Free-air temperature	8 9
V_{OH}	High-level output voltage	vs High-level output current	10, 13
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12, 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	15
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	16 17
V_O	Output voltage	vs Differential input voltage	18, 19
A_{VD}	Differential voltage amplification	vs Load resistance	20
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	21, 22 23, 24
z_o	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	29, 30 31
I_{DD}	Supply current	vs Supply voltage	32
SR	Slew rate	vs Load capacitance vs Free-air temperature	33 34
V_O	Inverting large-signal pulse response		35, 36
V_O	Voltage-follower large-signal pulse response		37, 38
V_O	Inverting small-signal pulse response		39, 40
V_O	Voltage-follower small-signal pulse response		41, 42
V_n	Equivalent input noise voltage	vs Frequency	43, 44
	Noise voltage (referred to input)	Over a 10-second period	45
THD + N	Total harmonic distortion plus noise	vs Frequency	46
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	47 48
	Gain margin	vs Load capacitance	49, 50
ϕ_m	Phase margin	vs Frequency vs Load capacitance	21, 22 51, 52
B_1	Unity-gain bandwidth	vs Load capacitance	53, 54

TYPICAL CHARACTERISTICS

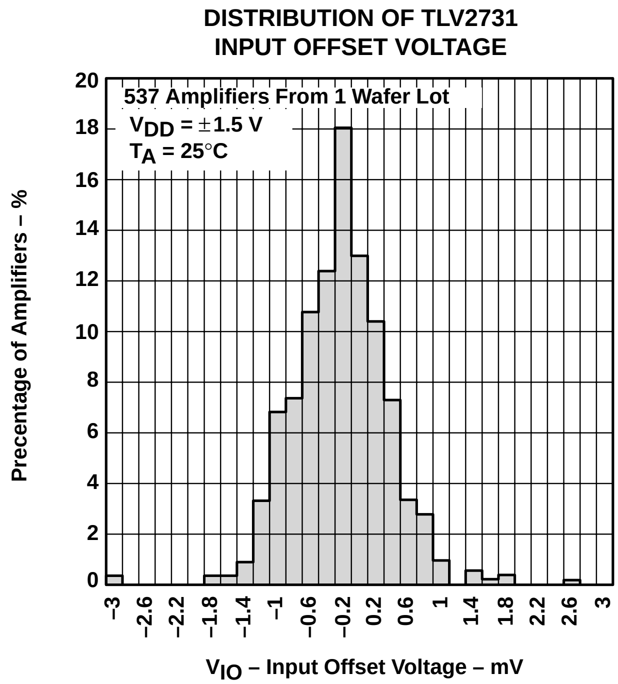


Figure 1

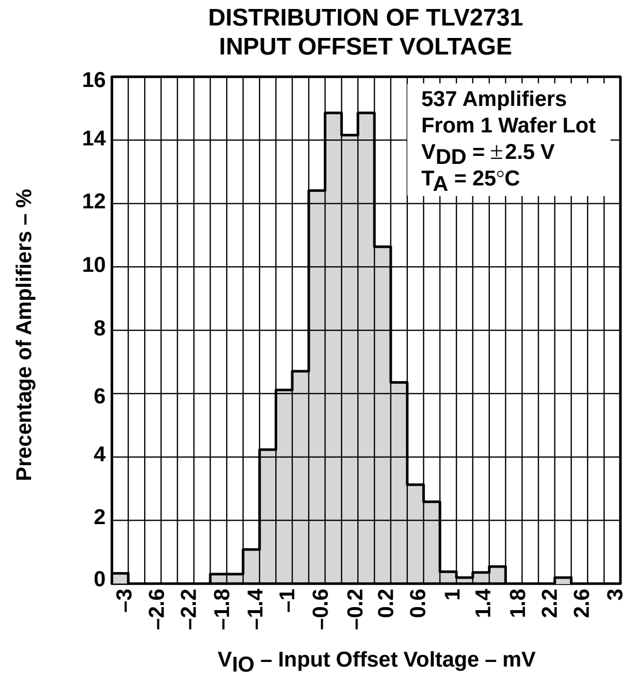


Figure 2

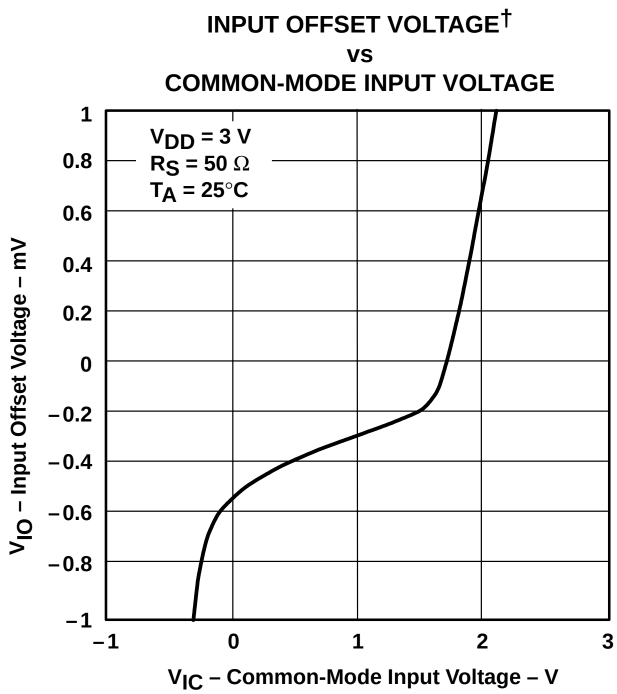


Figure 3

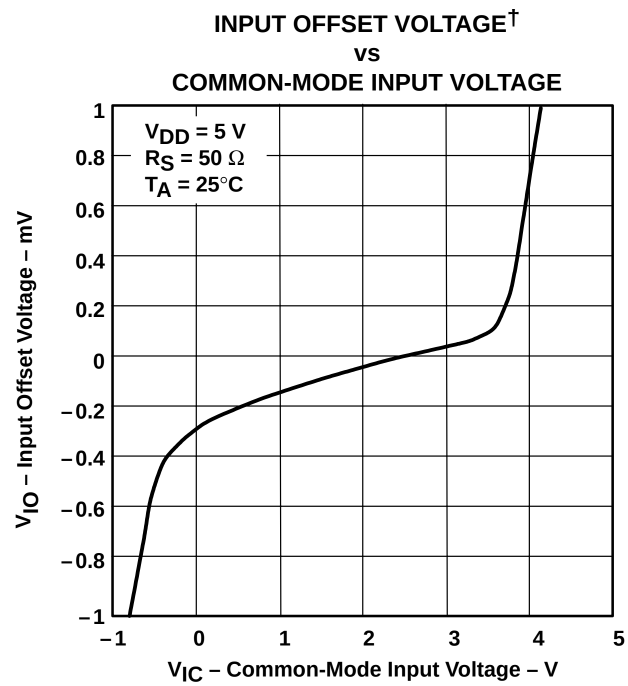


Figure 4

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

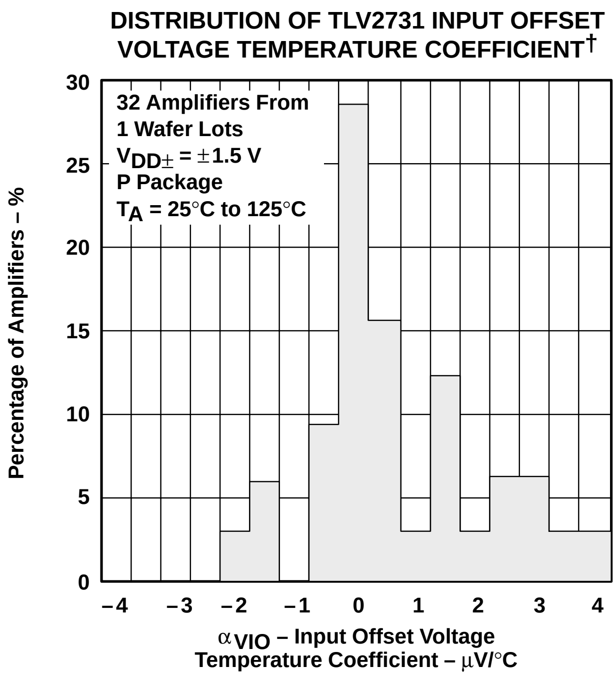


Figure 5

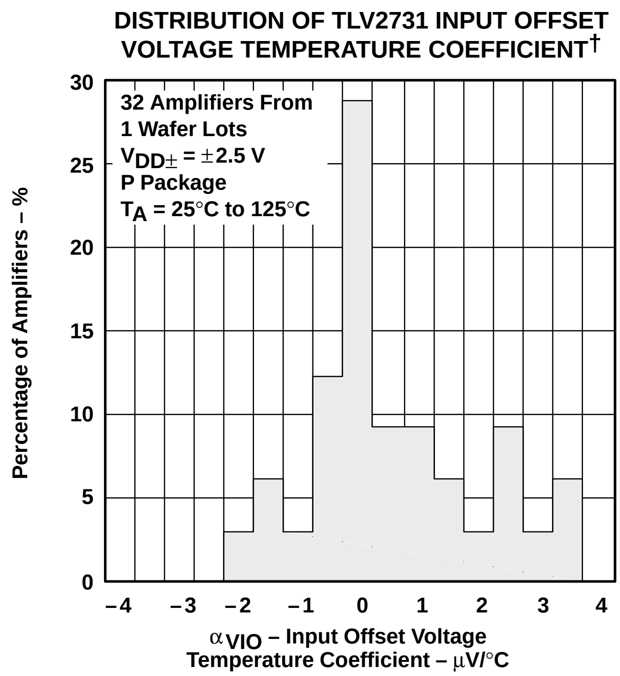


Figure 6

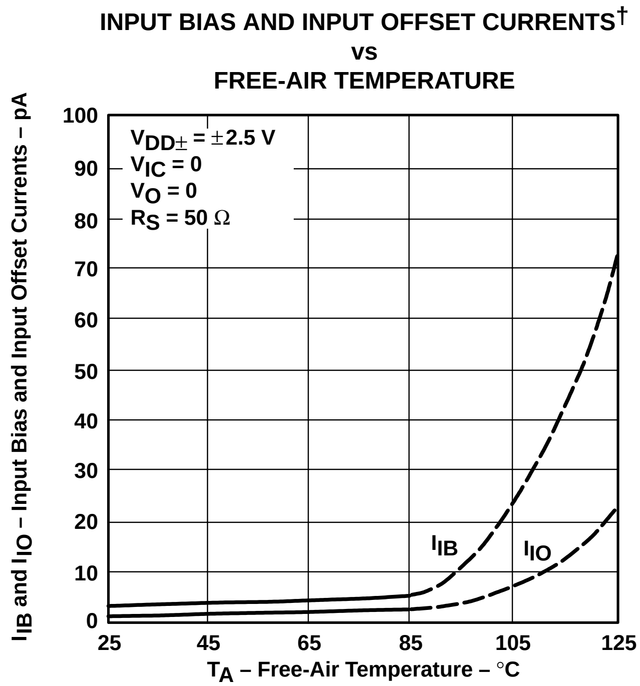


Figure 7

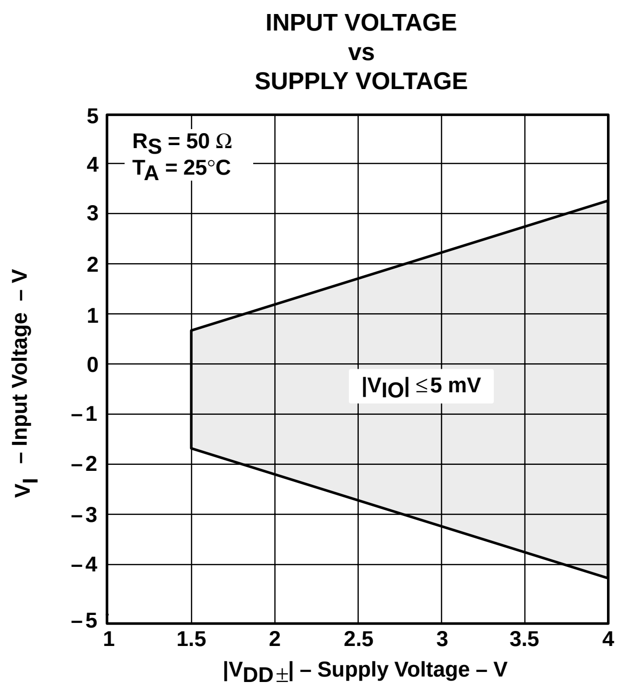


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

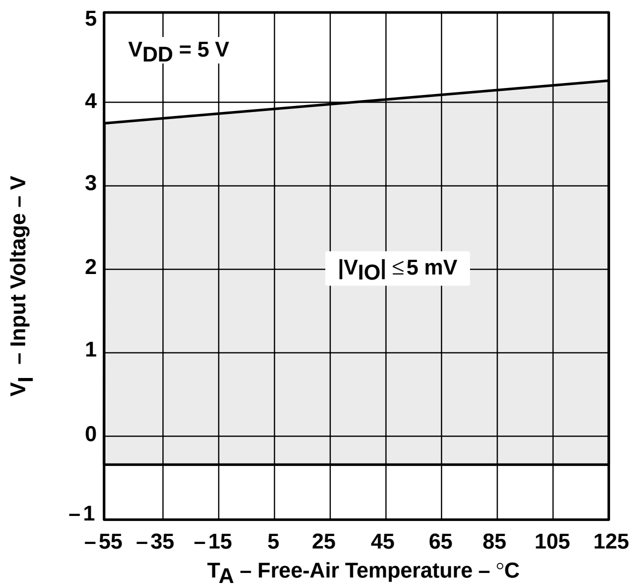


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

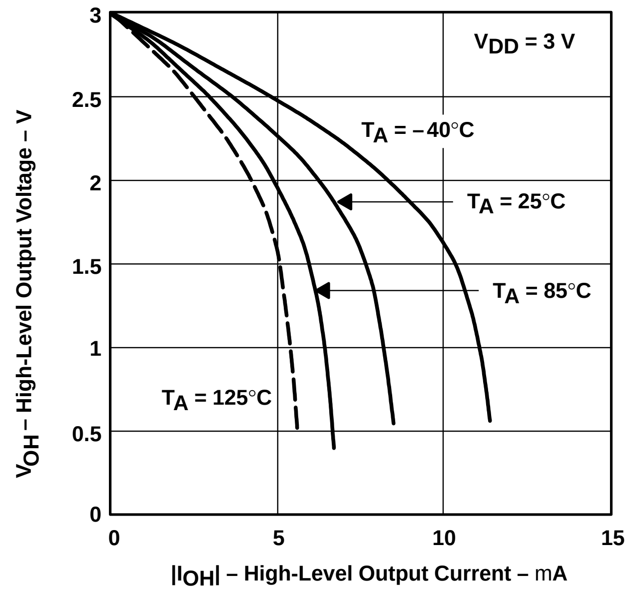


Figure 10

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

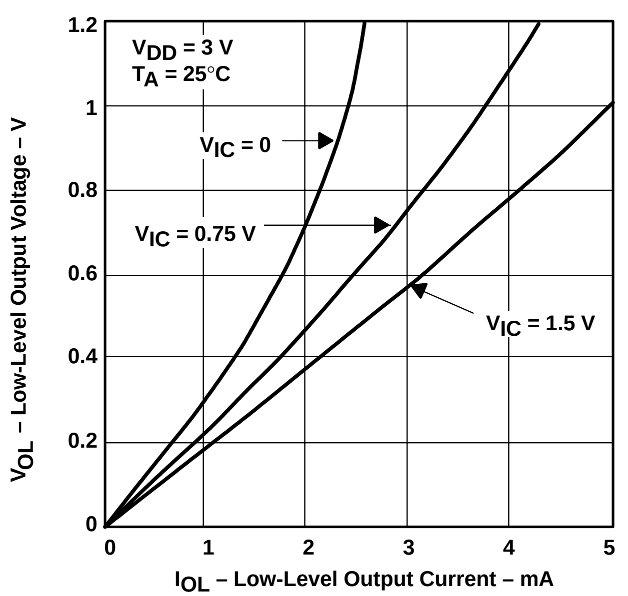


Figure 11

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

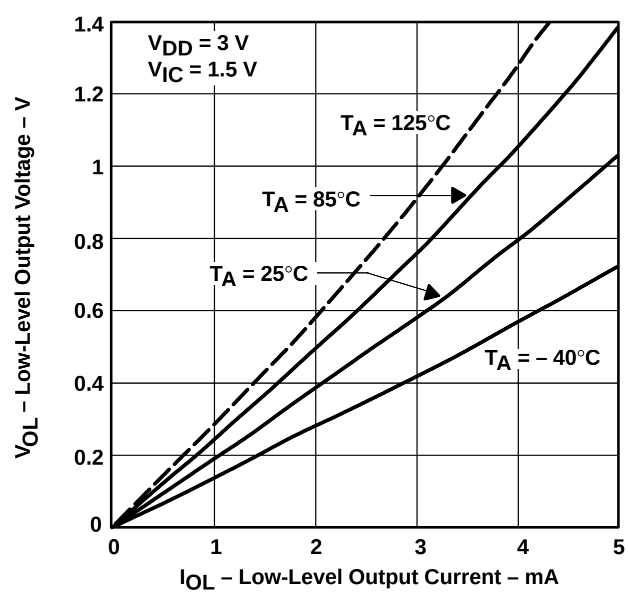


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

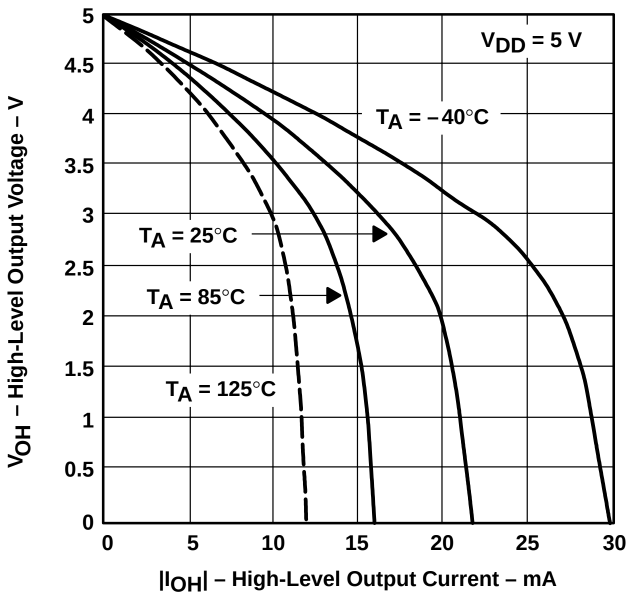


Figure 13

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

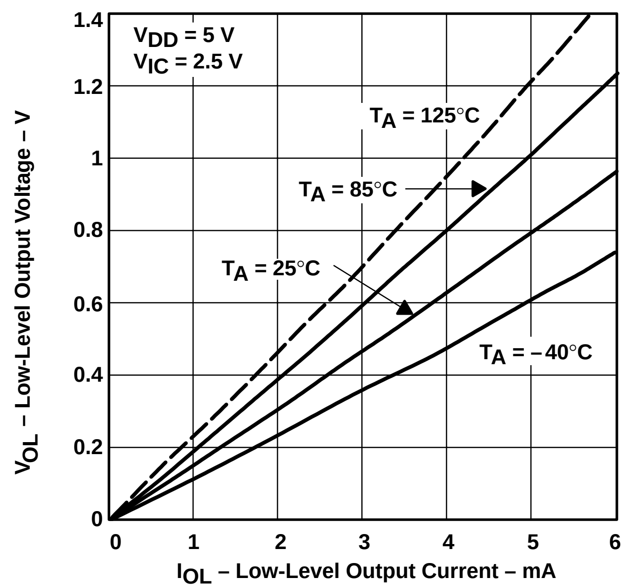


Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡ vs FREQUENCY

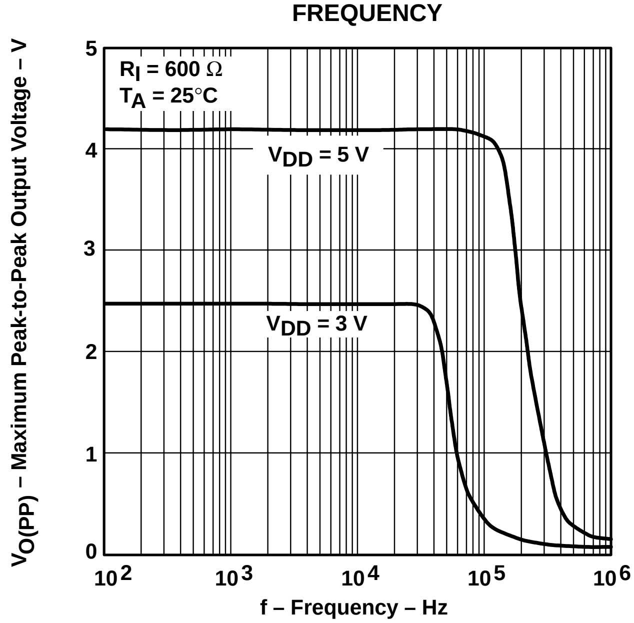


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

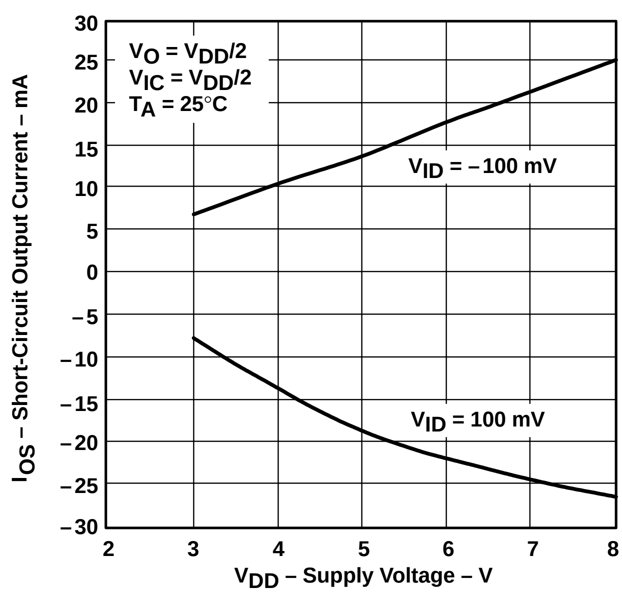


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†‡ vs FREE-AIR TEMPERATURE

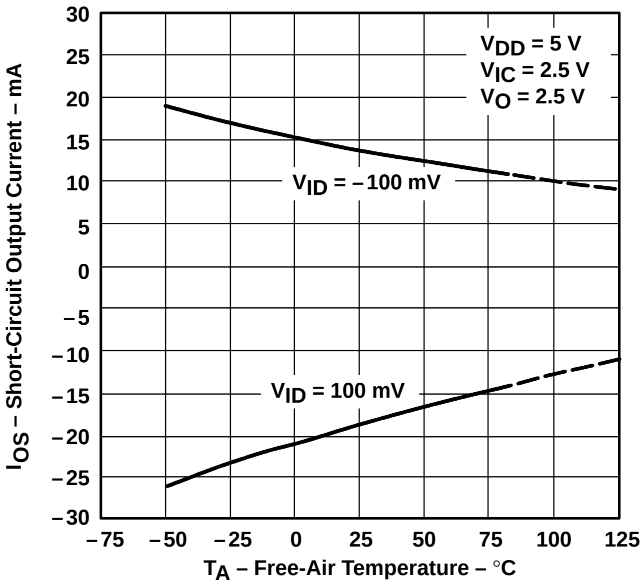


Figure 17

OUTPUT VOLTAGE‡ vs DIFFERENTIAL INPUT VOLTAGE

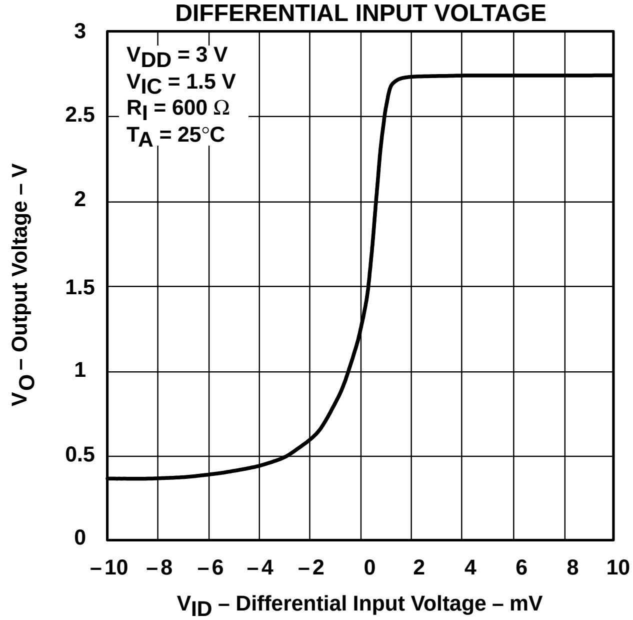


Figure 18

OUTPUT VOLTAGE‡ vs DIFFERENTIAL INPUT VOLTAGE

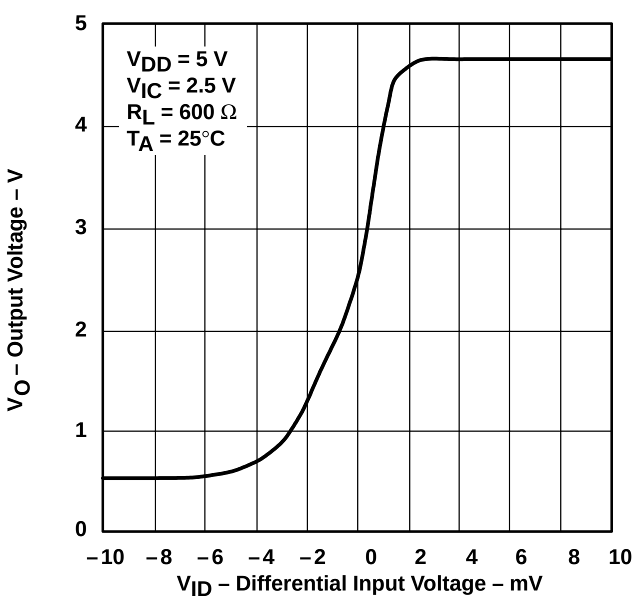


Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION‡ vs LOAD RESISTANCE

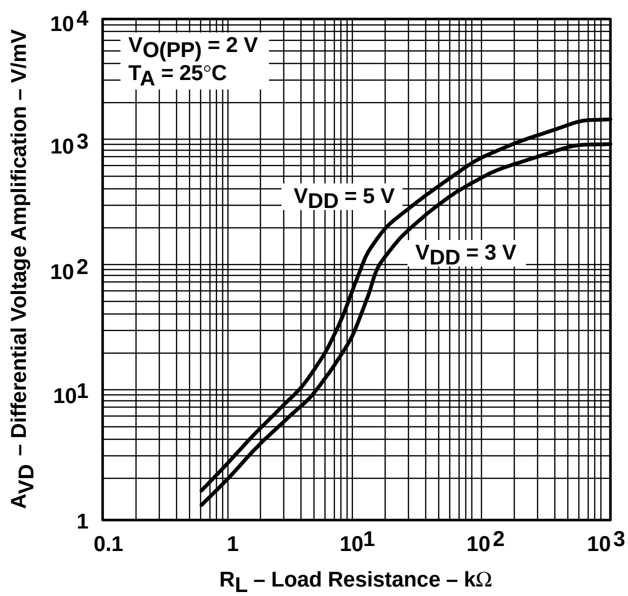


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

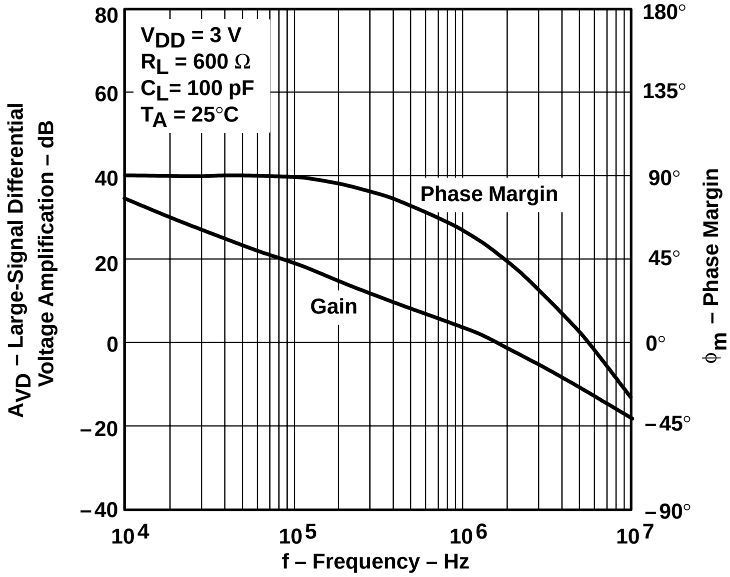


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

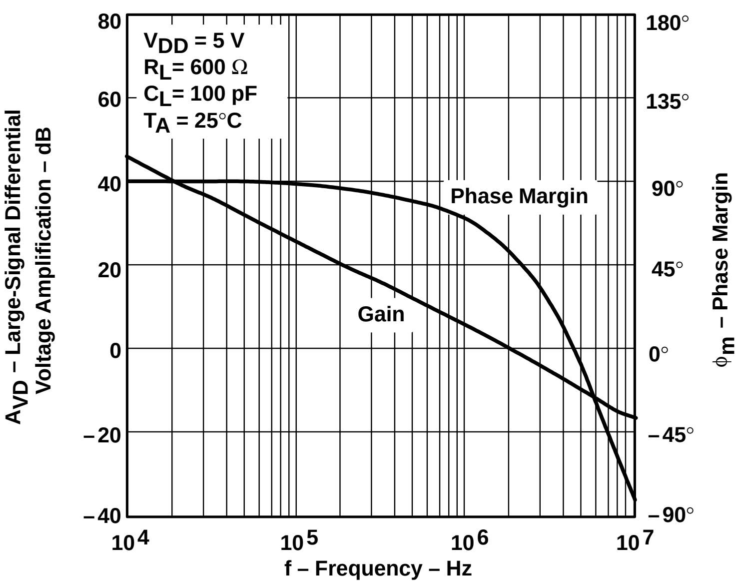


Figure 22

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

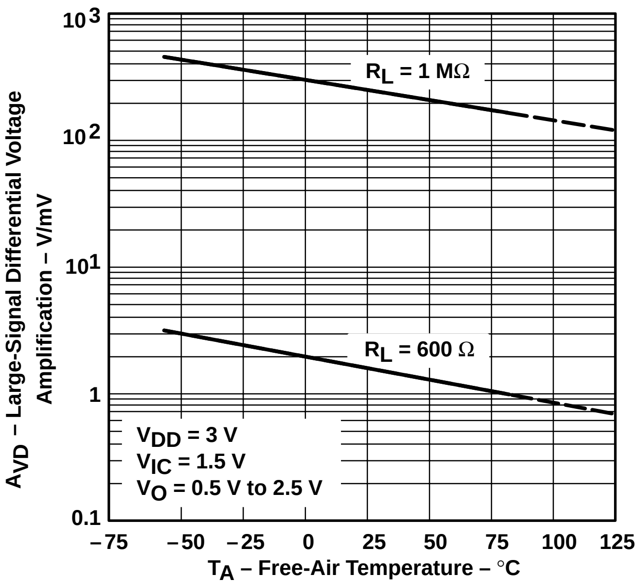


Figure 23

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

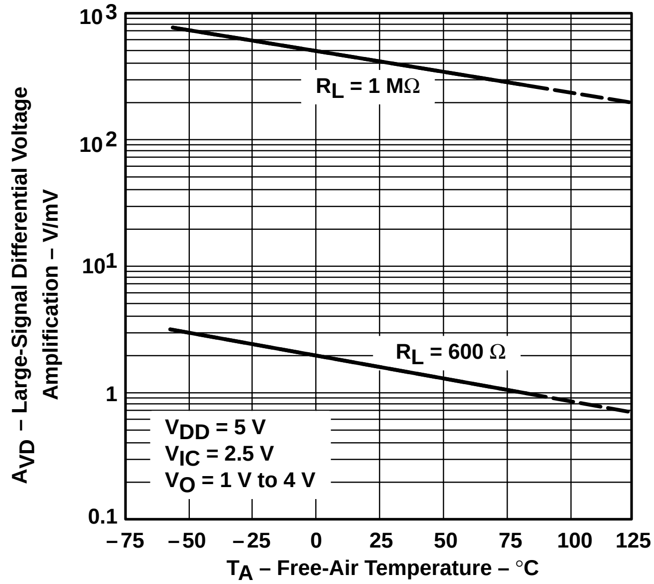


Figure 24

OUTPUT IMPEDANCE‡ vs FREQUENCY

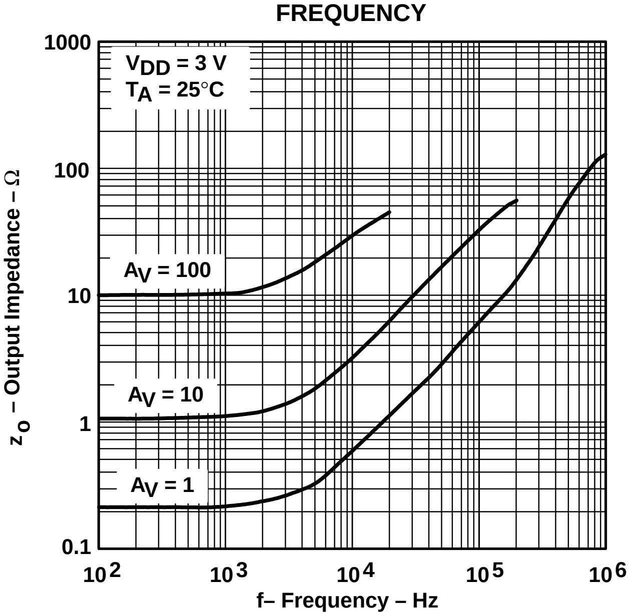


Figure 25

OUTPUT IMPEDANCE‡ vs FREQUENCY

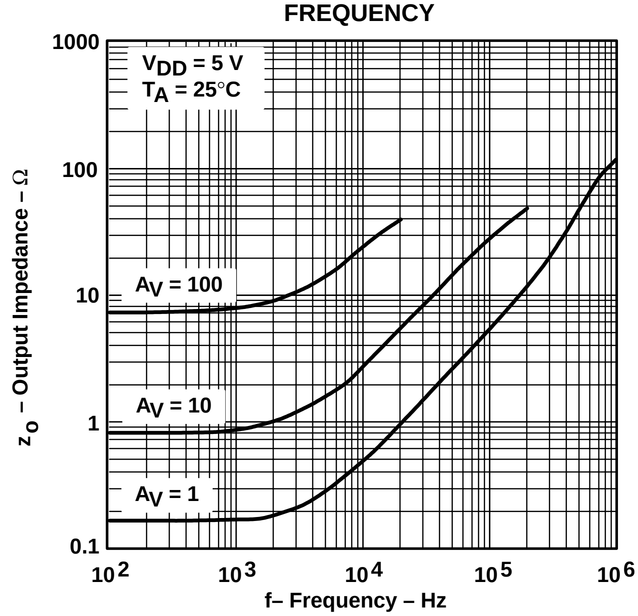


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO†
vs
FREQUENCY

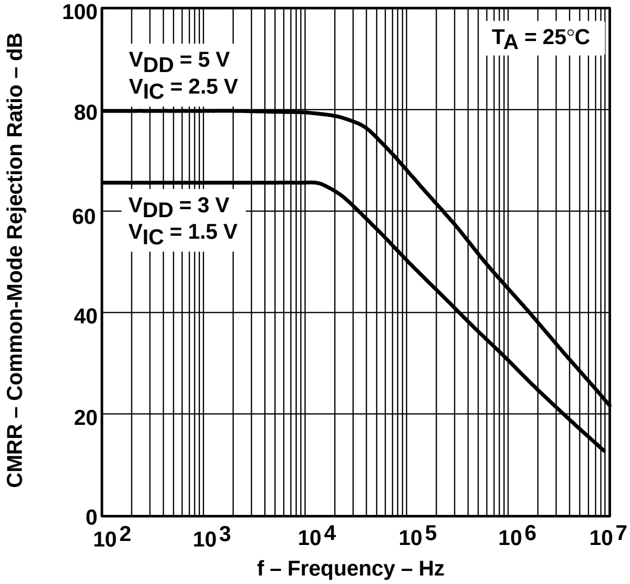


Figure 27

COMMON-MODE REJECTION RATIO†‡
vs
FREE-AIR TEMPERATURE

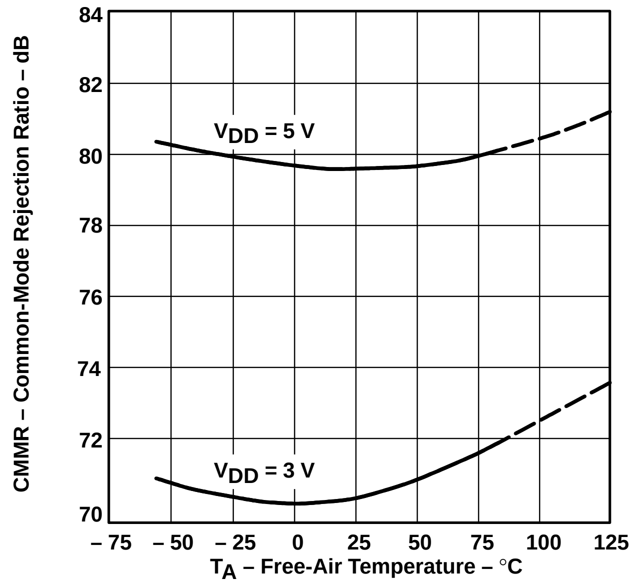


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

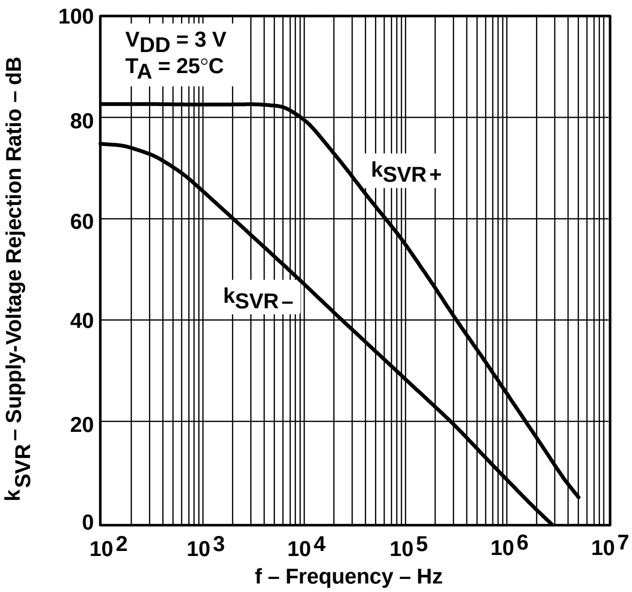


Figure 29

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

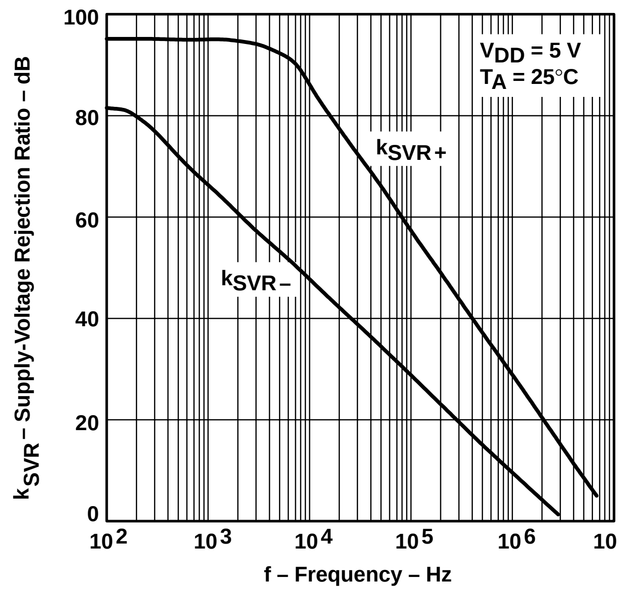


Figure 30

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

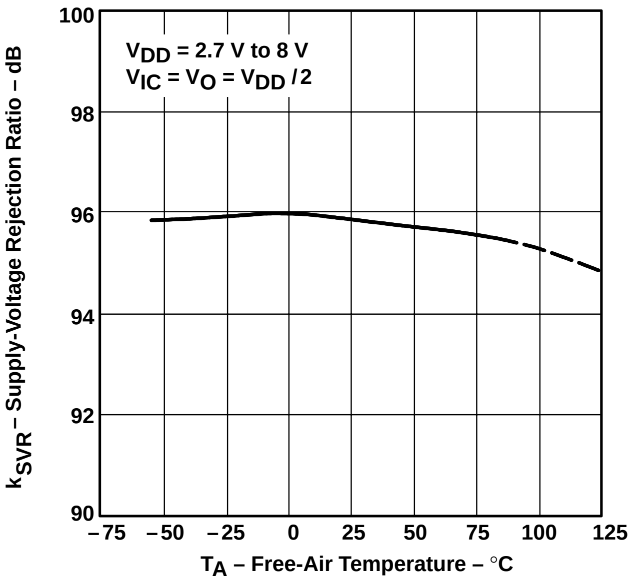


Figure 31

SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

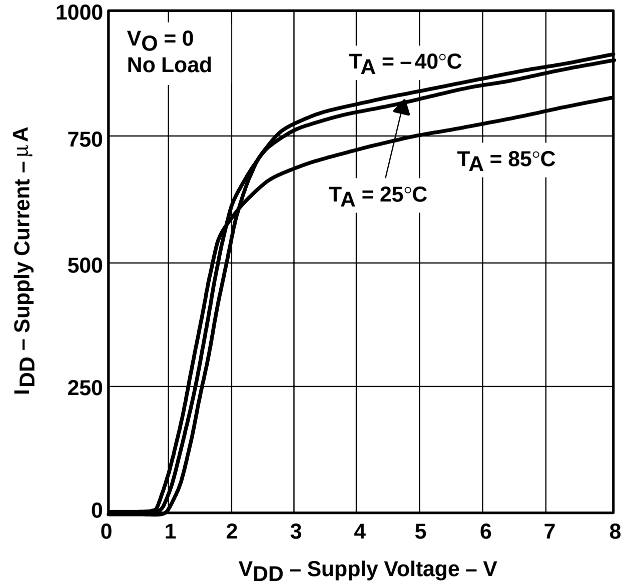


Figure 32

SLEW RATE‡
vs
LOAD CAPACITANCE

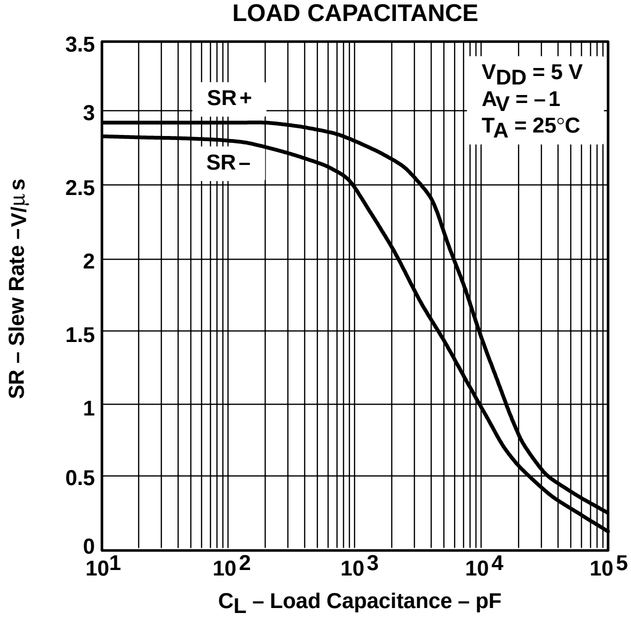


Figure 33

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

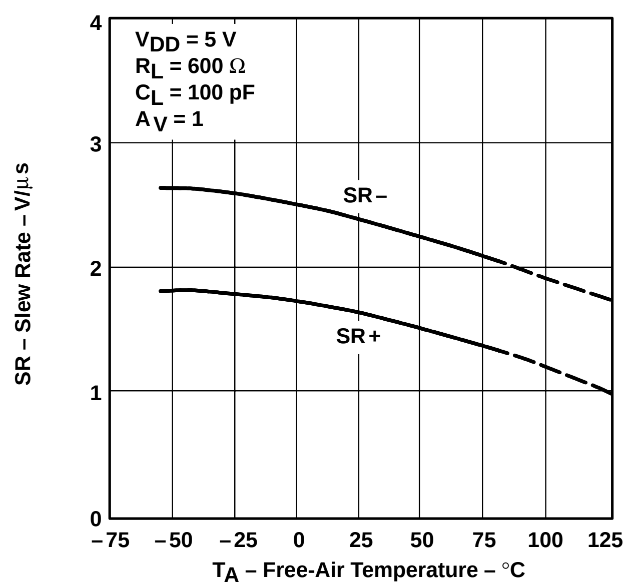


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

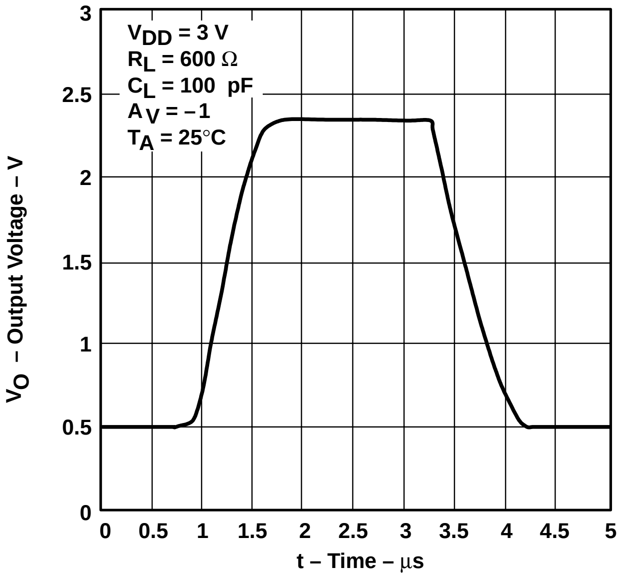


Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE†

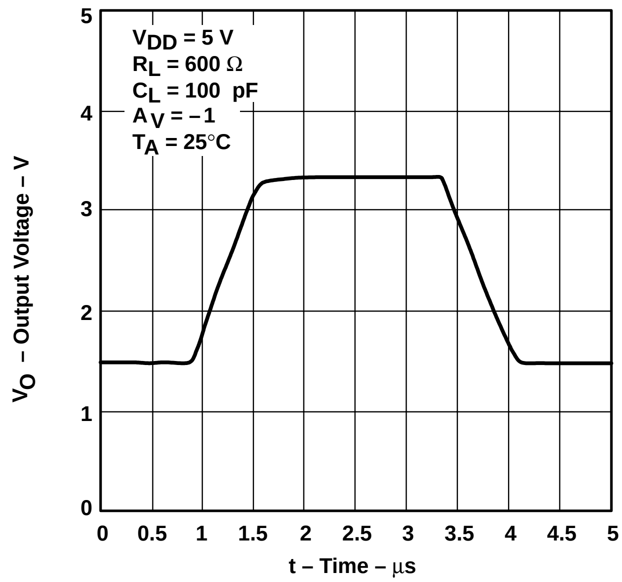


Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

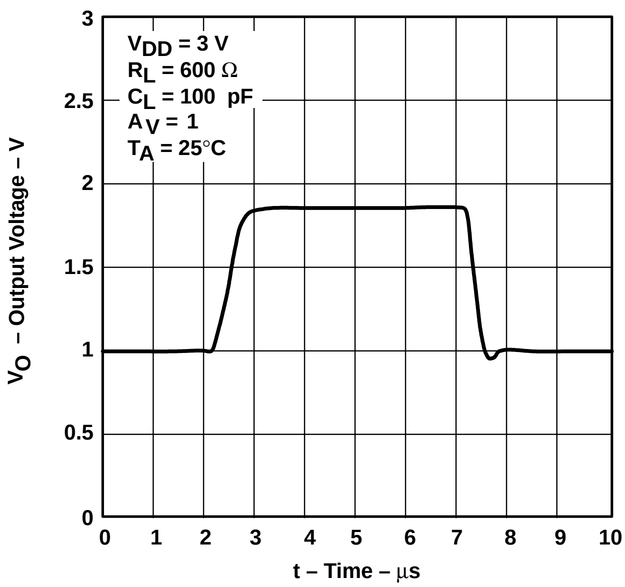


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

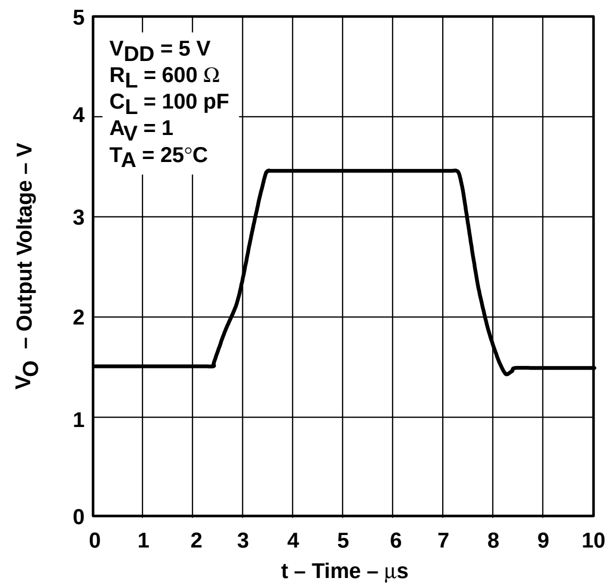


Figure 38

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

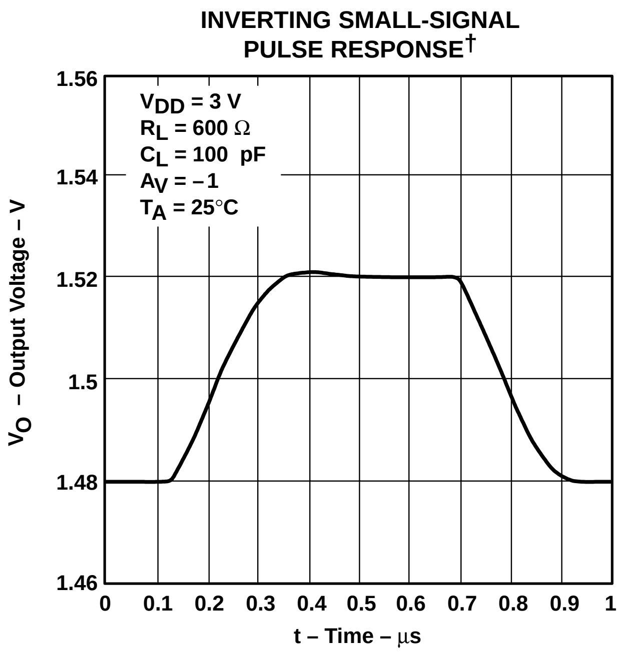


Figure 39

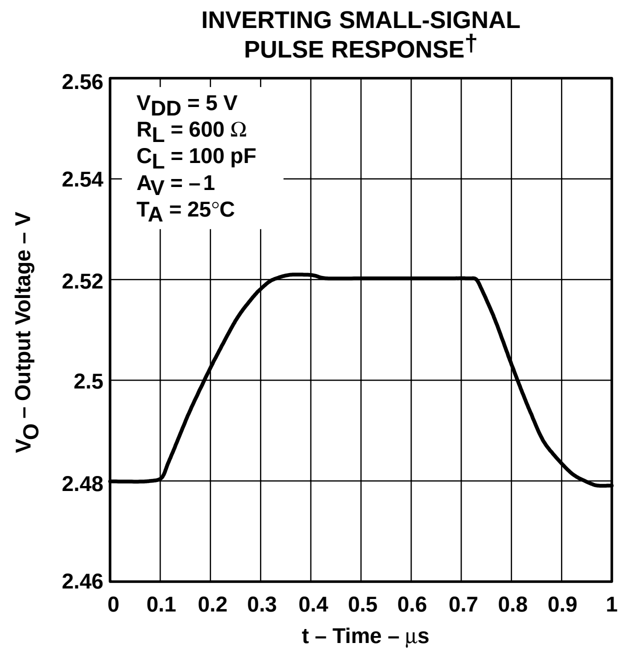


Figure 40

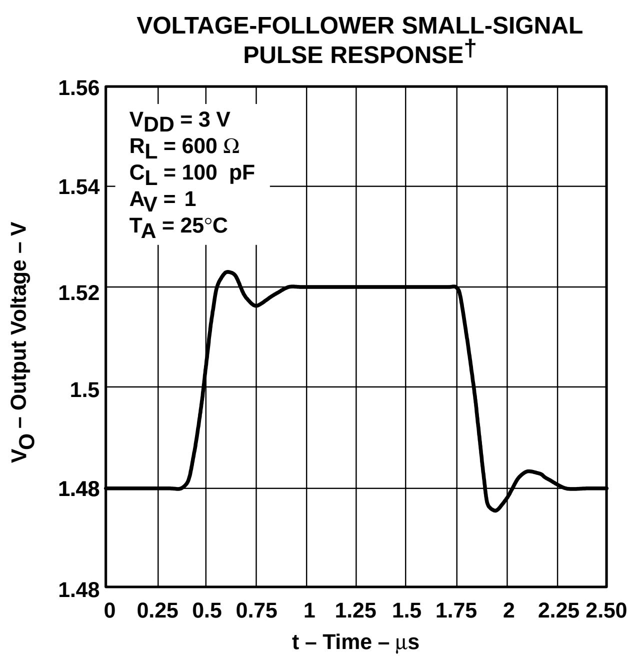


Figure 41

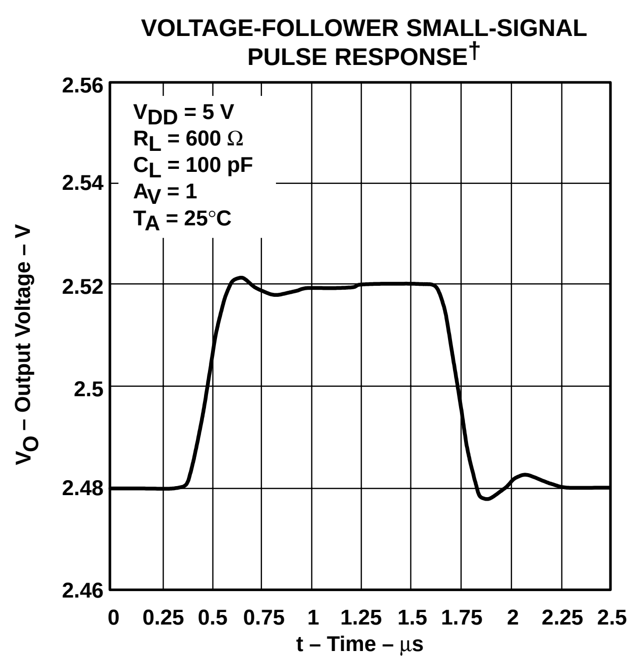


Figure 42

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

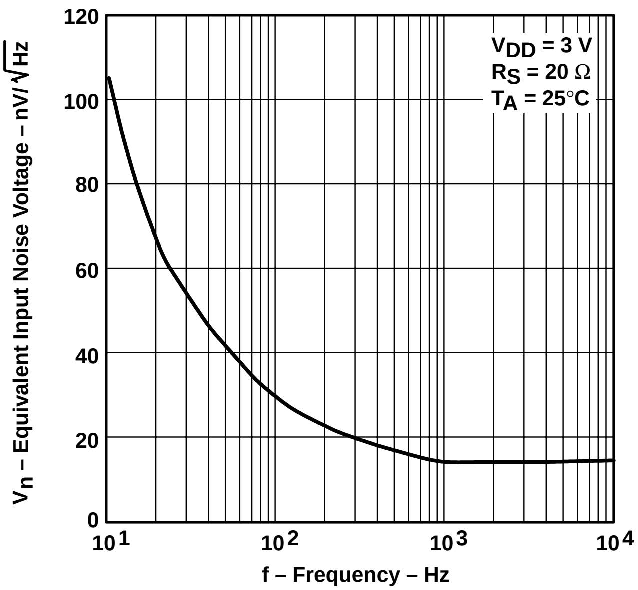


Figure 43

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

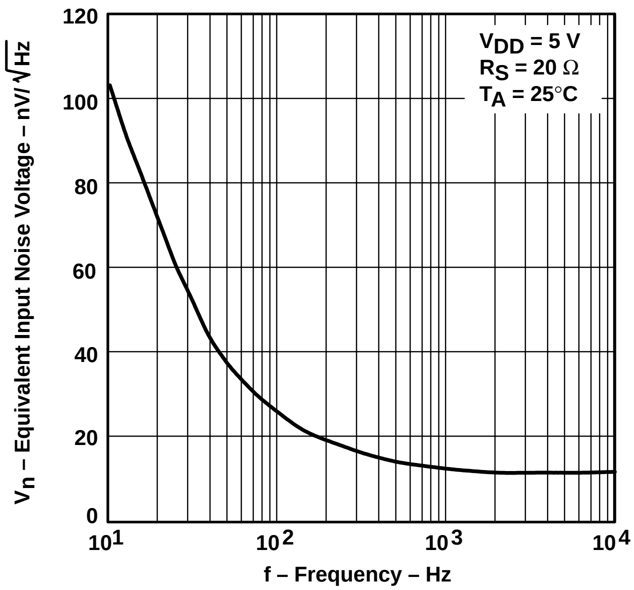


Figure 44

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†

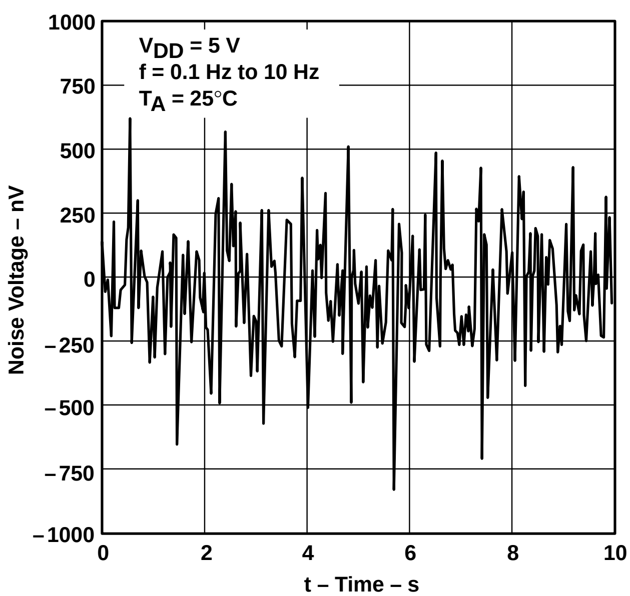


Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

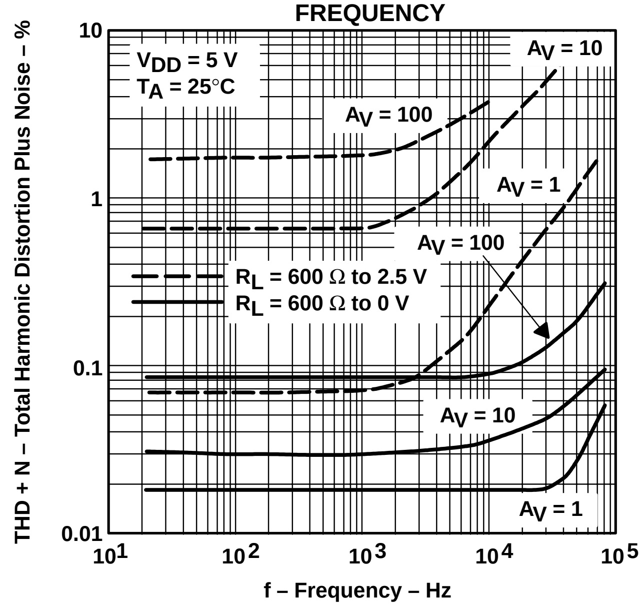


Figure 46

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

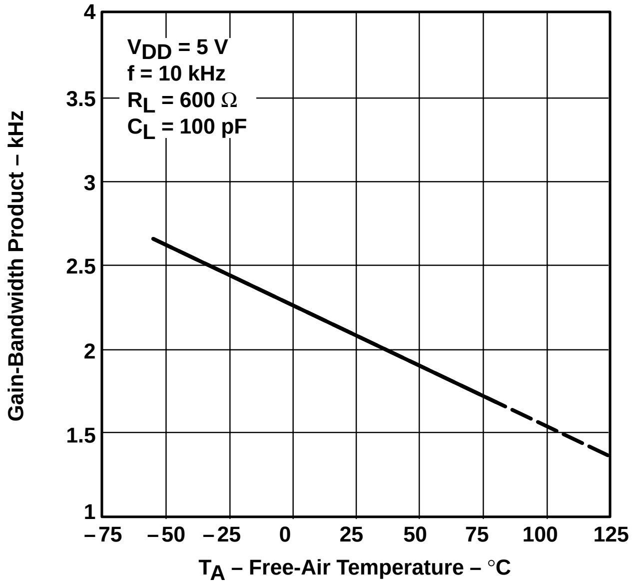


Figure 47

GAIN-BANDWIDTH PRODUCT‡
vs
SUPPLY VOLTAGE

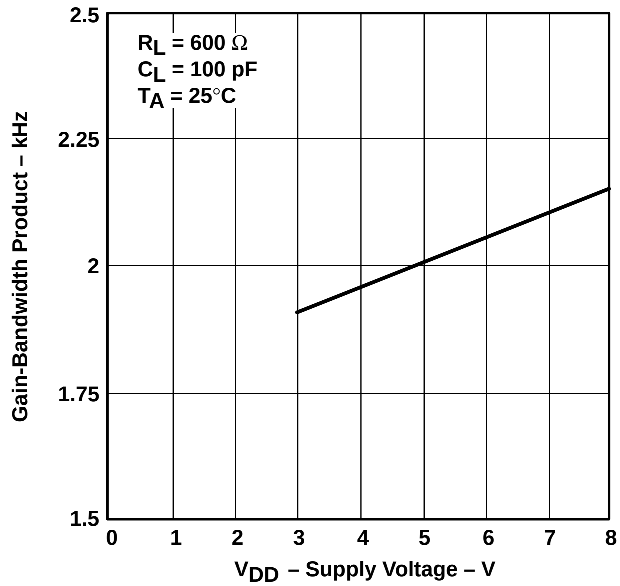


Figure 48

GAIN MARGIN‡
vs
LOAD CAPACITANCE

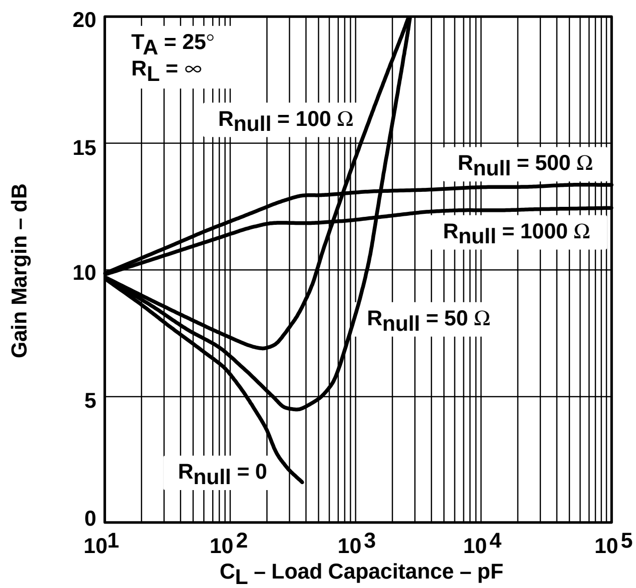


Figure 49

GAIN MARGIN‡
vs
LOAD CAPACITANCE

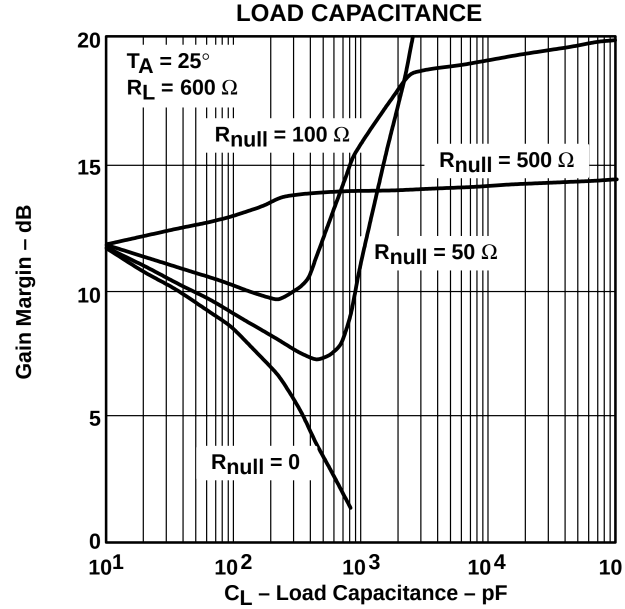


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN† vs LOAD CAPACITANCE

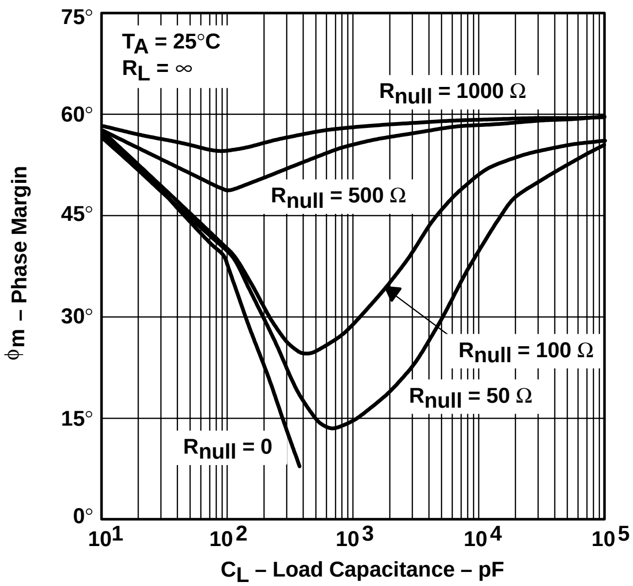


Figure 51

PHASE MARGIN† vs LOAD CAPACITANCE

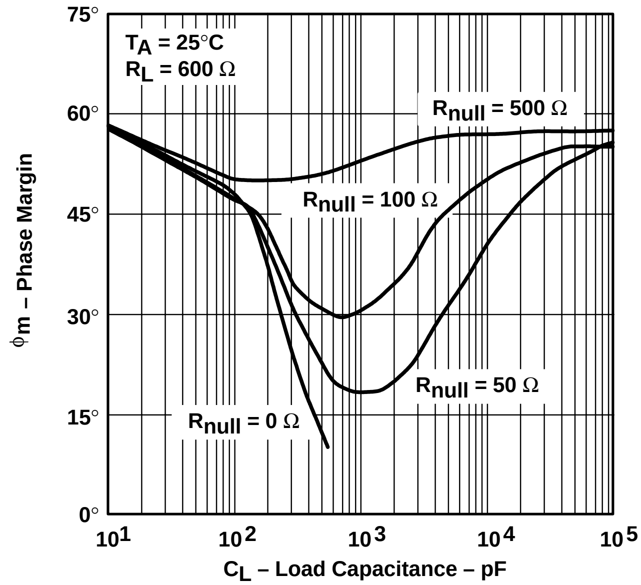


Figure 52

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

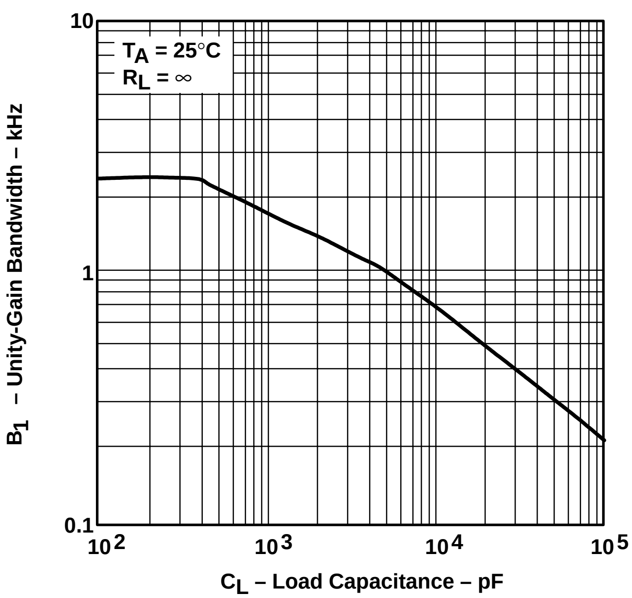


Figure 53

UNITY-GAIN BANDWIDTH† vs LOAD CAPACITANCE

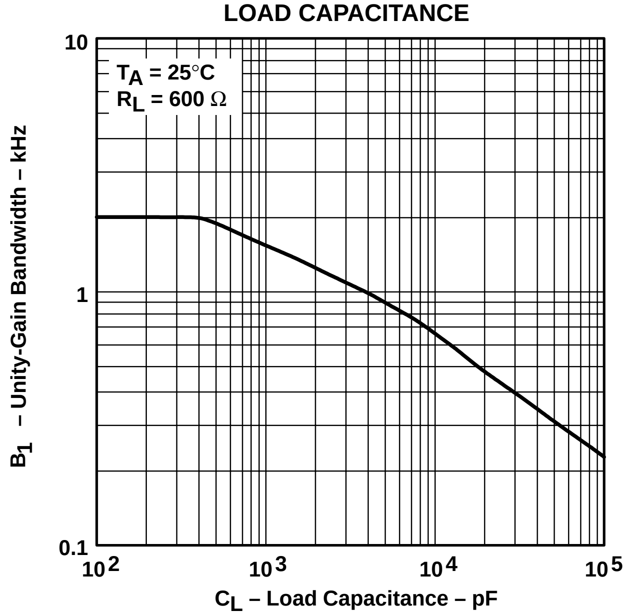


Figure 54

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

APPLICATION INFORMATION

driving large capacitive loads

The TLV2731 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins (R_{null} = 0).

A small series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 50 Ω, 100 Ω, 500 Ω, and 1000 Ω. The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \qquad (1)$$

Where :

$\Delta\phi_{m1}$ = Improvement in phase margin
UGBW = Unity-gain bandwidth frequency
R_{null} = Output series resistance
C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53 and Figure 54). To use equation 1, UGBW must be approximated from Figure 53 and Figure 54.

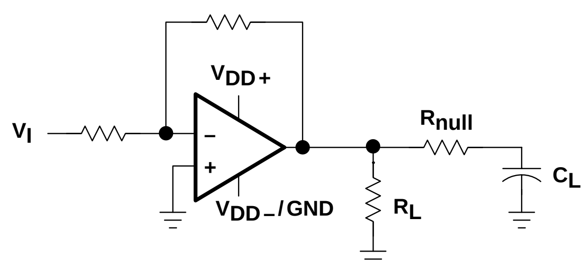


Figure 55. Series-Resistance Circuit

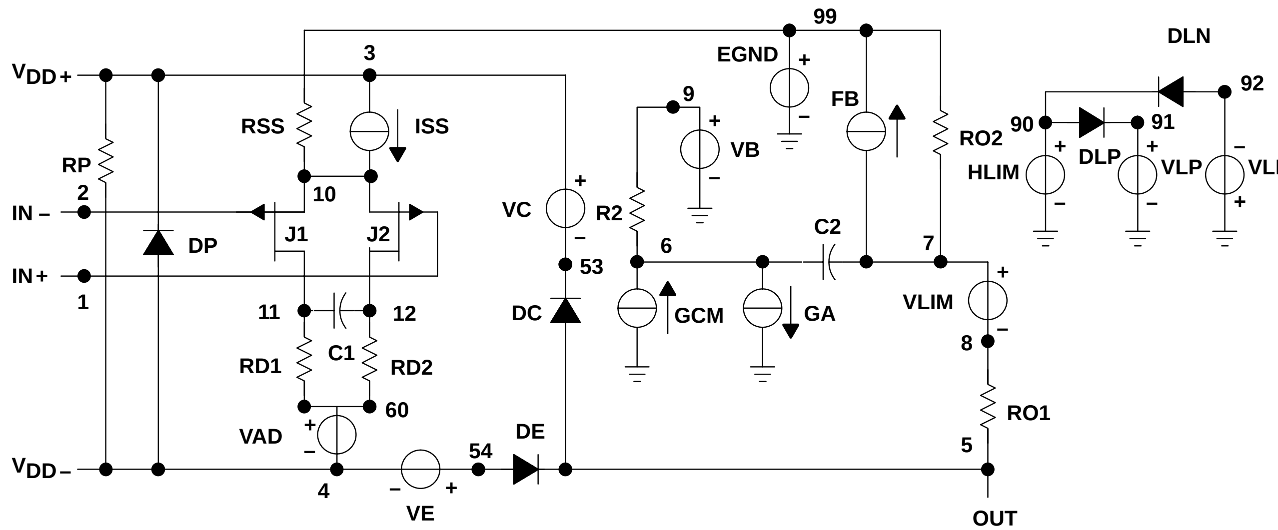
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 56 are generated using the TLV2731 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



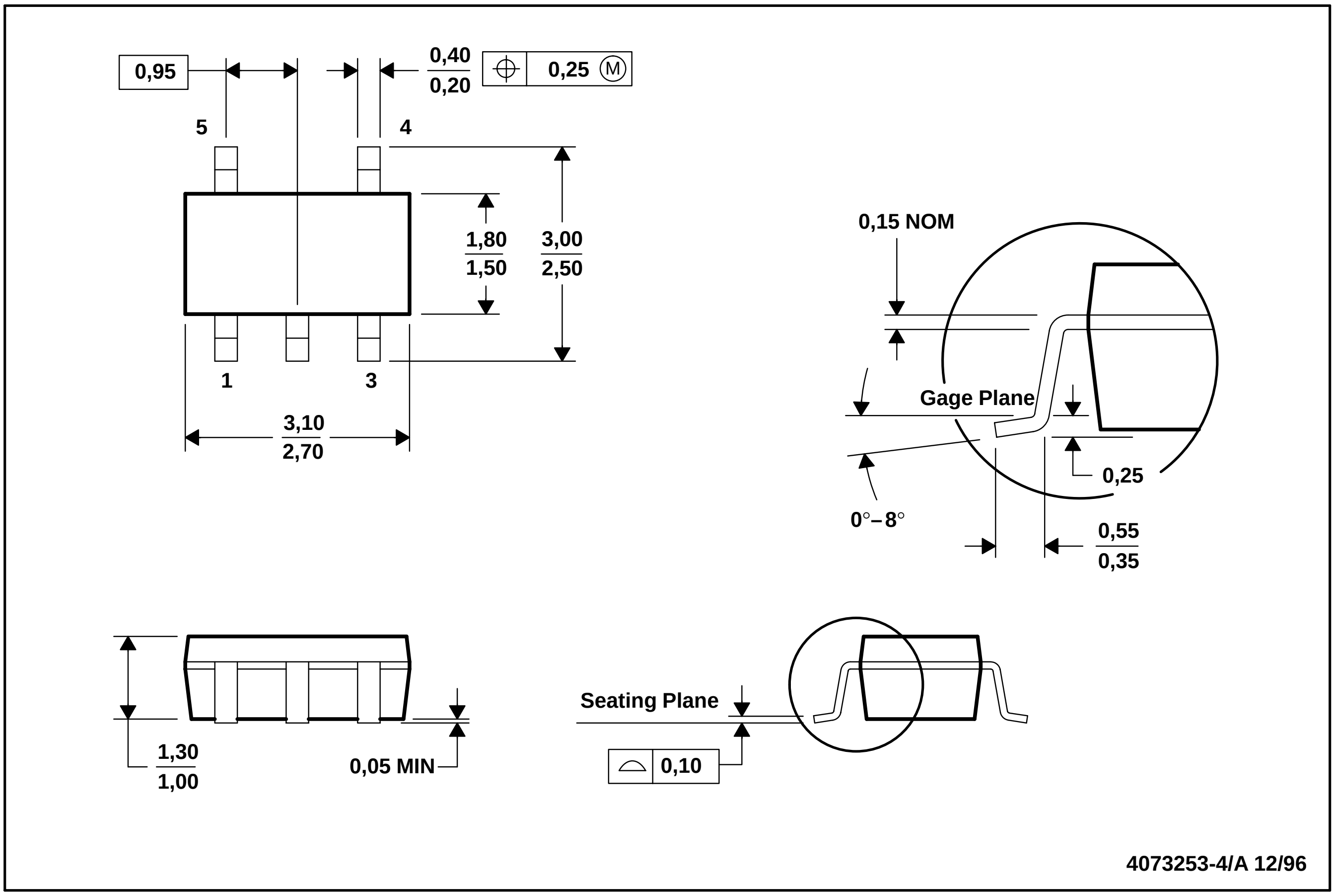

```
.SUBCKT TLV2731 1 2 3 4 5
        C1      11      12      13.51E–12
        C2      6       7       50.00E–12
        DC      5       53      DX
        DE      54      5       DX
        DLP     90      91      DX
        DLN     92      90      DX
        DP      4       3       DX
        EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7       99      POLY (5) VB VC VE VLP
        + VLN 0 90.83E3 –10E3 10E3 10E3 –10E3
        GA      6       0       11      12 314.2E–6
        GCM     0       6       10      99 242.35E–9
        ISS     3       10      DC      87.00E–6
        HLIM    90      0       VLIM 1K
        J1      11      2       10 JX
        J2      12      1       10 JX
        R2      6       9       100.0E3
RD1     60      11      3.183E3
RD2     60      12      3.183E3
R01     8       5       25
R02     7       99      25
RP      3       4       6.553E3
RSS     10      99      2.500E6
VAD     60      4       –.5
VB      9       0       DC 0
VC      3       53      DC .795
VE      54      4       DC .795
VLIM    7       8       DC 0
VLP     91      0       DC 12.4
VLN     0       92      DC 17.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=2.939E–3
+ VTO=–.065)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademark of MicroSim Corporation.

MECHANICAL INFORMATION

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLV2731CDBV	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI
TLV2731CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731CDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2731IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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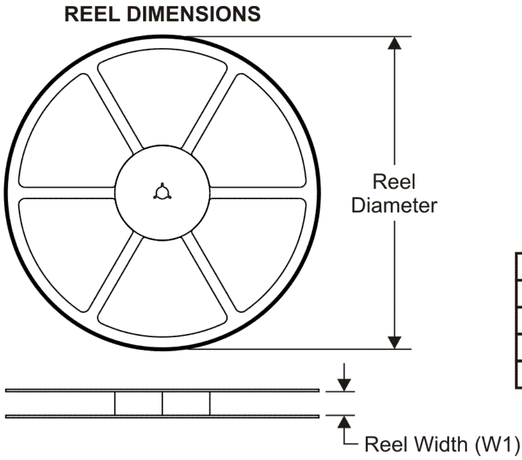
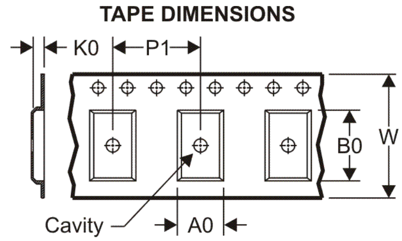
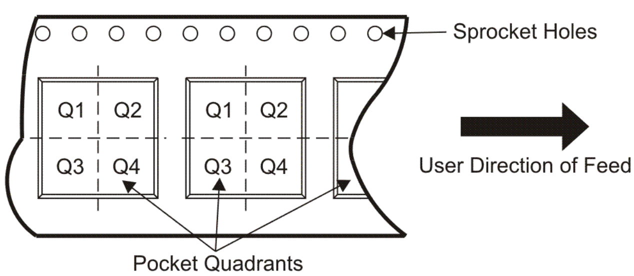
TAPE AND REEL INFORMATION





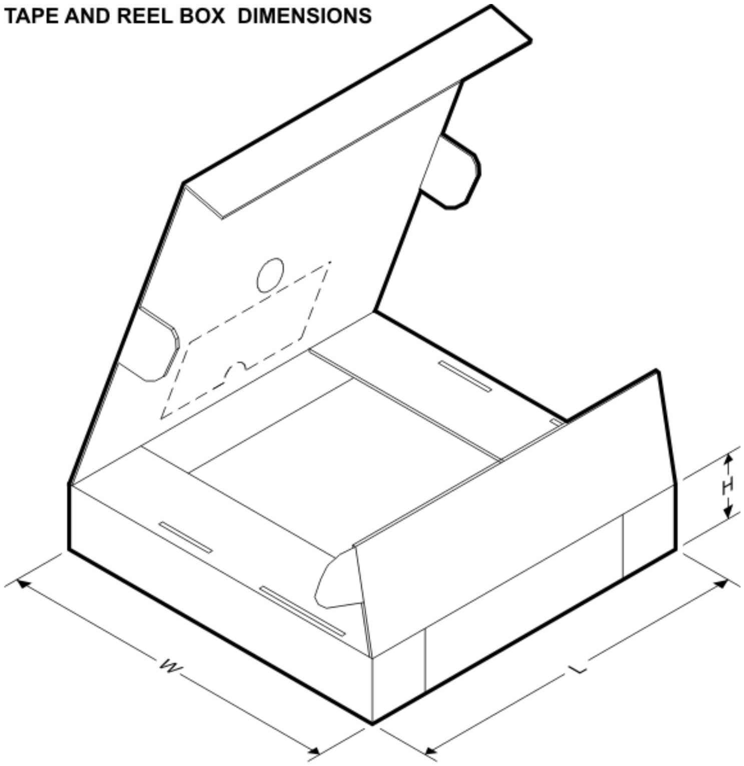
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2731CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2731IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2731CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2731CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2731IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2731IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0