

N-channel 650 V, 0.056 Ω typ., 42 A, MDmesh™ V Power MOSFET in a TO247-4 package

Datasheet – production data

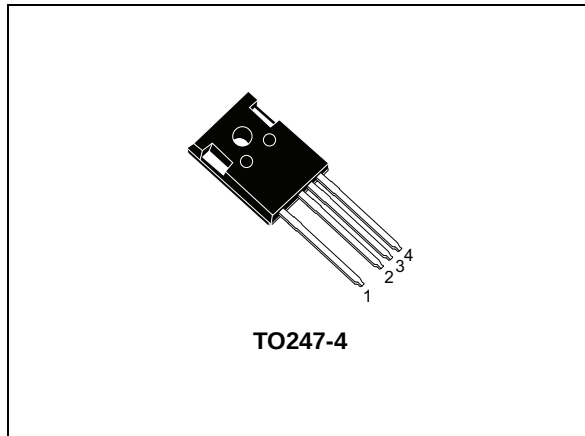
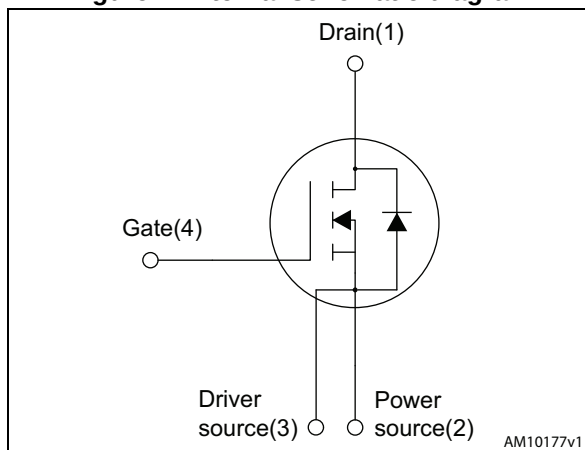


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STW57N65M5-4	710 V	0.063 Ω	42 A

- Higher V_{DS} rating
- Higher dv/dt capability
- Excellent switching performance thanks to the extra driving source pin
- Easy to drive
- 100% avalanche tested

Applications

- High efficiency switching applications:
 - Servers
 - PV inverters
 - Telecom infrastructure
 - Multi kW battery chargers

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STW57N65M5-4	57N65M5	TO247-4	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	42	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	26.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	168	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	11	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	960	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 42\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, peak $V_{DS} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
3. $V_{DS} \leq 520\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.50	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 21\text{ A}$		0.056	0.063	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	4200	-	pF
C_{oss}	Output capacitance		-	115	-	pF
C_{rss}	Reverse transfer capacitance		-	9	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	303	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	93	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.3	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 21\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	98	-	nC
Q_{gs}	Gate-source charge		-	23	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 28\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15) (see Figure 20)	-	79	-	ns
$t_{r(V)}$	Voltage rise time		-	9	-	ns
$t_{f(I)}$	Current fall time		-	8	-	ns
$t_{c(off)}$	Crossing time		-	14	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		42	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		168	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 42\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 17)	-	418		ns
Q_{rr}	Reverse recovery charge		-	8		μC
I_{RRM}	Reverse recovery current		-	40		A
t_{rr}	Reverse recovery time	$I_{SD} = 42\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	528		ns
Q_{rr}	Reverse recovery charge		-	12		μC
I_{RRM}	Reverse recovery current		-	44		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

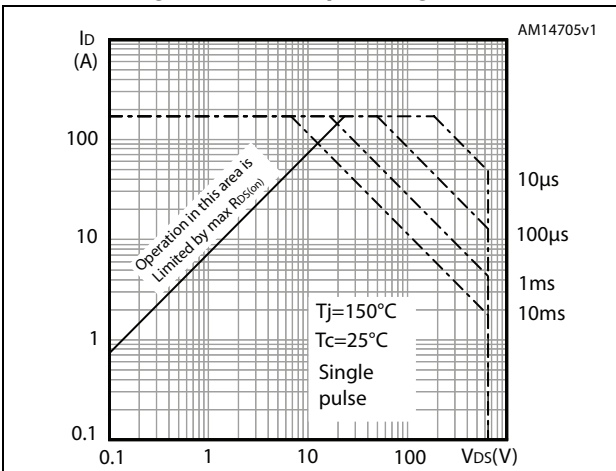


Figure 3. Thermal impedance

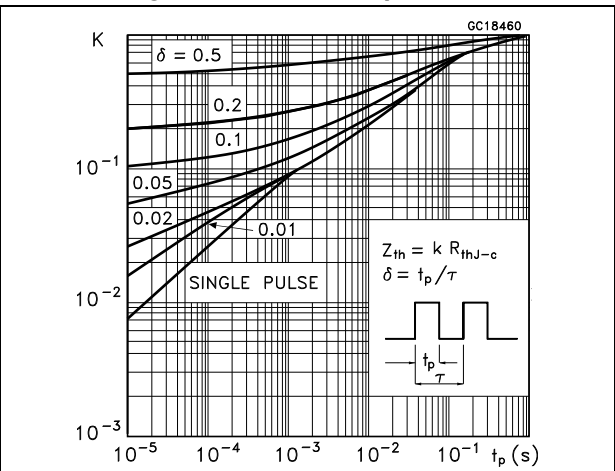


Figure 4. Output characteristics

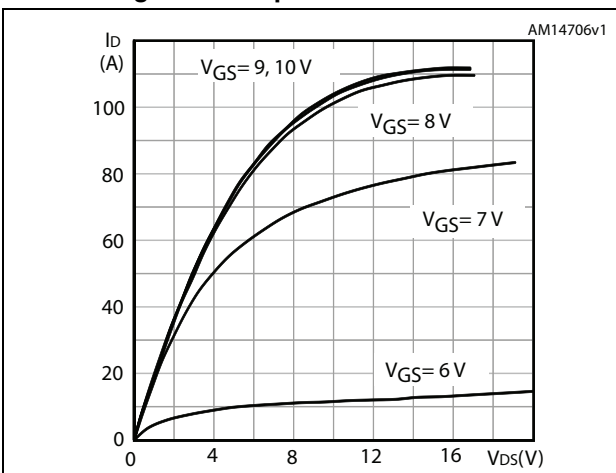


Figure 5. Transfer characteristics

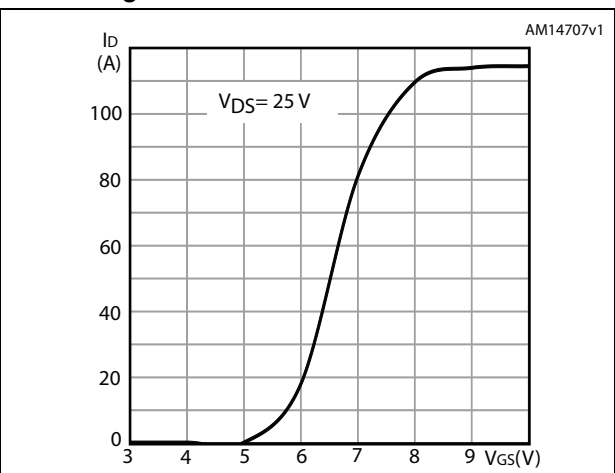


Figure 6. Gate charge vs gate-source voltage

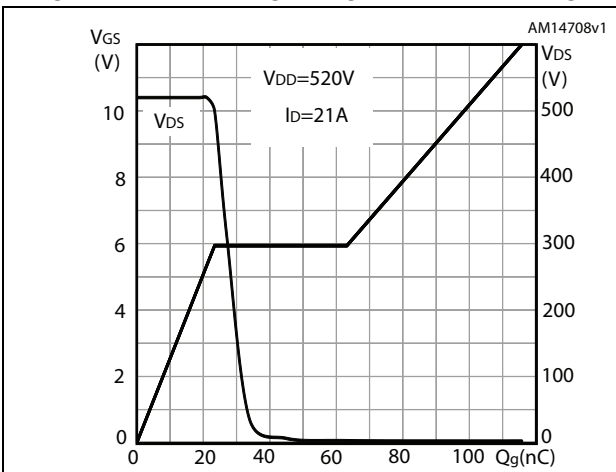


Figure 7. Static drain-source on-resistance

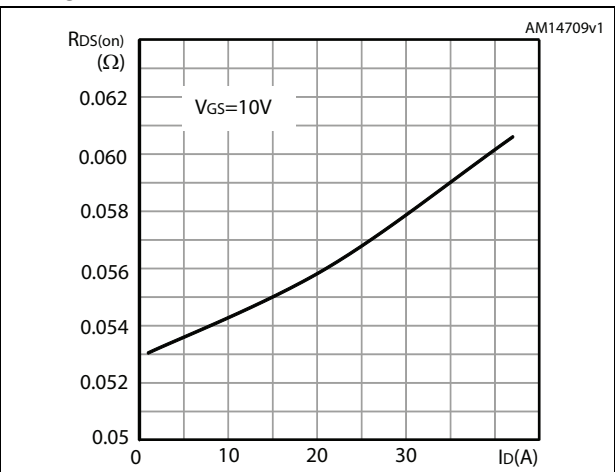


Figure 8. Capacitance variations

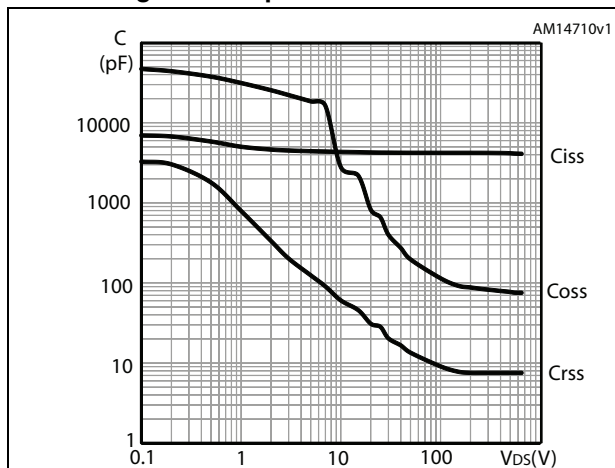


Figure 9. Output capacitance stored energy

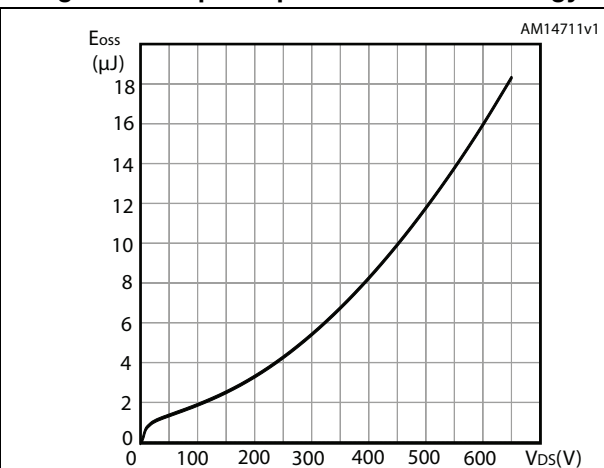


Figure 10. Normalized gate threshold voltage vs temperature

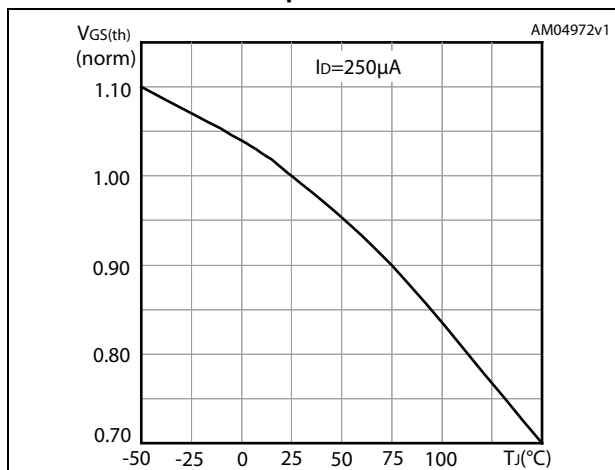


Figure 11. Normalized on-resistance vs temperature

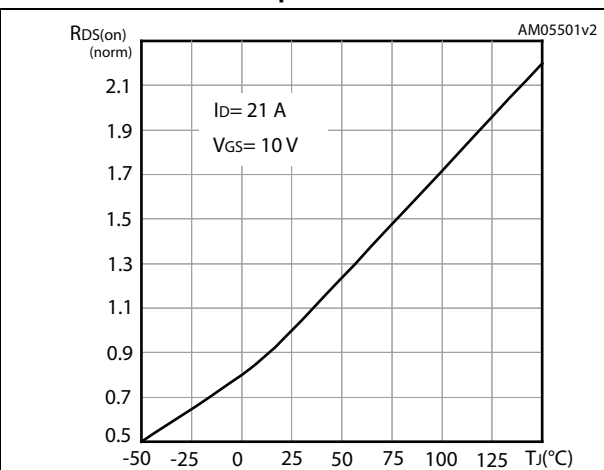


Figure 12. Source-drain diode forward characteristics

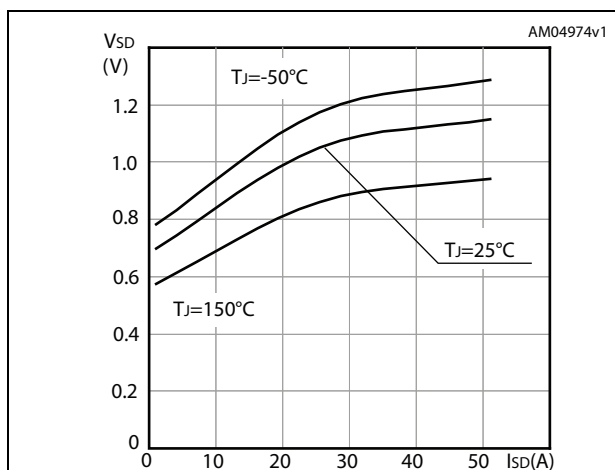
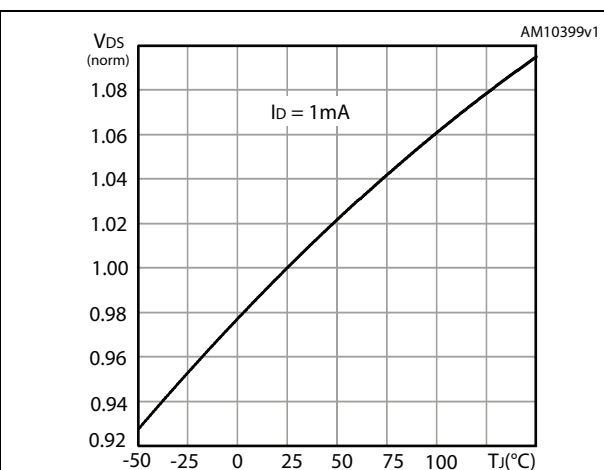
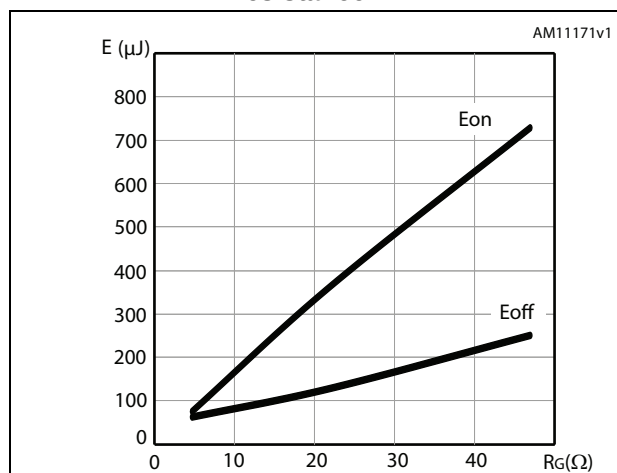
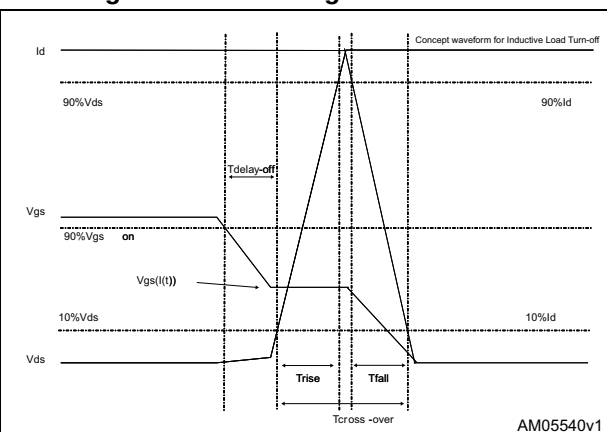
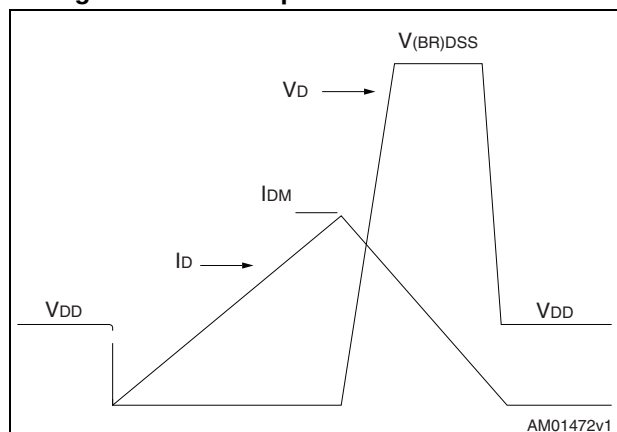
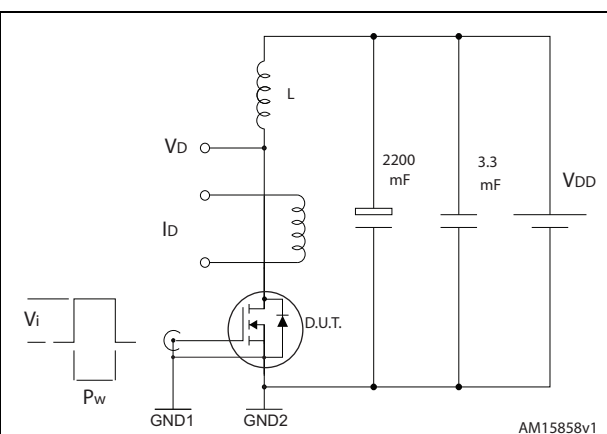
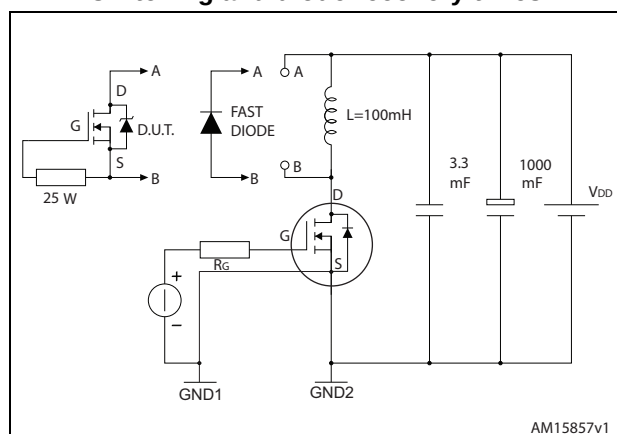
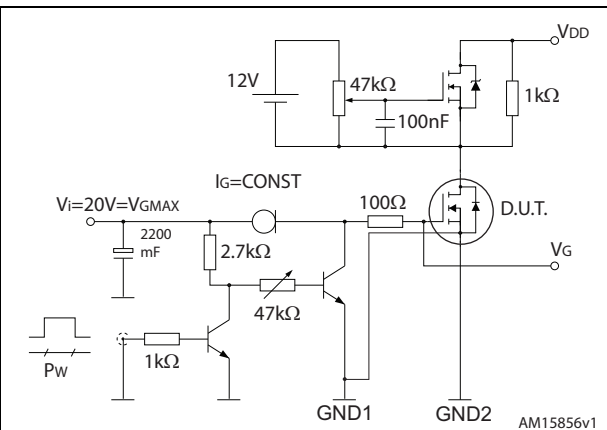
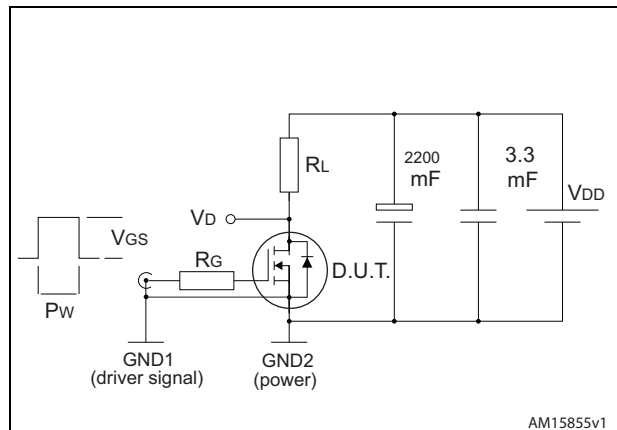
Figure 13. Normalized V_{DS} vs temperature

Figure 14. Switching losses vs gate resistance ⁽¹⁾



1. E_{on} including reverse recovery of a SiC diode.



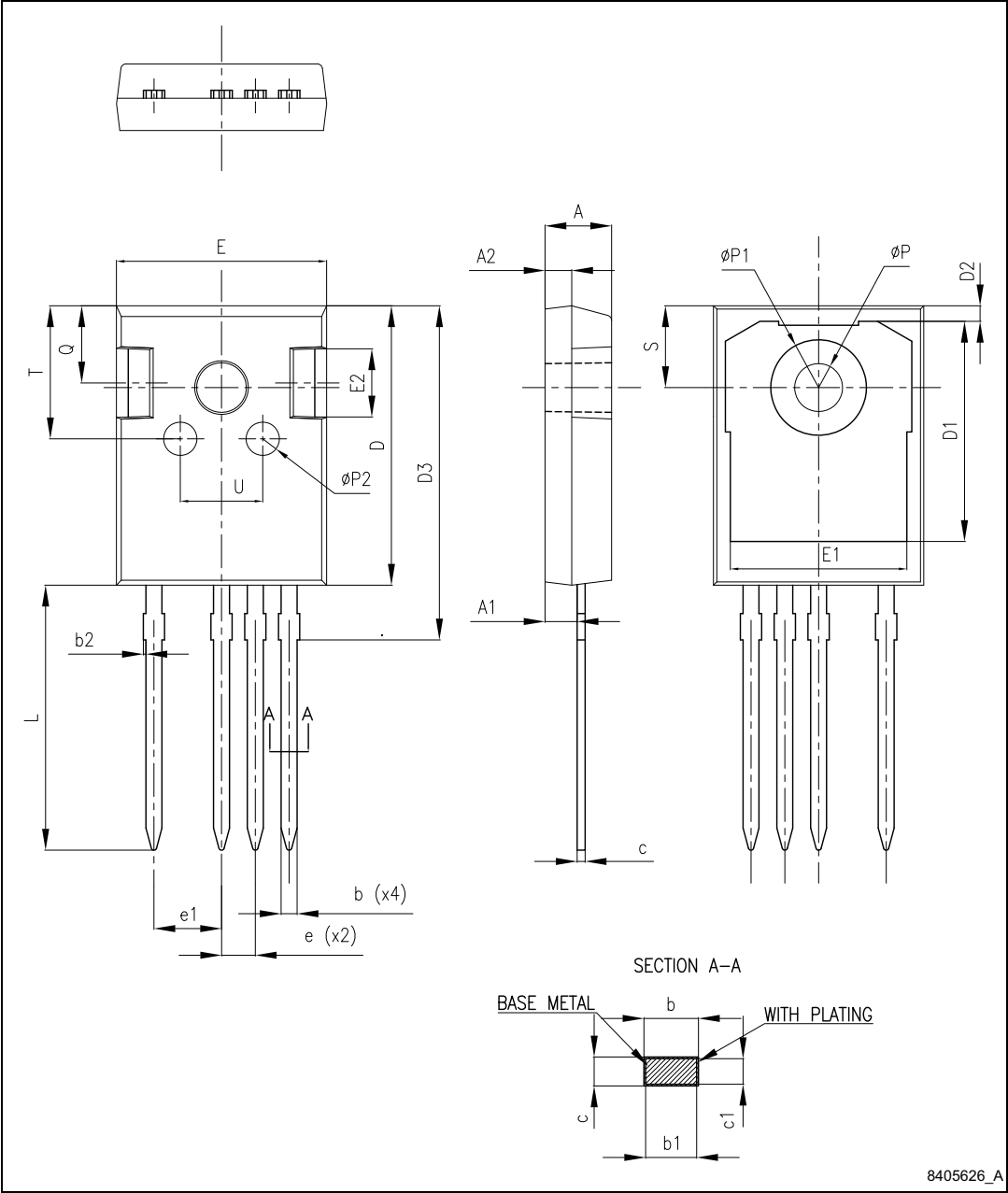
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. TO247-4 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

Figure 21. TO247-4 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
17-Apr-2013	1	First release.
28-Jun-2013	2	– Modified: Figure 1, 15, 16, 17, 18 – Minor text changes

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