CC3100MOD SimpleLink™ Certified Wi-Fi® Network Processor Internet-of-Things Module Solution for MCU Applications

1 Module Overview

1.1 Features

- The CC3100MOD is a Wi-Fi Module that Consists of the CC3100R11MRGC Wi-Fi Network Processor and Power-Management Subsystems. This Fully Integrated Module Includes all Required Clocks, SPI Flash, and Passives.
- Modular FCC, IC, and CE Certifications Save Customer Effort, Time, and Money
- Wi-Fi CERTIFIED™ Modules, With Ability to Request Certificate Transfer for Wi-Fi Alliance Members
- Wi-Fi Network Processor Subsystem
  - Featuring Wi-Fi Internet-On-a-Chip™
  - Dedicated ARM® MCU
    Completely Offloads Wi-Fi and Internet Protocols from the External Microcontroller
  - Wi-Fi Driver and Multiple Internet Protocols in ROM
  - 802.11 b/g/n Radio, Baseband, and Medium Access Control (MAC), Wi-Fi Driver, and Supplicant
  - TCP/IP Stack
    - Industry-Standard BSD Socket Application Programming Interfaces (APIs)
    - 8 Simultaneous TCP or UDP Sockets
    - 2 Simultaneous TLS and SSL Sockets
  - Powerful Crypto Engine for Fast, Secure Wi-Fi and Internet Connections With 256-Bit AES Encryption for TLS and SSL Connections
  - Station, AP, and Wi-Fi Direct™ Modes
  - WPA2 Personal and Enterprise Security
  - SimpleLink Connection Manager for Autonomous and Fast Wi-Fi Connections
  - SmartConfig™ Technology, AP Mode, and WPS2 for Easy and Flexible Wi-Fi Provisioning
  - TX Power
    - 17 dBm at 1 DSSS
    - 17.25 dBm at 11 CCK
    - 13.5 dBm at 54 OFDM
  - RX Sensitivity
    - –94.7 dBm at 1 DSSS
    - –87 dBm at 11 CCK
    - –73 dBm at 54 OFDM
  - Application Throughput
    - UDP: 16 Mbps
    - TCP: 13 Mbps
- Host Interface
  - Wide Range of Power Supply (2.3 to 3.6 V)
  - Interfaces With 8-, 16-, and 32-Bit MCU or ASICs Over a Serial Peripheral Interface (SPI) With up to 20-MHz Clock
  - Low Footprint Host Driver: Less than 6KB
  - Supports RTOS and No-OS Applications
- Power-Management Subsystem
  - Integrated DC-DC Converter With a Wide-Supply Voltage:
    - Direct Battery Mode: 2.3 to 3.6 V
  - Low-Power Consumption at 3.6 V
    - Hibernate With Real-Time Clock (RTC): 7 µA
    - Standby: 140 µA
    - RX Traffic: 54 mA at 54 OFDM
    - TX Traffic: 223 mA at 54 OFDM
  - Integrated Components on Module
    - 40.0-MHz Crystal With Internal Oscillator
    - 32.768-kHz Crystal (RTC)
    - 8-Mbit SPI Serial Flash RF Filter and Passive Components
  - Package and Operating Conditions
    - 1.27-mm Pitch, 63-Pin, 20.5-mm × 17.5-mm LGA Package for Easy Assembly and Low-Cost PCB Design
    - Operating Temperature Range: –20°C to 70°C

1.2 Applications

- Internet of Things (IoT)
- Cloud Connectivity
- Home Automation
- Home Appliances
- Access Control
- Security Systems
- Smart Energy
- Internet Gateway
- Industrial Control
- Smart Plug and Metering
- Wireless Audio
- IP Network Sensor Nodes
- Wearables

1.3 Description

Add Wi-Fi to low-cost, low-power microcontroller (MCU) for Internet of Things (IoT) applications. The CC3100MOD is FCC, IC, CE, and Wi-Fi CERTIFIED module is part of the new SimpleLink Wi-Fi family that dramatically simplifies the implementation of Internet connectivity. The CC3100MOD integrates all protocols for Wi-Fi and Internet, which greatly minimizes host MCU software requirements. With built-in security protocols, the CC3100MOD solution provides a robust and simple security experience. Additionally, the CC3100MOD is a complete platform solution including various tools and software, sample applications, user and programming guides, reference designs and the TI E2E™ support community. The CC3100MOD is available an LGA package that is easy to lay out with all required components including serial flash, RF filter, crystal, passive components fully integrated.

The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a-Chip and contains an additional dedicated ARM MCU that completely off-loads the host MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3100MOD module supports Station, Access Point, and Wi-Fi Direct modes. The module also supports WPA2 personal and enterprise security and WPS 2.0. This subsystem includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols. The power-management subsystem includes an integrated DC-DC converter with support for a wide range of supply voltages. This subsystem enables low-power consumption modes such as hibernate with RTC mode, which requires approximately 7 µA of current. The CC3100MOD module can connect to any 8-, 16-, or 32-bit MCU over the SPI or UART Interface. The device driver minimizes the host memory footprint requirements of less than 7KB of code memory and 700B of RAM memory for a TCP client application.

Table 1-1. Module Information(1)

PART NUMBER	PACKAGE	BODY SIZE
CC3100MODR11MAMOB	MOB (63)	20.5 mm × 17.5 mm

(1) For more information, see Section 9, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the CC3100MOD module.

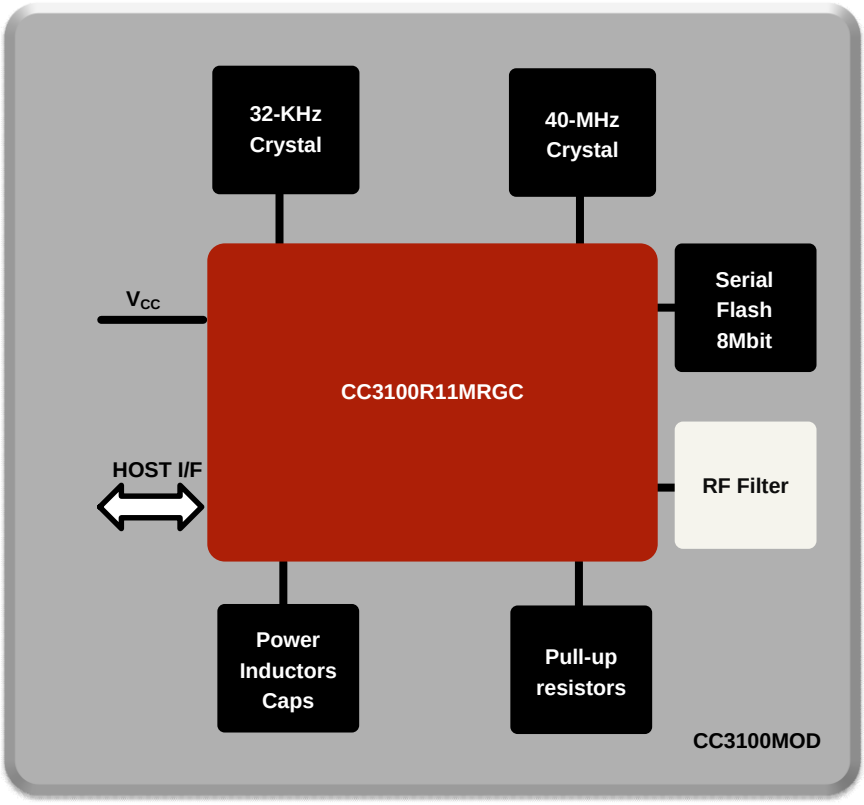


Figure 1-1. CC3100MOD Functional Block Diagram

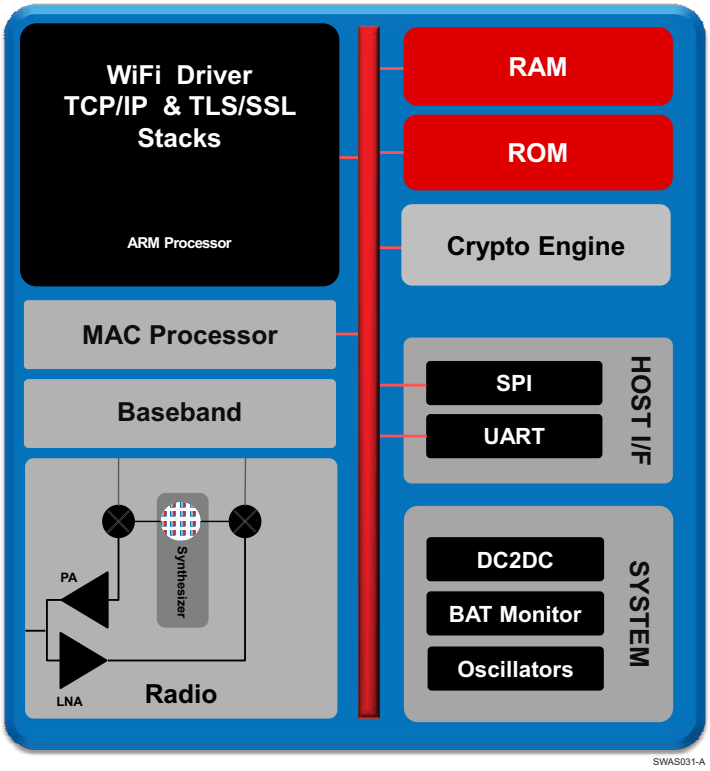


Figure 1-2. CC3100 Hardware Overview

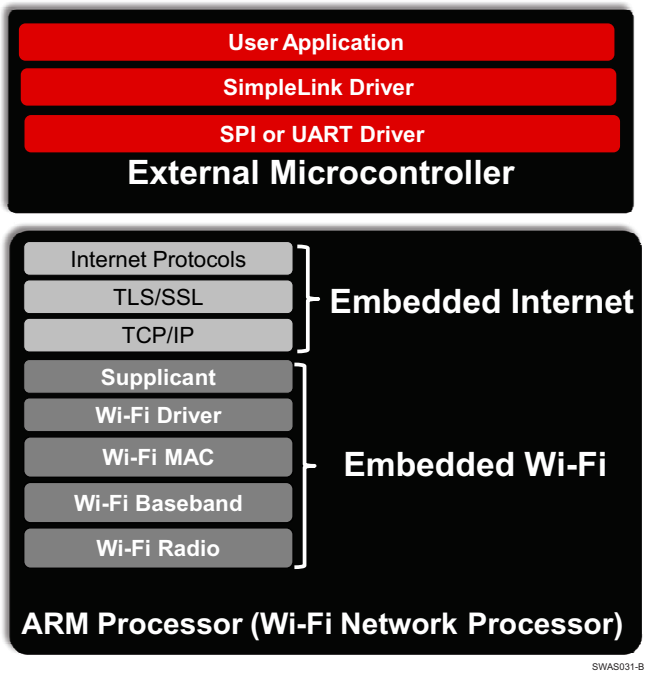


Figure 1-3. CC3100 Software Overview

Table of Contents

2 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial release.

3 Terminal Configuration and Functions

3.1 CC3100MOD Pin Diagram

Figure 3-1 shows the pin diagram for the CC3100MOD.

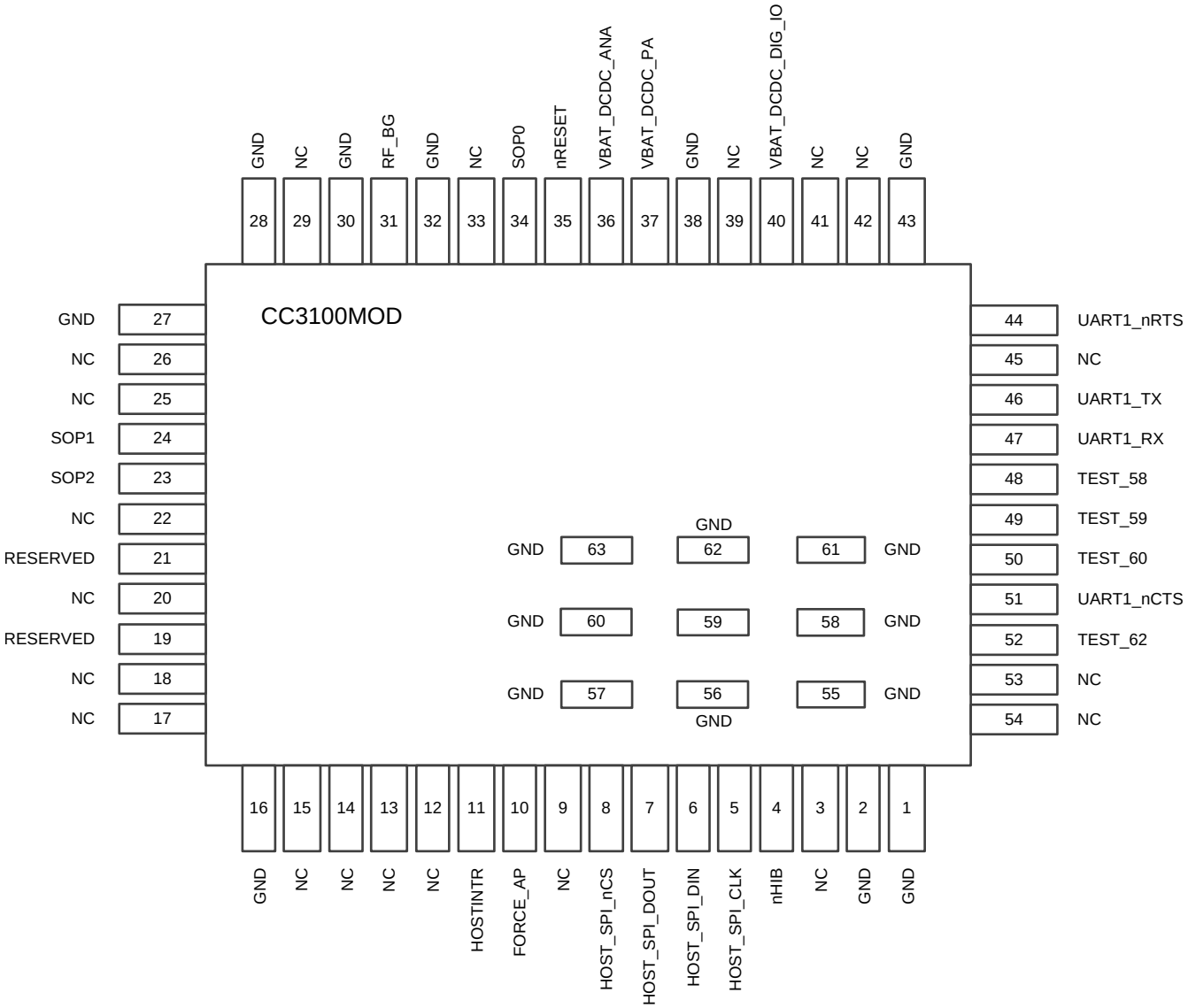


Figure 3-1. CC3100MOD Pin Diagram (Bottom View)

NOTE

Figure 3-1 shows the approximate location of pins on the module. For the actual mechanical diagram refer to Section 9.

3.2 Pin Attributes

Table 3-1 lists the pin descriptions of the CC3100MOD module.

NOTE

If an external device drives a positive voltage to signal pads when the CC3100MOD is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3100MOD can occur. To prevent current draw, TI recommends one of the following:

- All devices interfaced to the CC3100MOD must be powered from the same power rail as the CC3100MOD.
- Use level-shifters between the CC3100MOD and any external devices fed from other independent rails.
- The nRESET pin of the CC3100MOD must be held low until the VBAT supply to the device is driven and stable.

Table 3-1. Pin Attributes

MODULE PIN NO.	MODULE PIN NAME	TYPE	MODULE PIN DESCRIPTION
1	GND	-	Ground
2	GND	-	Ground
3	NC	-	Reserved. Do not connect
4	nHIB	I	Hibernate signal, active low. Refer to Figure 4-8.
5	HOST_SPI_CLK	I	Host interface SPI clock
6	HOST_SPI_DIN	I	Host interface SPI data input
7	HOST_SPI_DOUT	O	Host interface SPI data output
8	HOST_SPI_nCS	I	Host interface SPI chip select (active low)
9	NC	-	Reserved. Do not connect
10	FORCE_AP	-	For forced AP mode, pull to high on the board using a 100-kΩ resistor. Otherwise, pull down to ground using a 100-kΩ resistor.(1)
11	HOSTINTR	O	Interrupt output
12	NC	-	Reserved. Do not connect
13	NC	-	Reserved. Do not connect
14	NC	-	Reserved. Do not connect
15	NC	-	Reserved. Do not connect
16	GND	-	Ground
17	NC	-	Reserved. Do not connect
18	NC	-	Reserved. Do not connect
19	RESERVED	-	Reserved. Do not connect
20	NC	-	Unused. Do not connect.
21	RESERVED	-	Add 100-kΩ external pulldown resistor
22	NC	-	Reserved. Do not connect
23	SOP2	-	Add 10k pulldown to ground
24	SOP1	-	Reserved. Do not connect.
25	NC	-	Reserved. Do not connect
26	NC	-	Reserved. Do not connect
27	GND	-	Ground
28	GND	-	Ground
29	NC	-	Reserved. Do not connect
30	GND	-	Ground. Reference for RF signal

(1) Using a configuration file stored on flash, the vendor can optionally block any possibility of bringing up AP using the FORCE_AP pin.

Table 3-1. Pin Attributes (continued)

MODULE PIN NO.	MODULE PIN NAME	TYPE	MODULE PIN DESCRIPTION
31	RF_BG	I/O	2.4-GHz RF input/output
32	GND	-	Ground. Reference for RF signal
33	NC	-	Reserved. Do not connect
34	SOP0	-	Reserved. Do not connect.
35	nRESET	I	Power on reset. Does not require external RC circuit
36	VBAT_DCDC_ANA	-	Power supply for the module, can be connected to battery (2.3 V to 3.6 V)
37	VBAT_DCDC_PA	-	Power supply for the module, can be connected to battery (2.3 V to 3.6 V)
38	GND	-	Ground
39	VDD_ANA2	-	To be left unconnected. Used for prototype samples only.
40	VBAT_DCDC_DIG_IO	-	Power supply for the module, can be connected to battery (2.3 V to 3.6 V)
41	NC	-	Reserved. Do not connect
42	NC	-	Reserved. Do not connect
43	GND	-	Ground
44	UART1_nRTS	O	UART request to send, connect to external test point. Used for on-module flash reprogramming
45	NC	-	Reserved. Do not connect
46	UART1_TX	O	UART transmit, connect to external test point. Used for on-module flash reprogramming
47	UART1_RX	I	UART receive, connect to external test point. Used for on-module flash reprogramming
48	TEST_58	O	Connect to external test point
49	TEST_59	I	Connect to external test point
50	TEST_60	O	Connect to external test point
51	UART1_nCTS	I	UART clear to send, connect to external test point. Used for on-module flash reprogramming
52	TEST_62	O	Connect to external test point
53	NC	-	Reserved. Do not connect
54	NC	-	Reserved. Do not connect
55	GND	-	Thermal Ground
56	GND	-	Thermal Ground
57	GND	-	Thermal Ground
58	GND	-	Thermal Ground
59	GND	-	Thermal Ground
60	GND	-	Thermal Ground
61	GND	-	Thermal Ground
62	GND	-	Thermal Ground
63	GND	-	Thermal Ground

4 Specifications

4.1 Absolute Maximum Ratings

These specifications indicate levels where permanent damage to the module can occur. Functional operation is not ensured under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the module.

SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
VBAT and VIO	Respect to GND	–0.5	3.3	3.8	V
Digital I/O	Respect to GND	–0.5	–	VBAT + 0.5	V
RF pins		–0.5		2.1	V
Analog pins		–0.5		2.1	V
Temperature		–40		+85	°C

4.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–40	85	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)		–1.0	1.0	kV
		Charged device model (CDM), per JESD22-C101(2)	All pins	–250	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Power-On Hours

CONDITIONS	POH
$T_{Ambient}$ up to 85°C, assuming 20% active mode and 80% sleep mode	17,500

4.4 Recommended Operating Conditions

Function operation is not ensured outside this limit, and operation outside this limit for extended periods can adversely affect long-term reliability of the module.(1)

SYMBOL	CONDITION(2)	MIN	TYP	MAX	UNIT
VBAT and VIO	Battery mode	2.3	3.3	3.6	V
Operating temperature	–	–20	25	70	°C
Ambient thermal slew		–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV.

4.5 Brown-Out and Black-Out

The module enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Figure 4-1 and Figure 4-2). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations (such as a TX packet) cause a dip in the supply voltage, potentially triggering a brown-out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (4 contacts for a 2 x AA battery) and the wiring and PCB routing resistance.

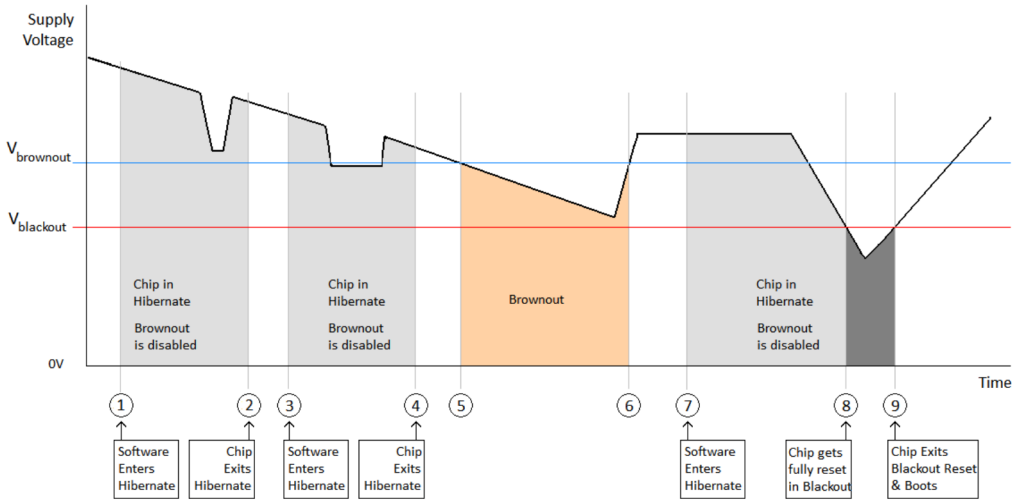


Figure 4-1. Brown-Out and Black-Out Levels (1 of 2)

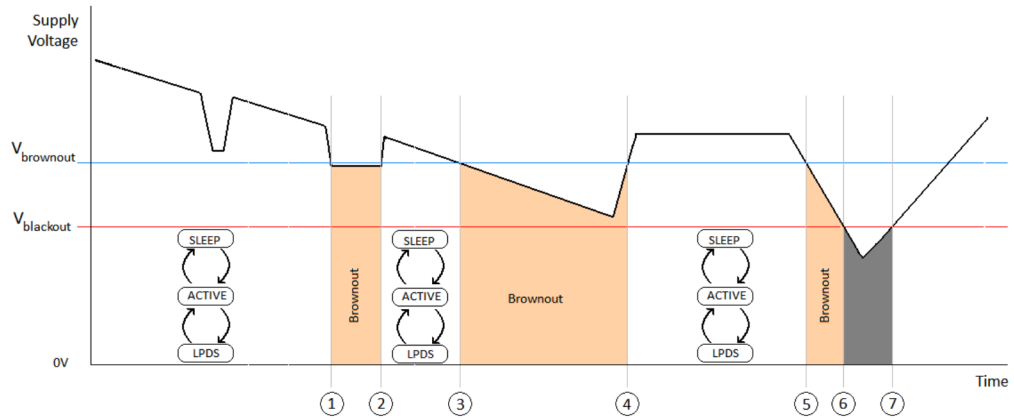


Figure 4-2. Brown-Out and Black-Out Levels (2 of 2)

In the brown-out condition, all sections of the CC3100MOD shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA.

The black-out condition is equivalent to a hardware reset event in which all states within the module are lost.

4.6 Electrical Characteristics (3.3 V, 25°C)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{IN}	Pin capacitance			4		pF
V_{IH}	High-level input voltage		0.65 × VDD		VDD + 0.5 V	V
V_{IL}	Low-level input voltage		–0.5		0.35 × VDD	V
I_{IH}	High-level input current			5		nA
I_{IL}	Low-level input current			5		nA
V_{OH}	High-level output voltage (VDD = 3.0 V)		2.4			V
V_{OL}	Low-level output voltage (VDD = 3.0 V)				0.4	V
I_{OH}	High-level source current, VOH = 2.4		6			mA
I_{OL}	Low-level sink current, VOH = 0.4		6			mA
Pin Internal Pullup and Pulldown (25°C)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**NOM**	**MAX**	**UNIT**
I_{OH}	Pullup current, V_{OH} = 2.4 (VDD = 3.0 V)		5		10	µA
I_{OL}	Pulldown current, V_{OL} = 0.4 (VDD = 3.0 V)		5			µA
V_{IL}	nRESET(1)			0.6		V

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

4.7 Thermal Resistance Characteristics for MOB Package

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	9.08	0.00
$R\Theta_{JB}$	Junction-to-board	10.34	0.00
$R\Theta_{JA}$	Junction-to-free air	11.60	0.00
$R\Theta_{JMA}$	Junction-to-moving air	5.05	< 1.00
Psi_{JT}	Junction-to-package top	9.08	0.00
Psi_{JB}	Junction-to-board	10.19	0.00

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70ºC is assumed.
(3) m/s = meters per second.

4.8 Reset Requirement

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operation mode level	ViH		0.65 × VBAT		V
Shutdown mode level(1)	ViL	0	0.6 V		V
Minimum time for nReset low for resetting the module		5			ms
Rise/fall times	Tr/Tf		20		µs

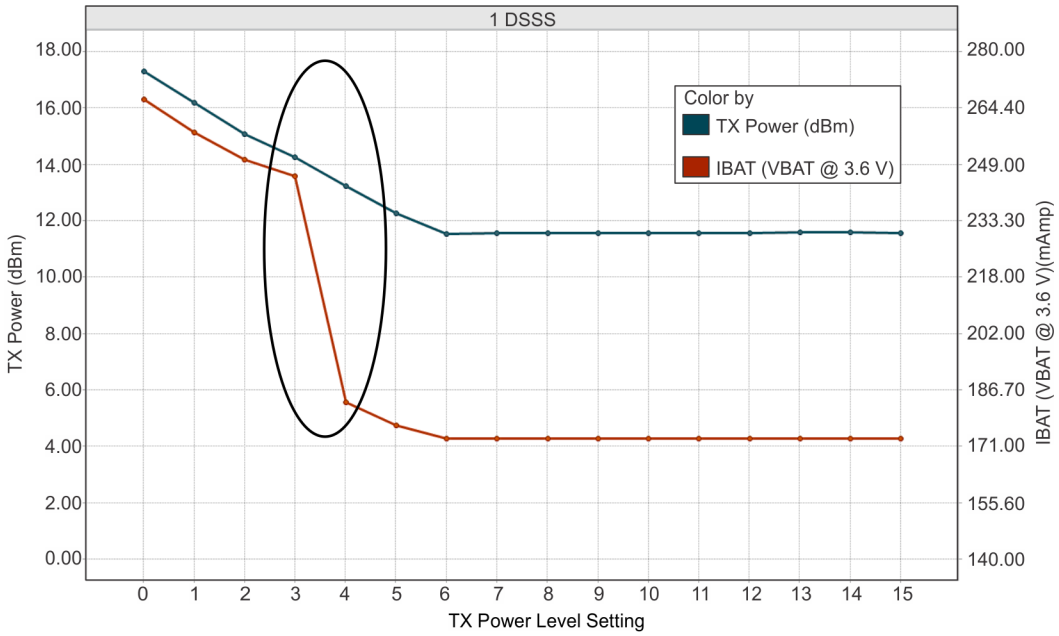
(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

4.9 Current Consumption

T_A = +25°C, V_{BAT} = 3.6 V

PARAMETER	TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
TX	1 DSSS	TX power level = 0		272		mA
		TX power level = 4		188		
	6 OFDM	TX power level = 0		248		
		TX power level = 4		179		
	54 OFDM	TX power level = 0		223		
		TX power level = 4		160		
RX (3)	1 DSSS			53		
	54 OFDM			53		
Idle connected (4)				0.715		
LPDS				0.140		
Hibernate				7		µA
Peak calibration current (3) (5)	V_{BAT} = 3.3 V			450		mA
	V_{BAT} = 2.3 V			620		

(1) TX power level = 0 implies maximum power. TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3100 system is a constant power-source system. The active current numbers scale inversely on the V_{BAT} voltage supplied.
(3) The RX current is measured with a 1-Mbps throughput rate.
(4) DTIM = 1
(5) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. Calibration is performed sparingly, typically when coming out of Hibernate and only if temperature has changed by more than 20°C or the time elapsed from prior calibration is greater than 24 hours.



Note: The area enclosed in the circle represents a significant reduction in current when transitioning from TX power level 3 to 4. In the case of lower range requirements (13-dbm output power), TI recommends using TX power level 4 to reduce the current.

Figure 4-3. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

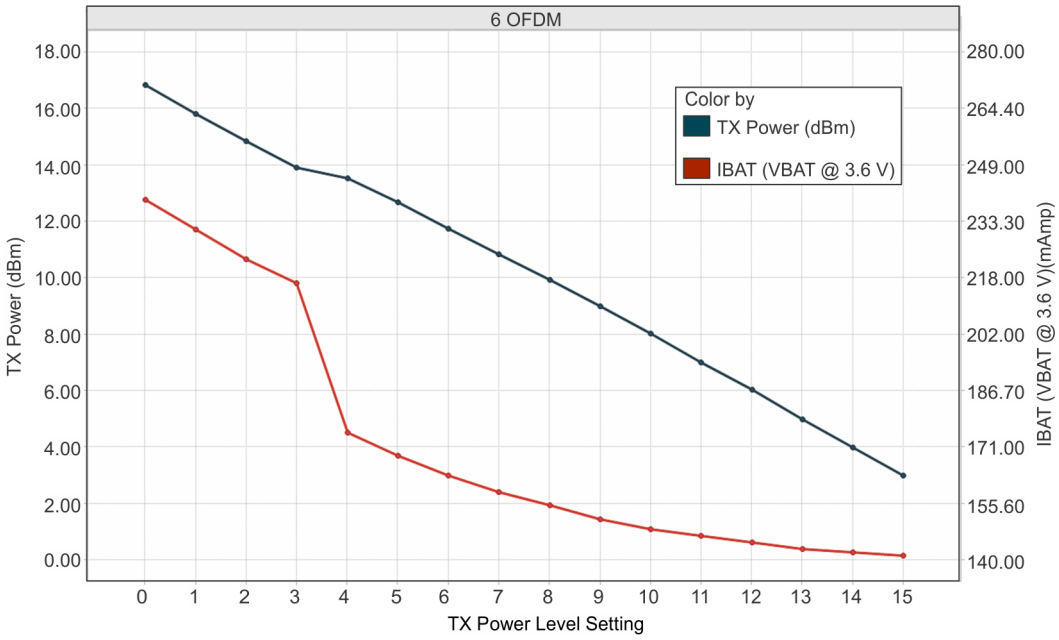


Figure 4-4. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

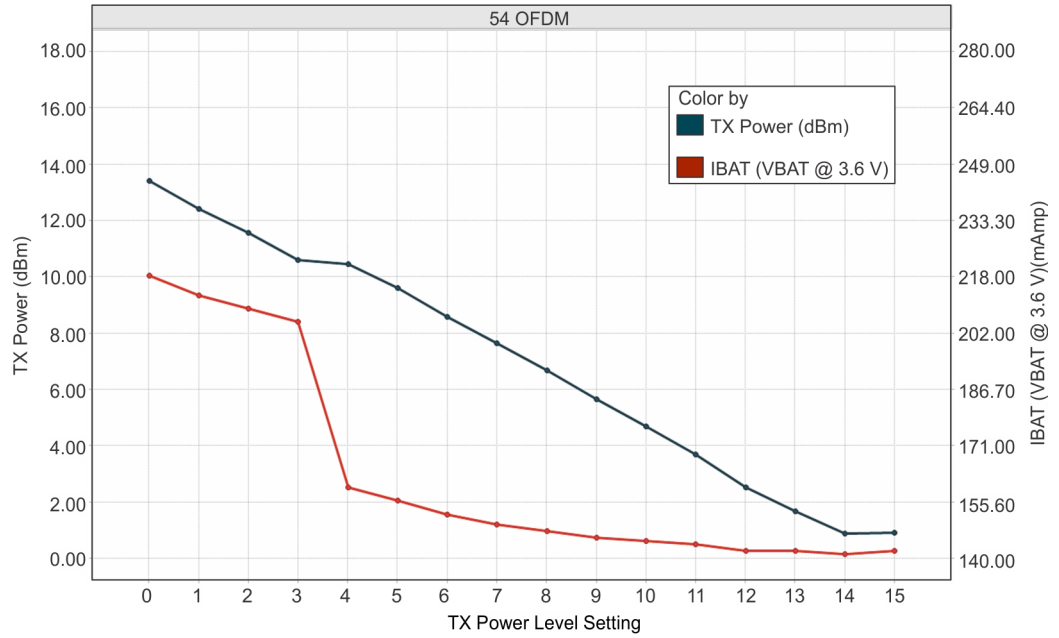


Figure 4-5. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

4.10 WLAN RF Characteristics

WLAN Receiver Characteristics

T_A = +25°C, V_{BAT} = 2.3 to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz)

PARAMETER	CONDITION (Mbps)	MIN	TYP	MAX	UNITS
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(10% PER)(1)	1 DSSS		–94.7		dBm
	2 DSSS		–92.6		
	11 CCK		–87.0		
	6 OFDM		–89.0		
	9 OFDM		–88.0		
	18 OFDM		–85.0		
	36 OFDM		–79.5		
	54 OFDM		–73.0		
	MCS7 (Mixed Mode)		–69.0		
Maximum input level (10% PER)	802.11b		–3.0		
	802.11g		–9.0		

(1) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

4.10.1 WLAN Transmitter Characteristics(1)

T_A = +25°C, V_{BAT} = 2.3 to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
Max RMS Output Power measured at 1 dB from IEEE spectral mask or EVM	1DSSS		17		dBm
	2DSSS		17		
	11CCK		17.25		
	6OFDM		16.25		
	9OFDM		16.25		
	18OFDM		16		
	36OFDM		15		
	54OFDM		13.5		
	MCS7 (Mixed Mode)		12		
Transmit center frequency accuracy		–20		20	ppm

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 and 2472 MHz) have reduced TX power to meet FCC emission limits.

4.11 Timing Characteristics

4.11.1 SPI Host Interface Timings

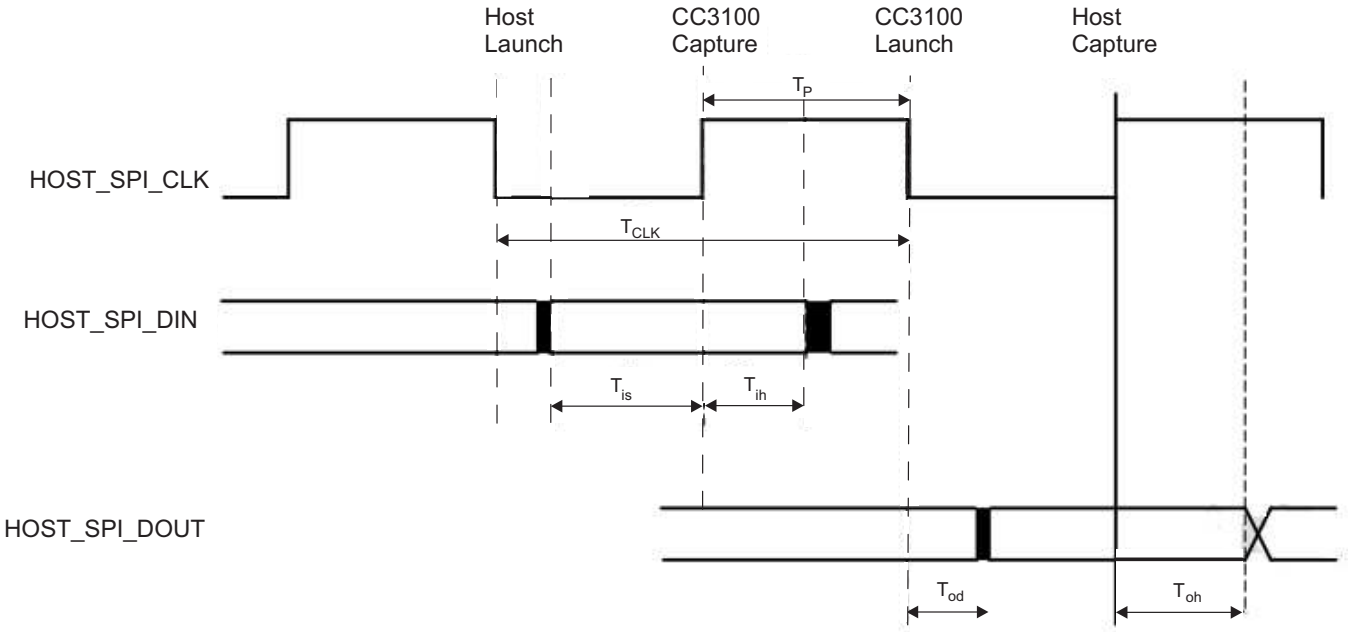


Figure 4-6. SPI Host Interface Timing(1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
F	Clock frequency		20	MHz
T_{CLK}	Clock period	41.6	0.35 × VBAT	ns
	Duty cycle	45%	55%	
T_{is}	RX setup time: minimum time in which data is stable before capture edge	4		ns
T_{ih}	RX hold time: minimum time in which data is stable after capture edge	4		ns
T_{od}	TX setup propagation time: maximum time from launch edge until data is stable		16	ns
T_{oh}	TX hold propagation time: minimum time of data stable after launch edge		24	ns
C_L	Capacitive load on interface		20	pF

(1) Ensure that nCS (active-low signal) is asserted 10 ns before the clock is toggled. nCS can be deasserted 10 ns after the clock edge

4.11.2 Wake-Up Sequence

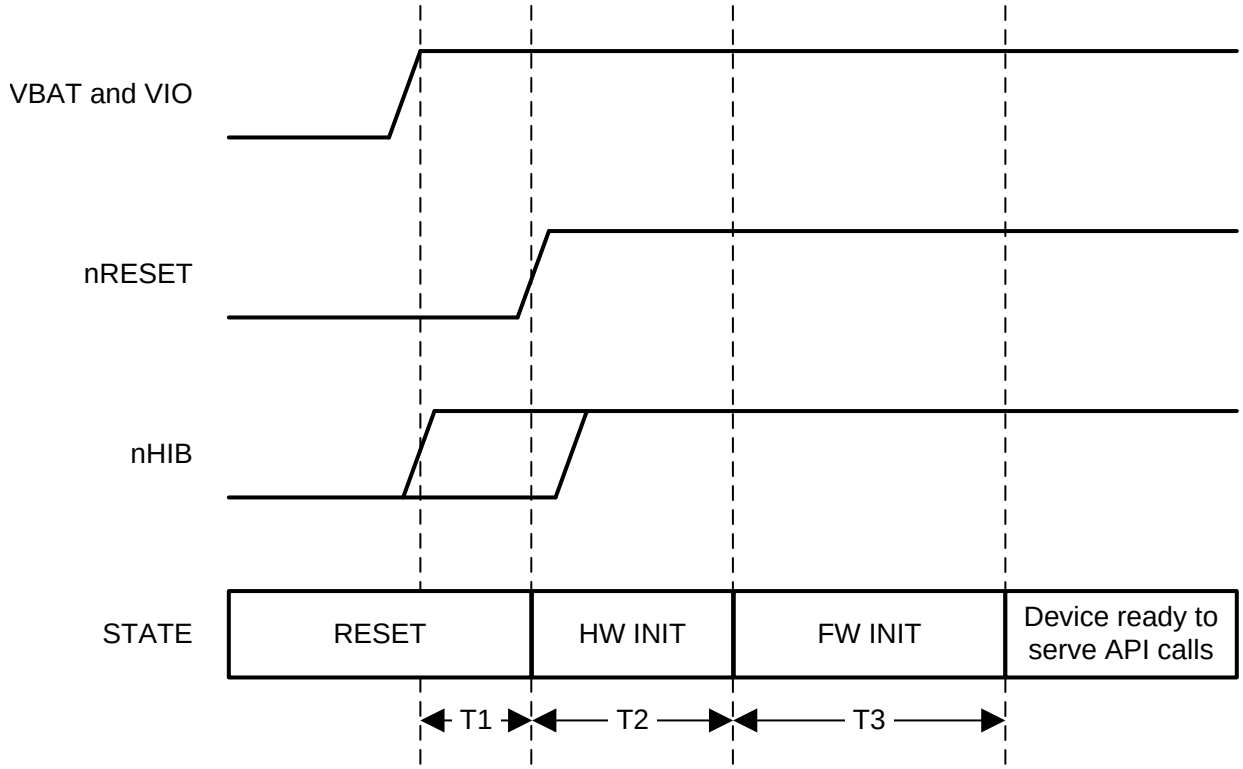


Figure 4-7. Wake-Up Sequence

Table 4-1. First-Time Power-Up and Reset Removal Timing Requirements (32K XTAL)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
T1	Supply settling time	Depends on application board power supply, decap, and so on		3 ms	
T2	Hardware wakeup time			25 ms	
T3	Initialization time	32-kHz XTAL settling + firmware initialization time + radio calibration		1.35 s	

4.11.3 Wakeup from Hibernate

Figure 4-8 shows the timing diagram for wakeup from the hibernate state.

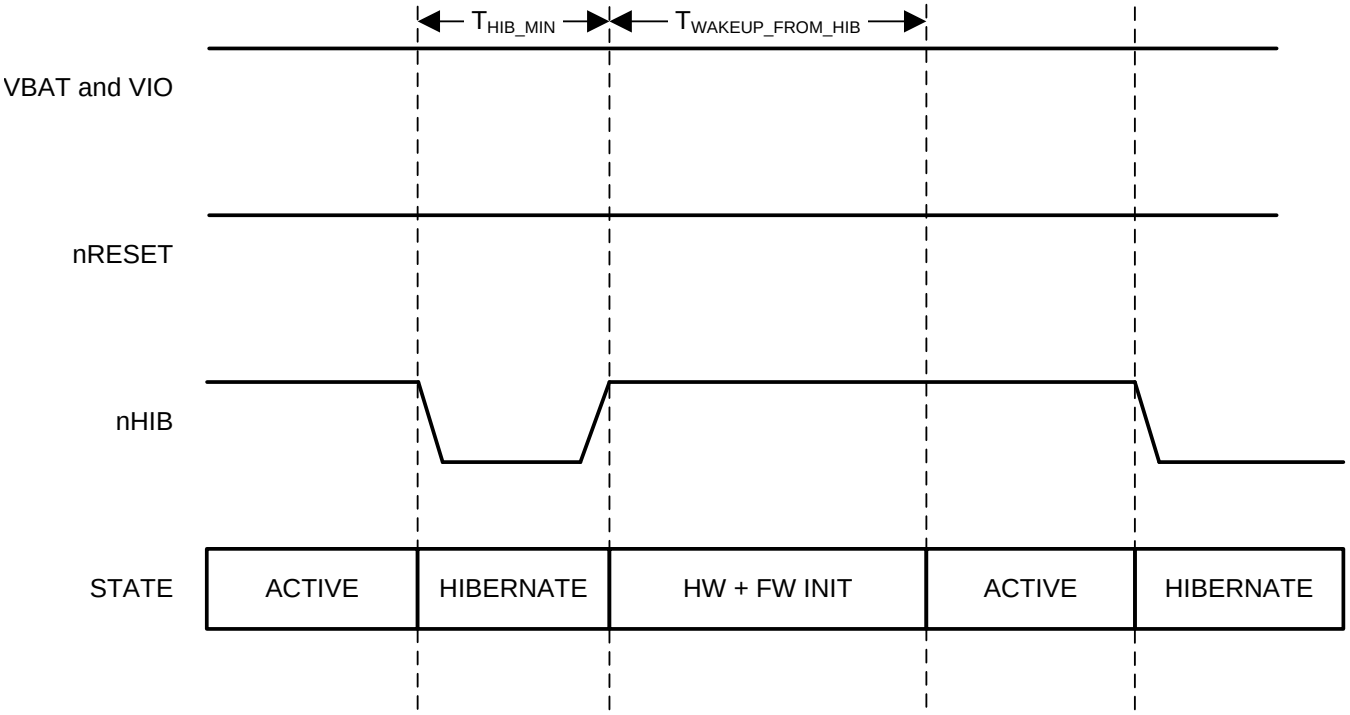


Figure 4-8. nHIB Timing Diagram

NOTE

The internal 32.768-kHz crystal oscillator is kept enabled by default when the chip goes to hibernate in response to nHIB being pulled low.

Table 4-2. nHIB Timing Requirements(1)

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
T_{hib_min}	Minimum hibernate time	Minimum LOW pulse width of nHIB	10 ms		
$T_{wake\_from\_hib}$	Hardware wakeup time plus firmware initialization time	See (2).		50 ms	

(1) Ensure that the nHIB low duration is not less than the specified width under all conditions, including power-ON, MCU hibernation, and so forth.
(2) If temperature changes by more than 20°C, initialization time from HIB can increase by 200 ms due to radio calibration.

4.11.4 Interfaces

This section describes the interfaces that are supported by the CC3100 module:

- Host SPI
- Host UART

4.11.4.1 Host SPI Interface Timing

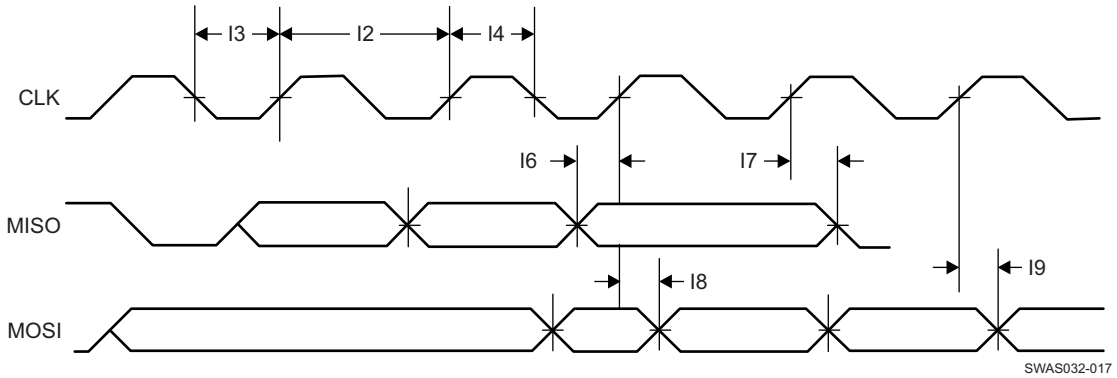


Figure 4-9. Host SPI Interface Timing

Table 4-3. Host SPI Interface Timing Parameters

PARAMETER NUMBER	PARAMETER(1)	PARAMETER NAME	MIN	MAX	UNIT
I1	F	Clock frequency @ V_{BAT} = 3.3 V		20	MHz
		Clock frequency @ V_{BAT} ≤ 2.1 V		12	
I2	t_{clk}(2)	Clock period	50		ns
I3	t_{LP}	Clock low period		25	ns
I4	t_{HT}	Clock high period		25	ns
I5	D	Duty cycle	45%	55%	
I6	t_{IS}	RX data setup time	4		ns
I7	t_{IH}	RX data hold time	4		ns
I8	t_{OD}	TX data output delay		20	
I9	t_{OH}	TX data hold time		24	ns

(1) The timing parameter has a maximum load of 20 pf at 3.3 V.
(2) Ensure that nCS (active-low signa)l is asserted 10 ns before the clock is toggled. nCS can be deasserted 10 ns after the clock edge.

4.11.4.2 SPI Host Interface

The device interfaces to an external host using the SPI interface. The CC3100 device can interrupt the host using the HOST_INTR line to initiate the data transfer over the interface. The SPI host interface can work up to a speed of 20 MHz.

Figure 4-10 shows the SPI host interface.

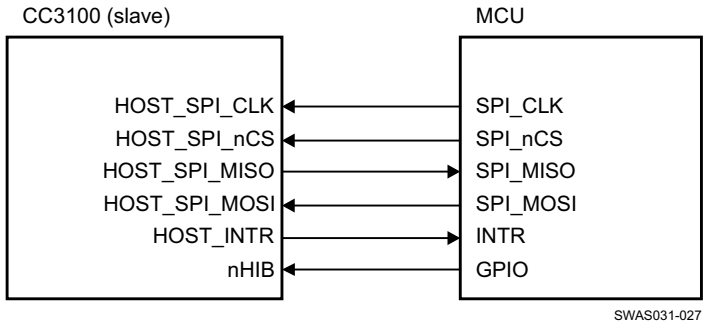


Figure 4-10. SPI Host Interface

Table 4-4 lists the SPI host interface pins.

Table 4-4. SPI Host Interface

Pin Name	Description
HOST_SPI_CLK	Clock (up to 20 MHz) from MCU host to CC3100 device
HOST_SPI_nCS	CS (active low) signal from MCU host to CC3100 device
HOST_SPI_MOSI	Data from MCU host to CC3100 device
HOST_INTR	Interrupt from CC3100 device to MCU host
HOST_SPI_MISO	Data from CC3100 device to MCU host
nHIB	Active-low signal that commands the CC3100 device to enter hibernate mode (lowest power state)

4.11.4.3 Host UART

The SimpleLink device requires the UART configuration described in Table 4-5.

Table 4-5. SimpleLink UART Configuration

Property	Supported CC3100 Configuration
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only(1)

(1) The SimpleLink device does not support automatic detection of the host length while using the UART interface.

4.11.4.3.1 5-Wire UART Topology

Figure 4-11 shows the typical 5-wire UART topology comprised of 4 standard UART lines plus one IRQ line from the device to the host controller to allow efficient low power mode.

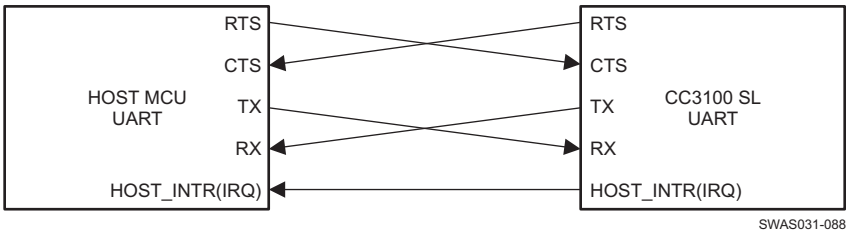


Figure 4-11. Typical 5-Wire UART Topology

This is the typical and recommended UART topology because it offers the maximum communication reliability and flexibility between the host and the SimpleLink device.

4.11.4.3.2 4-Wire UART Topology

The 4-wire UART topology eliminates the host IRQ line (see Figure 4-12). Using this topology requires one of the following conditions to be met:

- Host is always awake or active.
- Host goes to sleep but the UART module has receiver start-edge detection for auto wakeup and does not lose data.

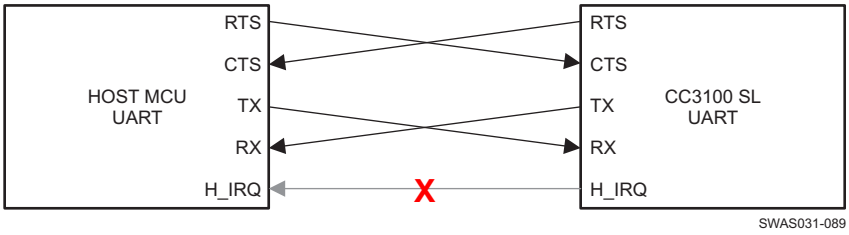


Figure 4-12. 4-Wire UART Configuration

4.11.4.3.3 3-Wire UART Topology

The 3-wire UART topology requires only the following lines (see Figure 4-13):

- RX
- TX
- CTS

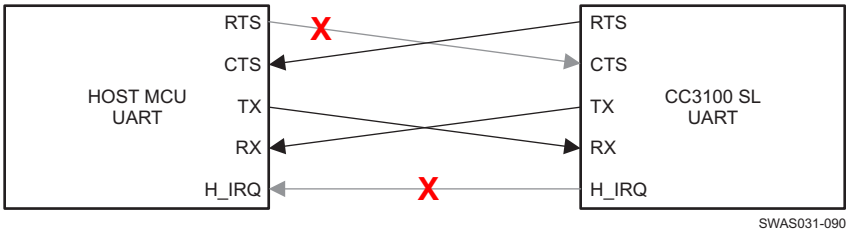


Figure 4-13. 3-Wire UART Topology

Using this topology requires one of the following conditions to be met:

- Host always stays awake or active.
- Host goes to sleep but the UART module has receiver start-edge detection for auto wakeup and does not lose data.
- Host can always receive any amount of data transmitted by the SimpleLink device because there is no flow control in this direction.

Because there is no full flow control, the host cannot stop the SimpleLink device to send its data; thus, the following parameters must be carefully considered:

- Max baud rate
- RX character interrupt latency and low-level driver jitter buffer
- Time consumed by the user's application

5 Detailed Description

5.1 Overview

5.1.1 Module Features

5.1.1.1 WLAN

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station with CCK and OFDM rates in the 2.4-GHz ISM band
- Auto-calibrated radio with a single-ended 50-Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in an NVMEM allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators
- SmartConfig technology: A 1-step, 1-time process to connect a CC3100MOD-enabled device to the home wireless network, removing dependency on the I/O capabilities of the host MCU; thus, it is usable by deeply embedded applications.
- 802.11 transceiver mode: Allows transmitting and receiving of proprietary data through a socket without adding MAC or PHY headers. This mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works together with the filtering options.

5.1.1.2 Network Stack

- Integrated IPv4 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC
- Support of eight simultaneous TCP, UDP, or RAW sockets
- Built-in network protocols: ARP, ICMP, DHCP client, and DNS client for easy connection to the local network and the Internet
- Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3100MOD provides critical information, such as device name, IP, vendor, and port number.

5.1.1.3 Host Interface and Driver

- Interfaces over a 4-wire serial peripheral interface (SPI) with any MCU or a processor at a clock speed of 20 MHz.
- Interfaces over UART with any MCU with a baud rate up to 3 Mbps. A low footprint driver is provided for TI MCUs and is easily ported to any processor or ASIC.
- Simple APIs enable easy integration with any single-threaded or multithreaded application.

5.1.1.4 System

- Works from a single preregulated power supply or connects directly to a battery
- Ultra-low leakage when disabled (hibernate mode) with a current of less than 7 µA with the RTC running
- Integrated clock sources

5.2 Functional Block Diagram

Figure 5-1 shows the functional block diagram of the CC3100MOD SimpleLink Wi-Fi solution.

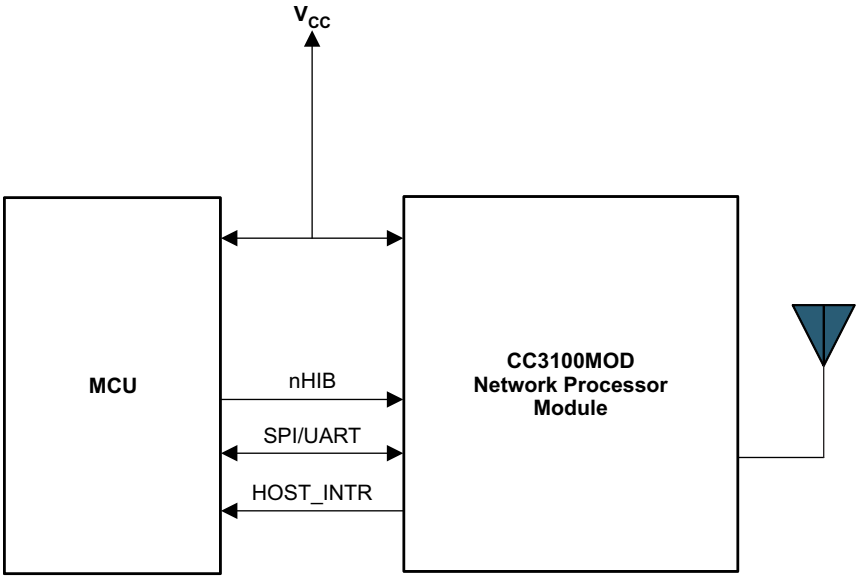


Figure 5-1. Functional Block Diagram

5.3 Wi-Fi Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated ARM MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3100MOD supports station, AP, and Wi-Fi Direct modes. The module also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi network processor includes an embedded IPv4 TCP/IP stack.

Table 5-1 summarizes the NWP features.

Table 5-1. Summary of Features Supported by the NWP Subsystem

ITEM	DOMAIN	CATEGORY	FEATURE	DETAILS
1	TCP/IP	Network Stack	IPv4	Baseline IPv4 stack
2	TCP/IP	Network Stack	TCP/UDP	Base protocols
3	TCP/IP	Protocols	DHCP	Client and server mode
4	TCP/IP	Protocols	ARP	Support ARP protocol
5	TCP/IP	Protocols	DNS/mDNS	DNS Address resolution and local server
6	TCP/IP	Protocols	IGMP	Up to IGMPv3 for multicast management
7	TCP/IP	Applications	mDNS	Support multicast DNS for service publishing over IP
8	TCP/IP	Applications	mDNS-SD	Service discovery protocol over IP in local network
9	TCP/IP	Applications	Web Sever/HTTP Server	URL static and dynamic response with template.
10	TCP/IP	Security	TLS/SSL	TLS v1.2 (client/server)/SSL v3.0
11	TCP/IP	Security	TLS/SSL	For the supported Cipher Suite, go to SimpleLink Wi-Fi CC3100 SDK.
12	TCP/IP	Sockets	RAW Sockets	User-defined encapsulation at WLAN MAC/PHY or IP layers
13	WLAN	Connection	Policies	Allows management of connection and reconnection policy
14	WLAN	MAC	Promiscuous mode	Filter-based Promiscuous mode frame receiver
15	WLAN	Performance	Initialization time	From enable to first connection to open AP less than 50 ms

Table 5-1. Summary of Features Supported by the NWP Subsystem (continued)

ITEM	DOMAIN	CATEGORY	FEATURE	DETAILS
16	WLAN	Performance	Throughput	UDP = 16 Mbps
17	WLAN	Performance	Throughput	TCP = 13 Mbps
18	WLAN	Provisioning	WPS2	Enrollee using push button or PIN method.
19	WLAN	Provisioning	AP Config	AP mode for initial product configuration (with configurable Web page and beacon Info element)
20	WLAN	Provisioning	SmartConfig	Alternate method for initial product configuration
21	WLAN	Role	Station	802.11bgn Station with legacy 802.11 power save
22	WLAN	Role	Soft AP	802.11 bg single station with legacy 802.11 power save
23	WLAN	Role	P2P	P2P operation as GO
24	WLAN	Role	P2P	P2P operation as CLIENT
25	WLAN	Security	STA-Personal	WPA2 personal security
26	WLAN	Security	STA-Enterprise	WPA2 enterprise security
27	WLAN	Security	STA-Enterprise	EAP-TLS
28	WLAN	Security	STA-Enterprise	EAP-PEAPv0/TLS
29	WLAN	Security	STA-Enterprise	EAP-PEAPv1/TLS
30	WLAN	Security	STA-Enterprise	EAP-PEAPv0/MSCHAPv2
31	WLAN	Security	STA-Enterprise	EAP-PEAPv1/MSCHAPv2
32	WLAN	Security	STA-Enterprise	EAP-TTLS/EAP-TLS
33	WLAN	Security	STA-Enterprise	EAP-TTLS/MSCHAPv2
34	WLAN	Security	AP-Personal	WPA2 personal security

5.4 Power-Management Subsystem

The CC3100 power-management subsystem contains DC-DC converters to accommodate the differing voltage or current requirements of the system. The module can operate from an input voltage ranging from 2.3 V to 3.6 V and can be directly connected to 2xAA Alkaline batteries.

The CC3100MOD is a fully integrated module based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC-DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

5.4.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the module is powered directly by the battery. All other voltages required to operate the device are generated internally by the DC-DC converters. This scheme is the most common mode for the device as it supports wide-voltage operation from 2.3 to 3.6 V.

5.5 Low-Power Operating Modes

This section describes the low-power modes supported by the module to optimize battery life.

5.5.1 Low-Power Deep Sleep

The low-power deep-sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The module draws about 7 µA from the supply in this low-power mode. The module can wake up in less than 3 ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 140 µA. During LPDS mode, the module retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit this sleep mode.

5.5.2 Hibernate

The hibernate mode is the lowest power mode in which all of the digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The real-time clock (RTC) is kept running and the module wakes up once the n_HIB line is asserted by the host driver. The wake-up time is longer than LPDS mode at about 50 ms.

NOTE

Wake-up time can be extended to 75 ms if a patch is loaded from the serial flash.

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Reference Schematics

Figure 6-1 shows the reference schematic for the CC3100MOD module.

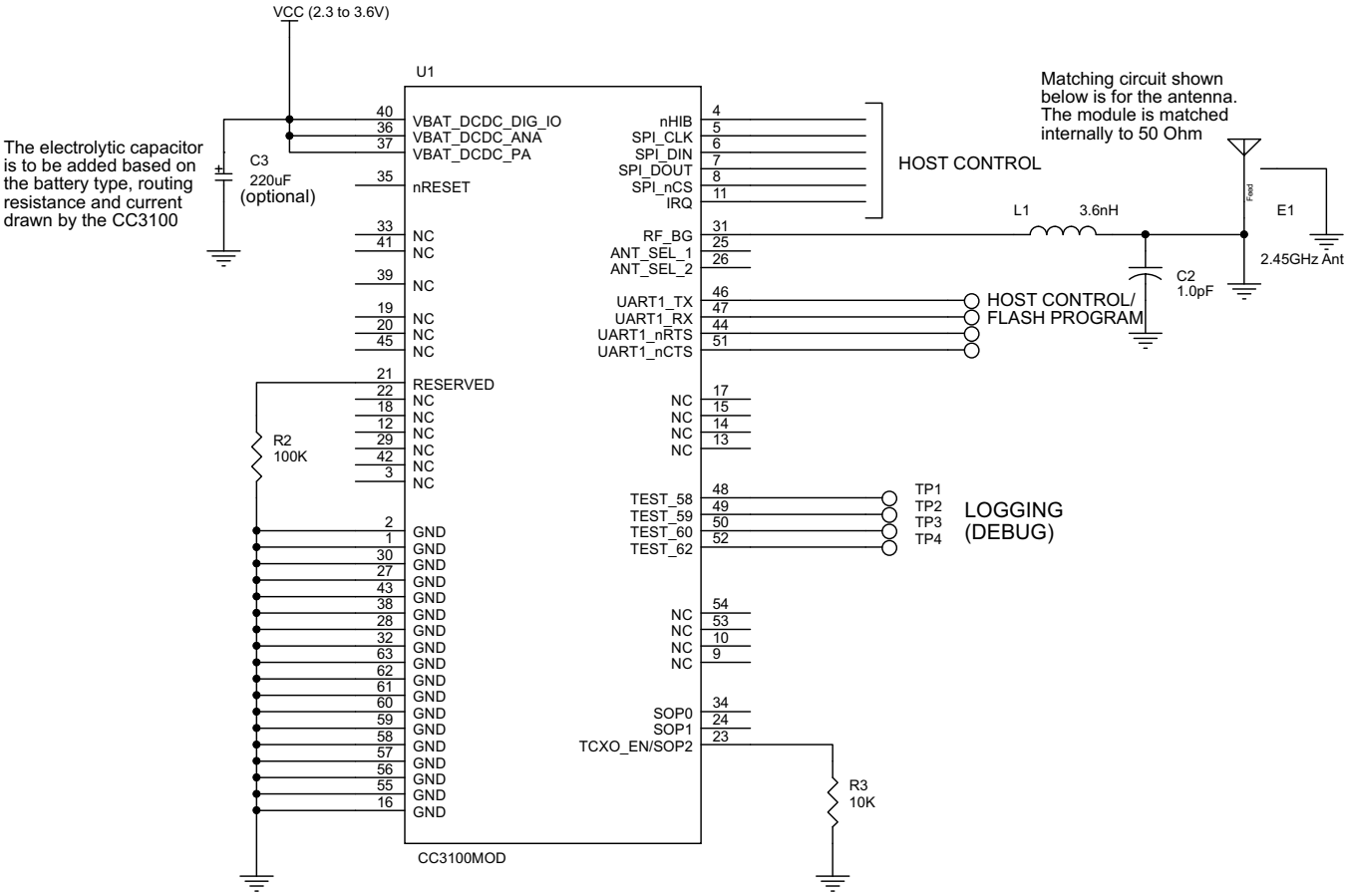


Figure 6-1. CC3100MOD Module Reference Schematic

6.2 Bill of Materials(1)

QUANTITY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	U1	CC3100MOD	Texas Instruments	CC3100MODR11MAMOB	SimpleLink Wi-Fi MCU Module
1	E1	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	ANT *Bluetooth* WLAN ZigBee® WIMAX
1	C2	1.0 pF	Murata Electronics North America	GJM1555C1H1R0BB01D	CAP CER 1 pF 50 V NP0 0402
1	L1	3.6 nH	Murata Electronics North America	LQP15MN3N6B02D	INDUCTOR 3.6 NH 0.1 NH 0402

(1) Resistors are not shown here. Any resistor of 5% tolerance can be used.

6.3 Layout Recommendations

6.3.1 RF Section (Placement and Routing)

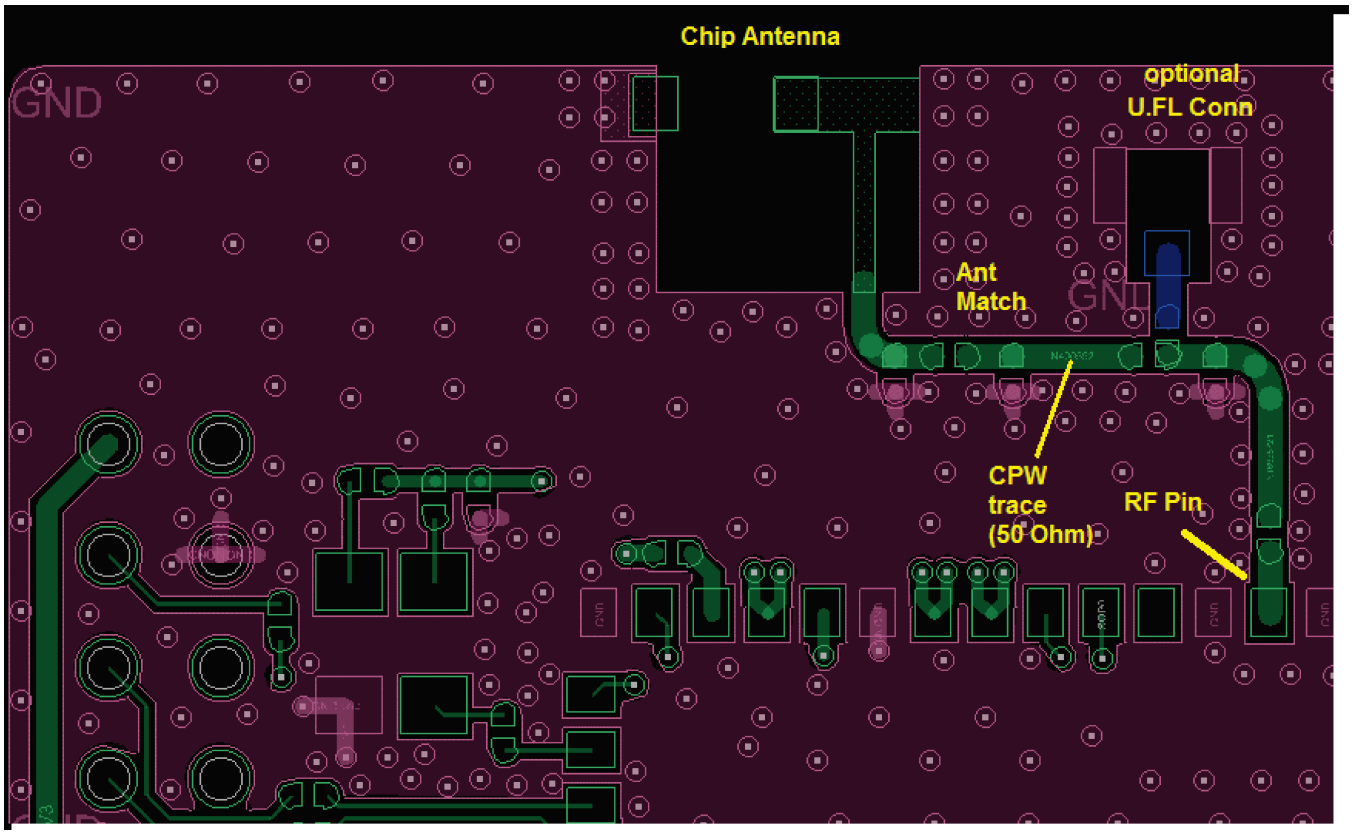


Figure 6-2. RF Section Layout

Being wireless device, the RF section gets the top priority in terms of layout. It is very important for the RF section to be laid out correctly to get the optimum performance from the device. A poor layout can cause low output power, EVM degradation, sensitivity degradation and mask violations.

6.3.2 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free space electromagnetic radiation. The placement and layout of the antenna is the key to increased range and data rates.

The following points need to be observed for the antenna.

SR NO.	GUIDELINES
1	Place the antenna on an edge or corner of the PCB
2	Make sure that no signals are routed across the antenna elements on all the layers of the PCB
3	Most antennas, including the chip antenna used on the booster pack require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure that there is provision to place matching components for the antenna. These need to be tuned for best return loss once the complete board is assembled. Any plastics or casing should also be mounted while tuning the antenna as this can impact the impedance.
5	Ensure that the antenna impedance is 50 Ω as the device is rated to work only with a 50-Ω system.
6	In case of printed antenna, ensure that the simulation is performed with the solder mask in consideration.
7	Ensure that the antenna has a near omni-directional pattern.
8	The feed point of the antenna is required to be grounded
9	To use the FCC certification of the Booster pack board, the antenna used should be of the same gain or lesser. In addition, the Antenna design should be exactly copied including the Antenna traces.

Table 6-1. Recommended Components

CHOICE	PART NUMBER	MANUFACTURER	NOTES
1	AH316M245001-T	Taiyo Yuden	Can be placed on edge of the PCB and uses very less PCB space
2	RFANT5220110A2T	Walsim	Need to place on the corner of PCB

6.3.3 Transmission Line

The RF signal from the device is routed to the antenna using a CPW-G (Coplanar Waveguide with ground) structure. This structure offers the maximum isolation across filter gap and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding

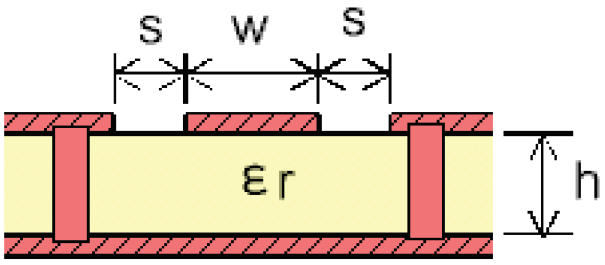


Figure 6-3. Coplanar Waveguide (Cross Section) with GND and Via Stitching

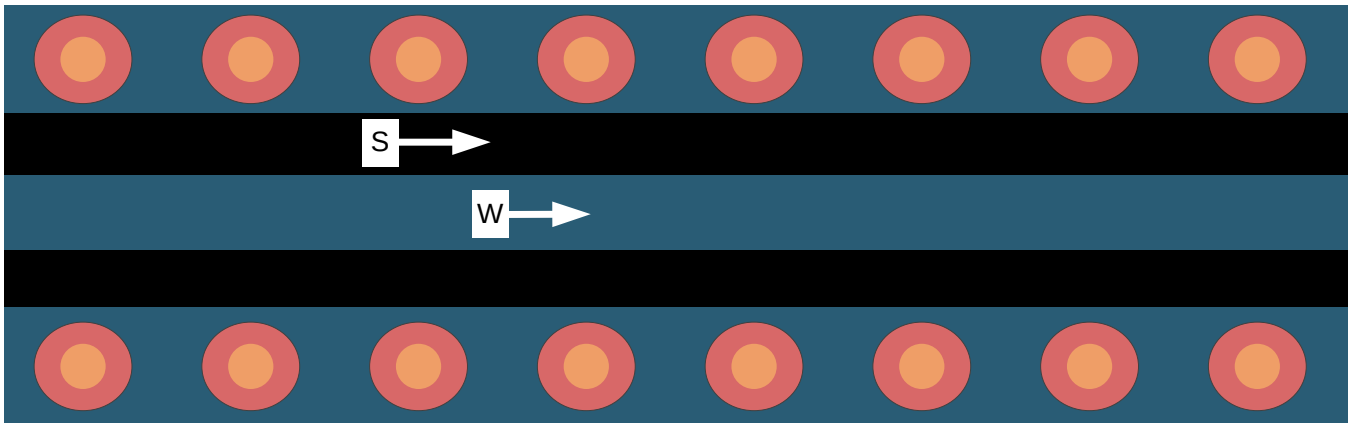


Figure 6-4. CPW with GND (Top View)

The recommended values for the PCB are provided for 4- and 2-layer boards in Table 6-2 and Table 6-3, respectively.

Table 6-2. Recommended PCB Values for 4-Layer Board (L1-L2 = 10 mils)

PARAMETER	VALUE	UNITS
W	20	mils
S	18	mils
H	10	mils
Er (FR-4 substrate)	4	

Table 6-3. Recommended PCB Values for 2-Layer Board (L1-L2 = 40 mils)

PARAMETER	VALUE	UNITS
W	35	mils
S	6	mils
H	40	mils
Er (FR-4 substrate)	3.9	

6.3.4 General Layout Recommendation

1. Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
2. Do not run signal traces underneath the module on a layer where the module is mounted.
3. RF traces must have 50-Ω impedance
4. RF trace bends must be gradual with a maximum bend of approximately 45 degrees and with trace mitered.
5. RF traces must not have sharp corners.
6. There must be no traces or ground under the antenna section.
7. RF traces must have via stitching on the ground plane beside the RF trace on both sides.
8. RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

7 Environmental Requirements and Specifications

7.1 Temperature

7.1.1 PCB Bending

The PCB bending specification shall maintain planeness at a thickness of less than 0.1 mm.

7.2 Handling Environment

7.2.1 Terminals

The product is mounted with motherboard through land grid array (LGA). To prevent poor soldering, do not touch the LGA portion by hand.

7.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product malfunction.

7.3 Storage Condition

7.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be a 12 months from the date the bag is sealed.

7.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

7.4 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12–24 hours

Baking times: 1 time

7.5 Soldering and Reflow Condition

1. Heating method: Conventional Convection or IR/convection
2. Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method.
3. Solder paste composition: Sn/3.0 Ag/0.5 Cu
4. Allowable reflow soldering times: 2 times based on the following reflow soldering profile (see Figure 7-1).
5. Temperature profile: Reflow soldering shall be done according to the following temperature profile (see Figure 7-1).
6. Peak temp: 245°C

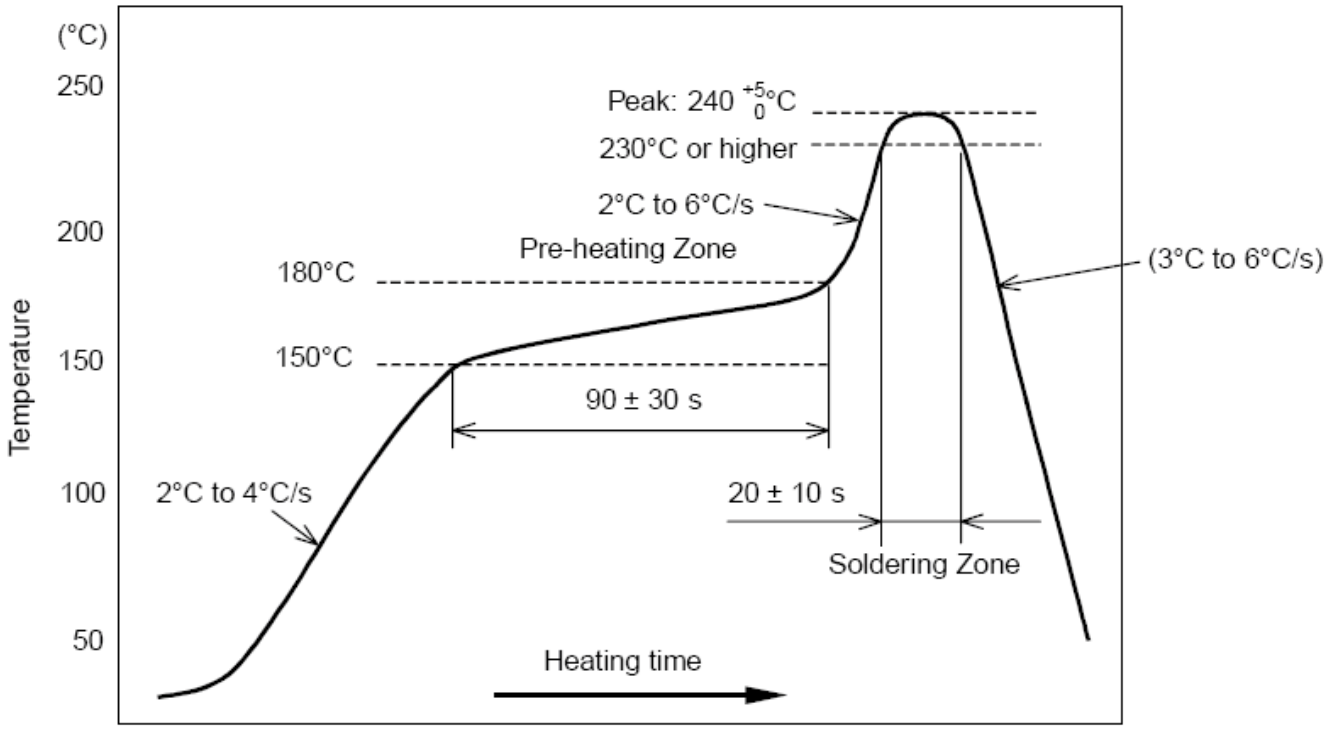


Figure 7-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

8 Product and Documentation Support

8.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the CC3100MOD applications:

Software Development Tools: Code Composer Studio Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any CC3100MOD application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the CC3100MOD platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.1 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in his or her module for production. To stay informed, sign up for the SDK Alert Me button on the tools page or www.ti.com/tool/cc3100sdk.

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3100MOD and support tools (see Figure 8-1).

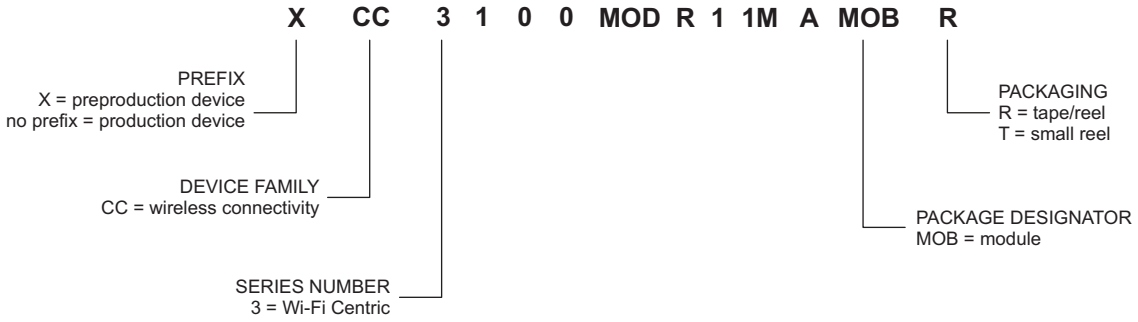


Figure 8-1. CC3100MOD Device Nomenclature

For orderable part numbers of CC3100MOD devices in the MOB package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.4 Trademarks

SimpleLink, Internet-On-a-Chip, SmartConfig, E2E, Code Composer Studio, DSP/BIOS, XDS are trademarks of Texas Instruments.
ARM is a registered trademark of ARM Limited.
Wi-Fi CERTIFIED, Wi-Fi Direct are trademarks of Wi-Fi Alliance.
Wi-Fi is a registered trademark of Wi-Fi Alliance.
ZigBee is a registered trademark of ZigBee Alliance.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

Figure 9-1 shows the CC3100MOD module.

9.1 Mechanical Drawing

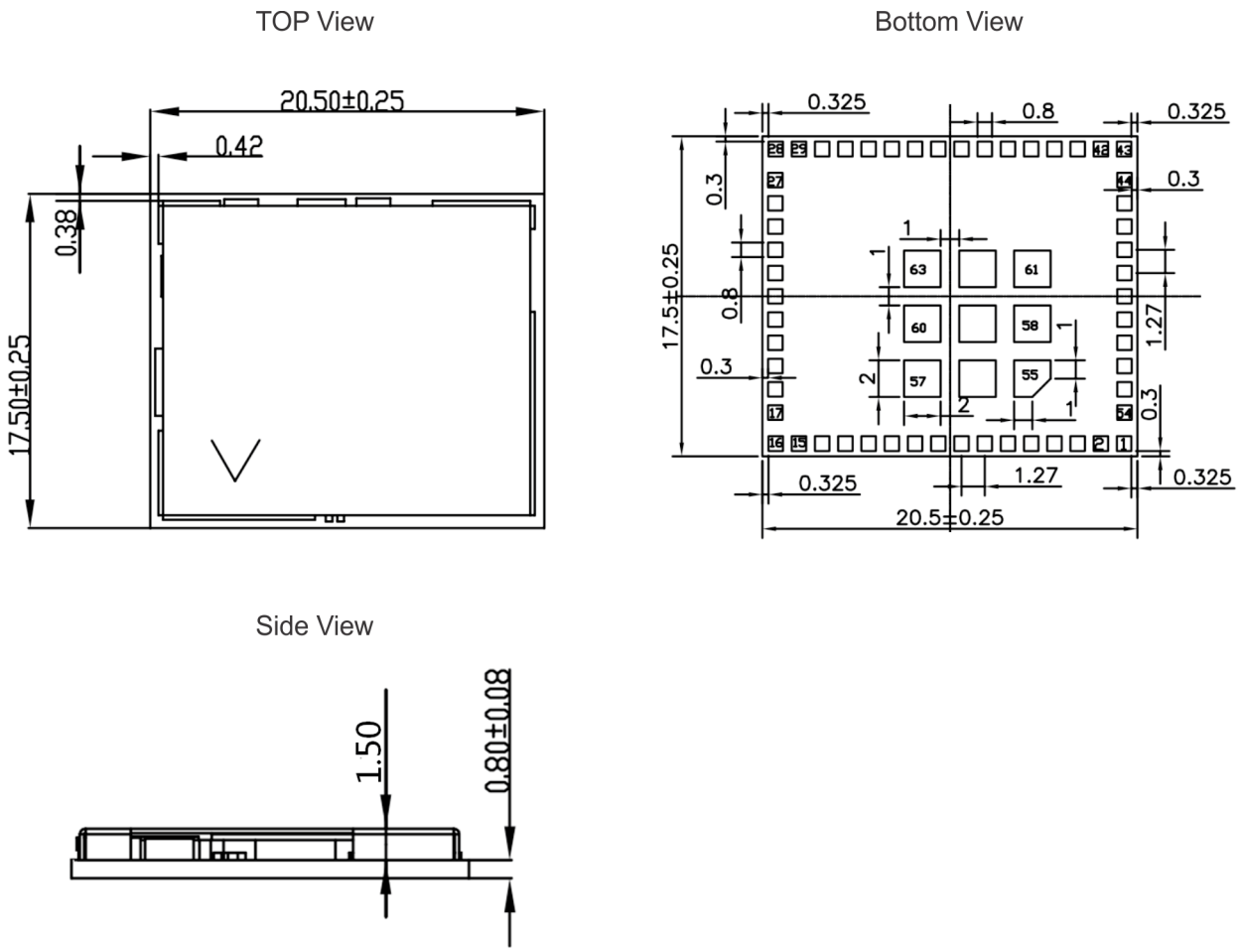


Figure 9-1. Mechanical Drawing

9.2 Package Option

We offer 2 reel size options for flexibility: a 1000-unit reel and a 250-unit reel.

9.2.1 Packaging Information

Orderable Device	Status (1)	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL, Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
CC3100MODR11MAMOBR	ACTIVE	MOB	63	1000	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3100MODR11MAMOB
CC3100MODR11MAMOBT	ACTIVE	MOB	63	250	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3100MODR11MAMOB

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

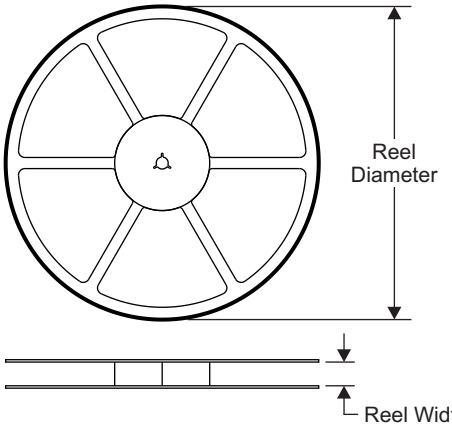
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

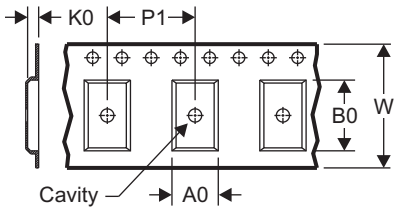
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

9.2.2 Tape and Reel Information

REEL DIMENSIONS

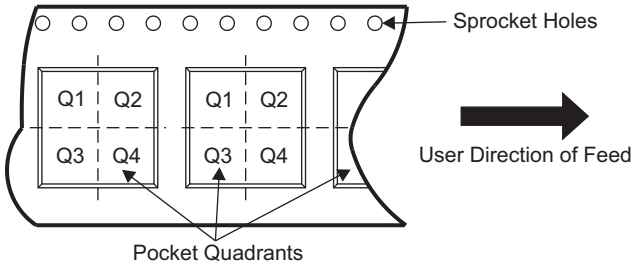


TAPE DIMENSIONS



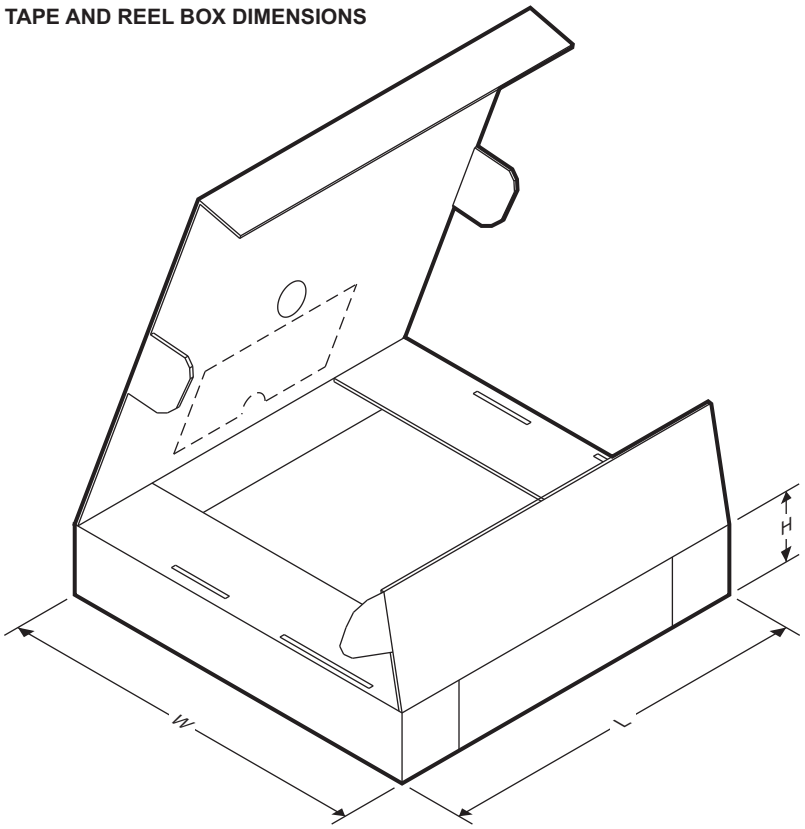
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3100MODR11MAMOBR	MOB	63	1000	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q3
CC3100MODR11MAMOBT	MOB	63	250	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3100MODR11MAMOBR	MOB	63	1000	354.0	354.0	55.0
CC3100MODR11MAMOBT	MOB	63	250	354.0	354.0	55.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC3100MODR11MAMOBR	ACTIVE	QFM	MOB	63	1000	Green (RoHS & no Sb/Br)	ENIG	Level-3-250C-168 HR	-20 to 70	CC3100MODR1M2AMOB Z64-CC31000MODR1 2015DJ3068(M) 3.3V, 400MA 451L-CC3100MODR1 MO-VVSS 001-A08147	Samples
CC3100MODR11MAMOBT	ACTIVE	QFM	MOB	63	250	Green (RoHS & no Sb/Br)	ENIG	Level-3-250C-168 HR	-20 to 70	CC3100MODR1M2AMOB Z64-CC31000MODR1 2015DJ3068(M) 3.3V, 400MA 451L-CC3100MODR1 MO-VVSS 001-A08147	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

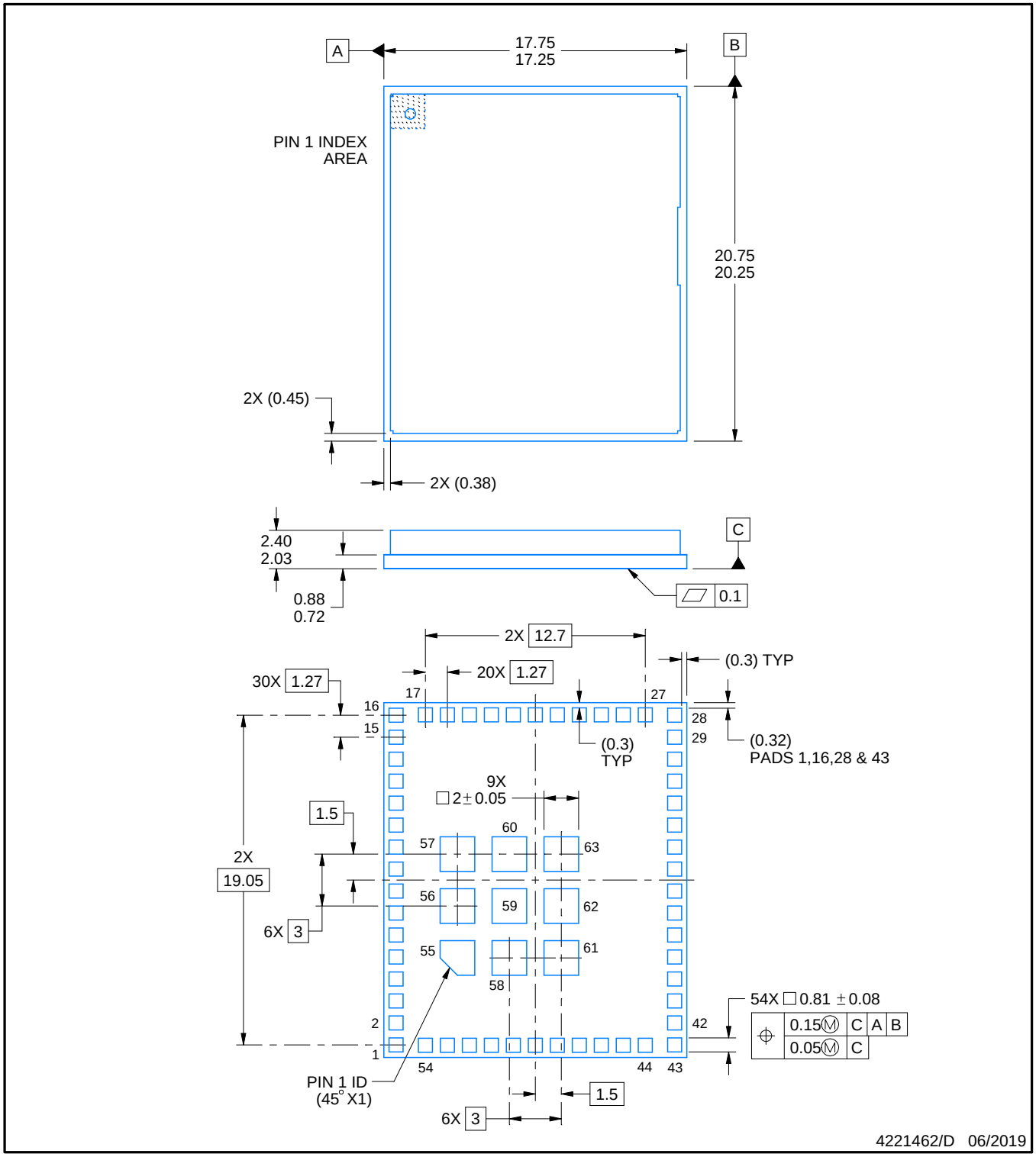
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

MOB0063A

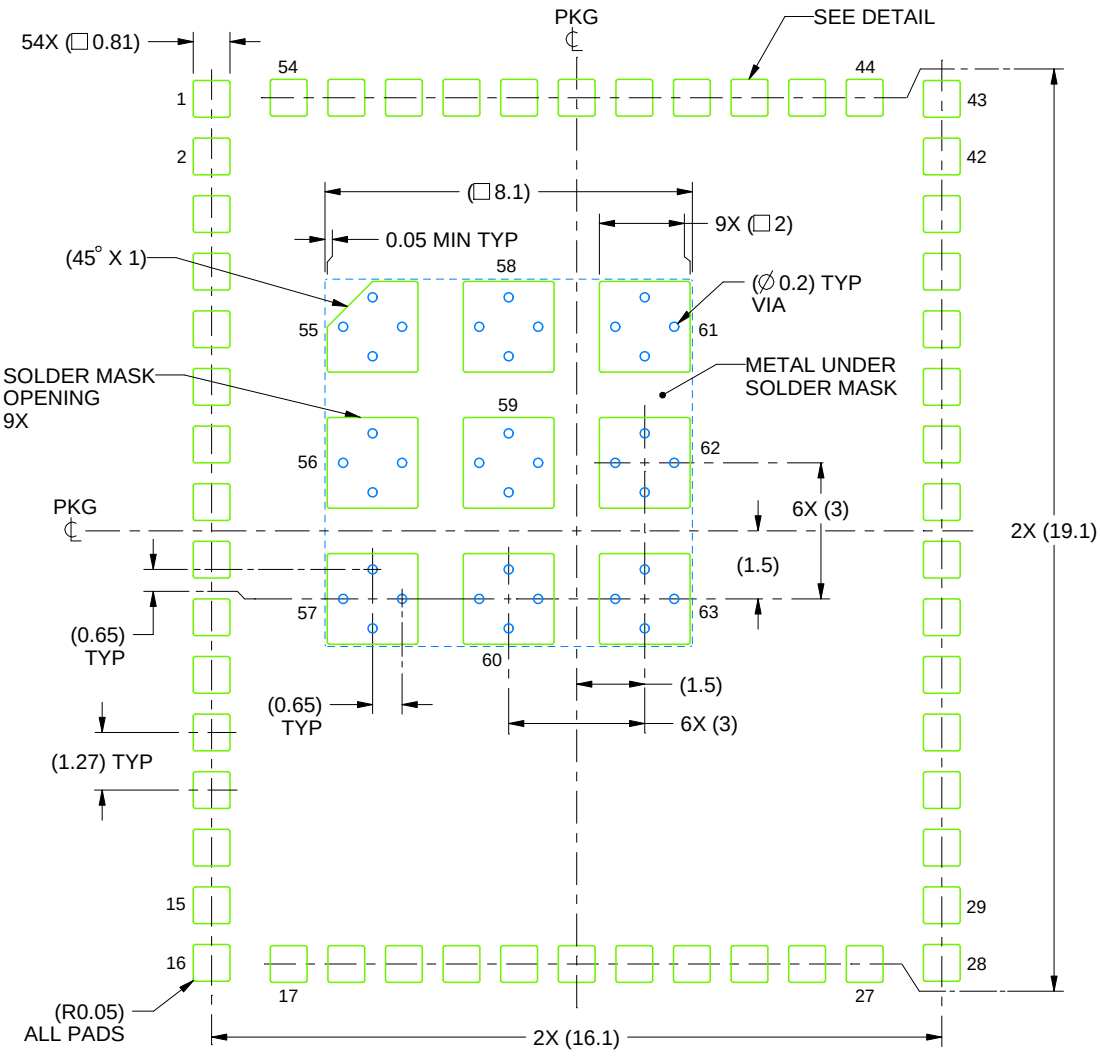
QFM - 2.4 mm max height

QUAD FLAT MODULE

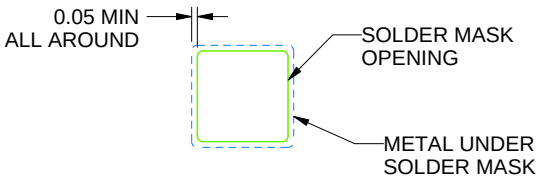


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:6X

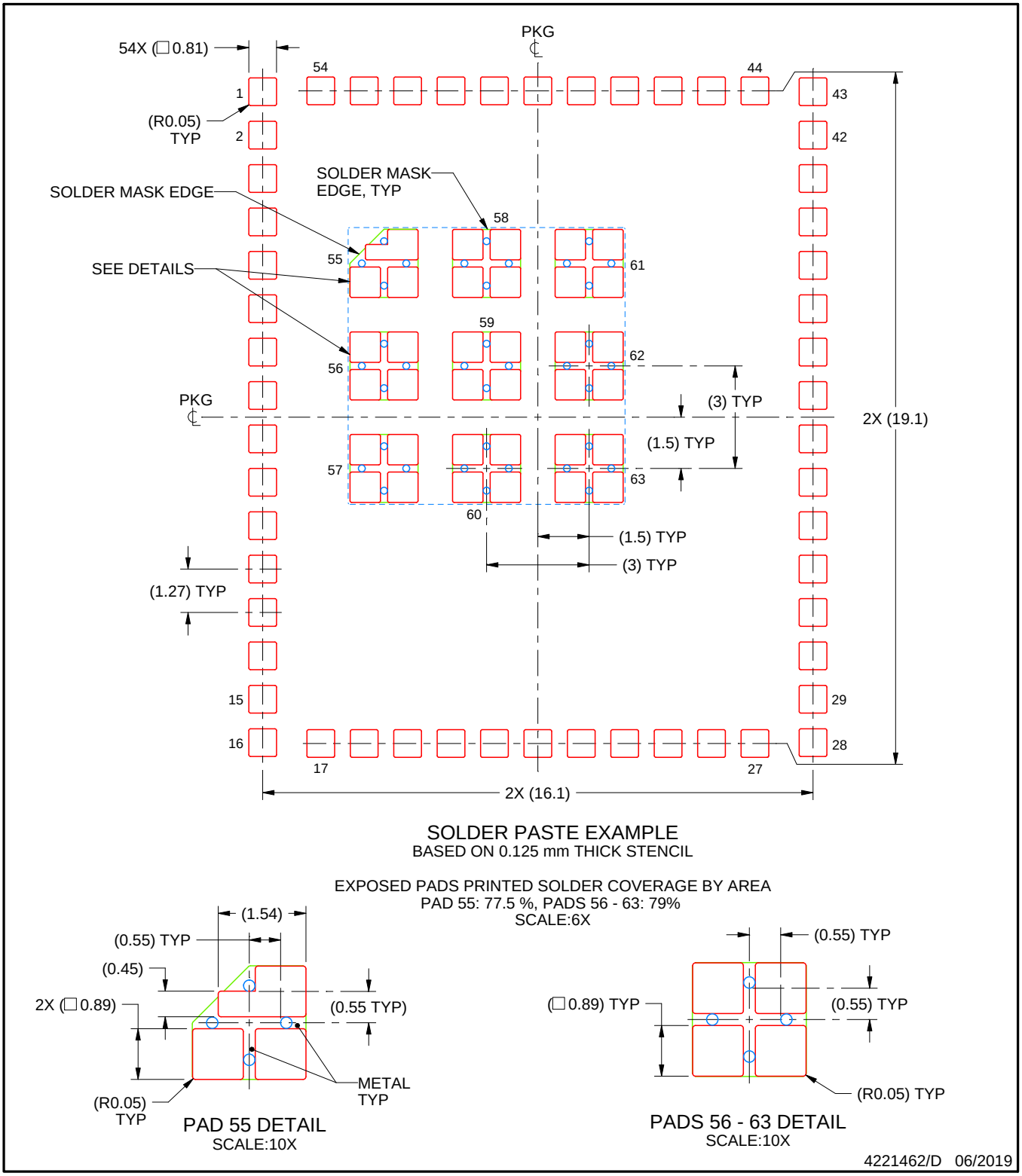


SIGNAL PADS DETAIL

4221462/D 06/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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