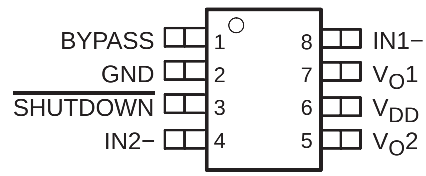
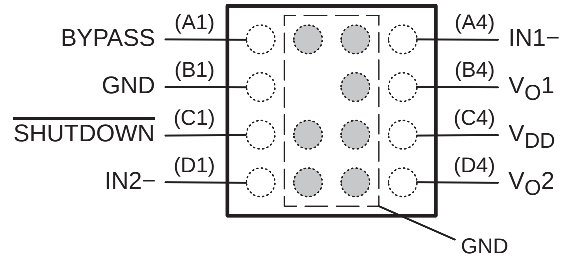
- **Minimal External Components Required**
- **1.6-V to 3.6-V Supply Voltage Range**
- **50-mW Stereo Output**
- **Low Supply Current . . . 0.75 mA**
- **Low Shutdown Current . . . 50 nA**
- **Gain Set Internally to 2 dB**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **3-mm × 5-mm MSOP Package (DGN)**
  - **5-mm × 6-mm SOIC Package (D)**
  - **2,5-mm × 2,5-mm MicroStar Junior™ BGA Package (ZQY)**

D or DGK PACKAGE (TOP VIEW)



ZQY PACKAGE (TOP VIEW)



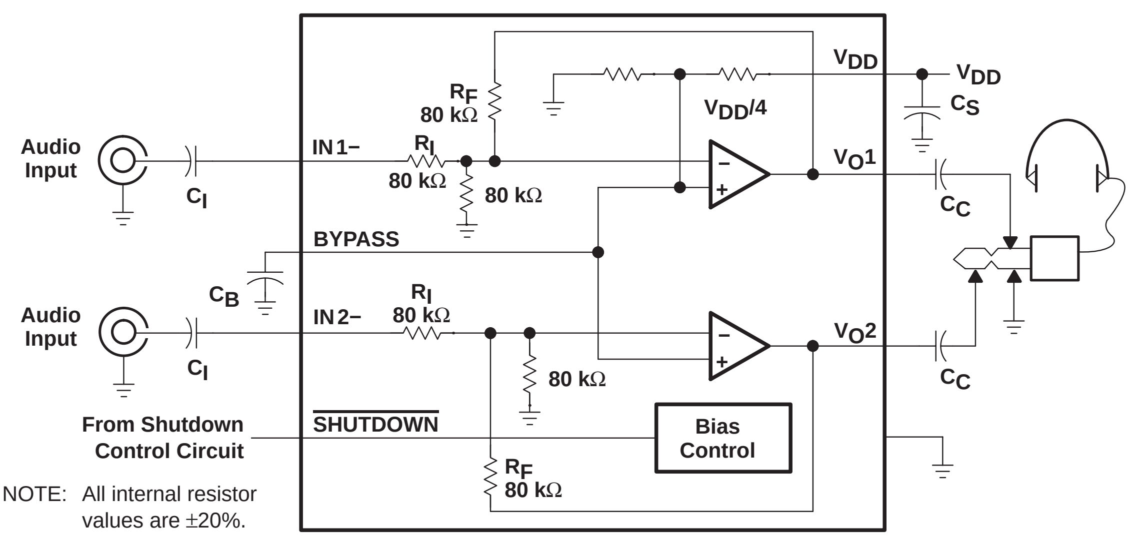
description

The TPA6101A2 is a stereo audio power amplifier packaged in an 8-pin SOIC package, an 8-pin MSOP package, or a 15-ball BGA package, capable of delivering 50 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is internally set to 2 dB (inverting) to save board space by eliminating six external resistors.

The TPA6101A2 is optimized for battery applications because of its low supply current, shutdown current, and THD+N. To obtain the low-supply-voltage range, the TPA6101A2 biases BYPASS to $V_{DD}/4$.

When driving a 16-Ω load with 40-mW output power from 3.3 V, THD+N is 0.08% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 30 mW into 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 0.3% across the audio band of 20 Hz to 20 kHz.

typical application circuit



NOTE: All internal resistor values are ±20%.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar BGA is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE			MSOP SYMBOLIZATION	BGA SYMBOLIZATION
	SMALL OUTLINE (D)	MSOP (DGK)	BGA (ZQY)		
−40°C to 85°C	TPA6101A2D	TPA6101A2DGK	TPA6101A2ZQYR	AJM	AAQI

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D, DGK	ZQY		
BYPASS	1	A1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at V_{DD}/4. Connect to a 0.1-µF to 1-µF low-ESR capacitor for best performance.
GND	2	B1	–	GND is the ground connection.
IN1−	8	A4	I	IN1− is the inverting input for channel 1.
IN2−	4	D1	I	IN2− is the inverting input for channel 2.
$\overline{\text{SHUTDOWN}}$	3	C1	I	Active-low input. When held low, the device is placed in a low-supply-current mode.
V_{DD}	6	C4	–	V_{DD} is the supply voltage terminal.
V_O1	7	B4	O	V_O1 is the audio output for channel 1.
V_O2	5	D4	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 4 V
Input voltage, V_I . . . . −0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . Internally Limited
Operating junction temperature range, T_J . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	710 mW	5.68 mW/°C	454 mW	369 mW
DGK	469 mW	3.75 mW/°C	300 mW	244 mW
ZQY	2 W	17.1 mW/°C	1.28 W	1.04 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.6	3.6	V
High-level input voltage, V_{IH} ($\overline{\text{SHUTDOWN}}$)		0.6 V_{DD}		V
Low-level input voltage, V_{IL} ($\overline{\text{SHUTDOWN}}$)			0.25 V_{DD}	V
Operating free-air temperature, T_A		–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_V = 2 dB		5	40	mV
PSRR	Power supply rejection ratio	V_{DD} = 3 V to 3.6 V		72		dB
I_{DD}	Supply current	$\overline{\text{SHUTDOWN}}$ = 3.6 V		0.75	1.5	mA
$I_{DD(SD)}$	Supply current in $\overline{\text{SHUTDOWN}}$ mode	$\overline{\text{SHUTDOWN}}$ = 0 V		50	250	nA
$\lvert I_{IH}\rvert$	High-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 3.6 V, $V_I = V_{DD}$			1	µA
$\lvert I_{IL}\rvert$	Low-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 3.6 V, V_I = 0 V			1	µA
Z_I	Input impedance			80		kΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Gain			2		dB
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		50		mW
THD+N	Total harmonic distortion + noise	P_O = 45 mW, 20 Hz−20 kHz		0.4%		
B_{OM}	Maximum output power BW	THD < 0.5%		> 20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz		47		dB
SNR	Signal-to-noise ratio	P_O = 50 mW		86		dB
V_n	Noise output voltage (no-noise weighting filter)			45		µV(rms)

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Gain			2		dB
P_O	Output power (each channel)	THD ≤ 0.1%, f = 1 kHz		35		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20 Hz−20 kHz		0.4%		
B_{OM}	Maximum output power BW	THD < 0.4%		>20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz		47		dB
SNR	Signal-to-noise ratio	P_O = 30 mW		86		dB
V_n	Noise output voltage (no-noise weighting filter)			50		µV(rms)

dc electrical characteristics at T_A = 25°C, V_{DD} = 1.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_V = 2 dB		5	40	mV
PSRR	Power supply rejection ratio	V_{DD} = 1.4 V to 1.8 V		80		dB
I_{DD}	Supply current	$\overline{\text{SHUTDOWN}}$ = 1.6 V		0.65	1.2	mA
$I_{DD(SD)}$	Supply current in $\overline{\text{SHUTDOWN}}$ mode	$\overline{\text{SHUTDOWN}}$ = 0 V		50	250	nA
$\lvert I_{IH} \rvert$	High-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 1.6 V, $V_I = V_{DD}$			1	µA
$\lvert I_{IL} \rvert$	Low-level input current ($\overline{\text{SHUTDOWN}}$)	V_{DD} = 1.6 V, V_I = 0 V			1	µA
Z_I	Input impedance			80		kΩ

ac operating characteristics, V_{DD} = 1.6 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Gain			2		dB
P_O	Output power (each channel)	THD ≤ 0.5%, f = 1 kHz		10		mW
THD+N	Total harmonic distortion + noise	P_O = 9.5 mW, 20 Hz−20 kHz		0.06%		
B_{OM}	Maximum output power BW	THD < 1%		> 20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz		47		dB
SNR	Signal-to-noise ratio	P_O = 10 mW		82		dB
V_n	Noise output voltage (no-noise weighting filter)			32		µV(rms)

ac operating characteristics, V_{DD} = 1.6 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G	Gain			2		dB
P_O	Output power (each channel)	THD ≤ 0.5%, f = 1 kHz		7.5		mW
THD+N	Total harmonic distortion + noise	P_O = 6.5 mW, 20 Hz−20 kHz		0.05%		
B_{OM}	Maximum output power BW	THD < 1%		>20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz		47		dB
SNR	Signal-to-noise ratio	P_O = 7.5 mW		84		dB
V_n	Noise output voltage (no-noise weighting filter)			32		µV(rms)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 3, 5, 7, 9, 11
		vs Output power	2, 4, 6, 8, 10, 12
		vs Output voltage	13, 14
P_O	Output power	vs Load resistance	15, 16
k_{SVR}	Supply ripple rejection ratio	vs Frequency	17, 18
Vn	Output noise voltage	vs Frequency	19, 20
	Crosstalk	vs Frequency	21, 22
	Closed−loop gain and phase	vs Frequency	23, 24, 25, 26
I_{DD}	Supply current	vs Supply voltage	27
P_D	Power dissipation	vs Output power	28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

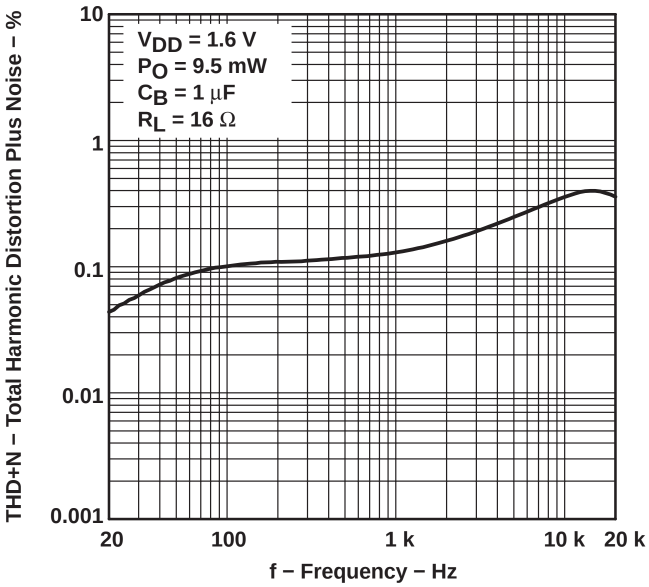


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

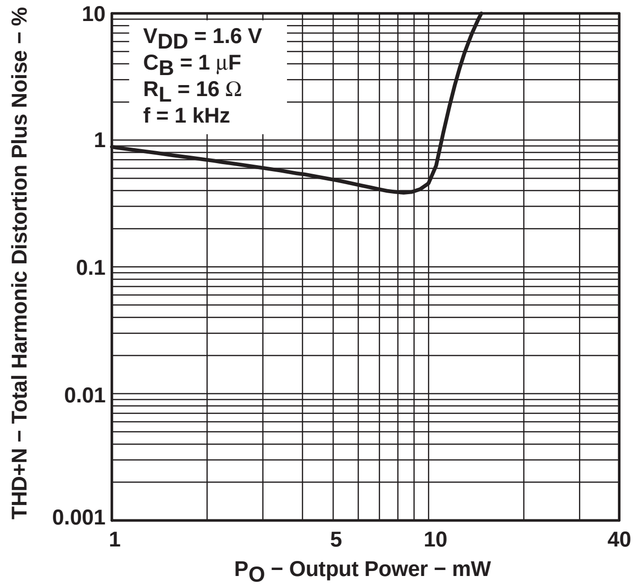


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

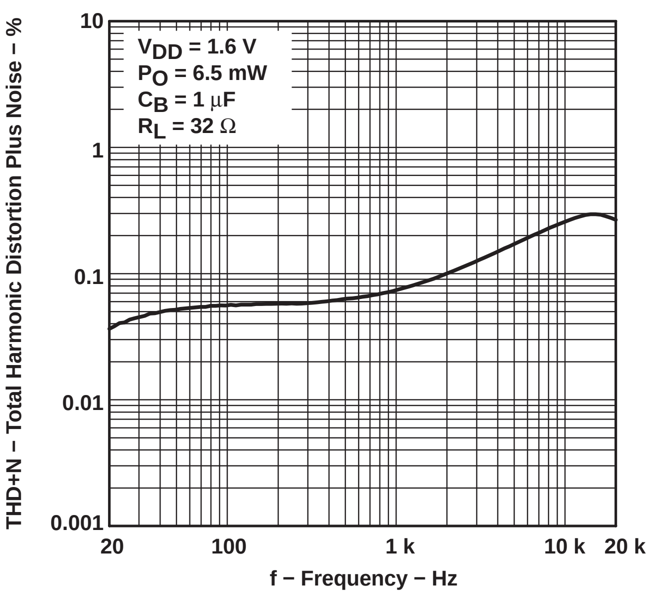


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

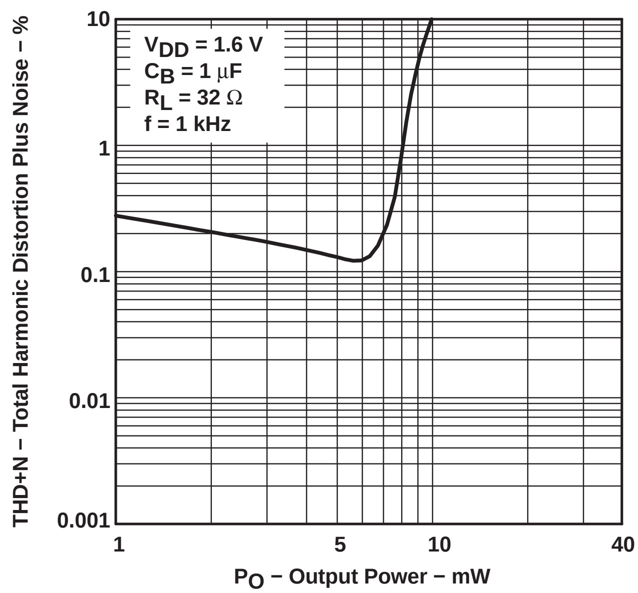


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

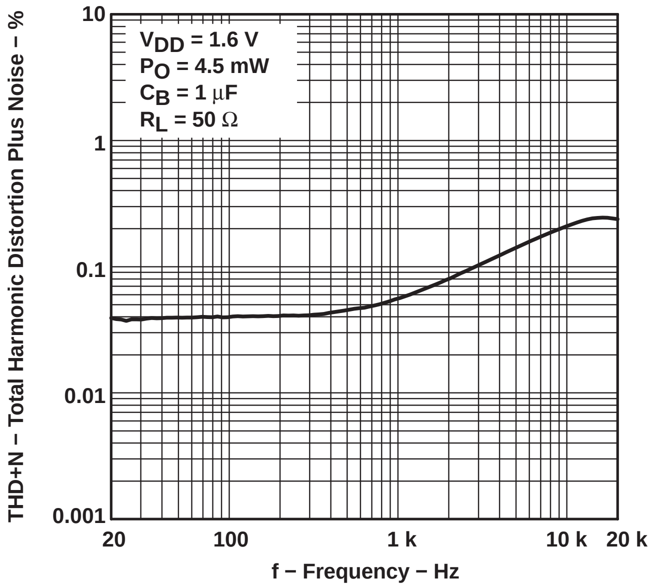


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

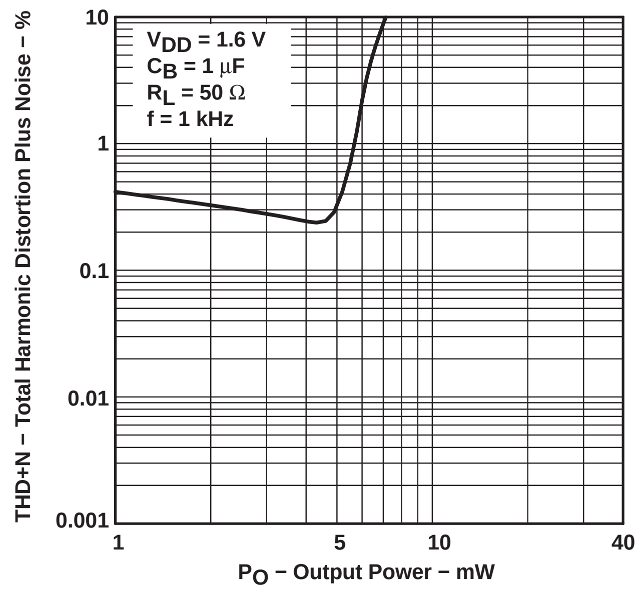


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

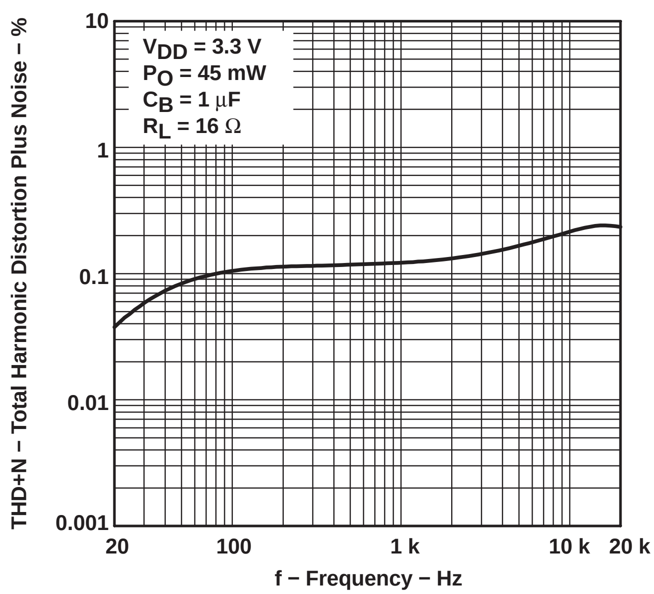


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

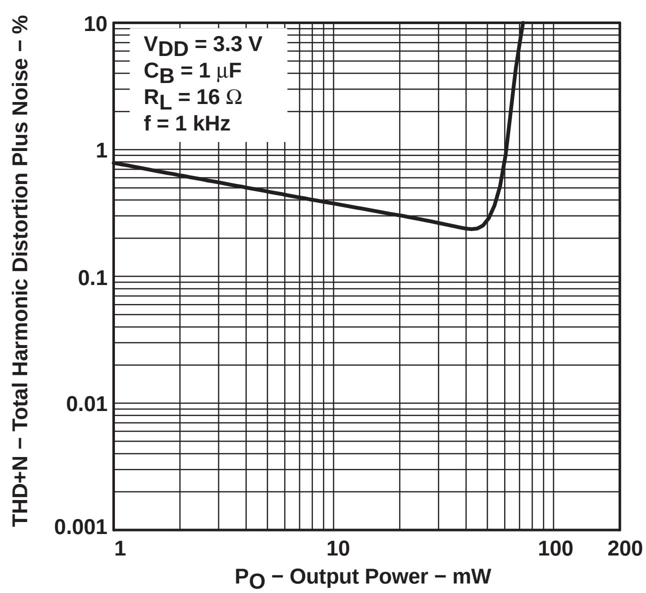


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

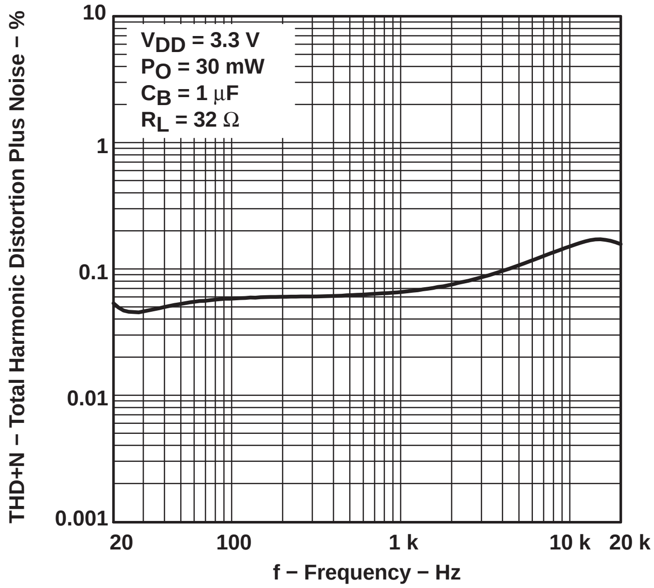


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

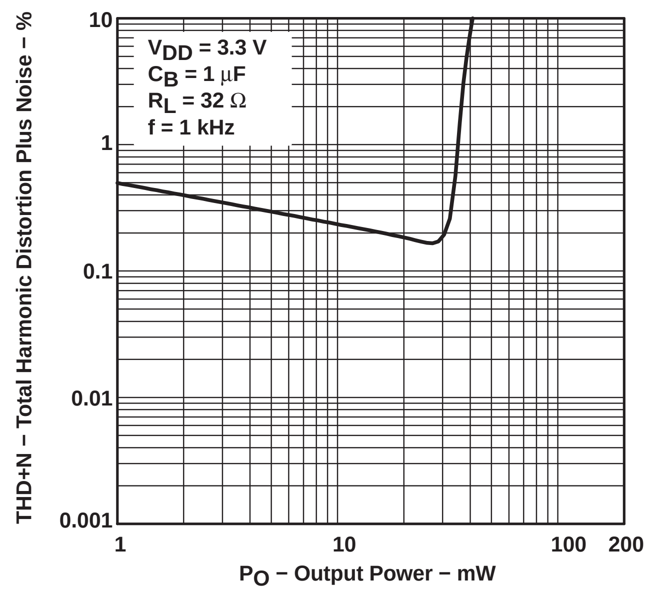


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

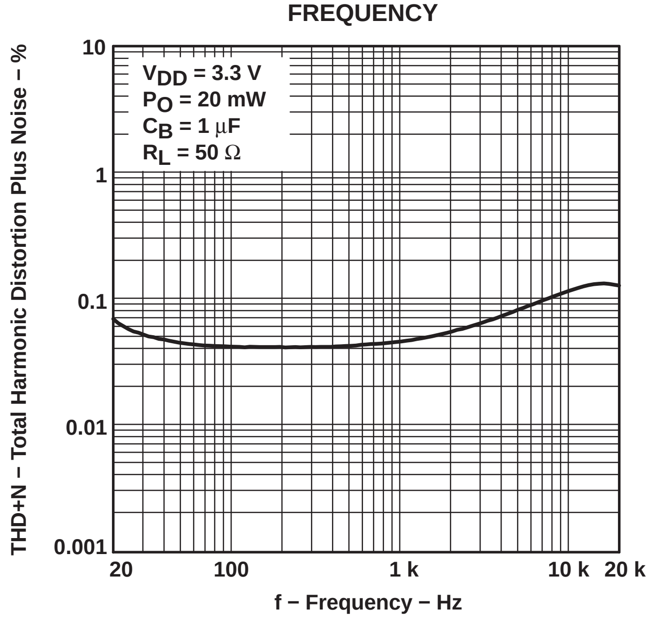


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

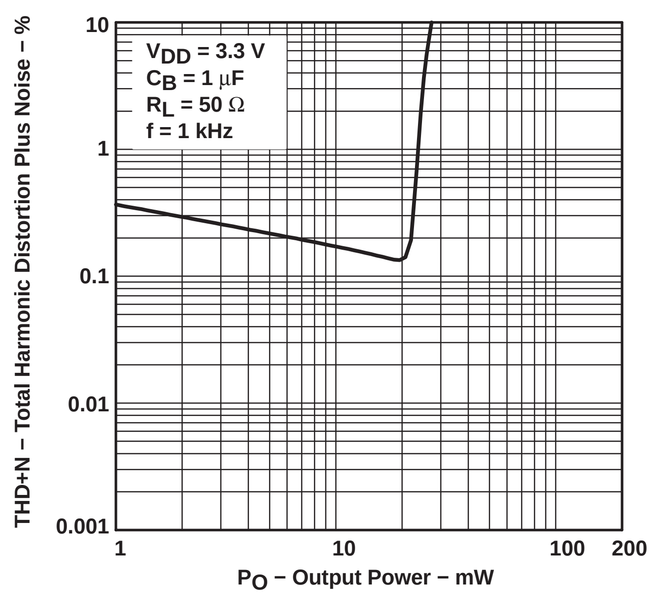


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

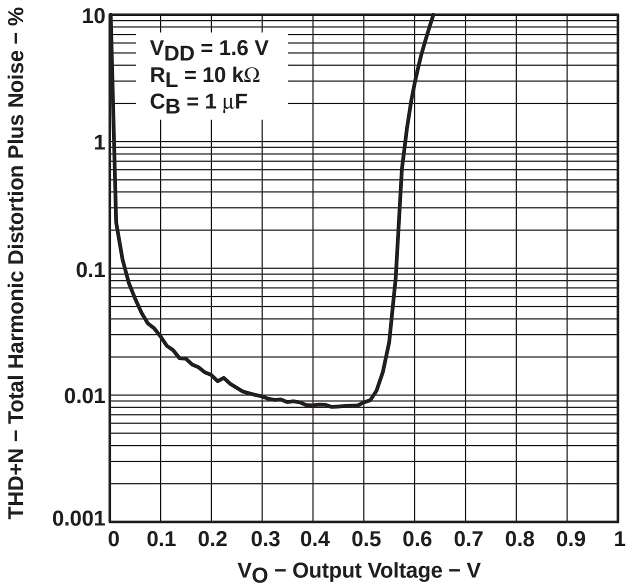


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

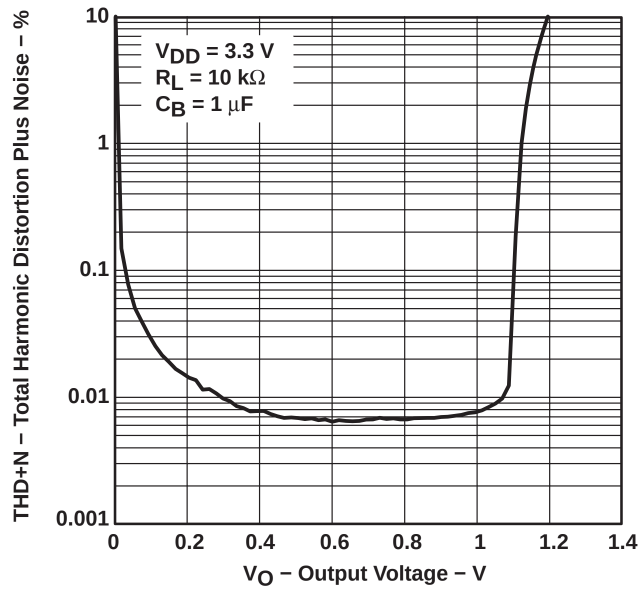


Figure 14

OUTPUT POWER
vs
LOAD RESISTANCE

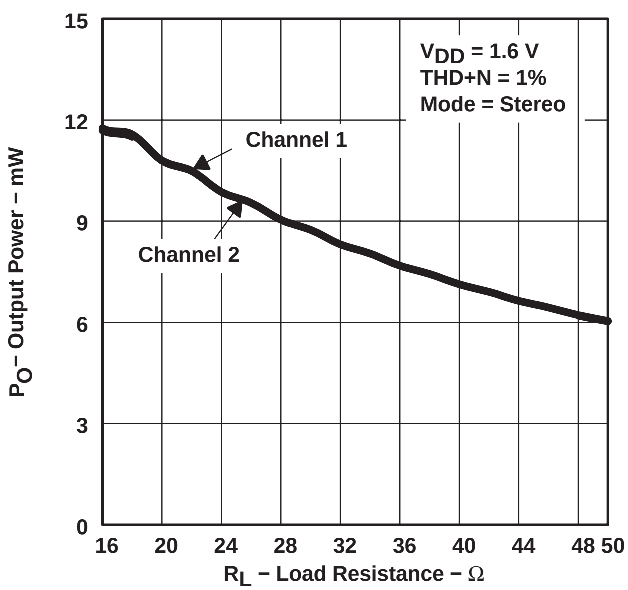


Figure 15

OUTPUT POWER
vs
LOAD RESISTANCE

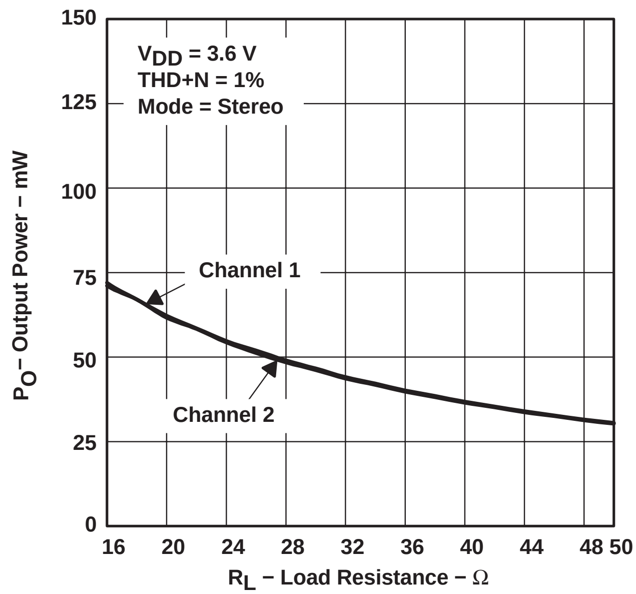


Figure 16

TYPICAL CHARACTERISTICS

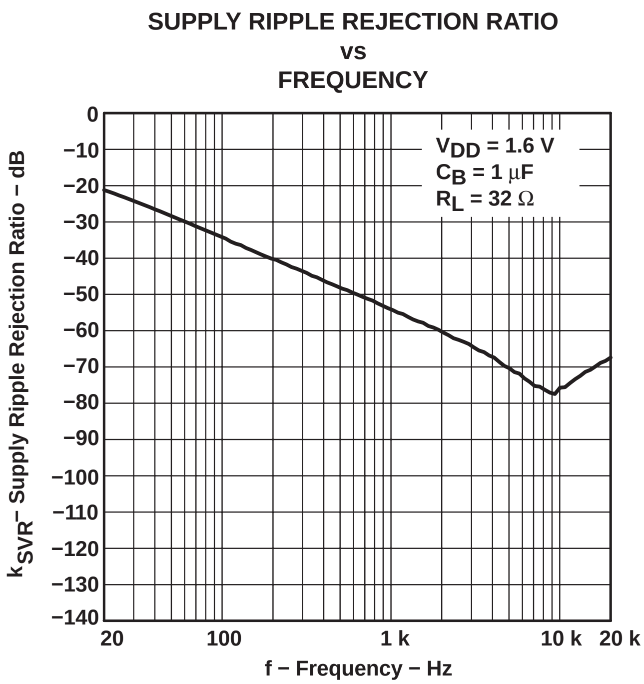


Figure 17

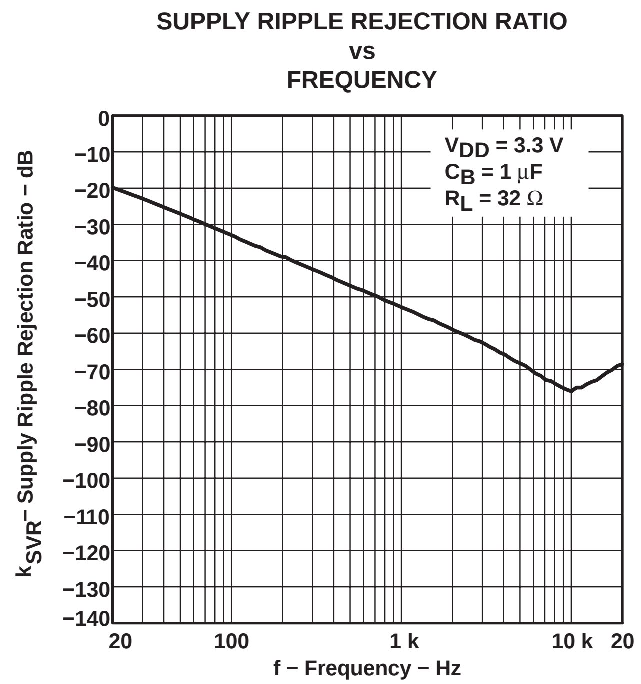


Figure 18

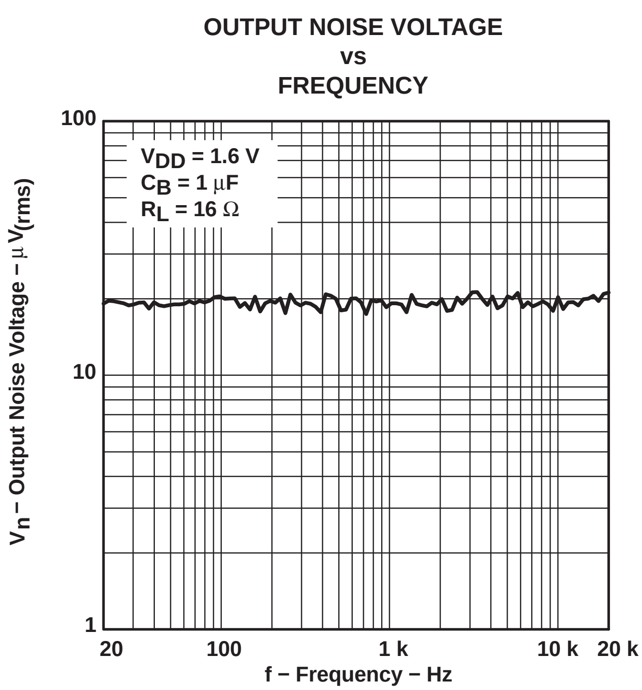


Figure 19

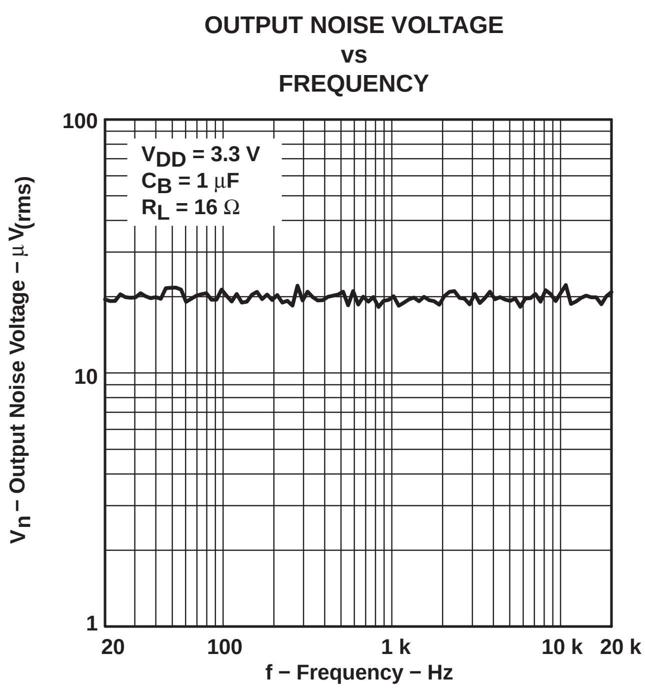


Figure 20

TYPICAL CHARACTERISTICS

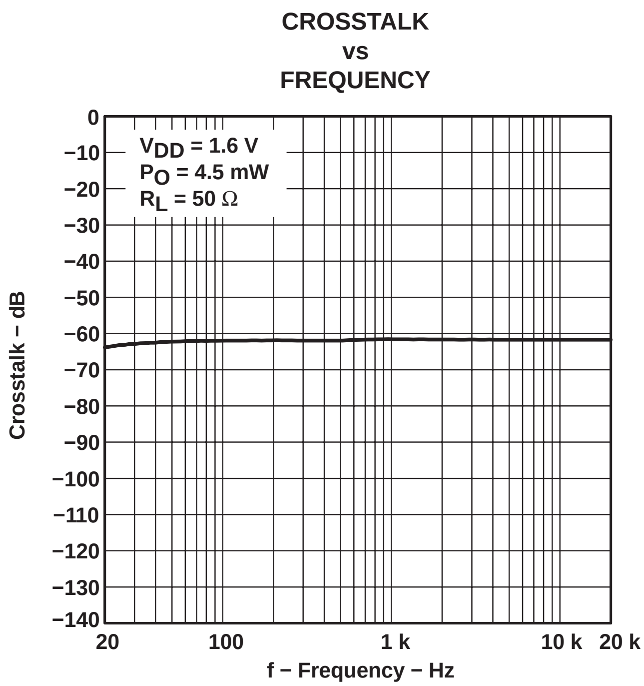


Figure 21

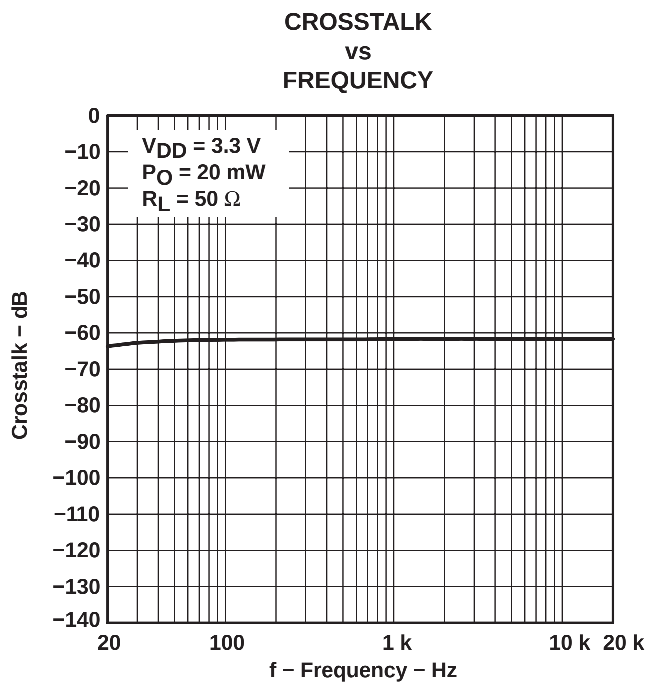


Figure 22

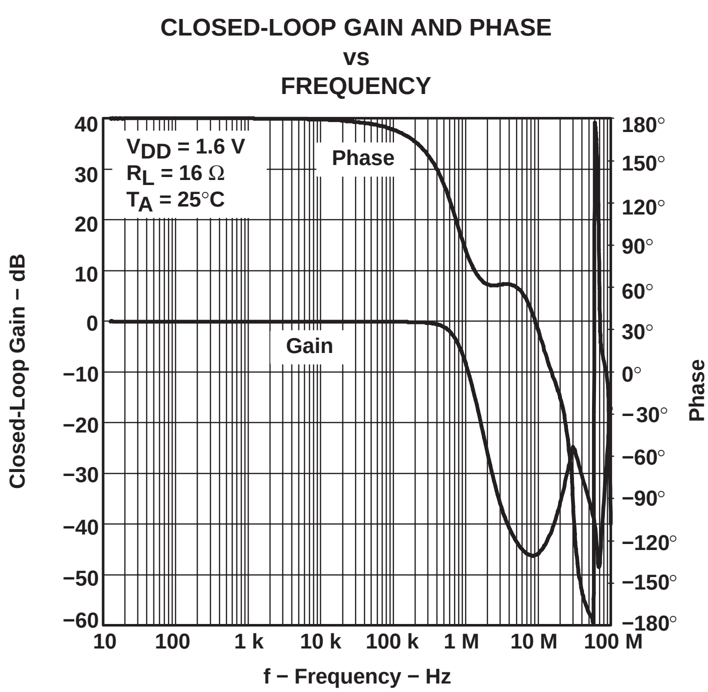


Figure 23

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

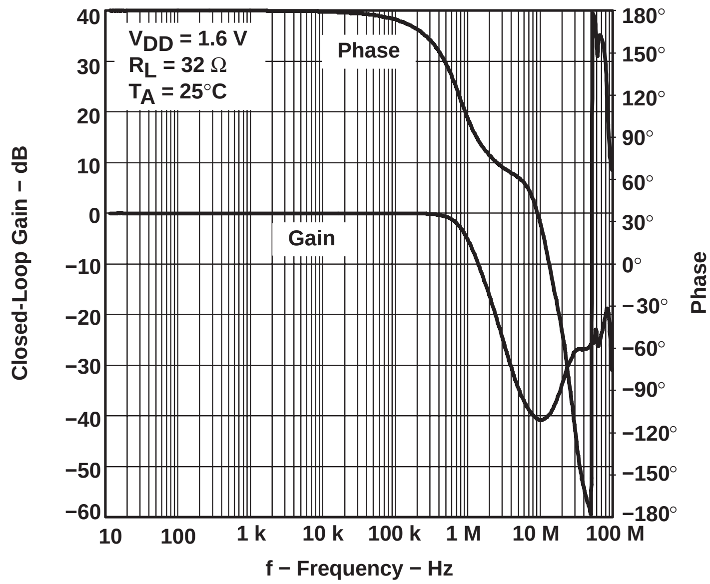


Figure 24

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

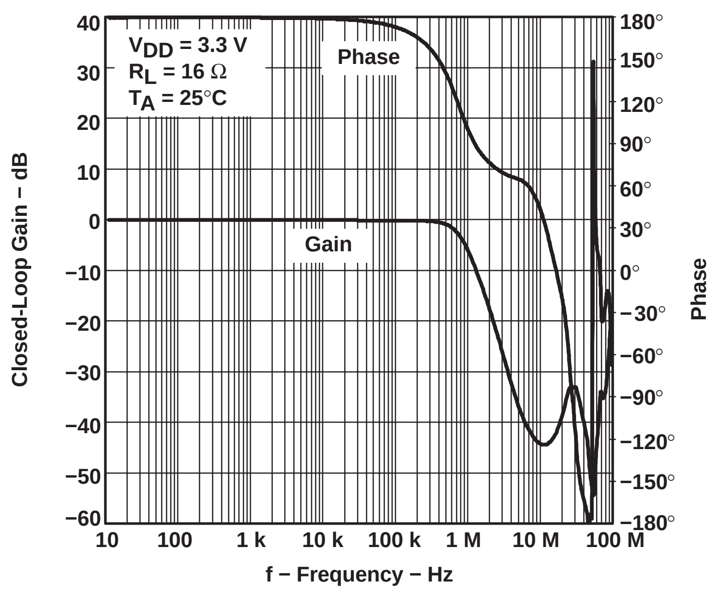


Figure 25

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

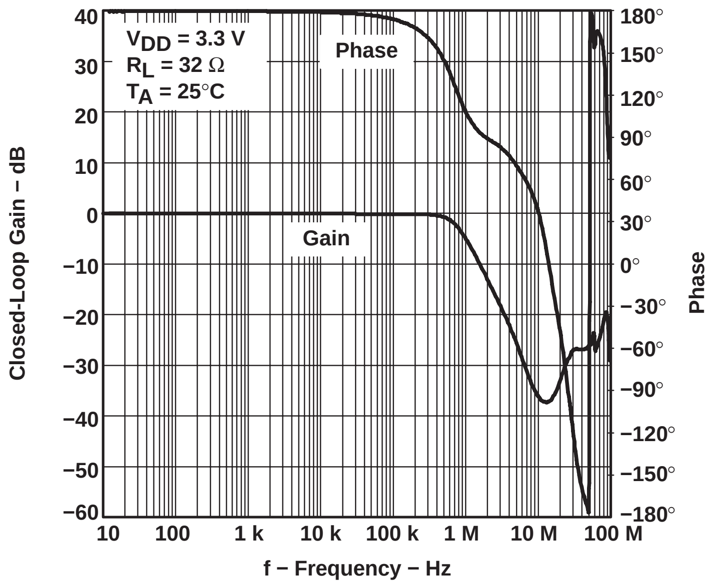


Figure 26

SUPPLY CURRENT vs SUPPLY VOLTAGE

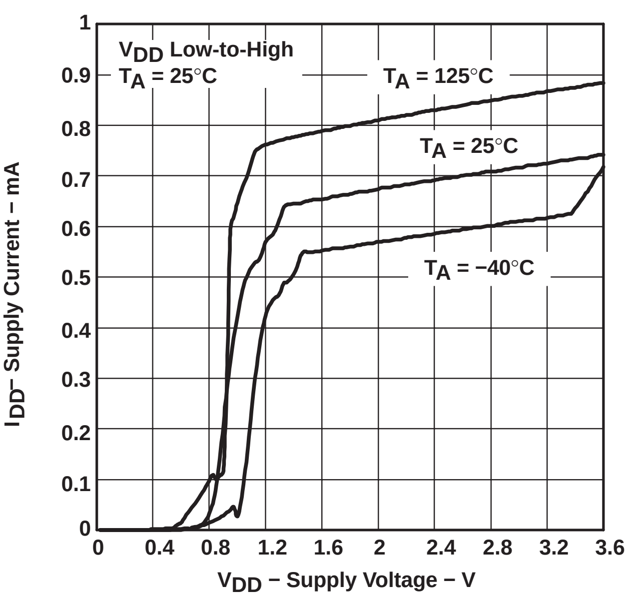


Figure 27

POWER DISSIPATION vs OUTPUT POWER

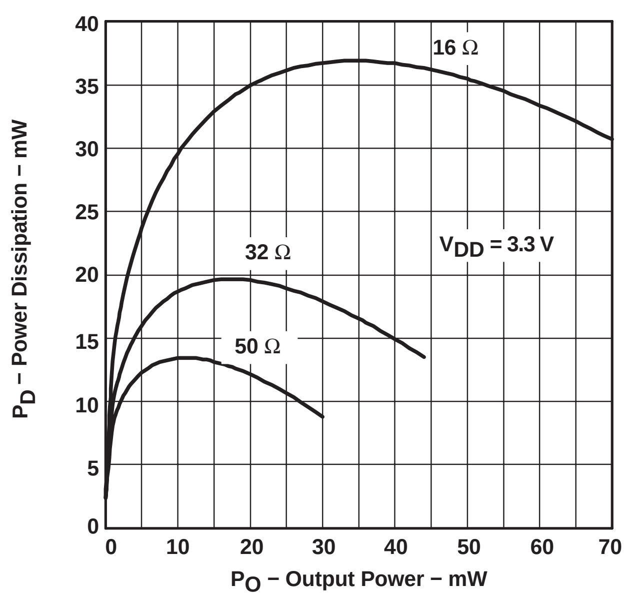


Figure 28

APPLICATION INFORMATION

input capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 1. R_I is set internally and is fixed at 80 kΩ.

$$f_c = \frac{1}{2\pi R_I C_I} \tag{1}$$

The value of C_I is important to consider, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 20 Hz. Equation 1 is reconfigured as equation 2.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{2}$$

In this example, C_I is approximately 0.1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc-offset voltage at the input to the amplifier that reduces useful headroom. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/4$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA6101A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger, aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor (C_B) serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Euation 3 should be maintained.

$$\frac{1}{\left(C_B \times 55\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \tag{3}$$

As an example, consider a circuit where C_B is 1 µF, C_I is 0.1 µF, and R_I is 80 kΩ. Inserting these values into Euation 3 results in: 18.18 ≤ 125 which satisfies the rule. Bypass capacitor (C_B) values of 0.47 µF to 1 µF and ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply, single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load from a high-pass filter is governed by Equation 4.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{4}$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low-frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low-Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line-level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 55\ k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{5}$$

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

3.3-V versus 1.6-V operation

The TPA6101A2 was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 0.75 mA (typical) to 0.65 mA (typical). The most important consideration is that of output power. Each amplifier can produce a maxium output voltage swing within a few hundred millivolts of the rails with a 10-kΩ load. However, this voltage swing decreases as the load resistance decreases, and the $r_{DS(on)}$ of the output stage transistors becomes more significant. For example, for a 32-Ω load, the maximum peak output voltage with V_{DD} = 1.6 V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6101A2D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6101A2	Samples
TPA6101A2DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJM	Samples
TPA6101A2ZQYR	ACTIVE	BGA MICROSTAR JUNIOR	ZQY	15	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AAQI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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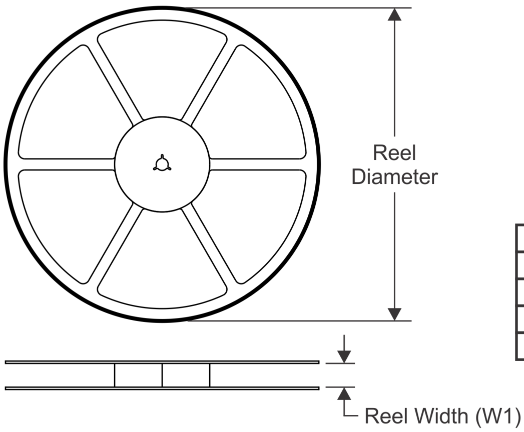
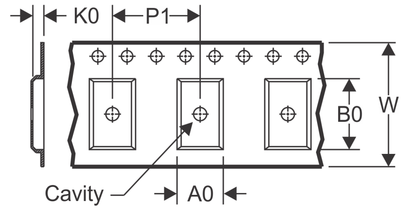
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

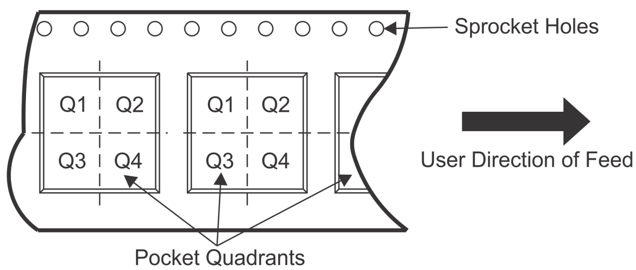


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

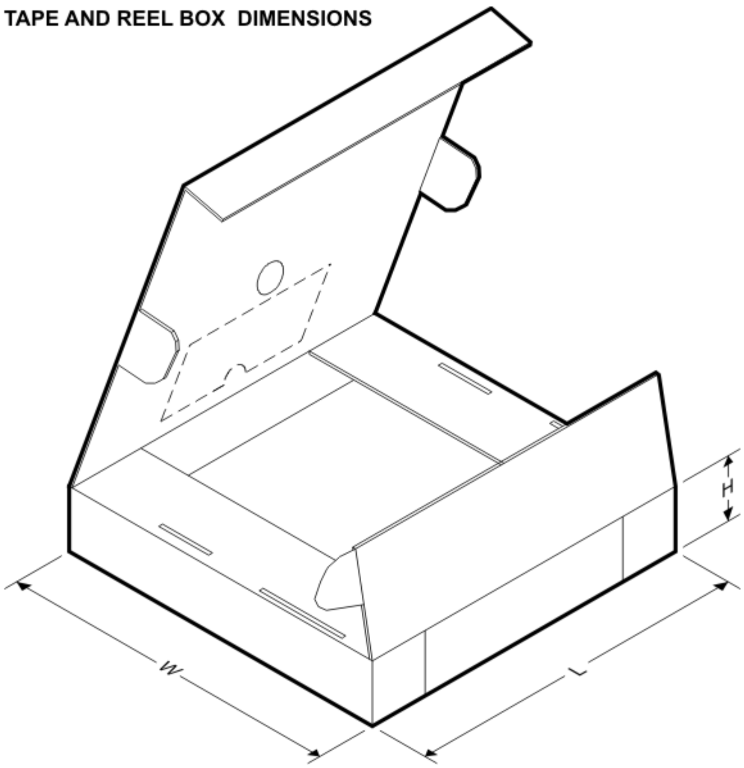
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6101A2DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6101A2ZQYR	BGA MICROSTAR JUNIOR	ZQY	15	2500	330.0	8.4	2.8	2.8	1.25	4.0	8.0	Q1

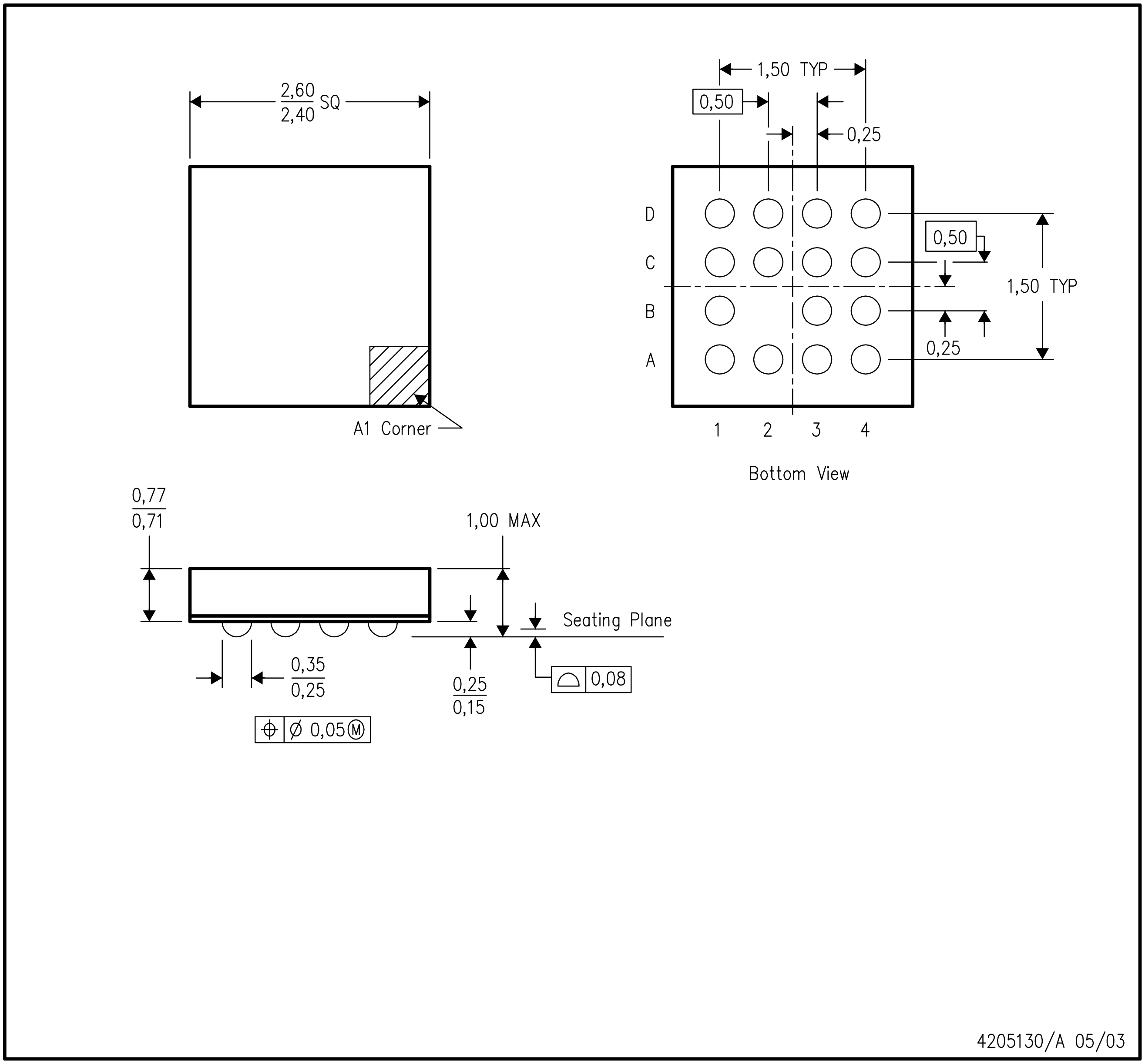
TAPE AND REEL BOX DIMENSIONS



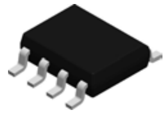
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6101A2DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPA6101A2ZQYR	BGA MICROSTAR JUNIOR	ZQY	15	2500	350.0	350.0	43.0

ZQY (S–PBGA–N15) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior configuration
- D. Falls within JEDEC MO–225
- E. This package is lead–free.

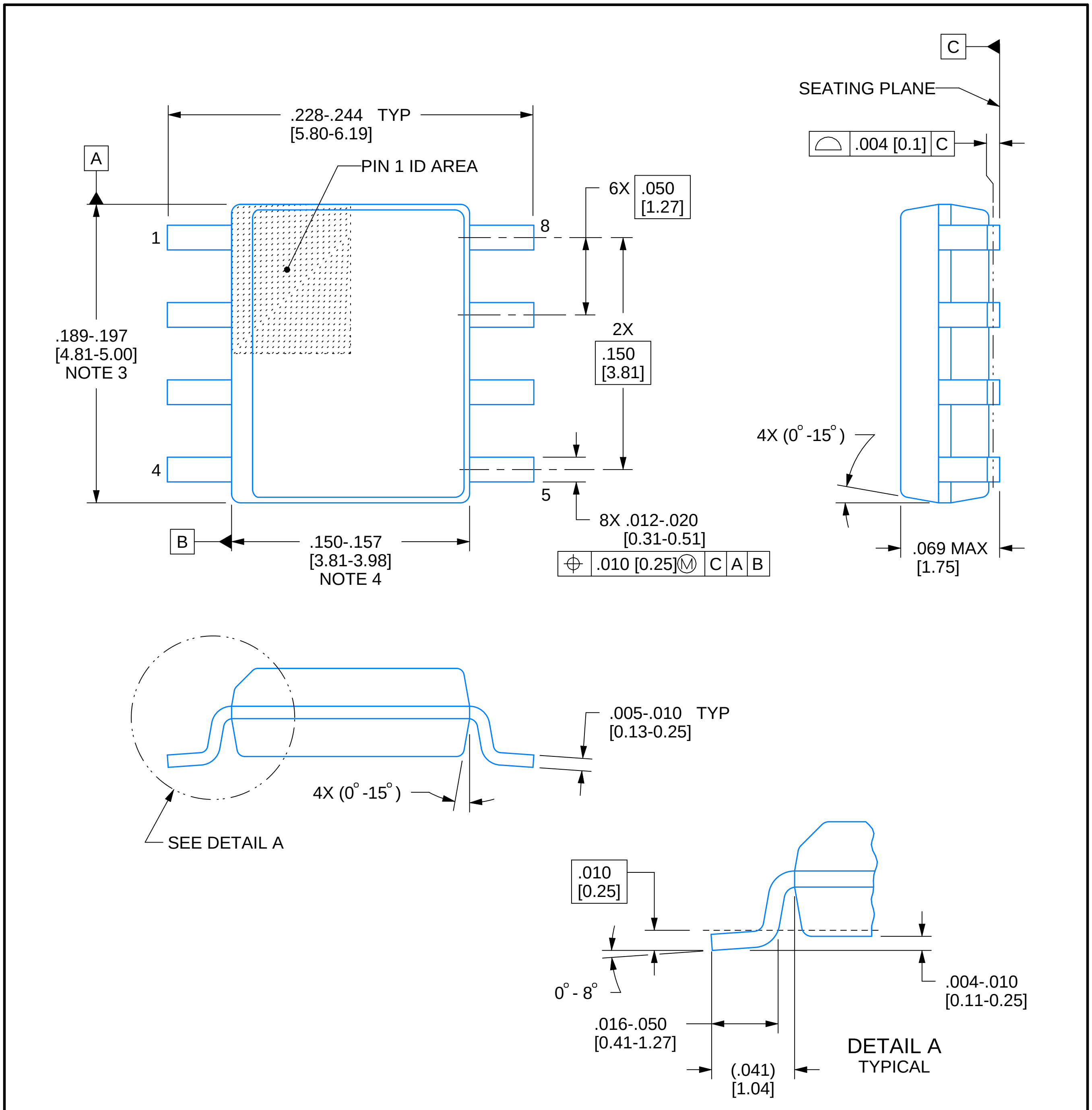


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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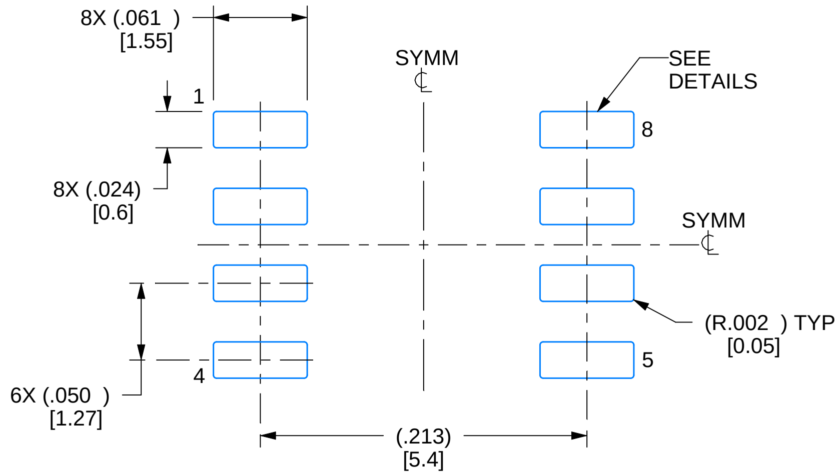
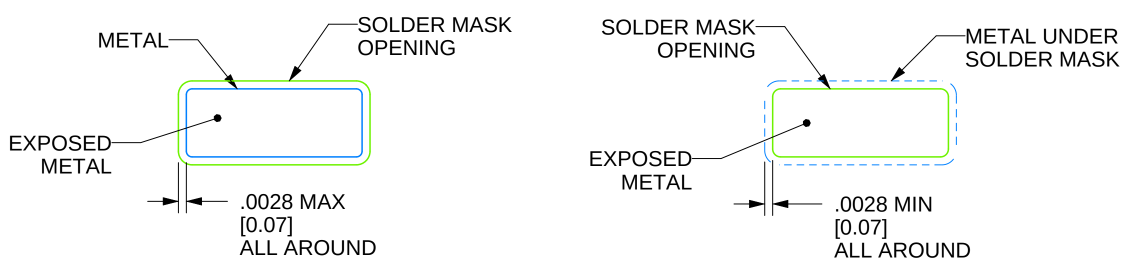
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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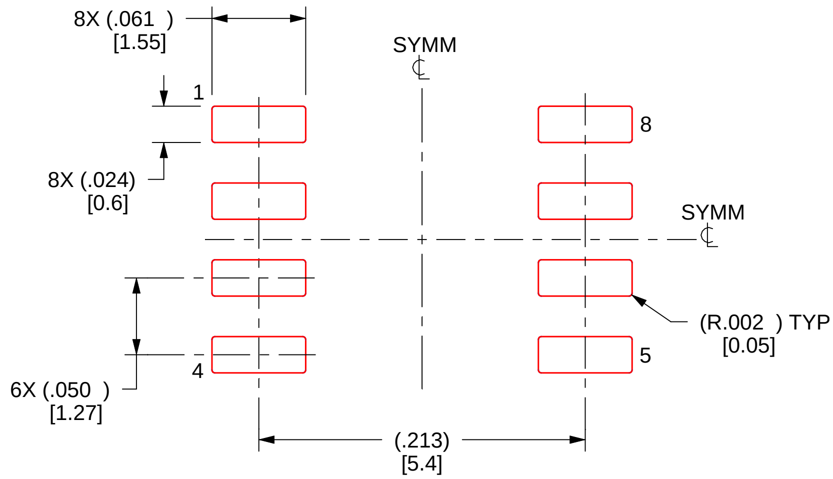
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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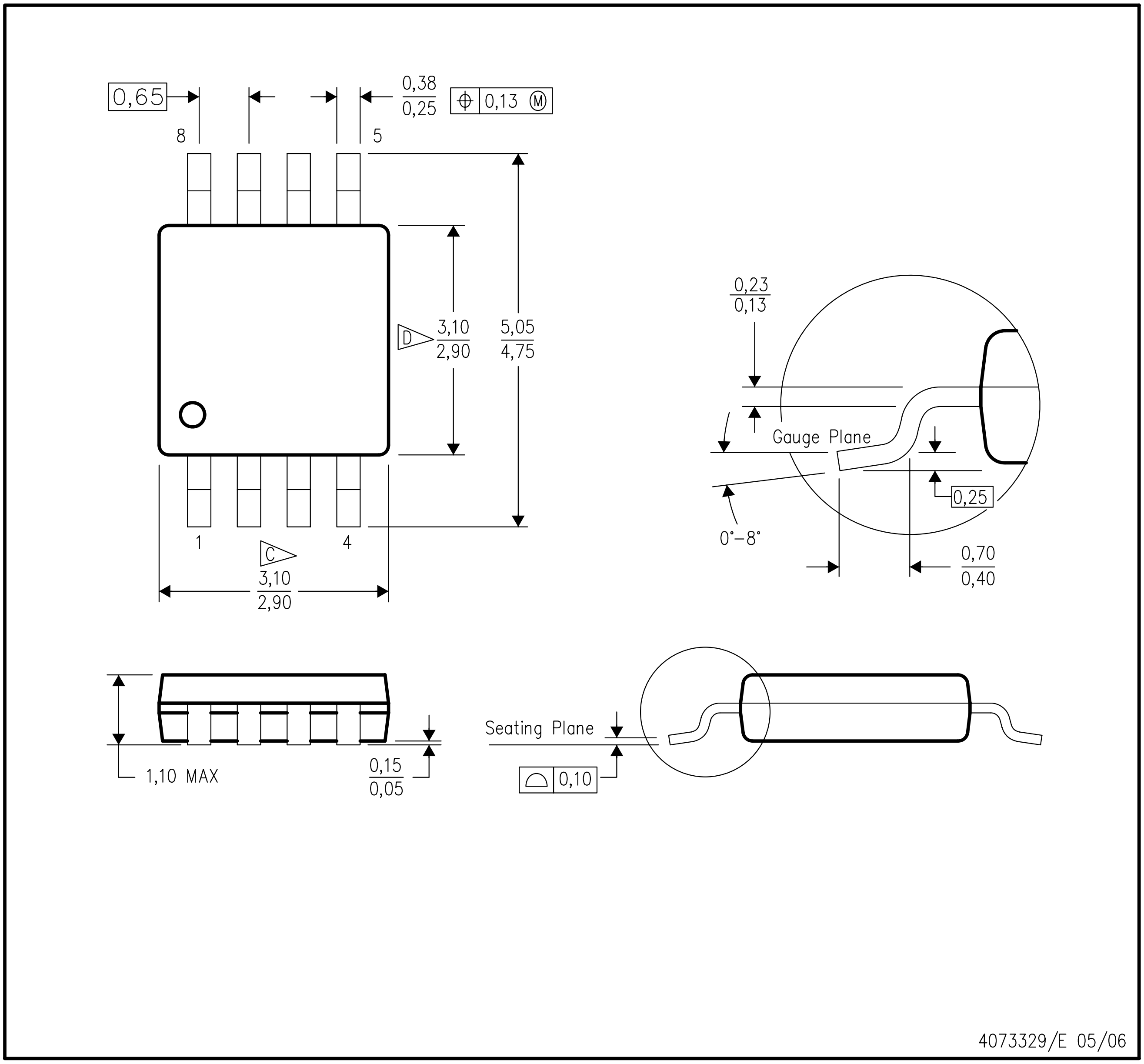
NOTES: (continued)

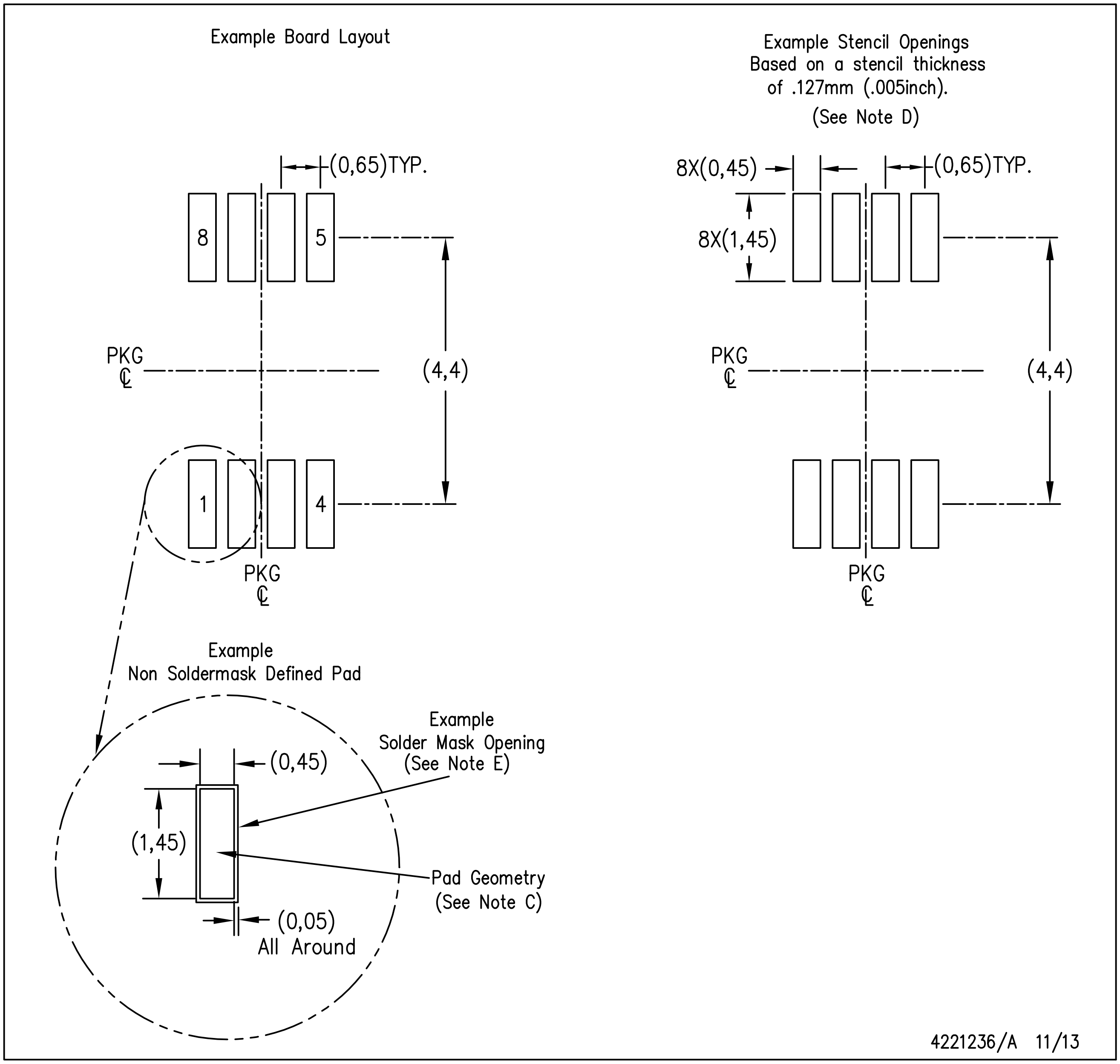
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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