16-A, 12-V INPUT NONISOLATED WIDE-OUTPUT ADJUST SIP MODULE

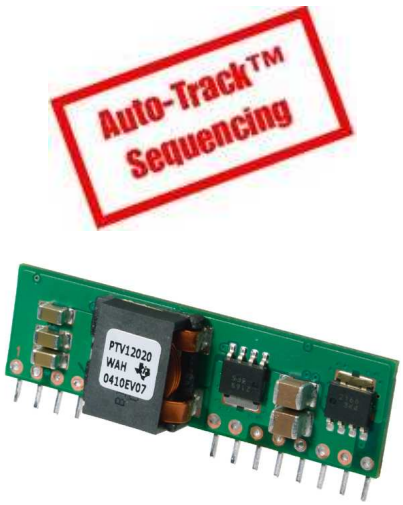
Check for Samples: PTV12020W/L

FEATURES

- **Up to 16-A Output Current**
- **12-V Input Voltage**
- **Wide-Output Voltage Adjust (1.2 V to 5.5 V)/(0.8 V to 1.8 V)**
- **Efficiencies up to 93%**
- **On/Off Inhibit**
- **Output Voltage Sense**
- **Prebias Start Up**
- **Undervoltage Lockout**
- **Auto-Track™ Sequencing**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Overtemperature Protection**
- **Operating Temperature: –40°C to 85°C**
- **Safety Agency Approvals: UL/IEC/CSA-22.2 60950-1**
- **POLA™ Alliance Compatible**

APPLICATIONS

- **Multivoltage Digital Systems**
- **High-End Computing**
- **Networking**



DESCRIPTION

The PTV12020 series of nonisolated power modules are part of a new class of complete dc/dc switching regulator modules from Texas Instruments. These regulators combine high performance with double-sided, surface mount construction to give designers the flexibility to power the most complex multiprocessor digital systems using off-the-shelf catalog parts.

The PTV12020 series is produced in a 12-pin, single in-line pin (SIP) package. The SIP footprint minimizes board space, and offers an alternate package option for space conscious applications. Operating from a 12-V input bus, the series provides step-down conversion to a wide range of output voltages, at up to 16 A of output current. The output voltage of the W-suffix parts can be set to any value over the range of 1.2 V to 5.5 V. The L-suffix parts have an adjustment range of 0.8 V to 1.8 V. The output voltage is set using a single external resistor.

This series includes Auto-Track™. Auto-Track™ simplifies the task of supply-voltage sequencing in a power system by enabling the output voltage of multiple modules to accurately track each other, or any external voltage, during power up and power down.

Other operating features include an on/off inhibit, and the ability to start up into an existing output voltage or prebias. For improved load regulation, an output voltage sense is provided. A nonlatching overcurrent trip and overtemperature shutdown protects against load faults.

Target applications include complex multivoltage, multiprocessor systems that incorporate the industry's high-speed DSPs, microprocessors, and bus drivers.

For start-up into a non-prebiased output, review page 13 in the *Application Information* section.

For start-up into a prebiased output, review page 17 in the *Application Information* section.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

POLA, Auto-Track, TMS320 are trademarks of Texas Instruments.

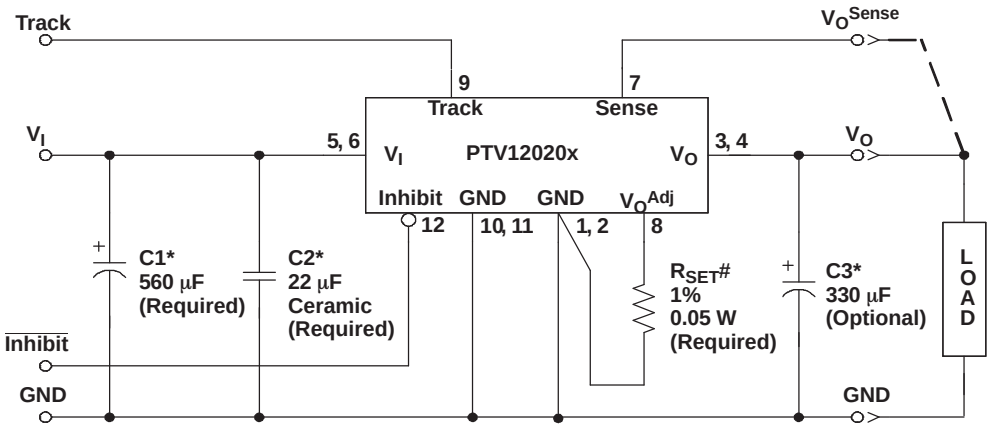
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2007, Texas Instruments Incorporated

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

STANDARD APPLICATION



* See the Application Information section for capacitor recommendations.
# R_{SET} is required to adjust the output voltage higher than its lowest value. See the Application Information section for values.

ORDERING INFORMATION

PTV12020 (Basic Model)			
Output Voltage	**Part Number**	**DESCRIPTION**	**Package(1)**
1.2 V – 5.5 V (Adjustable)	PTV12020WAH	Vertical T/H	EVC
0.8 V – 1.8 V (Adjustable)	PTV12020LAH	Vertical T/H	EVC

(1) See the applicable package drawing for dimensions and PC board layout.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
$V_{(Track)}$	Track input		–0.3 V to V_I +0.3 V
T_A	Operating temperature range	Over V_I range	–40°C to 85°C
	Lead temperature	5 seconds	260°C (2)
T_{stg}	Storage temperature		–55°C to 125°C
$V_{(Inhibit)}$	Inhibit (pin 12) input voltage		–0.3 V to 7 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This product is not compatible with surface-mount reflow solder processes.

PACKAGE SPECIFICATIONS

PTV12020x (Suffix AH)			
Weight			5.5 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted		500 Gs (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 Hz - 2000 Hz		10 Gs (1)

(1) Qualification limit.

Copyright © 2004–2007, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 12 V, V_O = 3.3 V, C1 = 560 µF, C2 = 22 µF, C3 = 0 µF, and $I_O = I_{O(max)}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTV12020W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Natural convection airflow		0		16 (1)	A
V_I	Input voltage range	Over I_O load range		10.8		13.2	V
V_O	Set-point voltage tolerance					±2% (2)	
	Temperature variation	–40°C < T_A < 85°C			±0.5%		
	Line regulation	Over V_I range			±5		mV
	Load regulation	Over I_O range			±10		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3 (2)	%V_o
	Adjust range	Over V_I range		1.2		5.5	V
η	Efficiency	$I_O = I_O$ max	R_{SET} = 280 Ω, V_O = 5 V		93%		
			R_{SET} = 2.0 kΩ, V_O = 3.3 V		91%		
			R_{SET} = 4.32 kΩ, V_O = 2.5 V		89%		
			R_{SET} = 11.5 kΩ, V_O = 1.8 V		86%		
			R_{SET} = 24.3 kΩ, V_O = 1.5 V		84%		
			R_{SET} = open cct., V_O = 1.2 V		81%		
	Output voltage ripple (pk-pk)	20-MHz bandwidth	V_O ≤ 2.5 V		1		%V_O
			V_O > 2.5 V		1.5		
I_O (trip)	Overcurrent threshold	Reset, followed by auto-recovery			30		A
	Transient response	1-A/µs load step, 50 to 100% I_O max, C3 = 330 µF					
			Recovery time		70		µs
			V_o over/undershoot		100		mV
	Track control (pin 9)	I_{IL} Input low current	Pin to GND			–0.13	mA
		Control slew-rate limit	C3 ≤ C3 (max)			1	V/ms
UVLO	Undervoltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
	Inhibit control (pin 12)	V_{IH} Input high voltage	Referenced to GND			Open (3)	V
		V_{IL} Input low voltage		–0.2		0.6	
		I_{IL} Input low current	Pin to GND		–0.24		mA
I_I (stby)	Input standby current	Inhibit (pin 12) to GND, Track (pin 9) open			10		mA
f_S	Switching frequency	Over V_I and I_O ranges		250	325	400	kHz
	External input capacitance		Nonceramic (C1)	560 (4)			µF
			Ceramic (C2)	22 (4)			
	External output capacitance (C3)	Capacitance value	Nonceramic	0	330 (5)	6,600 (6)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4 (7)			mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		4.9			10^6 Hrs

(1) See thermal derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C or better temperature stability.
(3) This control pin is pulled up to an internal supply voltage. To avoid risk of damage to the module, *do not* apply an external voltage greater than 7 V. If this input is left open-circuit, the module operates when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note, *Input and Output Capacitor Selection*, SLTA055.
(4) A 22-µF high-frequency ceramic capacitor and 560-µF electrolytic input capacitor are required for proper operation. The electrolytic capacitor must be rated for the minimum ripple current rating. Consult the Application Information for further guidance on input capacitor selection.
(5) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load improves the transient response.
(6) This is the calculated maximum. The minimum ESR limitation often results in a lower value. Consult the Application Information for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

Copyright © 2004–2007, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 12 V, V_O = 1.8 V, C1 = 560 µF, C2 = 22 µF, C3 = 0 µF, and $I_O = I_{O(max)}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTV12020L			UNIT
				MIN	TYP	MAX	
I_O	Output current	Natural convection airflow		0		16 (1)	A
V_I	Input voltage range	Over I_O load range		10.8		13.2	V
V_O	Set-point voltage tolerance					±2% (2)	
	Temperature variation	–40°C <T_A < 85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±12		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C				±3 (2)	%V_o
	Adjust range	Over V_I range		0.8		1.8	V
η	Efficiency	$I_O = I_O$ max	R_{SET} = 130 Ω, V_O = 1.8 V		87%		
			R_{SET} = 3.57 kΩ, V_O = 1.5 V		85%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V		83%		
			R_{SET} = 32.4 kΩ, V_O = 1 V		80%		
			R_{SET} = open cct., V_O = 0.8 V		77%		
	Output voltage ripple (pk-pk)	20-MHz bandwidth			2		%V_O
I_O (trip)	Overcurrent threshold	Reset, followed by auto-recovery			30		A
	Transient response	1-A/µs load step, 50 to 100% I_O max, C3 = 330 µF					
			Recovery time		70		µs
			V_o over/undershoot		100		mV
	Track control (pin 9)	I_{IL} Input low current	Pin to GND			–0.13	mA
		Control slew-rate limit	C3 ≤ C3 (max)			1	V/ms
	Inhibit control (pin 12)	V_{IH} Input high voltage	Referenced to GND			Open (3)	V
		V_{IL} Input low voltage		–0.2		0.6	
		I_{IL} Input low current	Pin to GND		–0.24		mA
I_I (stby)	Input standby current	Inhibit (pin 12) to GND, Track (pin 9) open			10		mA
UVLO	Undervoltage lockout	V_I increasing			9.5	10.4	V
		V_I decreasing		8.8	9		
f_S	Switching frequency	Over V_I and I_O ranges		200	250	300	kHz
	External input capacitance		Nonceramic (C1)	560 (4)			µF
			Ceramic (C2)	22 (4)			
	External output capacitance (C3)	Capacitance value	Nonceramic	0	330 (5)	6,600 (6)	µF
			Ceramic	0		300	
		Equivalent series resistance (nonceramic)		4 (7)			mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		4.9			10^6 Hrs

(1) See thermal derating curves for safe operating area (SOA), or consult factory for appropriate derating.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C or better temperature stability.
(3) This control pin is pulled up to an internal supply voltage. To avoid risk of damage to the module, *do not* apply an external voltage greater than 7 V. If this input is left open-circuit, the module operates when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note, *Input and Output Capacitor Selection*, SLTA055.
(4) A 22-µF high-frequency ceramic capacitor and 560-µF electrolytic input capacitor are required for proper operation. The electrolytic capacitor must be rated for the minimum ripple current rating. Consult the Application Information for guidance on input capacitor selection.
(5) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load improves the transient response.
(6) This is the calculated maximum. The minimum ESR limitation often results in a lower value. Consult the Application Informaiton for further guidance.
(7) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.

Copyright © 2004–2007, Texas Instruments Incorporated

PTV12020W Characteristic Data; 1.2 V to 5.5 V

EFFICIENCY
VS
OUTPUT CURRENT

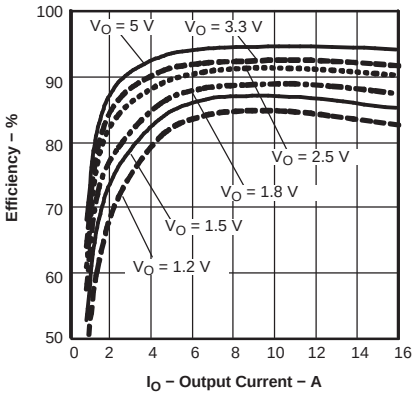


Figure 1.

OUTPUT VOLTAGE RIPPLE
VS
OUTPUT CURRENT

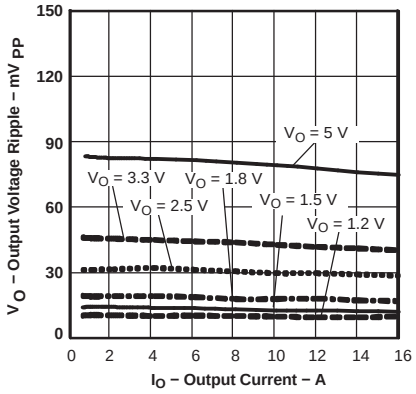


Figure 2.

POWER DISSIPATION
VS
OUTPUT CURRENT

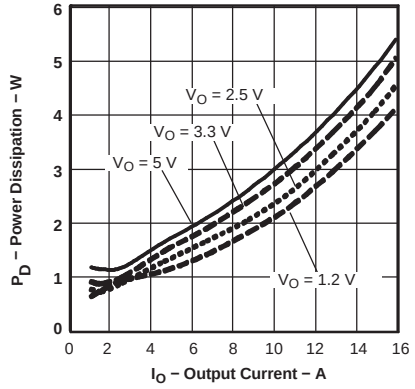


Figure 3.

TEMPERATURE DERATING
VS
OUTPUT CURRENT

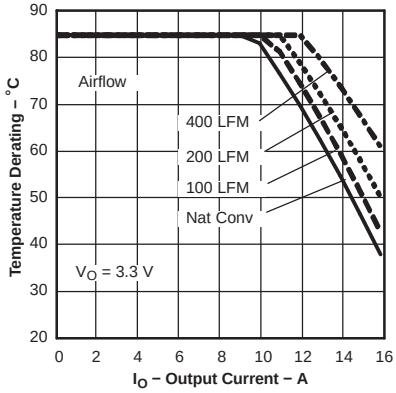


Figure 4.

TEMPERATURE DERATING
VS
OUTPUT CURRENT

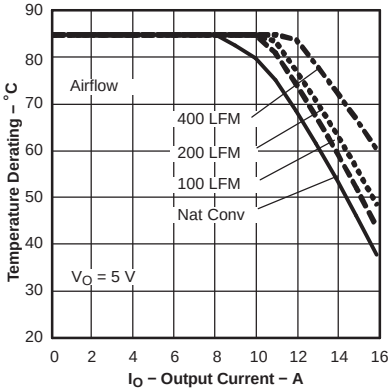


Figure 5.

Copyright © 2004–2007, Texas Instruments Incorporated

PTV12020L Characteristic Data; 0.8 V to 1.8 V

EFFICIENCY VS OUTPUT CURRENT

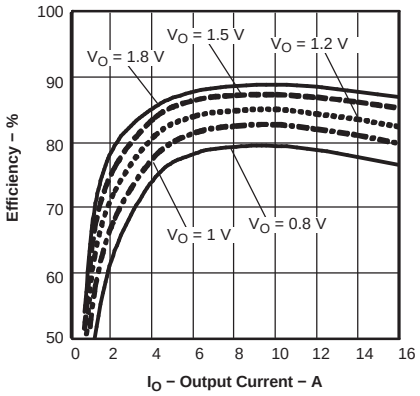


Figure 6.

OUTPUT VOLTAGE RIPPLE VS OUTPUT CURRENT

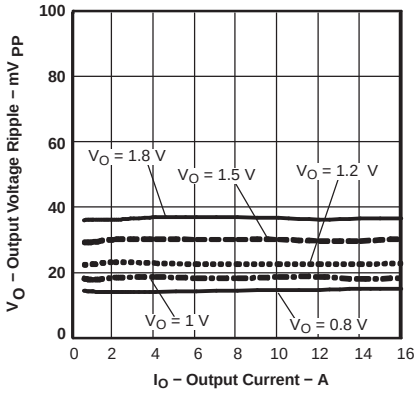


Figure 7.

POWER DISSIPATION VS OUTPUT CURRENT

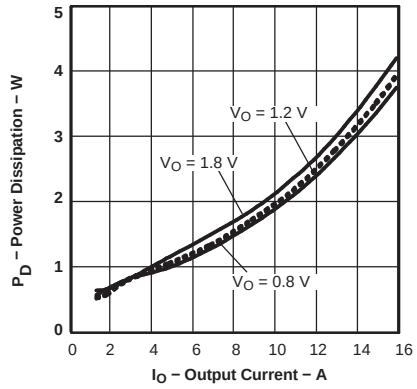


Figure 8.

TEMPERATURE DERATING VS OUTPUT CURRENT

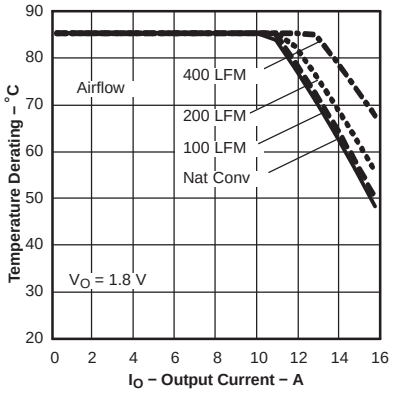


Figure 9.

Copyright © 2004–2007, Texas Instruments Incorporated

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	5, 6	The positive input voltage power node to the module, which is referenced to common GND.
V_O	3, 4	The regulated positive power output with respect to the GND node.
GND	1, 2, 10, 11	This is the common ground connection for the V_I and V_O power connections. It is also the 0 VDC reference for the control inputs.
Inhibit	12	The Inhibit pin is an open-collector/drain, active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the inhibit feature is not used, the control pin should be left open-circuit. The module then produces an output voltage whenever a valid input source is applied. Do not place an external pull-up on this pin. *For power-up into a non-prebiased output, it is recommended that AutoTrack be utilized for On/Off control. See the Application Information for additional details.*
V_OAdjust	8	A 1% resistor must be connected directly between this pin and GND (pin 1 or 2) to set the output voltage of the module higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is 1.2 V to 5.5 V for W-suffix devices and 0.8 V to 1.8 V for L-suffix devices. The resistor value required for a given output voltage may be calculated using a formula. If left open-circuit, the module output voltage defaults to its lowest value. For further information on output voltage adjustment, consult related application note, *Input and Output Capacitor Selection*, SLTA055. The specification table gives the standard resistor values for a number of common output voltages.
V_OSense	7	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy V_o Sense should be connected to V_O. It can also be left disconnected.
Track	9	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range, the output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. *NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. Consult the Application Information section for further guidance.*

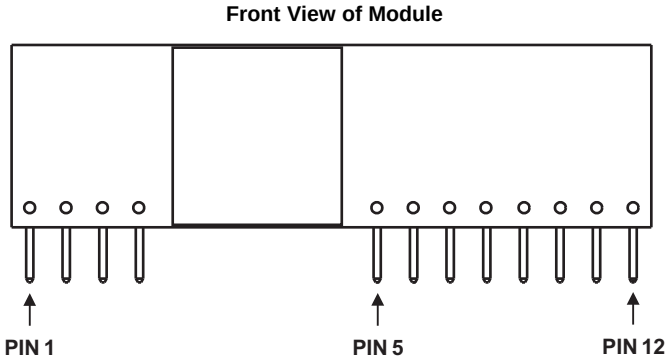


Figure 10. Pin/Terminal Locations

Copyright © 2004–2007, Texas Instruments Incorporated

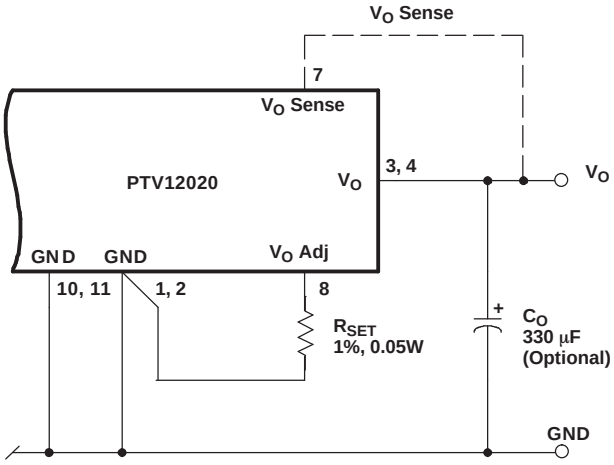
APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The V_O Adjust control (pin 8) sets the output voltage of the PTV12020 product. The adjustment range is from 1.2 V to 5.5 V for the W-suffix modules and 0.8 V to 1.8 V for L-suffix modules. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_OAdjust and GND (pin 1 or 2). Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides. For other output voltages, the value of the required resistor can either be calculated using Equation 1 or simply selected from the range of values given in Table 3.Figure 11 shows the placement of the required resistor.

Table 1. Standard Values of R_{SET} for Common Output Voltages

	PTV12020W		PTV12020L	
V_O (V) (Required)	R_{SET} (kΩ) (Standard Value)	V_O (V) (Actual)	R_{SET} (kΩ) (Standard Value)	V_O (V) (Actual)
5	0.280	5.009	N/A	N/A
3.3	2.0	3.294	N/A	N/A
2.5	4.32	2.503	N/A	N/A
2	8.06	2.010	N/A	N/A
1.8	11.5	1.801	0.130	1.800
1.5	24.3	1.506	3.57	1.499
1.2	Open	1.200	12.1	1.201
1.1	N/A	N/A	18.7	1.101
1.0	N/A	N/A	32.4	0.999
0.9	N/A	N/A	71.5	0.901
0.8	N/A	N/A	Open	0.800



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pin 8 and pins 1 or 2, using dedicated PCB traces.

(2) Never connect capacitors from V_OAdjust to either GND or V_O. Any capacitance added to the V_OAdjust pin affects the stability of the regulator.

Figure 11. V_OAdjust Resistor Placement

Copyright © 2004–2007, Texas Instruments Incorporated

Use Equation 1 to calculate the adjust resistor value. See Table 2 for parameters, R_s and V_{min}.

Equation 1. Output Voltage Adjust

$$R_{set} = 10\ k\Omega \times \frac{0.8\ V}{V_{out} - V_{min}} - R_S\ k\Omega \quad (1)$$

Table 2. Adjust Formula Parameters

PARAMETER	PART NUMBER	
	PTV12020W	PTV12020L
V_{MIN} (V)	1.2	0.8
V_{MAX} (V)	5.5	1.8
R_s(kΩ)	1.82	7.87

Table 3. Calculated Values of R_{SET} for Other Output Voltages

PTV12020W				PTV12020L	
V_O (V)	R_{SET} (kΩ)	V_O (V)	R_{SET} (kΩ)	V_O (V)	R_{SET} (kΩ)
1.200	Open	2.70	3.51	0.800	Open
1.250	158.0	2.80	3.18	0.825	312.0
1.300	78.2	2.90	2.89	0.850	152.0
1.350	51.5	3.00	2.62	0.875	98.8
1.400	38.2	3.10	2.39	0.900	72.1
1.450	30.2	3.20	2.18	0.925	56.1
1.50	24.8	3.30	1.99	0.950	45.5
1.55	21.0	3.40	1.82	0.975	37.8
1.60	18.2	3.50	1.66	1.000	32.1
1.65	16.0	3.60	1.51	1.025	27.7
1.70	14.2	3.70	1.38	1.050	24.1
1.75	12.7	3.80	1.26	1.075	21.2
1.80	11.5	3.90	1.14	1.100	18.8
1.85	10.5	4.00	1.04	1.125	16.7
1.90	9.61	4.10	0.939	1.150	15.0
1.95	8.85	4.20	0.847	1.175	13.5
2.00	8.18	4.30	0.761	1.200	12.1
2.05	7.59	4.40	0.680	1.250	9.91
2.10	7.07	4.50	0.604	1.300	8.13
2.15	6.60	4.60	0.533	1.350	6.68
2.20	6.18	4.70	0.466	1.400	5.46
2.25	5.80	4.80	0.402	1.450	4.44
2.30	5.45	4.90	0.342	1.50	3.56
2.35	5.14	5.00	0.285	1.55	2.8
2.40	4.85	5.10	0.231	1.60	2.13
2.45	4.58	5.20	0.180	1.65	1.54
2.50	4.33	5.30	0.131	1.70	1.02
2.55	4.11	5.40	0.085	1.75	0.551
2.60	3.89	5.50	0.041	1.80	0.130
2.65	3.70				

Copyright © 2004–2007, Texas Instruments Incorporated

Capacitor Recommendations for the PTV12020 Series of Power Modules

Input Capacitors

The required input capacitors are a 22-µF ceramic and 560-µF electrolytic type. For V_O > 2.1 V and I_O ≥ 11 A, the 560-µF capacitance must be rated for 1,200 mArms ripple current capability. For other conditions, V_O > 2.1 V at I_O < 11 A and V_O ≤ 2.1 V for all loads, the ripple current rating must be at least 750 mArms. Where applicable, Table 4 gives the maximum output voltage and current limits for a capacitor's rms ripple current rating.

The above ripple current requirements are *conditional* that the 22-µF ceramic capacitor is present. The 22-µF X5R/X7R ceramic capacitor is necessary to reduce both the magnitude of ripple current through the electroytic capacitor and the amount of ripple current reflected back to the input source. Ceramic capacitors should be located within 0.5 in. (1,3 cm) of the module's input pins. Additional ceramic capacitors can be added to reduce the RMS ripple current requirement for the electrolytic capacitor.

Ripple current (Arms) rating, less than 100-mΩ equivalent series resistance (ESR), and temperature are the major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 × (max. DC voltage + AC ripple). This is standard practice to ensure reliability. Only a few tantalum capacitors were found to have sufficient voltage rating to meet this requirement. At temperatures below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

Output Capacitor (Optional)

For applications with load transients (sudden changes in load current), regulator response benefits from external output capacitance. The recommended output capacitance of 330 µF allows the module to meet its transient response specification. For most applications, a high-quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C. For operation below 0°C, tantalum, ceramic, or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 4.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed approximately 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

Tantalum Capacitors

Tantalum-type capacitors can only be used on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have reduced power dissipation and surge current ratings. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered before the maximum capacitance value is reached.

Capacitor Table

Table 4 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

Note: This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Copyright © 2004–2007, Texas Instruments Incorporated

Table 4. Input/Output Capacitors

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Part Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Optional Output Bus	
Panasonic, Aluminum FC (Radial)	25	330	0.090	775	10 × 12.5	2	1	EEUFC1E331 (V_O≤ 2.1V, or V_O>2.1V & I_O≤ 10A)
	25	560	0.065	1205	12.5 × 15	1	1	EEUFC1E561S
FK (SMD)	25	1,000	0.060	1100	12.5 × 13.5	1	1	EEVFK1E102Q (V_O≤ 3.4V)
	35	680	0.060	1100	12.5 × 13.5	1	1	EEVFK1V681Q (V_O≤ 3.4V)
United Chemi-Con	25	680	0.068	1050	10 × 16	1	1	LXZ16VB681M10X16LL (V_O≤3.4V)
LXZ, Aluminum (Radial)	16	330	0.090	760	10 × 12.5	2	1	LXZ25VB331M10X12LL (V_O≤2.1V, or V_O>2.1V & I_O≤10A)
FX, OS-Con (SMD)	16	330	0.018	4500	10 × 10.5	2	≤ 3	16FX330M
PS, Poly-Aluminum (Radial)	16	330	0.014	5060	10 × 12.5	2	≤ 2	16PS330MJ12
PXA, Poly-Aluminum (SMD)	16	330	0.014	5050	10 × 12.2	2	≤ 3	PXA16VCMJ12
Nichicon, Aluminum	25	560	0.060	1060	12.5 × 15	1	1	UPM1E561MHH6 (V_O≤3.4V)
PM (Radial)	35	560	0.048	1360	16 × 15	1	1	UPM1V561MHH6
HD (Radial)	25	680	0.038	1430	10 × 16	1	1	UHD1C681MHR
Panasonic, Poly-Aluminum WA (SMD)	16	330	0.022	4100	10 × 10.2	2	≤ 3	EEFWA1C331P
S/SE (SMD)	6.3	180	0.005	4000	7.3× 4.3× 4.2	N/R (1)	≤ 1	EEFSE0J181R (V_O≤5.1V)
Sanyo TP, Poscap	10	330	0.025	3000	7.3× 4.3× 3.8	N/R (1)	≤ 4	10TPE330M
SP, Os-Con	16	270	0.018	>3500	10 × 10.5	2 (2)	≤ 3	16SP270M
SVP, Os-Con (SMD)	16	330	0.016	4700	11 × 12	2	≤ 3	16SVP330M
AVX, Tantalum, Series III	10	470	0.045	>1723	7.3× 5.7× 4.1	N/R (1)	≤ 5	TPSE477M010R0045 (V_O≤5.1V)
TPS (SMD)	10	330	0.045	>1723	7.3× 5.7× 4.1	N/R (1)	≤ 5	TPSE337M010R0045 (V_O≤5.1V)
Kemet (SMD) T520, Poly-Tant	10	330	0.040	1800	7.3× 4.3× 4	N/R (1)	≤ 5	T520X337M010AS
T530, Poly-Tant/Organic	10	330	0.010	>3800	7.3× 4.3× 4	N/R (1)	≤ 1	T530X337M010ASE010
	6.3	470	0.010	4200	7.3× 4.3× 4	N/R (1)	≤ 1	T530X477M006ASE010 (V_O≤5.1V)
Vishay-Sprague 595D, Tantalum (SMD)	10	470	0.100	1440	7.2× 6× 4.1	N/R (1)	≤ 5	595D477X0010R2T (V_O≤5.1V)
94SA, Os-Con (Radial)	16	1,000	0.015	9740	16 × 25	1	≤ 2	94SA108X0016HBP
Kemet, Ceramic X5R (SMD)	16	10	0.002	—	3225	≥2 (3)	≤ 5	C1210C106M4PAC
	6.3	47	0.002		3225	N/R (1)	≤ 5	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3	100	0.002	—	3225	N/R (1)	≤ 3	GRM32ER60J107M
	6.3	47			3225	N/R (1)	≤ 5	GRM32ER60J476M
	16	22				≥1 (3)	≤ 5	GRM32ER61C226K
	16	10				≥2 (3)	≤ 5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3	100	0.002	—	3225	N/R (1)	≤ 3	C3225X5R0J107MT
	6.3	47			3225	N/R (1)	≤ 5	C3225X5R0J476MT
	16	22				≥1 (3)	≤ 5	C3225X5R1C226MT
	16	10				≥2 (3)	≤ 5	C3225X5R1C106MT

(1) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(2) Total capacitance of 540 µF is acceptable based on the combined ripple current rating.
(3) Ceramic capacitors are required to complement electrolytic types at the input and to reduce high-frequency ripple current.

Copyright © 2004–2007, Texas Instruments Incorporated

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, or the total amount of load capacitance is above 3,000 µF, the selection of output capacitors becomes more important.

Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

Introduction

The PTH/PTV family of non-isolated, wide-output adjustable power modules are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, nonisolated modules with the same footprint and form factor. POLA parts are also ensured to be interoperable, thereby, providing customers with second-source availability.

From the basic, *Just Plug it In* functionality of the 6-A modules, to the 30-A rated feature-rich PTHxx030, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 5 provides a quick reference to the features by product series and input bus voltage.

Table 5. Operating Features by Series and Input Bus Voltage

Series	Input Bus (V)	I_O (A)	Adjust (Trim)	On/Off Inhibit	Over-Current	Prebias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
PTHxx050	3.3	6	•	•	•	•	•			
	5	6	•	•	•	•	•			
	12	6	•	•	•	•	•			
PTHxx060	3.3 / 5	10	•	•	•	•	•	•	•	
	12	10	•	•	•	•	•	•	•	
PTHxx010	3.3 / 5	15	•	•	•	•	•	•	•	
	12	12	•	•	•	•	•	•	•	
PTVxx010	5	8	•	•	•	•	•			
	12	8	•	•	•	•	•			
PTHxx020	3.3 / 5	22	•	•	•	•	•	•	•	•
	12	18	•	•	•	•	•	•	•	•
PTVxx020	5	18	•	•	•	•	•		•	•
	12	16	•	•	•	•	•		•	•
PTHxx030	3.3 / 5	30	•	•	•	•	•	•	•	•
	12	26	•	•	•	•	•	•	•	•

For simple point-of-use applications, the PTH12050 (6A) provides operating features such as an on/off inhibit, output voltage trim, prebias start-up and overcurrent protection. The PTH12060 (10A), and PTH12010 (12A) include an output voltage sense, and margin up/down controls. Then the higher output current, PTH12020 (18A) and PTH12030 (26A) products incorporate overtemperature shutdown protection.

The PTV12010 and PTV12020 are similar parts offered in a vertical, single in-line pin (SIP) profile, at slightly lower current ratings.

All of the products referenced in Table 5 include Auto-Track™. This feature was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described in the following sections.

Copyright © 2004–2007, Texas Instruments Incorporated

POWER-UP INTO A NON-PREBIASED OUTPUT — AUTO-TRACK™ FUNCTION

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

Basic Power-Up Using Auto-Track™

For applications requiring output voltage on/off control, each series of the PTH family incorporates the track control pin. The Auto-Track feature should be used instead of the inhibit feature wherever there is a requirement for the output voltage from the regulator to be turned on/off.

Figure 12 shows the typical application for basic start-up. Note the discrete transistor (Q1). The track input has its own internal pull-up to a potential of 5 V to 13.2 V The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor or supply voltage supervisor (TPS3808 or TPS7712) is recommended for control.

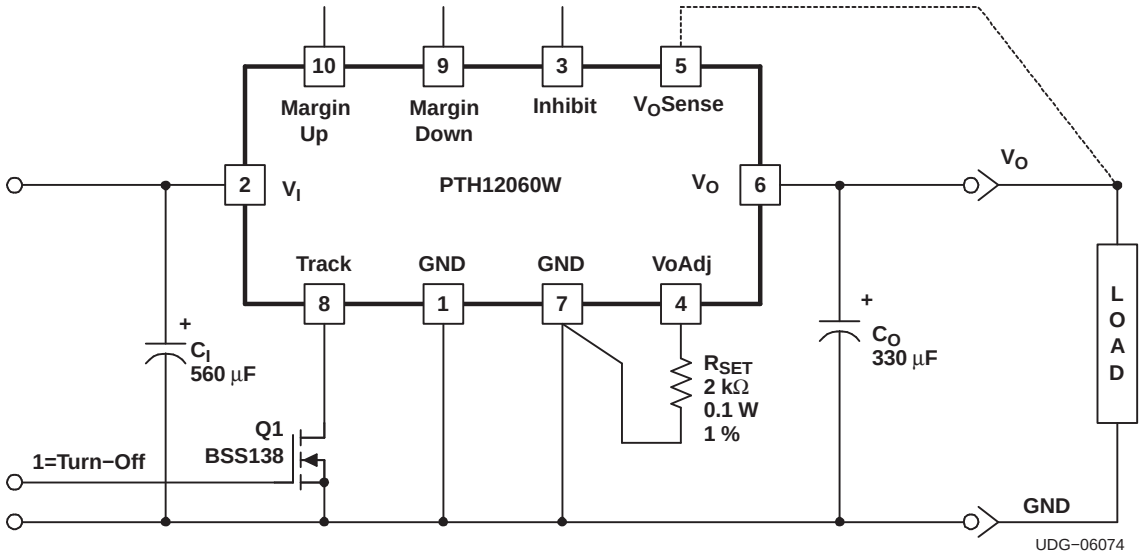


Figure 12. Basic Start-up Control Circuit

Turning on Q1 applies a low voltage to the track control pin and disables the output of the module. If Q1 is then turned off, the output ramps immediately to the regulated output voltage. A regulated output voltage is produced within 35 ms. With the initial application of the input source voltage, the track pin must be held low (Q1 turned ON) for at least 40 ms. Figure 13 shows the typical rise in both the output voltage and input current, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 Vds. The waveforms were measured with a 10-A constant current load.

Copyright © 2004–2007, Texas Instruments Incorporated

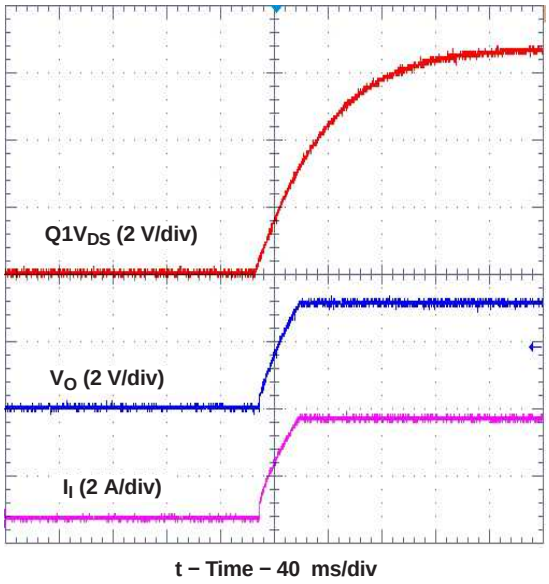


Figure 13. Power-Up from Track Control

NOTE

If a prebias condition is not present, it is highly recommended that the Track control pin be used for controlled power-up and power-down. If Track control is not used, the output voltage starts up and overshoots by as much as 10%, before settling at the output voltage setpoint.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Copyright © 2004–2007, Texas Instruments Incorporated

Typical Auto-Track Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 14.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential through R_{TRK} as defined in Figure 14. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 40 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 14 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of two 12-V input Auto-Track modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 43 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 43-ms time period is controlled by the capacitor C3. The value of 3.3 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 15 shows the output voltage waveforms from the circuit of Figure 14 after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 16. In order for a simultaneous power-down to occur, the track inputs must be pulled low before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that a valid input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the maximum output capacitance and the Auto-Track slew rate. If the *Track* pin is pulled low at a slew rate greater than 1 V/ms, the discharge of the output capacitors will induce large currents which could exceed the peak current rating of the module. This will result in a reduction in the maximum allowable output capacitance as listed in the Electrical Characteristics table. When controlling the *Track* pin of the PTH12060W using a voltage supervisor IC, the slew rate is increased, therefore $C_{O(max)}$ is reduced to 2200 µF.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 40 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

Copyright © 2004–2007, Texas Instruments Incorporated

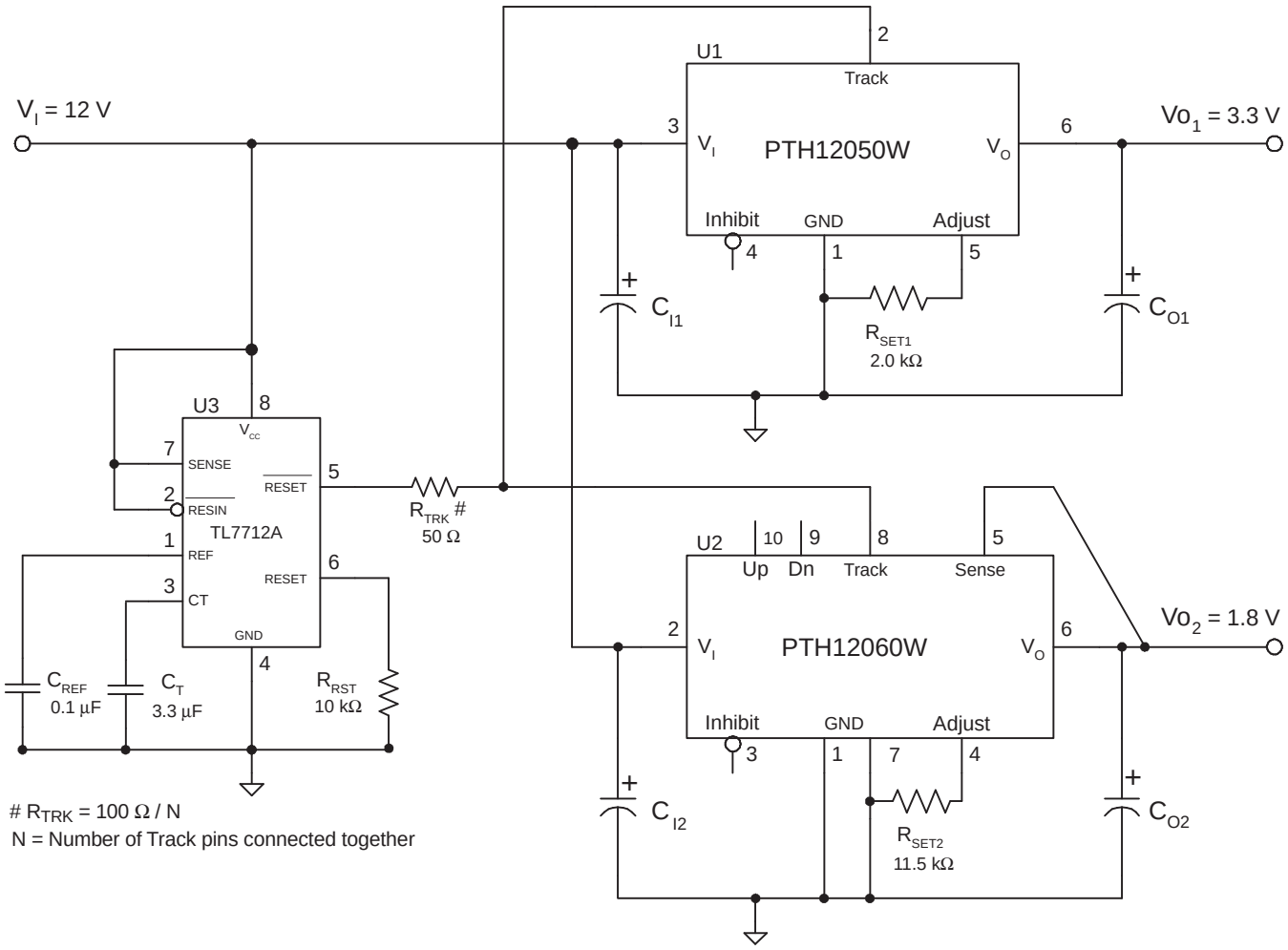


Figure 14. Sequenced Power Up and Power Down Using Auto-Track

Copyright © 2004–2007, Texas Instruments Incorporated

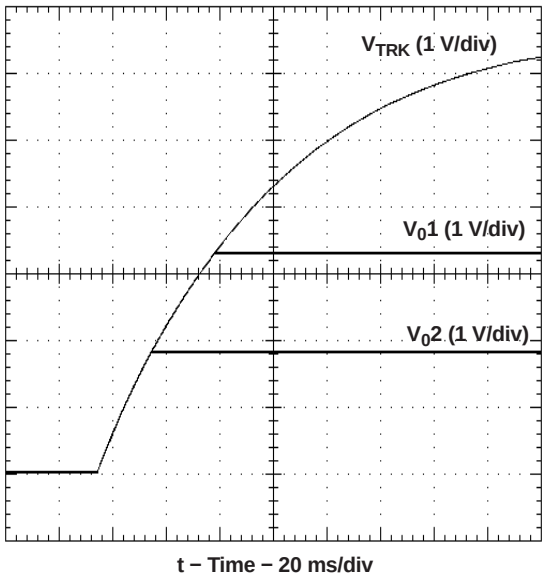


Figure 15. Simultaneous Power Up With Auto-Track Control

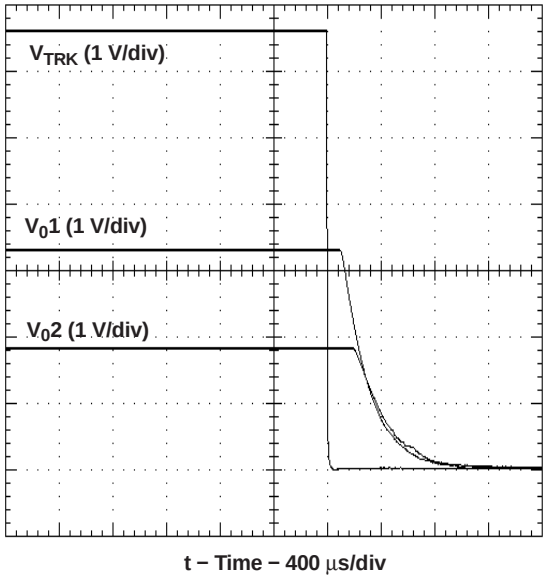


Figure 16. Simultaneous Power Down with Auto-Track Control

POWER-UP INTO A PREBIASED OUTPUT — START-UP USING INHIBIT CONTROL

The capability to start up into an output prebias condition is now available to all the 12-V input, PTH series of power modules. (Note that this is a feature enhancement for the many of the W-suffix products) [1].

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12-V input PTH modules all incorporate synchronous rectifiers, but does not sink current during startup, or whenever the Inhibit pin is held low.

Conditions for Prebias Holdoff

In order for the module to allow an output prebias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a prebias voltage when the Inhibit pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled [2]. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its Inhibit), the input voltage must always be greater than the applied prebias source. This condition must exist throughout the power-up sequence [3].

The soft-start period is complete when the output begins rising above the prebias voltage. Once it is complete the module functions as normal, and sinks current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a prebias condition is not present, the soft-start period is complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest. to its output.

Prebias Demonstration Circuit

Figure 17 shows the startup waveforms for the demonstration circuit shown in Figure 18. The initial rise in V_O2 is the prebias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (I_O2) is negligible until its output voltage rises above the applied prebias.

Copyright © 2004–2007, Texas Instruments Incorporated

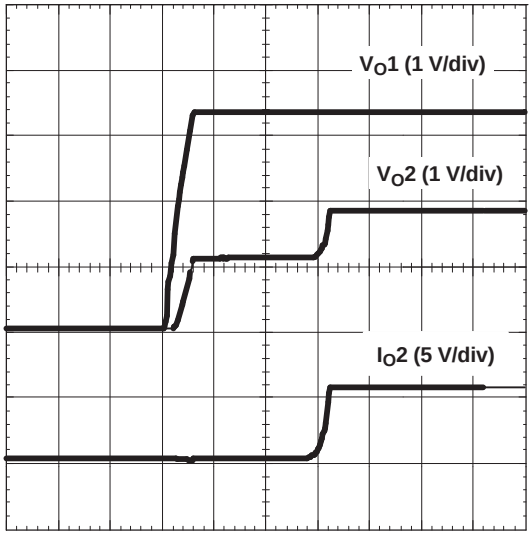


Figure 17. Prebias Startup Waveforms

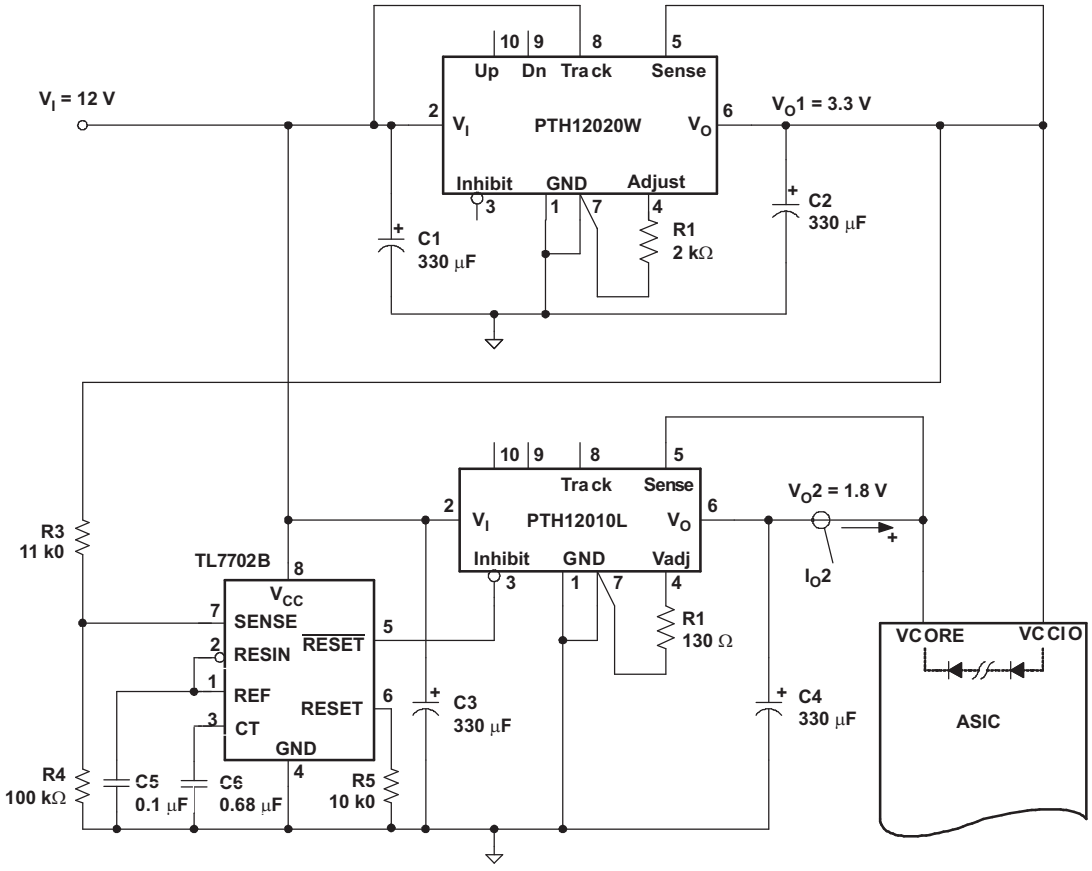


Figure 18. Application Circuit Demonstrating Prebias Startup

Notes:

1. Output prebias holdoff is an inherent feature to all PTH120x0L and PTV120x0W/L modules. It has now been incorporated into all modules (including W-suffix modules with part numbers of the form PTH120x0W), with a production lot date code of *0423* or later.
2. The prebias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the

Copyright © 2004–2007, Texas Instruments Incorporated

voltage applied to the Track control pin, the output sinks current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the Track pin to the input voltage, V_I. This raises the Track pin voltage well above the set-point voltage prior to the module's start up, thereby, defeating the Auto-Track feature.

3. To further ensure that the regulator's output does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the applied prebias source. This condition must exist *throughout* the power-up sequence of the power system.

Copyright © 2004–2007, Texas Instruments Incorporated

Remote Sense

Products with this feature incorporate an output voltage sense pin, V_OSense. A remote sense improves the load regulation performance of the module by allowing it to compensate for any *IR* voltage drop between its output and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance.

To use this feature simply connect the V_OSense pin to the V_O node, close to the load circuit (see data sheet standard application circuit). If a sense pin is left open-circuit, an internal low-value resistor (15-Ω or less) connected between the pin and the output node, ensures the output remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured from V_OSense to GND, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby, the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

The PTH12020, PTV12020, and PTH12030 products have overtemperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

Note: The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Copyright © 2004–2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTV12020LAH	ACTIVE	SIP MODULE	EVC	12	40	RoHS Exempt & non-Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTV12020WAD	ACTIVE	SIP MODULE	EVC	12	40	RoHS Exempt & non-Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTV12020WAH	ACTIVE	SIP MODULE	EVC	12	40	RoHS Exempt & non-Green	SN	N / A for Pkg Type	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

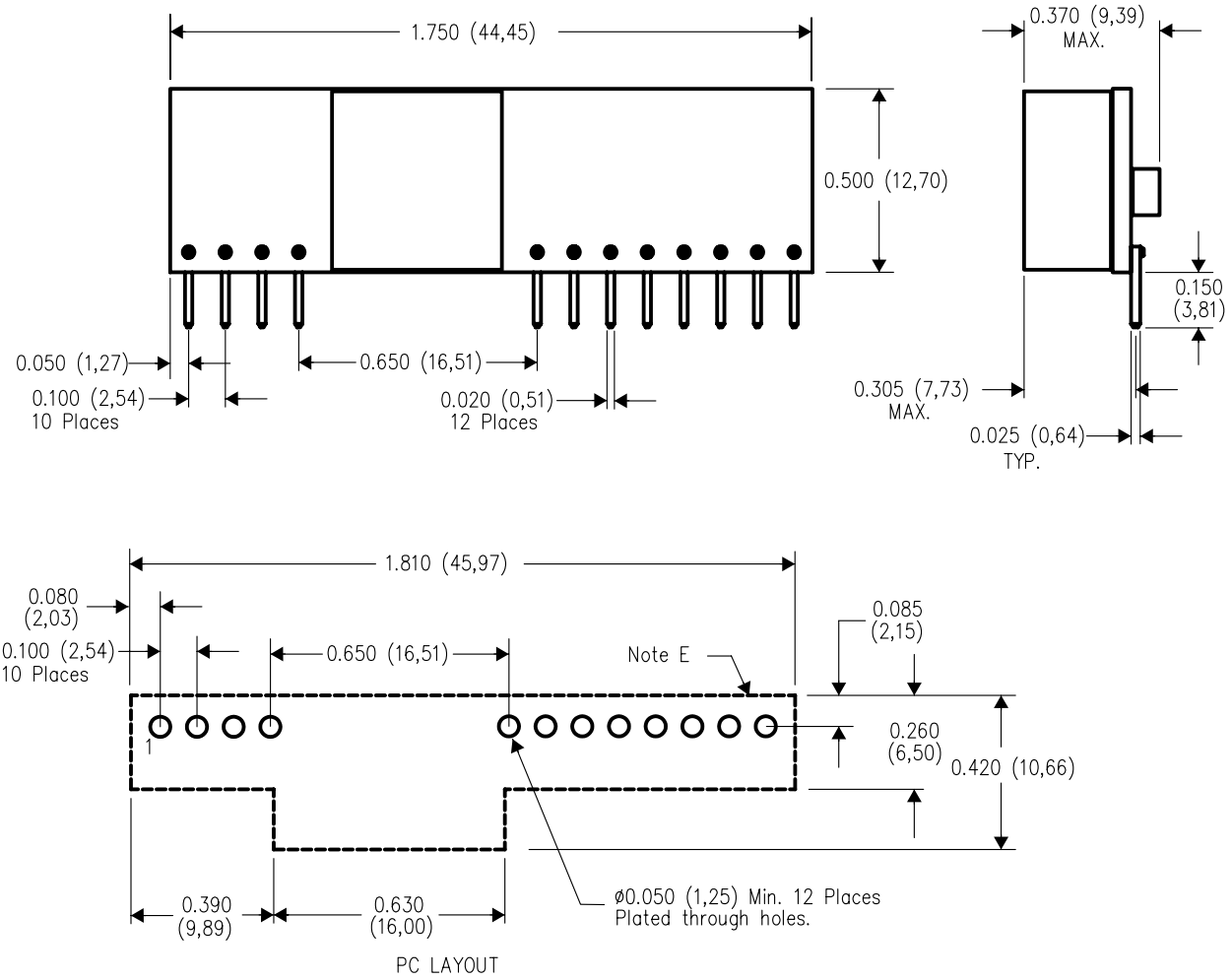
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EVC (R–PDSS–T12) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated