

2 line IPAD™, EMI filter and ESD protection in Micro QFN package

Features

- Dual line EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consumption: 1.0 mm x 1.45 mm
- Very thin package: 0.6 mm max
- High efficiency in ESD suppression (IEC 61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging.
- Lead free package
- Easy layout and flexibility due to single line topology
- Low capacitance

Complies with following standards

- IEC 61000-4-2 level 4, input and output pins
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3B (all pins)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Keyboard for mobile phones
- Computers and printers
- Communication systems
- MCU Boards

Description

The EMIF02-1003M6 is a 2 line highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on all pins.

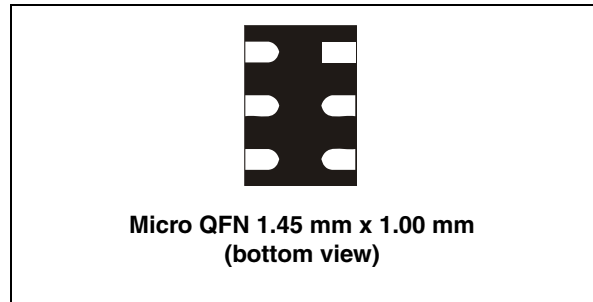


Figure 1. Pin configuration (top view)

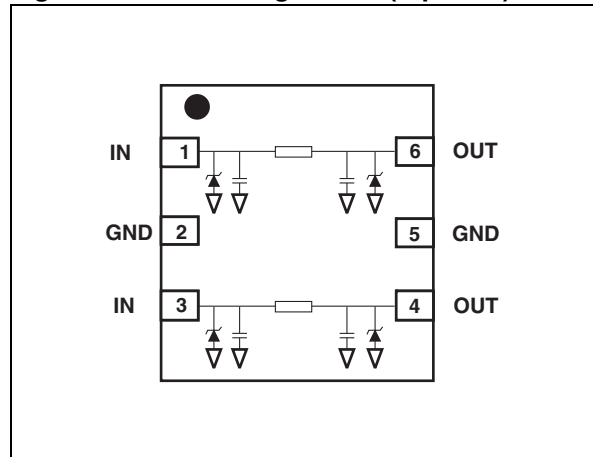
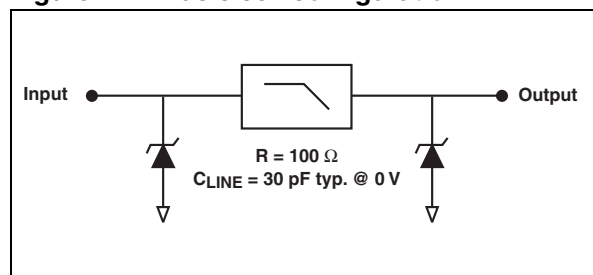


Figure 2. Basic cell configuration



TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute ratings (limiting values at $T_{amb} = 25\text{ °C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2 air discharge on input and output pins	15	kV
	ESD discharge IEC61000-4-2 contact discharge on input and output pins	8	
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

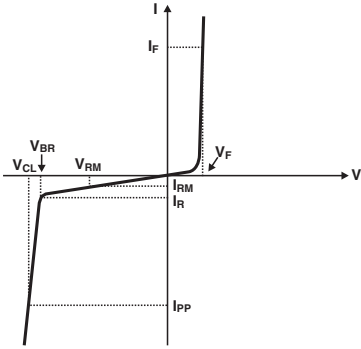
Symbol	Parameter				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic resistance				
I_{PP}	Peak pulse current				
$R_{I/O}$	Series resistance between Input & Output				
C_{line}	Input capacitance per line				
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	5	6.5	8	V
I_{RM}	$V_{RM} = 3\text{ V per line}$			100	nA
$R_{I/O}$	Tolerance $\pm 10\%$		100		Ω
C_{line}	$V_R = 0\text{ V}_{DC}$, $V_{OSC} = 30\text{ mV}$, $F = 1\text{ MHz}$		30	39	pF
S21	$F = 900\text{ MHz}$			-26	dB

Figure 4. Analog cross talk measurements

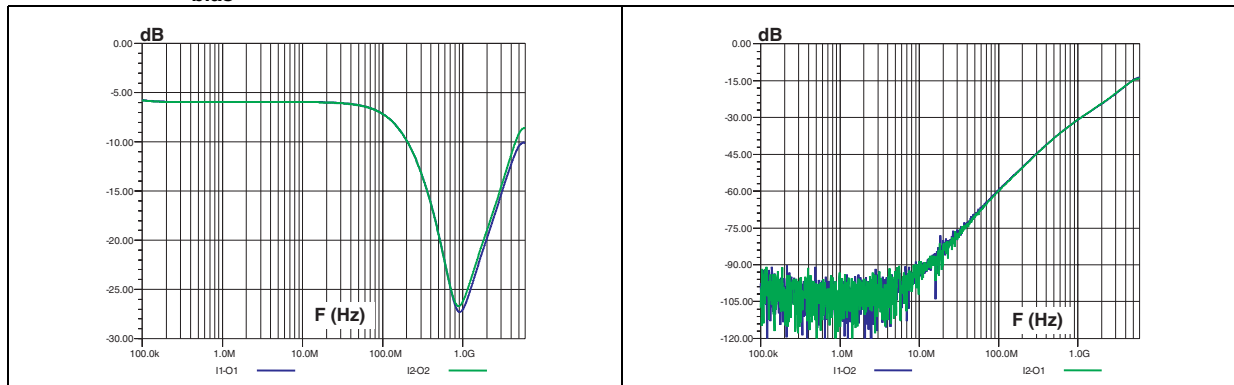
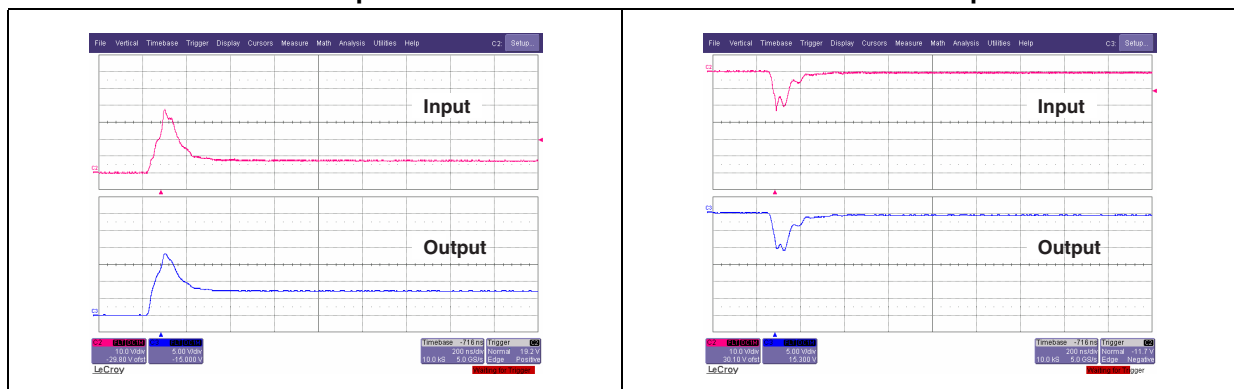


Figure 6. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input and on one output

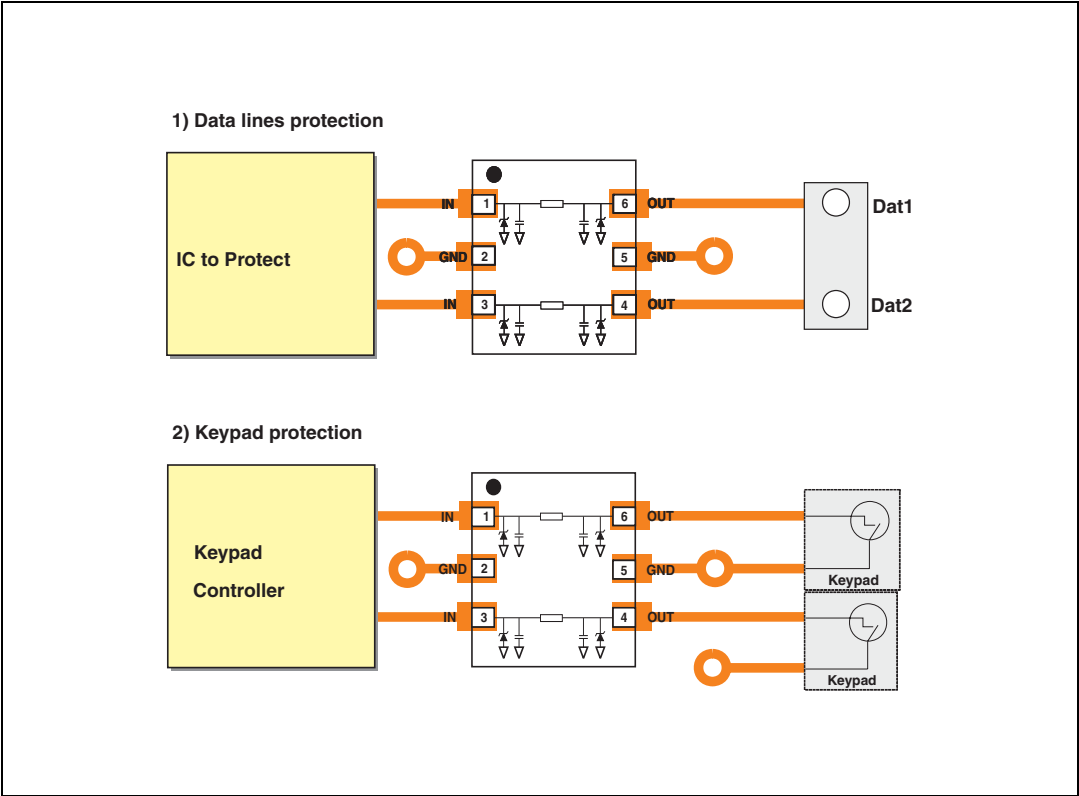


A line graph showing the relationship between C_{LINE} (pF) on the y-axis and V_{LINE} (V) on the x-axis. The y-axis ranges from 0 to 35 pF with major grid lines every 5 units. The x-axis ranges from 0 to 5 V with major grid lines every 1 unit. A single data series is plotted as a solid blue line with circular markers at each data point. The curve starts at approximately (0, 30) and decreases monotonically, reaching about 15 pF at 5 V.

V_{LINE} (V)	C_{LINE} (pF)
0.0	30.0
0.2	28.0
0.4	26.5
0.6	25.0
0.8	23.5
1.0	22.5
1.2	21.5
1.4	20.5
1.6	19.5
1.8	18.5
2.0	18.0
2.2	17.5
2.4	17.0
2.6	16.5
2.8	16.0
3.0	15.5
3.2	15.0
3.4	14.8
3.6	14.5
3.8	14.2
4.0	14.0
4.2	13.8
4.4	13.5
4.6	13.2
4.8	13.0
5.0	12.8

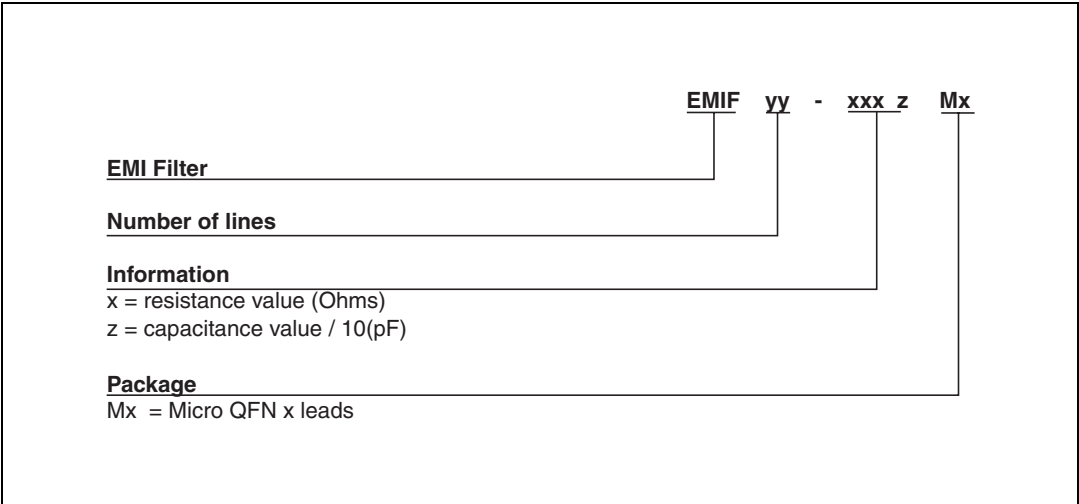
2 Application schematic

Figure 8. Application schematic



3 Ordering information scheme

Figure 9. Ordering information scheme



4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. Micro QFN 1.45 x 1.00 6L dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 10. Footprint in mm [inches]

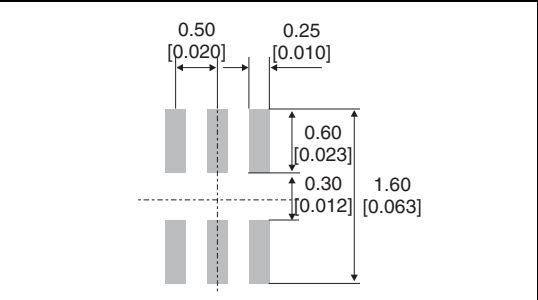
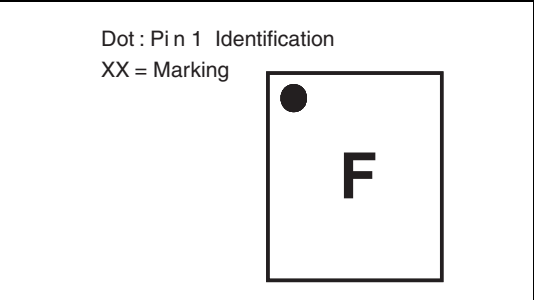


Figure 11. Marking



Technical drawing of a 35mm film strip frame, showing dimensions and pin locations. The drawing includes a side view on the left and a top view of the frame with three sprocket holes. Dimensions are given in millimeters (mm) with tolerances.

Dimensions:

- Frame width: 8.0 ± 0.3
- Frame height: 1.65
- Distance from left edge to first sprocket hole center: 0.75
- Distance between sprocket hole centers: 2.0 ± 0.05 , 4.00 ± 0.1 , and 4.00
- Sprocket hole diameter: $\phi 1.5 \pm 0.1$
- Distance from sprocket hole center to right edge: 1.75 ± 0.1
- Distance from sprocket hole center to frame edge: 3.5 ± 0.03
- Distance from sprocket hole center to frame edge: 1.20

Pin Locations:

- Pin 1 location is indicated by a dot in the first sprocket hole.
- Pin 2 location is indicated by a dot in the second sprocket hole.
- Pin 3 location is indicated by a dot in the third sprocket hole.

User direction of unreeling: Indicated by an arrow pointing to the right.

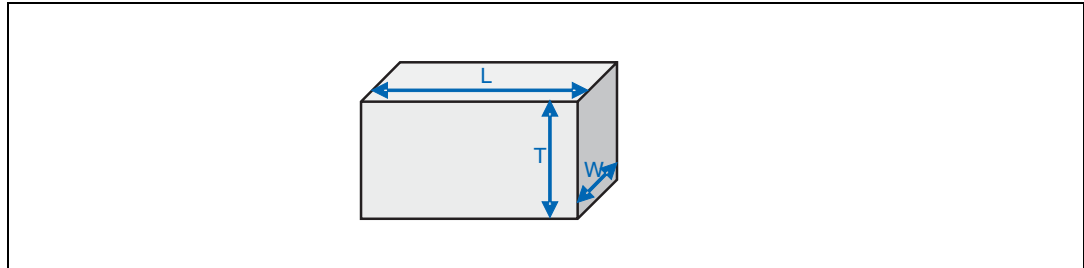
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil Opening Dimensions: L (Length), W (Width), T (Thickness).

Figure 13. Stencil opening dimensions



- b) General Design Rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - Aspect Ratio = $\frac{W}{T} \geq 1.5$
 - Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$
2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
 - c) Stencil opening for leads: Opening to footprint ratio is 90%.

5.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 μm .

5.3 Placement

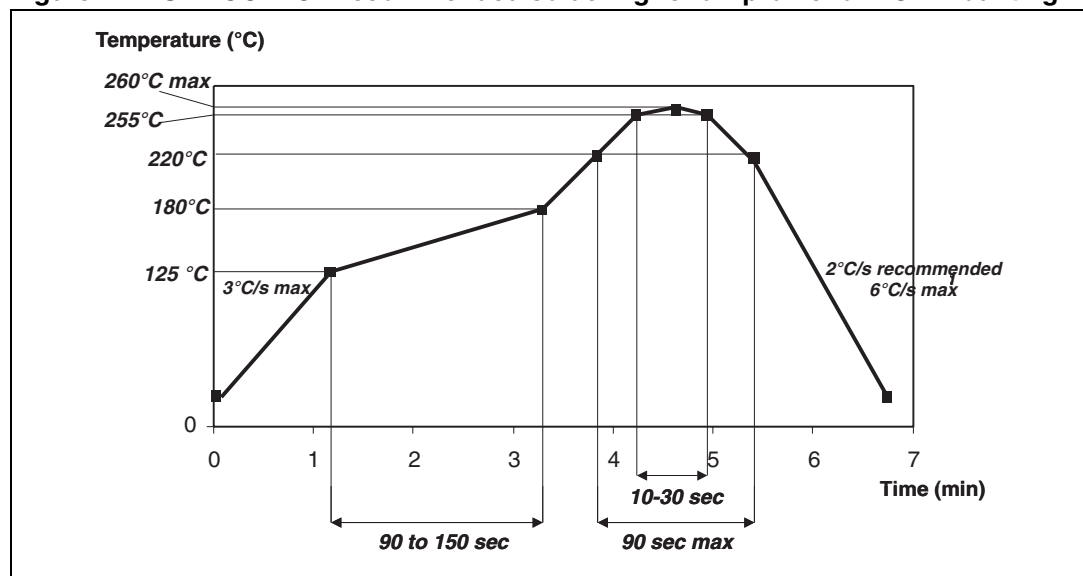
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 14. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-1003M6	F ⁽¹⁾	Micro QFN	2.2 mg	3000	Tape and reel (7")

1. The marking can be rotated by 90° to differentiate assembly location

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Oct-2007	1	Initial release.

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