TPS22966 5.5-V, 6-A, 16-mΩ On-Resistance Dual-Channel Load Switch

1 Features

- Input Voltage Range: 0.8 V to 5.5 V
- Integrated Dual-Channel Load Switch
- On-Resistance
  - R_{ON} = 16 mΩ at V_{IN} = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 3.6 V (V_{BIAS} = 5 V)
  - R_{ON} = 16 mΩ at V_{IN} = 1.8 V (V_{BIAS} = 5 V)
- 6-A Maximum Continuous Switch Current per Channel
- Low Quiescent Current
  - 80 µA (Both Channels)
  - 60 µA (Single Channel)
- Low Control Input Threshold Enables Use of 1.2-, 1.8-, 2.5-, and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD) (Optional)
- SON 14-Pin Package With Thermal Pad
- ESD Performance Tested per JESD 22
  - 2-kV HBM and 1-kV CDM

2 Applications

- Ultrabook™
- Notebooks and Netbooks
- Tablet PCs
- Consumer Electronics
- Set-top Boxes and Residental Gateways
- Telecom Systems
- Solid-State Drives (SSD)

3 Description

The TPS22966 is a small, low R_{ON}, dual-channel load switch with controlled turnon. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.8 V to 5.5 V and can support a maximum continuous current of 6 A per channel. Each switch is independently controlled by an on and off input (ON1 and ON2), which can interface directly with low-voltage control signals. In TPS22966, a 220-Ω on-chip load resistor is added for quick-output discharge when switch is turned off.

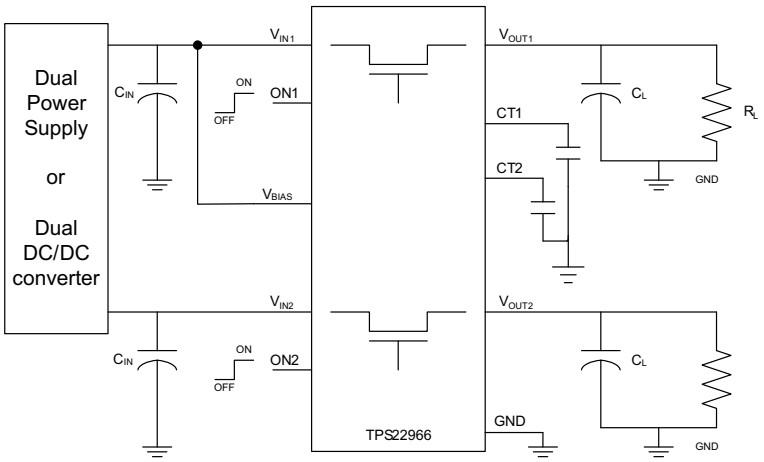
The TPS22966 is available in a small, space-saving 2-mm × 3-mm 14-SON package (DPU) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22966	WSON (14)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision E (February 2015) to Revision F — **Page**

- Changed (TPS22966 only) to (Optional) in the *Features* section. ... 1

Changes from Revision D (January 2015) to Revision E — **Page**

- Added temperature operating ranges to Electrical Characteristics (V_{BIAS} = 5.0 V) table. ... 5
- Added temperature operating ranges to Electrical Characteristics (V_{BIAS} = 2.5 V) table. ... 6
- Updated graphics in the Typical Characteristics section. ... 8

Changes from Revision C (June 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (December 2012) to Revision C — **Page**

- Added VBIAS to ABSOLUTE MAXIMUM RATINGS table. ... 4
- Updated SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION. ... 7
- Updated Test Circuit Diagram ... 14
- Updated Functional Block Diagram. ... 15

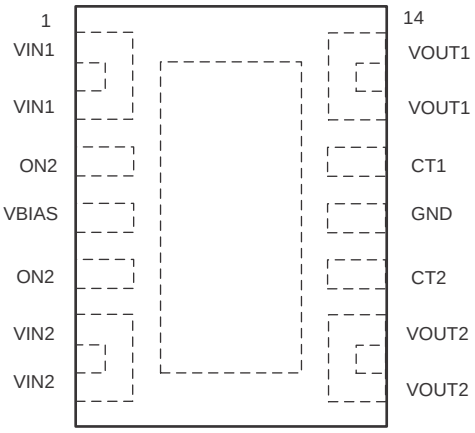
Changes from Revision A (July 2012) to Revision B — **Page**

- Updated Application Schematic. ... 1

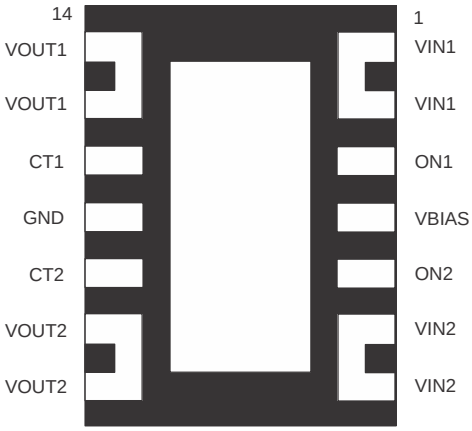
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5 Pin Configuration and Functions

DPU Package
14-Pin WSON
Top View



DPU Package
14-Pin WSON
Bottom View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8 V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See the *Application Information* section for more information
2	VIN1	I	Switch 1 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8 V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See the *Application Information* section for more information
3	ON1	I	Active high switch 1 control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See the *Application Information* section
5	ON2	I	Active high switch 2 control input. Do not leave floating
6	VIN2	I	Switch 2 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8 V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See the *Application Information* section for more information
7	VIN2	I	Switch 2 input. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8 V to V_{BIAS}. Place an optional decoupling capacitor between this pin and GND for reduce VIN dip during turnon of the channel. See the *Application Information* section for more information
8	VOUT2	O	Switch 2 output
9	VOUT2	O	Switch 2 output
10	CT2	O	Switch 2 slew rate control. Can be left floating. Capacitor used on this pin mudt be rated for a minimum of 25 V for desired rise time performance
11	GND	—	Ground
12	CT1	O	Switch 1 slew rate control. Can be left floating. Capacitor used on this pin must be rated for a minimum of 25 V for desired rise time performance
13	VOUT1	O	Switch 1 output
14	VOUT1	O	Switch 1 output
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout* section for layout guidelines

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT(2)
$V_{IN1,2}$	Input voltage	–0.3	6	V
$V_{OUT1,2}$	Output voltage	–0.3	6	V
$V_{ON1,2}$	ON-pin voltage	–0.3	6	V
V_{BIAS}	V_{BIAS} voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel		6	A
I_{PLS}	Maximum pulsed switch current per channel, pulse <300 µs, 2% duty cycle		8	A
T_J	Maximum junction temperature		125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.5	V
$V_{ON1,2}$	ON voltage		0	5.5	V
$V_{OUT1,2}$	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.5 V	0	0.5	V
$C_{IN1,2}$	Input capacitor		1(1)		µF
T_A	Operating free-air temperature (2)		–40	105	°C

(1) See the *Input Capacitor (Optional)* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part-package in the application (θ_{JA}), as given by the following equation: $TA_{(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

6.4 Thermal Information

THERMAL METRIC (1)		TPS22966 DPU (WSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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Thermal Information (continued)

THERMAL METRIC (1)		TPS22966 DPU (WSON) 14 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

6.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies where V_{BIAS} = 5 V. Typical values are for T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 5 V		–40°C to +105°C		80	120	µA
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V, $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 5 V		–40°C to +105°C		60	120	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +105°C			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 5 V	–40°C to +105°C		0.5	8	µA
			$V_{IN1,2}$ = 3.3 V	–40°C to +105°C		0.1	3	
			$V_{IN1,2}$ = 1.8 V	–40°C to +105°C		0.07	2	
			$V_{IN1,2}$ = 0.8 V	–40°C to +105°C		0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance (per channel)	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		16	19	mΩ
				–40°C to +85°C			21	
				–40°C to +105°C			23	
			V_{IN} = 3.3 V	25°C		16	19	
				–40°C to +85°C			21	
				–40°C to +105°C			23	
			V_{IN} = 1.8 V	25°C		16	19	
				–40°C to +85°C			21	
				–40°C to +105°C			23	
			V_{IN} = 1.5 V	25°C		16	19	
				–40°C to +85°C			21	
				–40°C to +105°C			23	
			V_{IN} = 1.2 V	25°C		16	19	
				–40°C to +85°C			21	
				–40°C to +105°C			23	
			V_{IN} = 0.8 V	25°C		16	19	
				–40°C to +85°C			21	
				–40°C to +105°C			23	
R_{PD}	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 15 mA		–40°C to +85°C		220	300	Ω
				–40°C to +105°C			330	

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6.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies where V_{BIAS} = 2.5 V. Typical values are for T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (both channels)	I_{OUT1} = I_{OUT2} = 0 mA, $V_{IN1,2}$ = $V_{ON1,2}$ = V_{BIAS} = 2.5 V		–40°C to +85°C		32	37	µA
				–40°C to +105°C			40	
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current (single channel)	I_{OUT1} = I_{OUT2} = 0 mA, V_{ON2} = 0 V $V_{IN1,2}$ = V_{ON1} = V_{BIAS} = 2.5 V		–40°C to +105°C		23	40	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V		–40°C to +105°C			2	µA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current (per channel)	$V_{ON1,2}$ = 0 V, $V_{OUT1,2}$ = 0 V	$V_{IN1,2}$ = 2.5 V	–40°C to +105°C		0.13	3	µA
			$V_{IN1,2}$ = 1.8 V	–40°C to +105°C		0.07	2	
			$V_{IN1,2}$ = 1.2 V	–40°C to +105°C		0.05	2	
			$V_{IN1,2}$ = 0.8 V	–40°C to +105°C		0.04	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		21	24	mΩ
				–40°C to +85°C			27	
				–40°C to +105°C			29	
			V_{IN} = 1.8 V	25°C		19	22	
				–40°C to +85°C			25	
				–40°C to +105°C			27	
			V_{IN} = 1.5 V	25°C		18	21	
				–40°C to +85°C			24	
				–40°C to +105°C			26	
			V_{IN} = 1.2 V	25°C		18	21	
				–40°C to +85°C			24	
				–40°C to +105°C			26	
			V_{IN} = 0.8 V	25°C		17	20	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
R_{PD}	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +85°C		260	300	Ω
				–40°C to +105°C			330	

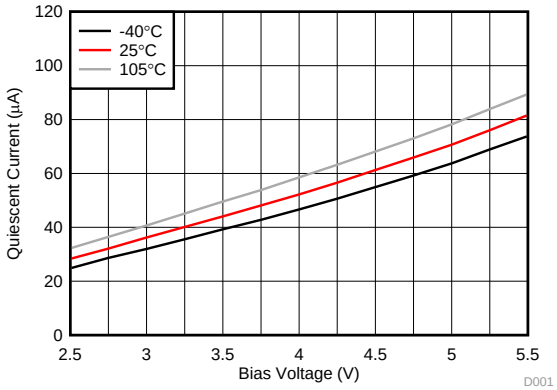
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6.7 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1310		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		6		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1720		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		460		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		550		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		170		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		325		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		16		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		400		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2050		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		5		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2275		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2.5		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		990		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1300		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		130		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		875		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		16		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		870		

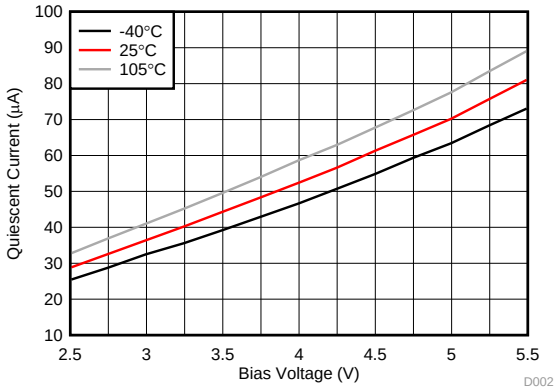
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6.8 Typical DC Characteristics



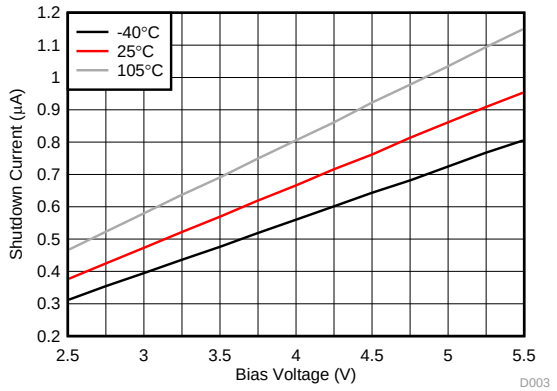
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 5$ V V_{OUT} = Open

Figure 1. Quiescent Current vs Bias Voltage Both Channels



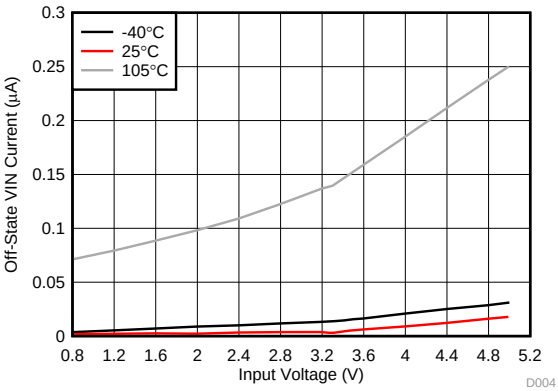
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 5$ V V_{OUT} = Open

Figure 2. Quiescent Current vs Bias Voltage Single Channel



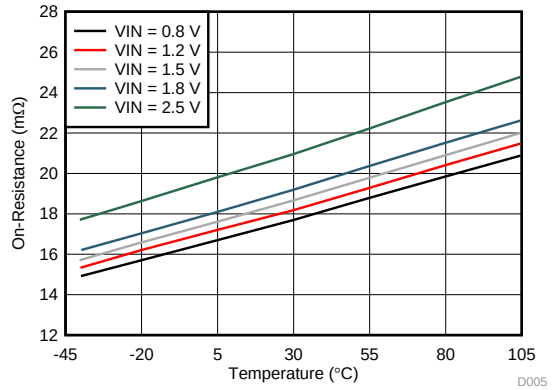
$V_{IN1} = V_{IN2} = V_{BIAS}$ $V_{ON1} = V_{ON2} = 0$ V $V_{OUT} = 0$ V

Figure 3. Shutdown Current vs Bias Voltage Both Channels



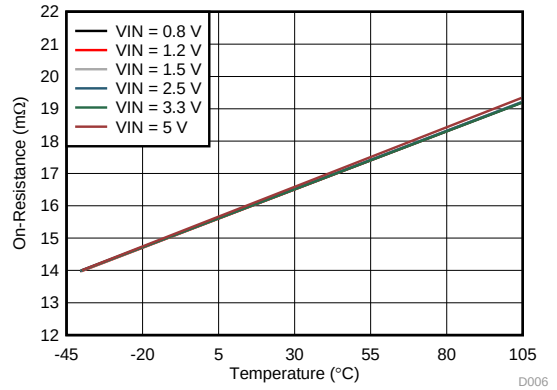
$V_{BIAS} = 5$ V $V_{ON} = 0$ V $V_{OUT} = 0$ V

Figure 4. Off-State VIN Current vs Input Voltage Single Channel



$V_{BIAS} = 2.5$ V $I_{OUT} = -200$ mA

Figure 5. On-Resistance vs Temperature Single Channel

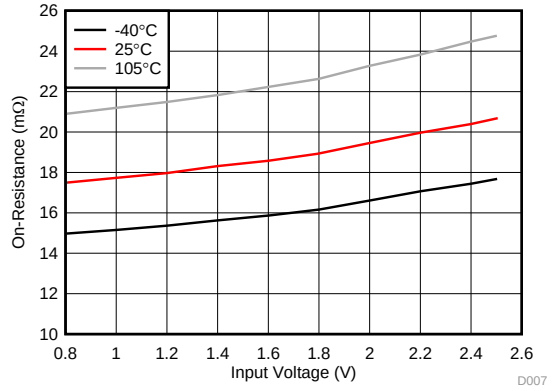


$V_{BIAS} = 5$ V $I_{OUT} = -200$ mA

Figure 6. On-Resistance vs Temperature Single Channel

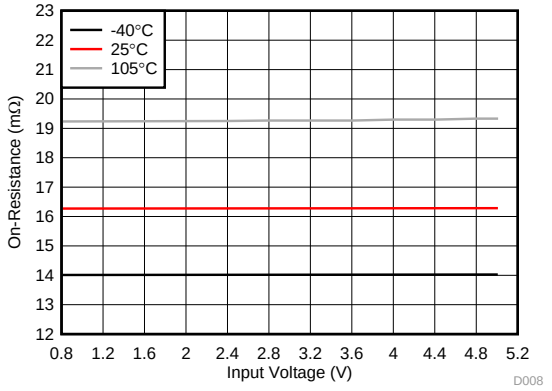
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Typical DC Characteristics (continued)



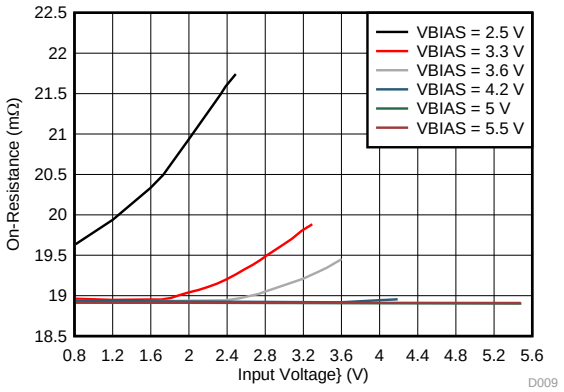
V_{BIAS} = 2.5 V I_{OUT} = –200 mA

Figure 7. On-Resistance vs Input Voltage Single Channel



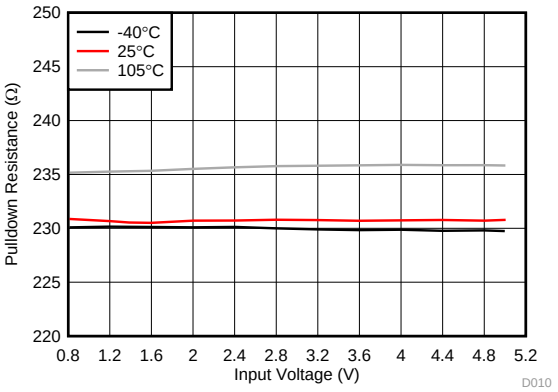
V_{BIAS} = 5 V I_{OUT} = –200 mA

Figure 8. On-Resistance vs Input Voltage Single Channel



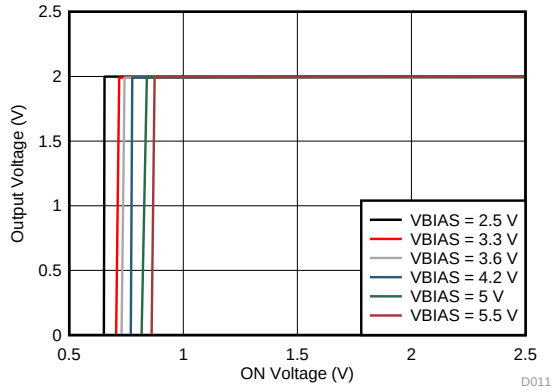
T_A = 25°C

Figure 9. On-Resistance vs Input Voltage Single Channel



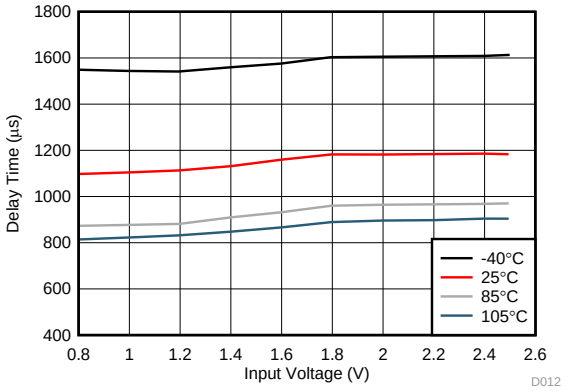
V_{BIAS} = 5 V I_{OUT} = 1 mA V_{ON} = 0 V

Figure 10. Pulldown Resistance vs Input Voltage Single Channel



T_A = 25°C

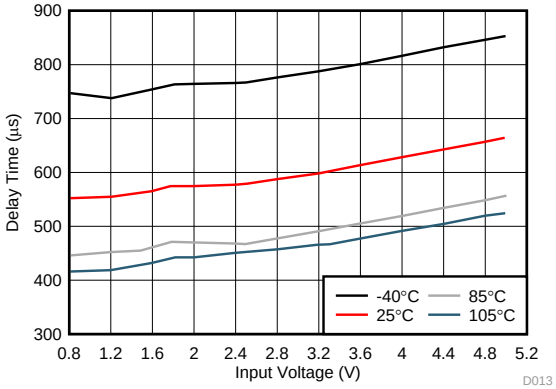
Figure 11. Output Voltage vs ON Voltage Single Channel



V_{BIAS} = 2.5 V CT = 1 nF

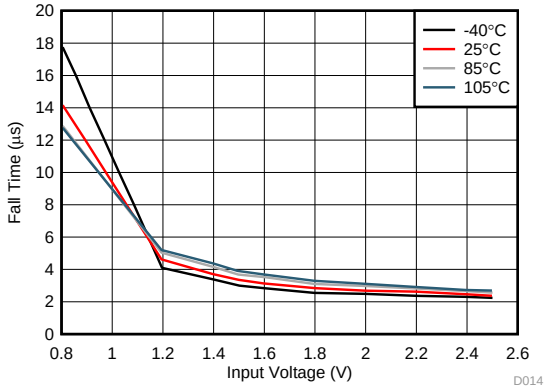
Figure 12. Delay Time vs Input Voltage

Typical DC Characteristics (continued)



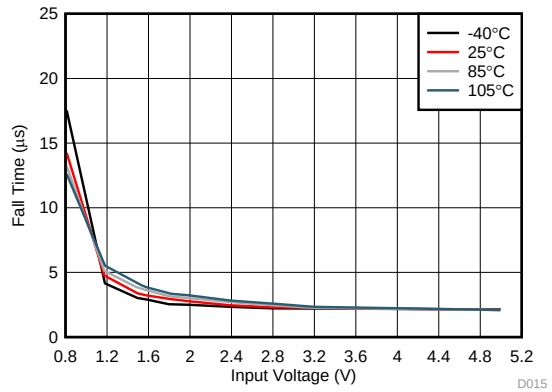
V_{BIAS} = 5 V CT = 1 nF

Figure 13. Delay Time vs Input Voltage



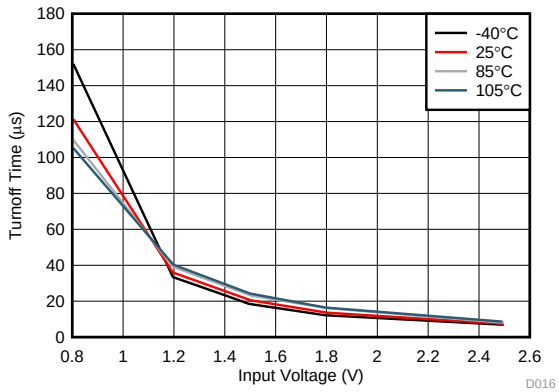
V_{BIAS} = 2.5 V CT = 1 nF

Figure 14. Fall Time vs Input Voltage



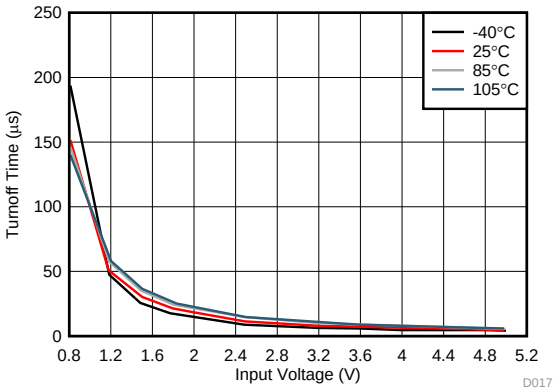
V_{BIAS} = 5 V CT = 1 nF

Figure 15. Fall Time vs Input Voltage



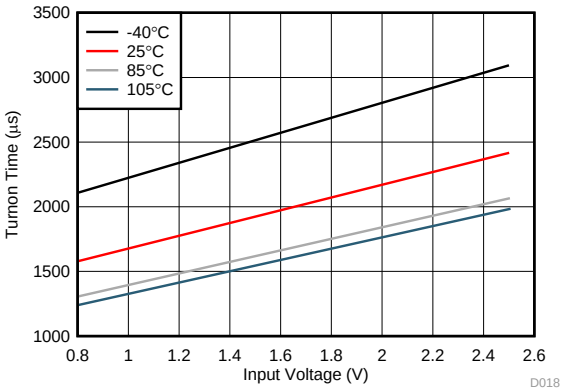
V_{BIAS} = 2.5 V CT = 1 nF

Figure 16. Turnoff Time vs Input Voltage



V_{BIAS} = 5 V CT = 1 nF

Figure 17. Turnoff Time vs Input Voltage

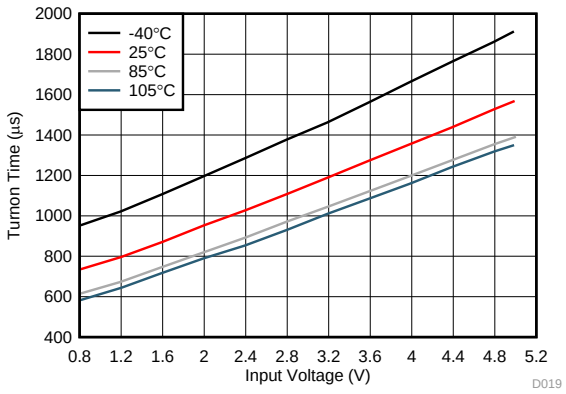


V_{BIAS} = 2.5 V CT = 1 nF

Figure 18. Turnon Time vs Input Voltage

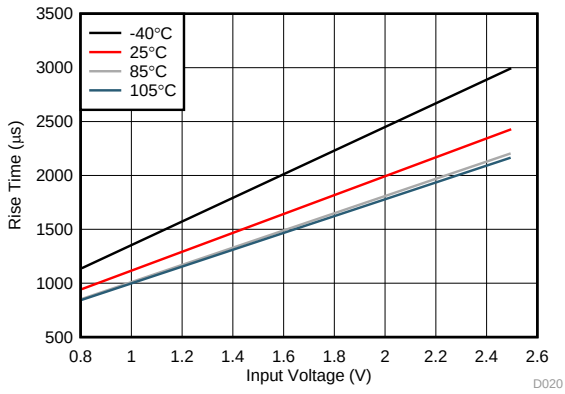
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Typical DC Characteristics (continued)



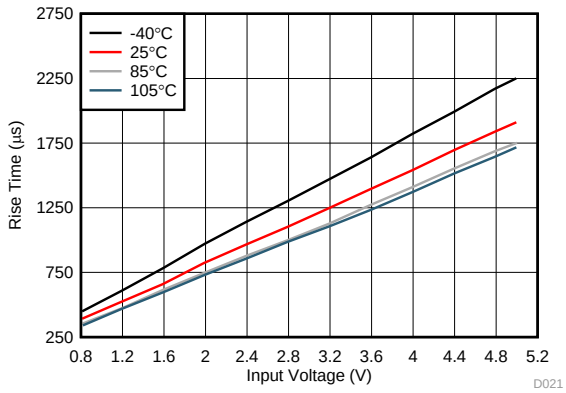
V_{BIAS} = 5 V CT = 1 nF

Figure 19. Turnon Time vs Input Voltage



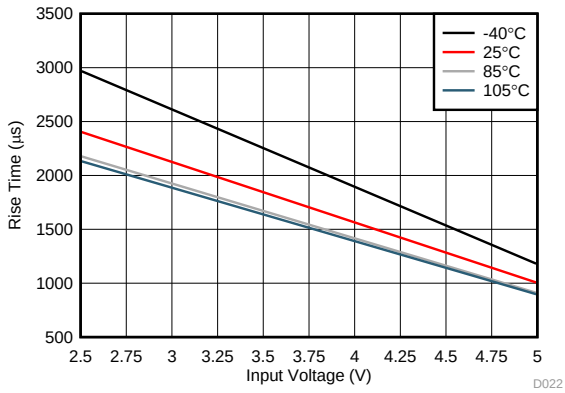
V_{BIAS} = 2.5 V CT = 1 nF

Figure 20. Rise Time vs Input Voltage



V_{BIAS} = 5 V CT = 1 nF

Figure 21. Rise Time vs Input Voltage (V_{BIAS} = 5 V, CT = 1 nF)



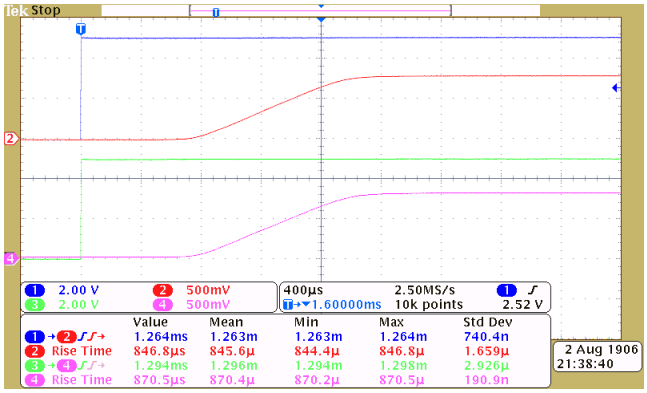
V_{IN} = 2.5 V CT = 1 nF

Figure 22. Rise Time vs Bias Voltage

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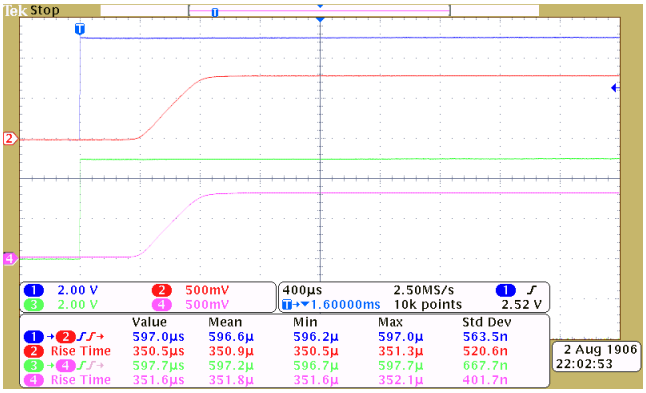
6.9 Typical AC Characteristics

At T_A = 25ºC, CT = 1 nF



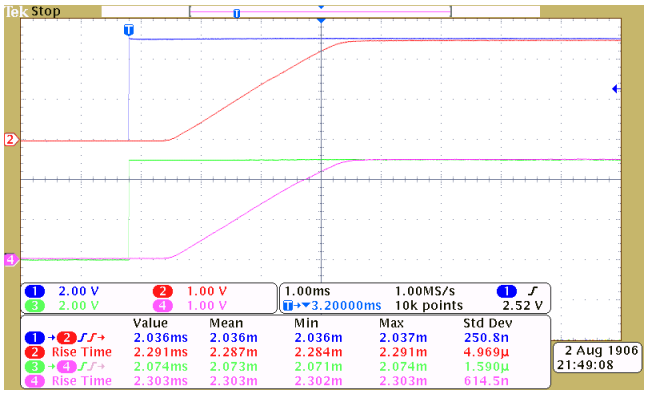
V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 23. Turnon Response Time



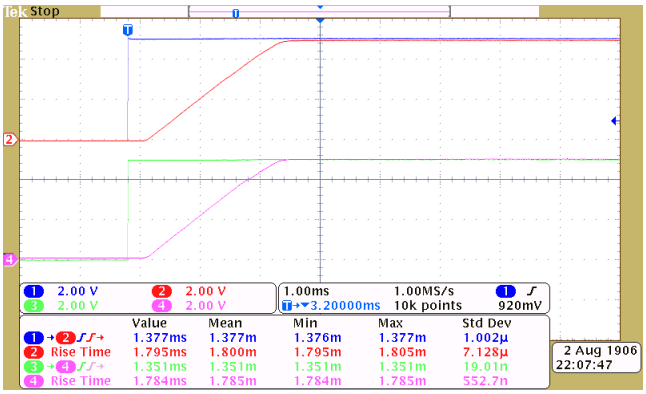
V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 24. Turnon Response Time



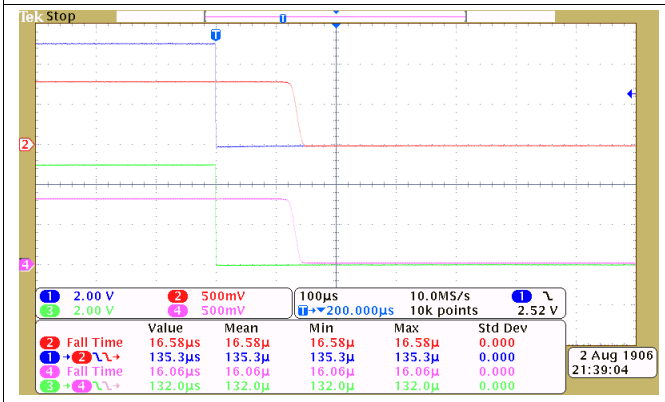
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 25. Turnon Response Time



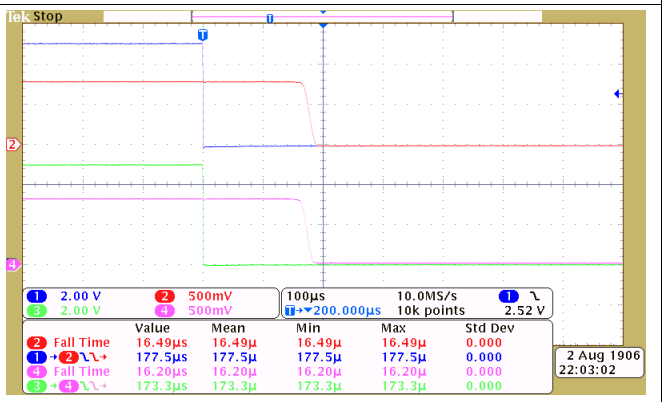
V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 26. Turnon Response Time



V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 27. Turnoff Response Time



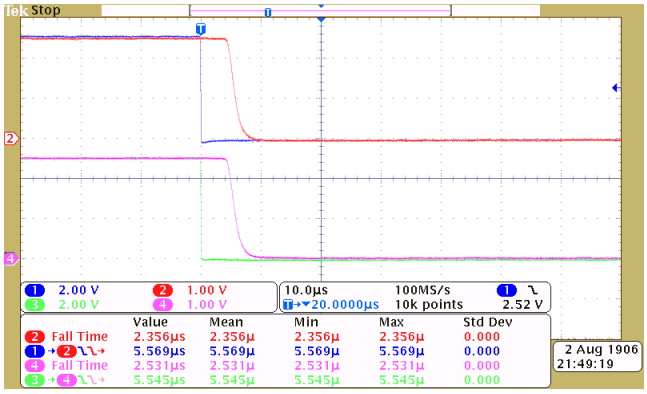
V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 28. Turnoff Response Time

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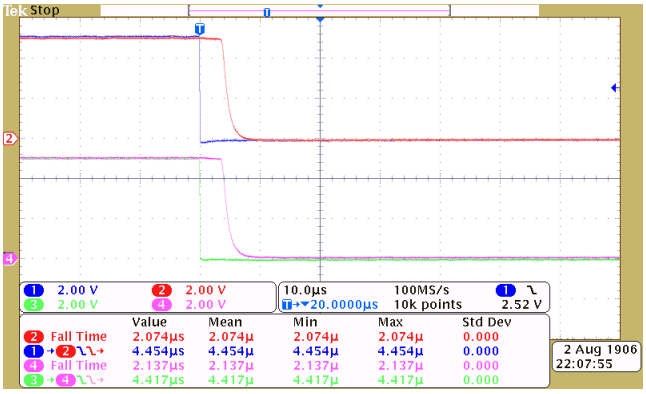
Typical AC Characteristics (continued)

At T_A = 25ºC, CT = 1 nF



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 29. Turnoff Response Time

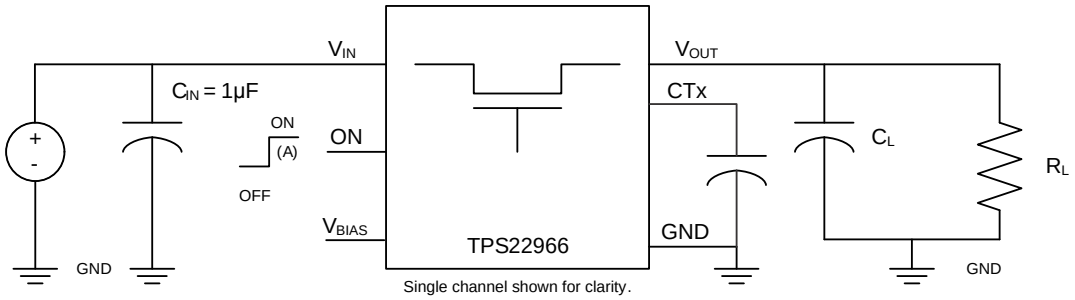


V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

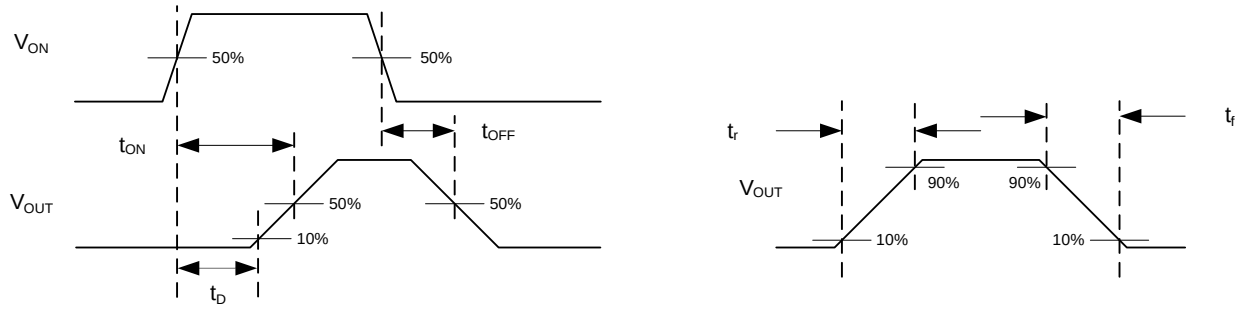
Figure 30. Turnoff Response Time

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7 Parameter Measurement Information



Test Circuit



t_{ON} and t_{OFF} Waveforms

(A) Rise and fall times of the control signal is 100 ns.

Figure 31. Test Circuit and t_{ON}-t_{OFF} Waveforms

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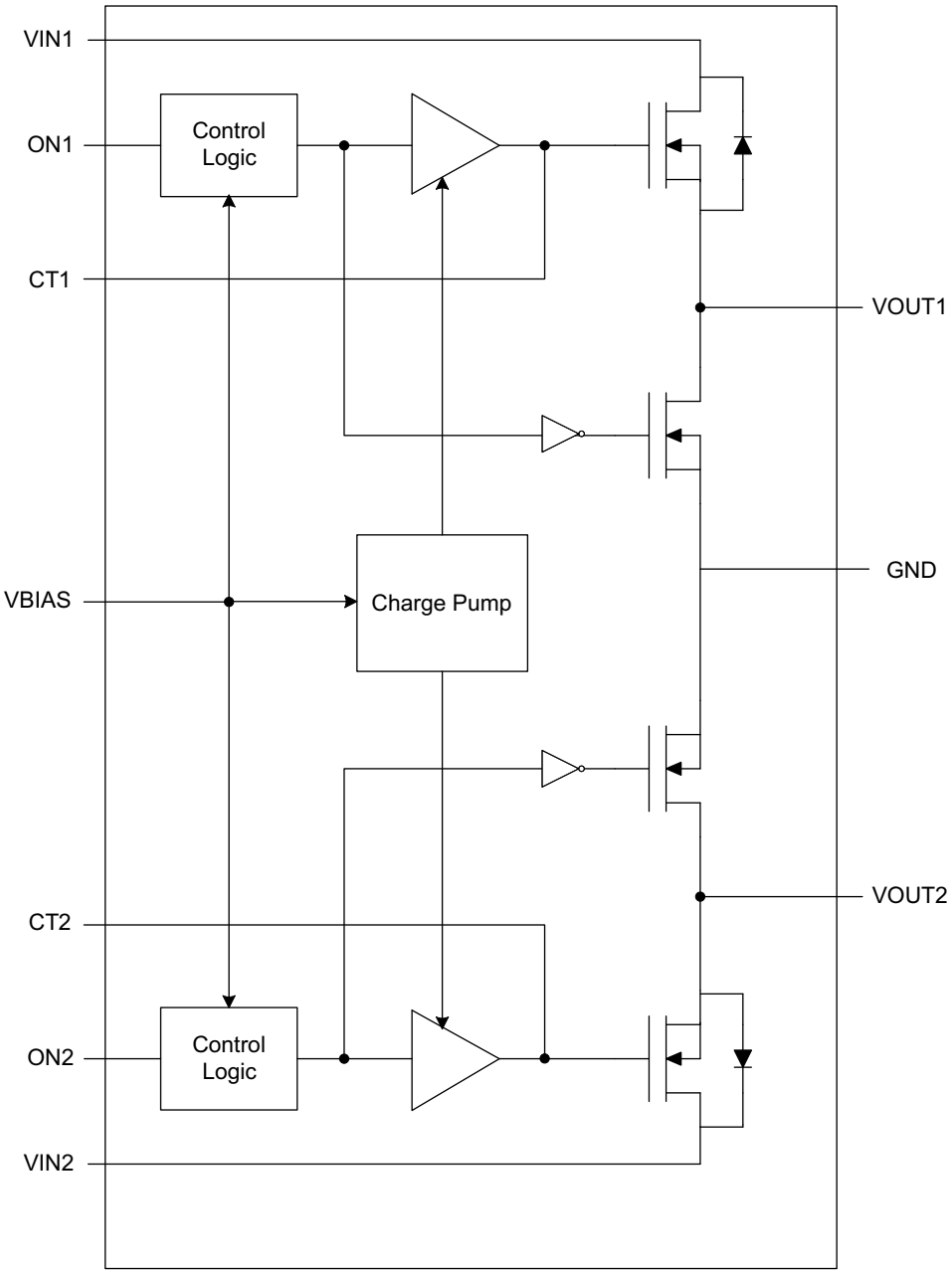
8 Detailed Description

8.1 Overview

The TPS22966 device is a dual-channel, 6-A load switch in a 14-terminal SON package. To reduce the voltage drop in high current rails, the device implements an low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

8.3.2 Input Capacitor (Optional)

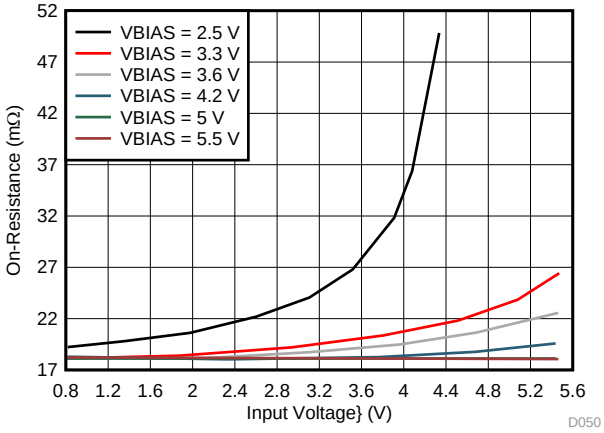
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

8.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see Figure 4).

8.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics* table. See Figure 32 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Make sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



$V_{IN} > V_{BIAS}$ I_{OUT}= –200 mA

Figure 32. On-Resistance vs Input Voltage Single Channel

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8.4 Device Functional Modes

Table 1 lists the TPS22966 functions.

Table 1. Functions Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application demonstrates how the TPS22966 can be used to limit inrush current when powering on downstream modules.

9.2 Typical Application

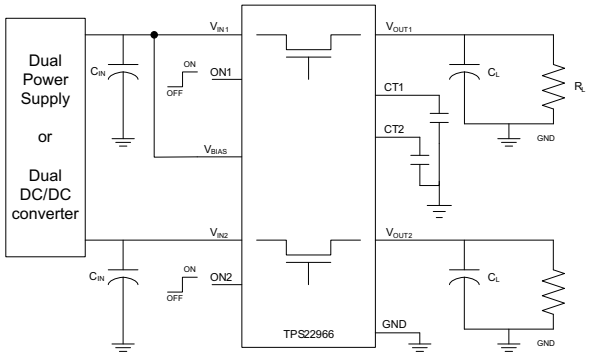


Figure 33. Typical Application Circuit

9.2.1 Design Requirements

Table 2 shows the TPS22966 desgin parameters.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage	3.3 V
Bias voltage	5 V
Load capacitance (C_L)	22 µF
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 1.

Inrush Current = C × dV/dt

where

- C is the output capacitance
- dV is the output voltage
- dt is the rise time (1)

The TPS22966 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using Table 2 and Equation 1 as shown in Equation 2.

400 mA = 22 µF × 3.3 V/dt (2)

dt = 181.5 µs (3)

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To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

9.2.2.1 Adjustable Rise Time

A capacitor to GND on the CTx pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V must be used on the CTx pin. An approximate formula for the relationship between CTx and slew rate is given in Equation 4. Equation 4 accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CTx = 0 pF. (Use Table 3 to determine rise times for when CTx = 0 pF).

$$SR = 0.32 \times CT + 13.7 \quad (4)$$

where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CTx pin (in pF)
- The units for the constant 13.7 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 3 shows rise time values measured on a typical device. Rise times shown in Table 3 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition, and the ON pin is asserted high.

Table 3. Rise Time Values

CTx (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1µF, C_{IN} = 1µF, R_L = 10Ω						
	(1) 5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.8 V
0	124	88	63	60	53	49	42
220	481	323	193	166	143	133	109
470	855	603	348	299	251	228	175
1000	1724	1185	670	570	469	411	342
2200	3328	2240	1308	1088	893	808	650
4700	7459	4950	2820	2429	1920	1748	1411
10000	16059	10835	6040	5055	4230	3770	3033

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP.

9.2.3 Application Curves

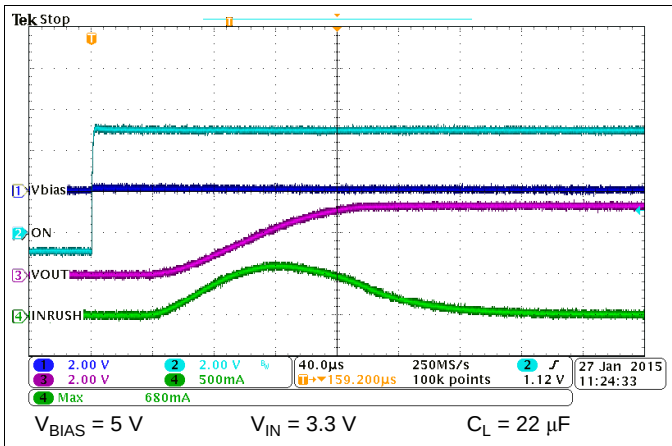


Figure 34. Inrush Current with CT = 0 pF

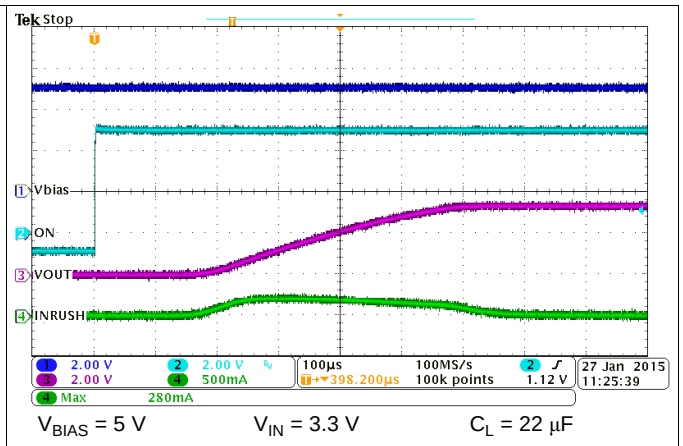


Figure 35. Inrush Current with CT = 220 pF

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10 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.5 V and a VIN range of 0.8 V to VBIAS.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

Notice the thermal vias located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

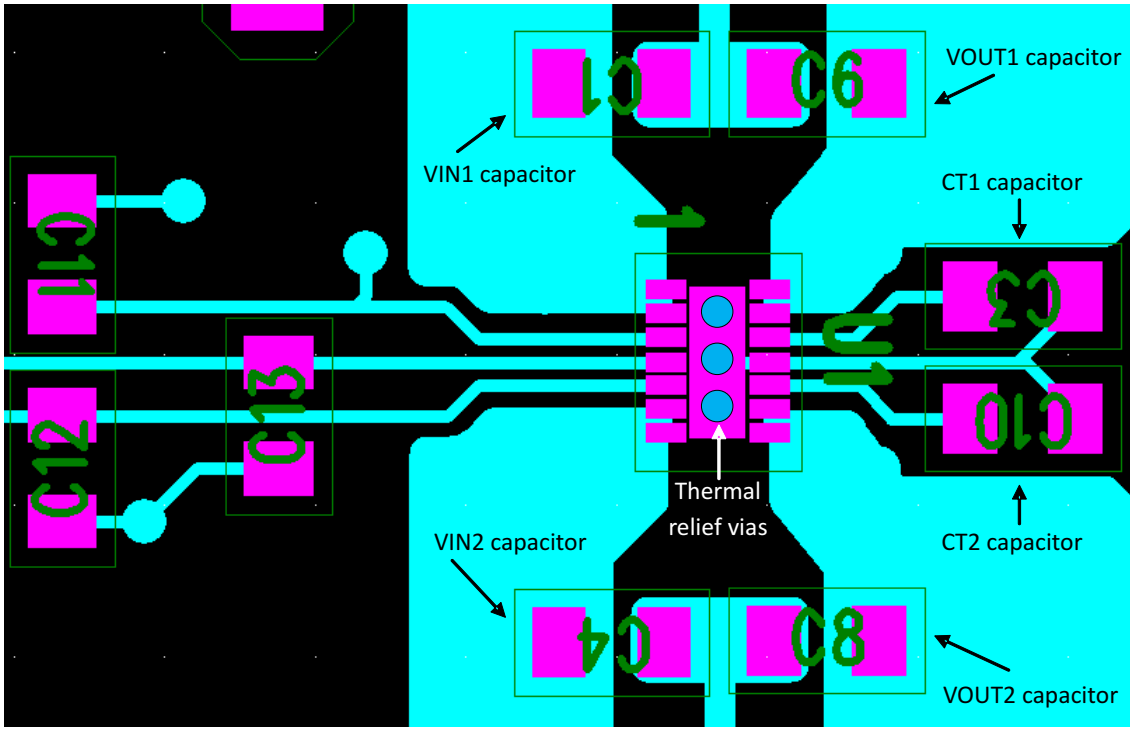


Figure 36. PCB Layout Example

11.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 5:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22966)
- T_A is the ambient temperature of the device

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Thermal Considerations (continued)

- θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout. (5)

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *TPS22966 Dual Channel Load Switch in Parallel Configuration*, SLVA585A
- *Basics of Load Switches*, SLVA652
- *Managing Inrush Current*, SLVA670A
- *Quiescent Current vs Shutdown Current for Load Switch Power Consumption*, SLVA757
- *Using the TPS22966EVM-007*, SLVU757A
- *Load Switch Thermal Considerations*, SLVUA74

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Trademarks

Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22966DPUR	ACTIVE	WSON	DPU	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB966	Samples
TPS22966DPUT	ACTIVE	WSON	DPU	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB966	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS22966 :

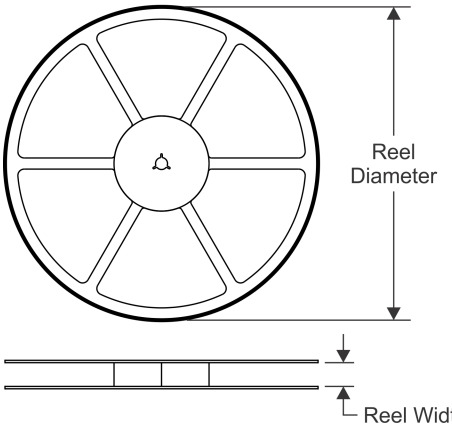
- Automotive: TPS22966-Q1

NOTE: Qualified Version Definitions:

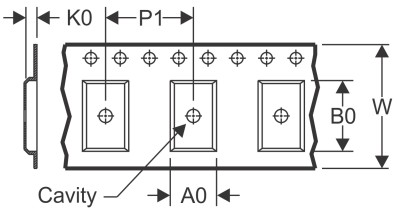
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

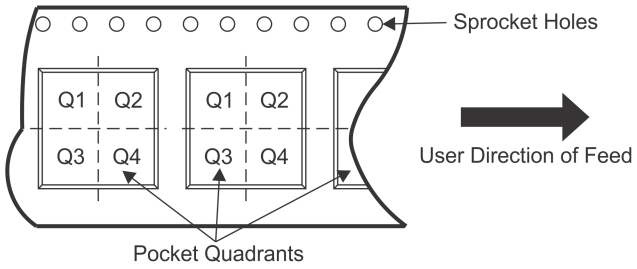


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

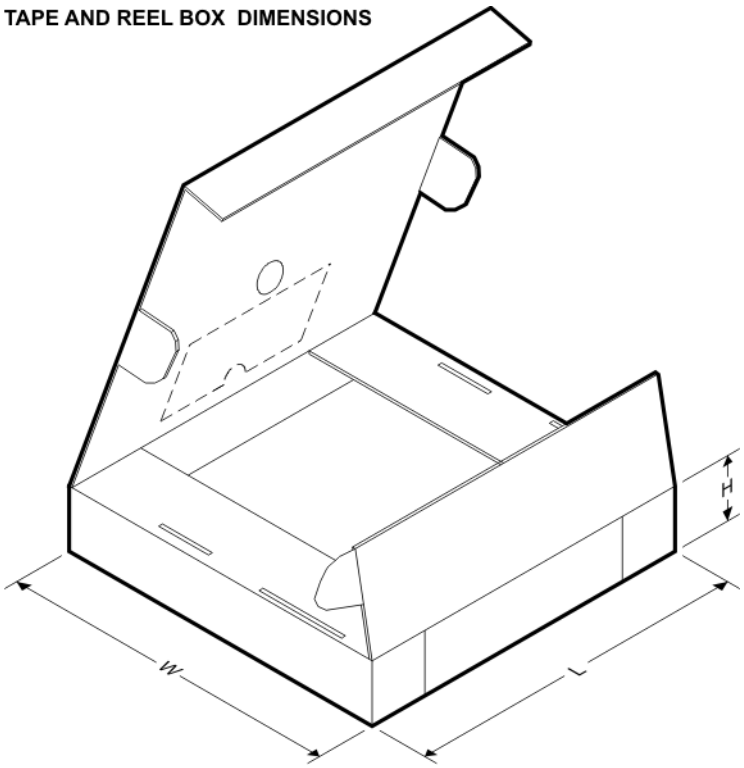
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22966DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22966DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22966DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

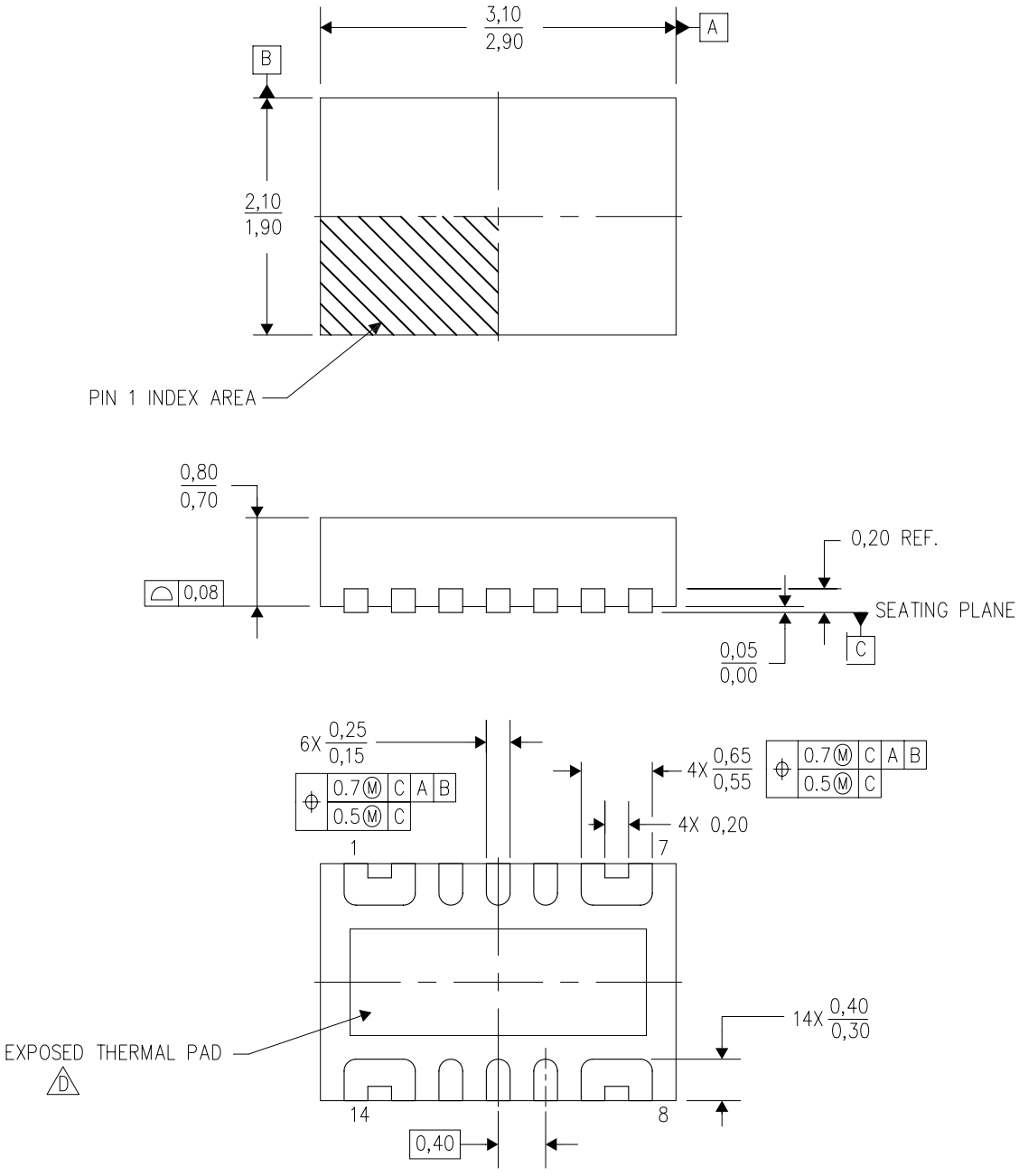
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22966DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22966DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22966DPUT	WSON	DPU	14	250	210.0	185.0	35.0

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. This package is Pb–free.

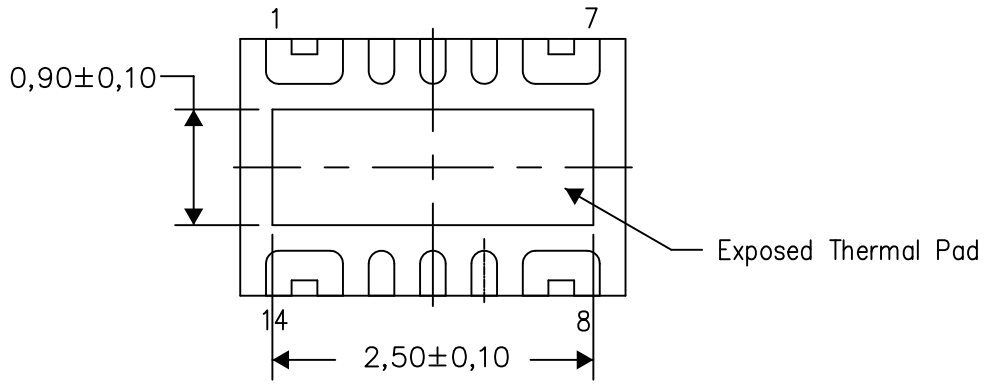
DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



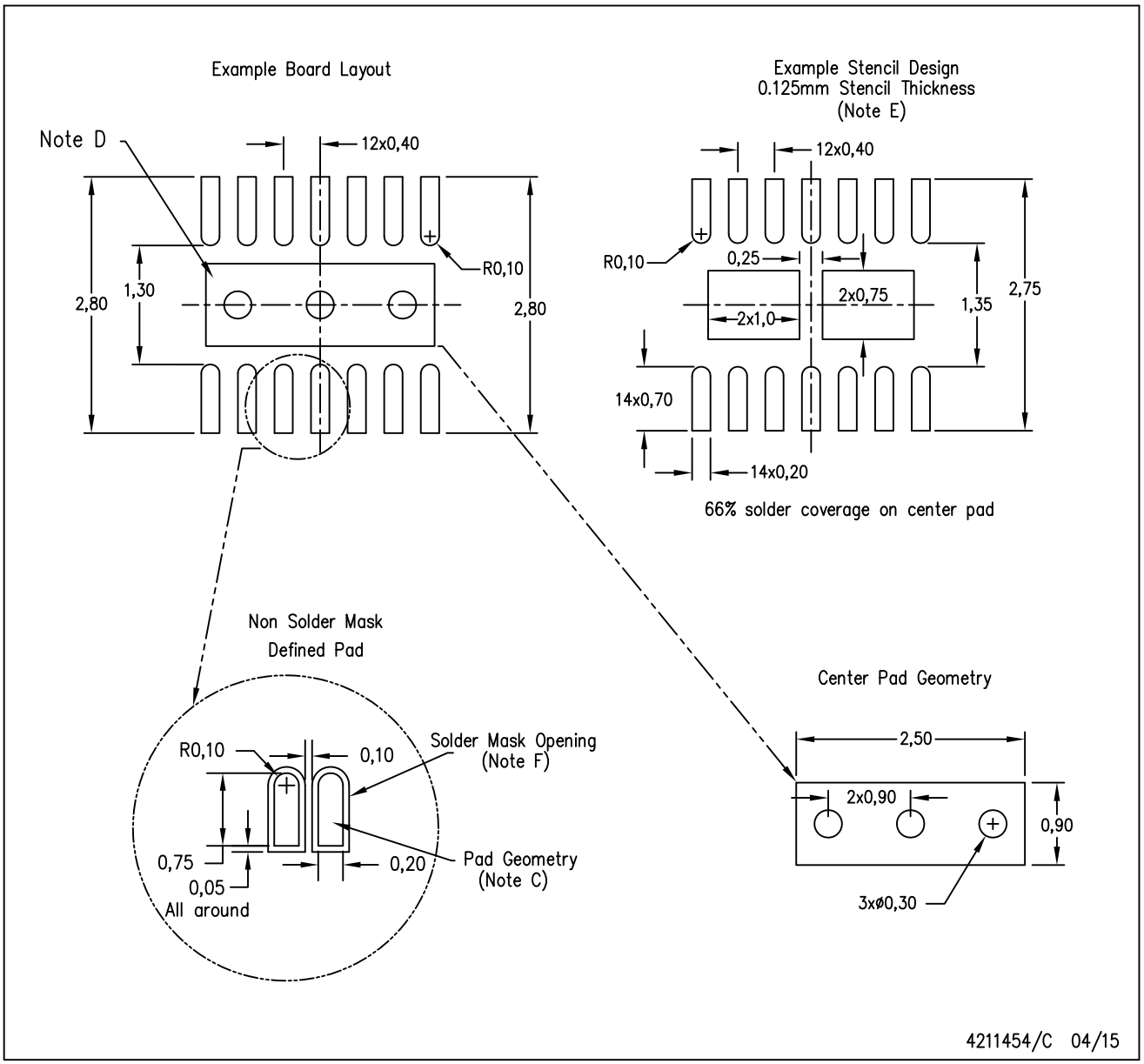
Bottom View

Exposed Thermal Pad Dimensions

4211395/C 04/15

NOTE: All linear dimensions are in millimeters

DPU (R–PWSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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