

PIC18F85J11 Family Silicon Errata and Data Sheet Clarification

The PIC18F85J11 family devices that you have received conform functionally to the current Device Data Sheet (DS39774D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC18F85J11 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A6).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICKit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICKit™ 3.
2. From the main menu in MPLAB IDE, select Configure>Select Device, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (Debugger>Select Tool).
4. Perform a "Connect" operation to the device (Debugger>Connect). Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F85J11 family silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾			
		A3	A4	A5	A6
PIC18F63J11	390Xh	3h	4h	5h	6h
PIC18F64J11	392Xh				
PIC18F65J11	396Xh				
PIC18F83J11	398Xh				
PIC18F84J11	39AXh				
PIC18F85J11	39EXh				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC18F6XJXX/8XJXX Family Flash Microcontroller Programming Specification" (DS39644) for detailed information on Device and Revision IDs for your specific device.

PIC18F85J11 FAMILY

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾				
				A3	A4	A5	A6	
Reset	BOR	1.	BOR and POR may occur at the same time.	X	X	X	X	
MSSP	I ² C™ Slave	2.	If the SSPBUF register is not read within a window after the SSPIF interrupt, the module may not receive the correct data.	X	X	X	X	
MSSP	I ² C Master	3.	The clock may get narrow if the slave performs a clock stretch.	X	X	X	X	
EUSART	Enable/Disable	4.	If interrupts are enabled, disabling and re-enabling the module requires a 2 T _{CY} delay.	X	X	X	X	
Timer1/3	Counter	5.	Timer1/3 in Internal Counter mode will not increment in the instruction count where the timer is disabled.	X	X	X	X	
Timer1/3	Prescale	6.	Timer1/3 prescale will take an additional count to switch when prescaler value is changed.	X	X	X	X	
EUSART	Synchronous mode	7.	The TRMT bit may not indicate when the TSR register is empty.	X	X	X	X	
POR	Two-Speed Start-up/Fail-Safe Clock Monitor	8.	The Two-Speed Start-up (IESO, CONFIG2L<7>) and the Fail-Safe Clock Monitor (FCMEN, CONFIG2L<6>) bits will not work correctly.	X	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A6).

1. Module: Reset

When a Brown-out Reset (BOR) occurs and the BOR bit is reset, the Power-on Reset (POR) bit may also be reset. The resulting state matches that of the RCON register following a Power-on Reset event.

Consequently, an application may not be able to detect whether a BOR or POR event has occurred.

Work around

None.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

2. Module: MSSP (I²C™ Slave)

In extremely rare cases, when configured for I²C™ slave reception, the MSSP module may not receive the correct data. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature. This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPxIF bit is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

3. Module: MSSP (I²C™ Master)

When in I²C Master mode, if the slave performs clock stretching, the first clock pulse after the slave releases the SCL line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/reception.

Work around

The clock pulse will be the normal width if the slave does not perform clock stretching.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

4. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTAx<7> = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed

Work around

Add a 2 Tcy delay after re-enabling the EUSART.

1. Disable receive interrupts (RCxIE bit, PIRx<5> = 0).
2. Disable the EUSART (RCSTA<7> = 0).
3. Re-enable the EUSART (RCSTA<7> = 1).
4. Re-enable receive interrupts (PIRx<5> = 1). (This is the first Tcy delay.)
5. Execute a NOP instruction. (This is the second Tcy delay.)

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

PIC18F85J11 FAMILY

5. Module: Timer 1/3

When either Timer1 or Timer3 is configured for the internal clock source ($F_{osc}/4$, $TxCON<1>$ ($TMRxCS$) = 0) and in the 8/16-Bit Counter mode ($TxCON<7>$ (RD16) = 0 or 1), $TMRxH$ and $TMRxL$ will not increment on the instruction that turns off the counter ($TxCON<0>$ ($TMRxON$) = 0).

Work around

None.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

6. Module: Timer 1/3

When either Timer1 or Timer3 is in the 8/16-Bit Counter mode ($TxCON<7>$ (RD16) = 0 or 1), incrementing the prescale value ($TxCON<5:4>$ ($TXCKPS<1:0>$)) will take an additional count at the previous value before the prescale value is updated.

For example, changing the prescale value from 1:4 to 1:8 will occur four instruction cycles after the execution of the instruction to update the prescaler.

Work around

None.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

7. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In Synchronous Slave Transmission mode, the TRMT bit ($TXSTAx<1>$) may not indicate when the TSR register is empty.

Work around

Instead of polling the TRMT bit to determine the status of the EUSART, poll the $TXxIF$ flag ($PIRx<4>$) to determine when new data can be written to the TXREG register.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

8. Module: POR

The Two-Speed Start-up (IESO, $CONFIG2L<7>$) and the Fail-Safe Clock Monitor (FCMEN, $CONFIG2L<6>$) bits will not work correctly. The Two-Speed Start-up and Fail-Safe Clock Monitor are always enabled after initial power-up.

The Two-Speed Start-up and the Fail-Safe Clock Monitor will work correctly after a WDT/MCLR/Reset instruction, RESET, and will also work correctly after a wake-up from Sleep.

Work around

None.

Affected Silicon Revisions

A3	A4	A5	A6				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39774D):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 “Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)” has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin, ENVREG, must always be connected directly to either a supply voltage or to ground. Tying ENVREG to VDD enables the regulator, while tying it to ground disables the regulator. Refer to **Section 23.3.2 “On-Chip Regulator and BOR”** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR ($< 5\Omega$) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 μF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in [Table 2-1](#). Capacitors with equivalent specifications can be used.

Designers may use [Figure 2-3](#) to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 26.0 “Electrical Characteristics”** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 26.0 “Electrical Characteristics”** for information on VDD and VDDCORE.

Note that the “LF” versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP

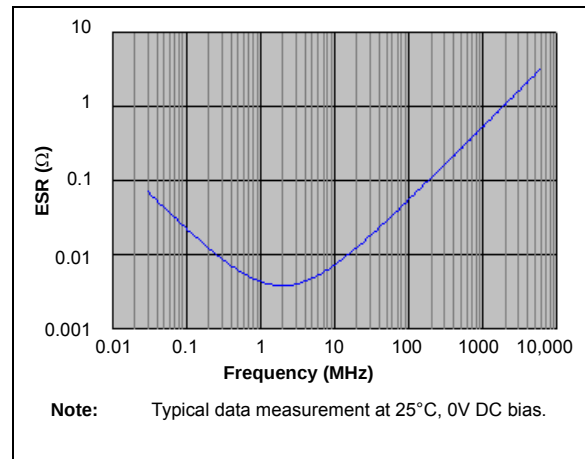


TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 μF	$\pm 10\%$	16V	-55 to 125°C
TDK	C3216X5R1C106K	10 μF	$\pm 10\%$	16V	-55 to 85°C
Panasonic	ECJ-3YX1C106K	10 μF	$\pm 10\%$	16V	-55 to 125°C
Panasonic	ECJ-4YB1C106K	10 μF	$\pm 10\%$	16V	-55 to 85°C
Murata	GRM32DR71C106KA01L	10 μF	$\pm 10\%$	16V	-55 to 125°C
Murata	GRM31CR61C106KC31L	10 μF	$\pm 10\%$	16V	-55 to 85°C

PIC18F85J11 FAMILY

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the VDDCORE voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

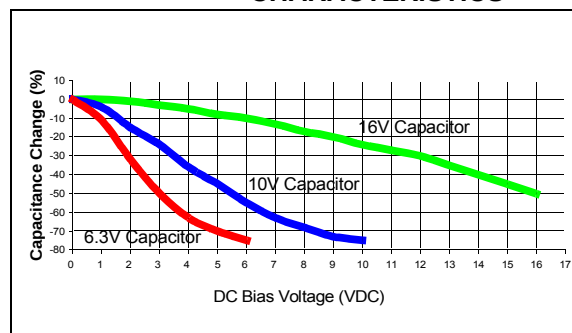
Typical low cost, 10 μ F ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as $\pm 10\%$ to $\pm 20\%$ (X5R and X7R), or $-20\%/+80\%$ (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: $\pm 15\%$ over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of $+22\%/-82\%$. Due to the extreme temperature tolerance, a 10 μ F nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum VDDCORE voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the Vddcore regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for X7R type and Y5V type capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the VDDCORE voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V VDDCORE voltage. Suggested capacitors are shown in Table 2-1.

PIC18F85J11 FAMILY

2. Module: Electrical Characteristics

Changes shown in bold have been made to the D005 parameter in [Section 26.1 “DC Characteristics: Supply Voltage PIC18F85J11 Family \(Industrial\)”](#). The updated table is shown below:

26.1 DC Characteristics: Supply Voltage PIC18F85J11 Family (Industrial)

PIC18F85J90 Family (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D001	VDD	Supply Voltage	VDDCORE 2.0	— —	3.6 3.6	V V	ENVREG tied to Vss ENVREG tied to VDD
D001B	VDDCORE	External Supply for Microcontroller Core	2.0	—	2.70	V	ENVREG tied to Vss
D001C	AVDD	Analog Supply Voltage	VDD – 0.3	—	VDD + 0.3	V	
D001D	AVSS	Analog Ground Potential	Vss – 0.3	—	Vss + 0.3	V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5	—	—	V	
D003	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	—	—	0.7	V	See Section 5.3 “Power-on Reset (POR)” for details
D004	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	See Section 5.3 “Power-on Reset (POR)” for details
D005	VBOR	Brown-out Reset Voltage	1.75⁽²⁾	2.0	2.4	V	

Note 1: This is the limit to which VDDCORE can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When the BOR is enabled, the part will continue to operate until the BOR occurs. This is valid although VDD may be below the minimum voltage.

3. Module: I/O Ports

In [Section 11.6 “PORTE, TRISE and LATE Registers”](#), the following changes are made. The changes are shown in bold text.

11.6 PORTE, TRISE and LATE Registers

PORTE is a 7-bit wide, bidirectional port. The corresponding Data Direction and Data Latch registers are TRISE and LATE. **All pins on PORTE are digital only. PORTE<7:3> can tolerate voltages up to 5.5V and PORTE<2:0> are only VDD level tolerant.**

4. Module: I/O Ports

In [Section 11.8 “PORTG, TRISG and LATG Registers”](#), the following changes are made. The changes are shown in bold text.

11.8 PORTG, TRISG and LATG Registers

PORTG is a 5-bit wide, bidirectional port. The corresponding Data Direction and Data Latch registers are TRISG and LATG. **All pins on PORTG are digital only. PORTG<4> and PORTG<1> can tolerate voltages up to 5.5V. PORTG<3:2> and PORTG<0> are VDD level tolerant only.**

PIC18F85J11 FAMILY

APPENDIX A: DOCUMENT REVISION HISTORY

Rev D Document (12/2010)

Initial release of the combined, silicon errata/data sheet clarification document. New data sheet clarifications 1 (Guidelines for Getting Started with PIC18FJ Microcontrollers), 2 (Electrical Characteristics) and 3-5 (I/O Ports).

This document replaces these errata documents:

- DS80318A, "*PIC18F85J11 Family Rev. A3 Silicon Errata*"
- DS80423A, "*PIC18F85J11 Family Rev. A4 Silicon Errata*"
- DS80383C, "*PIC18F85J11 Family Data Sheet Errata*"

Rev E Document (9/2011)

Updated data sheet clarification 2 (Electrical Characteristics).

Rev F Document (10/2011)

Added new silicon issue 8 (POR).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2011, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-61341-705-8

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2009 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/02/11