TPD4E6B06 4-Channel Bidirectional Low Capacitance ESD Protection Device With 15-kV Contact and Ultra-Low Clamping Voltage

1 Features

- IEC 61000-4-2 Level 4
  - ±15-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-5 (Surge): 3 A (8/20 µs)
- IO Capacitance: 4.8 pF (Typical)
- R_{DYN}: 0.75 Ω (Typical)
- DC Breakdown Voltage: ±6 V (Minimum)
- Ultra Low Leakage Current: 100 nA (Maximum)
- Clamping Voltage: 10 V (Maximum at I_{PP} = 1 A)
- Industrial Temperature Range: –40°C to +125°C
- Space Saving DPW Package (0.8 mm × 0.8 mm)

2 Applications

- Audio Lines
  - Microphone
  - Earphone
  - Speakerphone
- SD Interface
- SIM Interface
- Mobile Keyboard or Other Buttons
- Cell Phones
- eBook
- Portable Media Players
- Digital Camera
- Tablet PC
- Wearables

3 Description

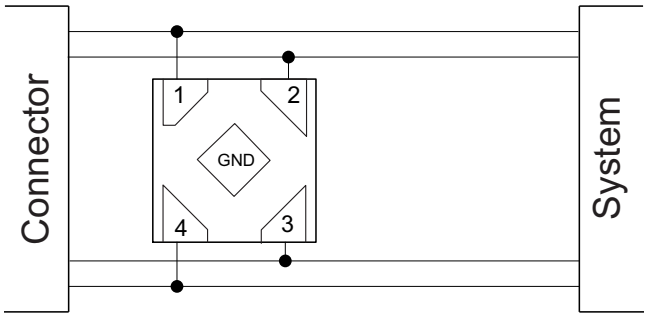
The TPD4E6B06 is a four channel electrostatic discharge (ESD) protection device in an ultra small DPW package. It is the industry's smallest 4-channel transient voltage suppressor (TVS) diode with a 0.48-mm pitch. This larger pitch helps save on printed-circuit board (PCB) manufacturing costs. The device provides IEC61000-4-2 compliance up to 15-kV contact discharge. It has an ESD clamp circuit with back-to-back diodes for bipolar-bidirectional signal support. The 4.8-pF (typical) line capacitance is suitable for a wide range of applications supporting data rates up to 700 MHz.

Device Information(1)

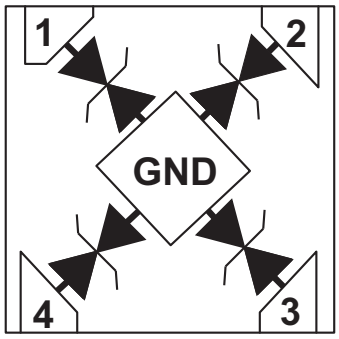
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E6B06	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Pinout



0.8 mm x 0.8mm X2SON Package
(Bottom View)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2017) to Revision C — **Page**

- Added "Power Supply Recommendations" section ... 12

Changes from Revision A (December 2015) to Revision B — **Page**

- Changed the value of R_{DYN} from 0.75 and 0.65 to 0.45 and 0.42 respectively, in the *Electrical Characteristics* table ... 5

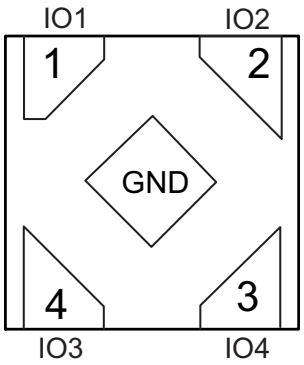
Changes from Original (May 2014) to Revision A — **Page**

- Updated the *Handling Ratings* table into an *ESD Ratings* table and moved T_{stg} to the *Absolute Maximum Ratings* table ... 4
- Added new note to *Absolute Maximum Ratings* table ... 4
- Added frequency test condition to *IO capacitance* in the *Electrical Characteristics* table ... 5
- Added *Community Resources* ... 14

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5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO	NAME		
1	IO1	IO	ESD protected line
2	IO2	IO	ESD protected line
3	IO3	IO	ESD protected line
4	IO4	IO	ESD protected line
5	GND	—	Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Current (t_p – 8/20 µs)(4)		3	A
	IEC 61000-4-5 Power (t_p – 8/20 µs)(4)		40	W
Operating temperature		–40	125	°C
Storage temperature	T_{stg}	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) Measured at 25°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPD4E6B06 DPW (X2SON) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	245.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	245.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = –40°C to +125°C (unless otherwise specified)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA	–5.5		5.5	V
V_{BRF}	Break-down voltage	$I_{IO\ to\ GND}$ = 1 mA	6			V
V_{BRR}	Break-down voltage	$I_{GND\ to\ IO}$ = 1 mA	6			V
I_{LEAK}	Leakage current	V_{IO} = 5 V			100	nA
V_{CLAMP}	Clamp voltage with ESD strike	I = 1 A, IO to GND, 8/20 µs(1)		10		V
		I = 5 A, IO to GND, 8/20 µs(1)		13		V
		I = 1 A, IO to GND, 8/20 µss(1)		9		V
		I = 5 A, IO to GND, 8/20 µs(1)		13		V
R_{DYN}	Dynamic resistance	Any IO to GND pin(2)		0.45		Ω
		GND to any IO pin(2)		0.42		Ω
C_L	IO capacitance	V_{IO} = 2.5 V; f = 10 MHz		4.8	7	pF

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.
(2) Extraction of RDYN using least squares fit of TLP characteristics between I = 10 A and I = 20 A.

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6.6 Typical Characteristics

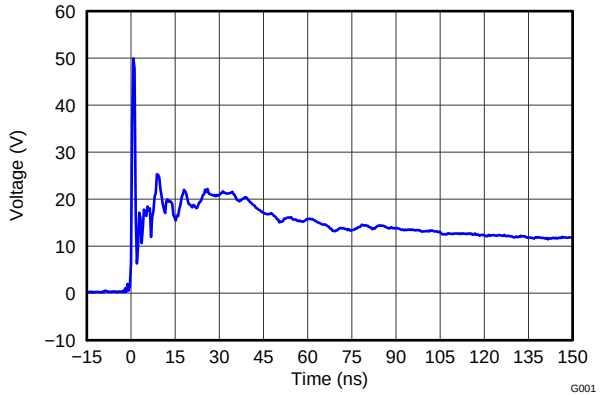


Figure 1. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

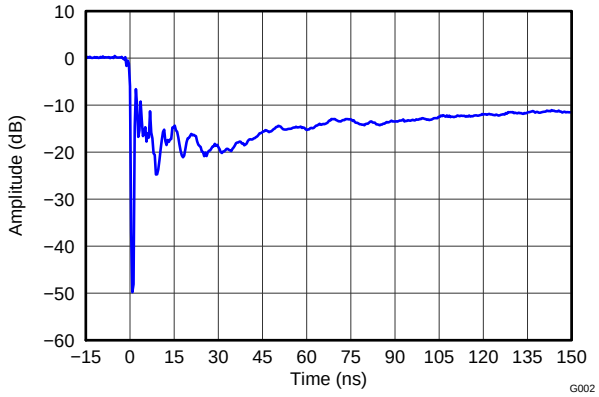


Figure 2. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

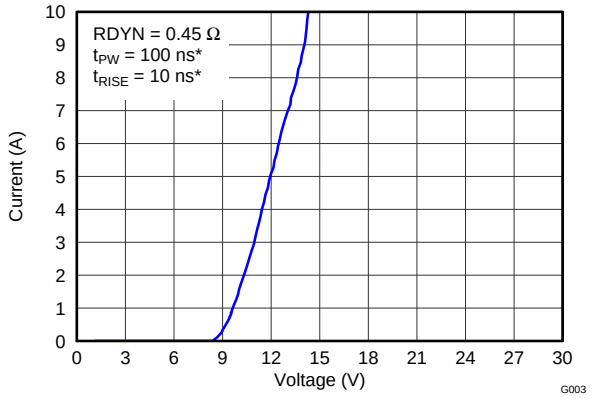


Figure 3. TLP, t_{PW} = 100 ns, t_{RISE} = 10 ns, IO to GND

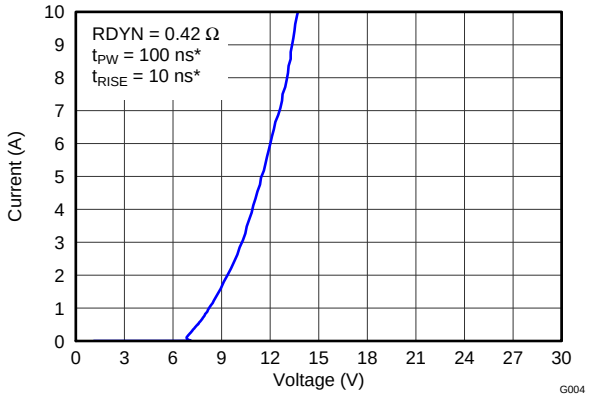


Figure 4. TLP, t_{PW} = 100 ns, t_{RISE} = 10 ns, GND to IO

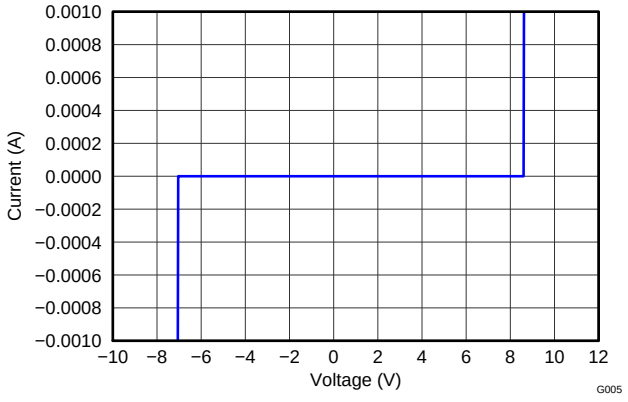


Figure 5. IV Curve

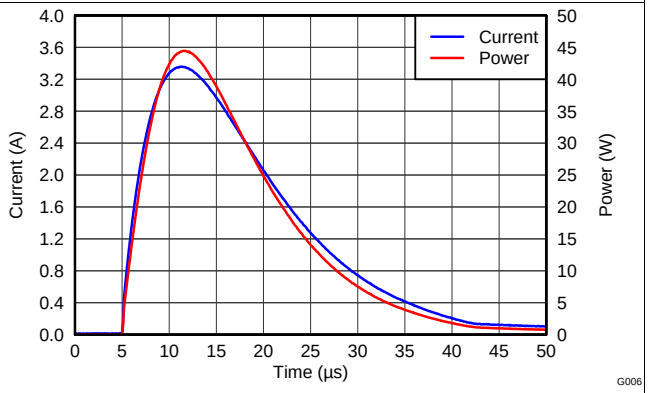


Figure 6. Surge Curves, IO to GND

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Typical Characteristics (continued)

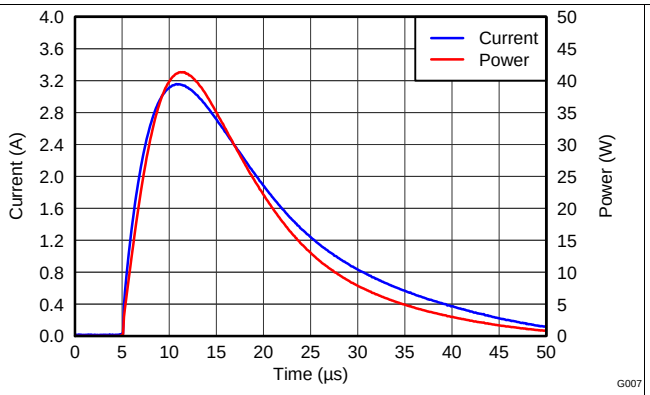


Figure 7. Surge Curves, GND to IO

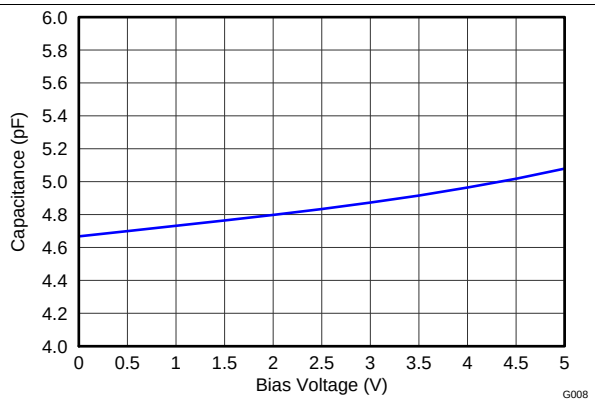


Figure 8. Capacitance

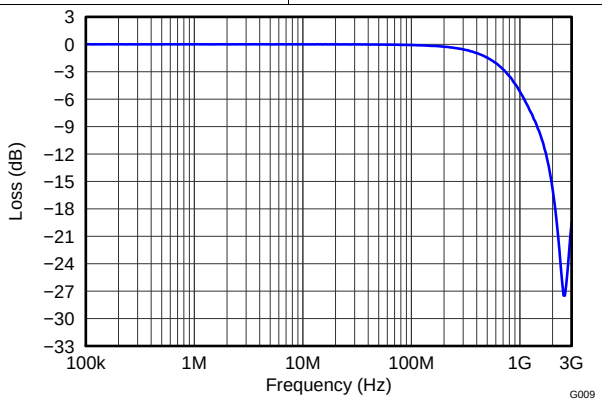


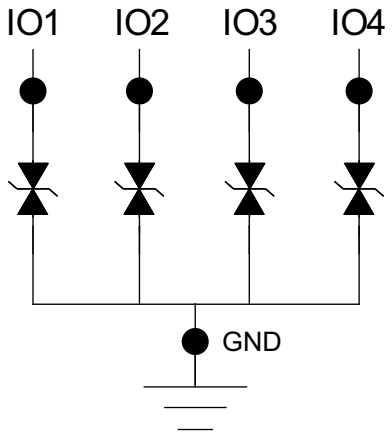
Figure 9. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E6B06 is a four channel ESD Protection device in an ultra small DPW package. It is the industry's smallest 4-CH ESD protection device with 0.48-mm pitch. This larger pitch helps save on PCB manufacturing costs. The device provides IEC61000-4-2 compliance up to 15-kV contact discharge. It has an ESD clamp circuit with back-to-back diodes for bipolar/bidirectional signal support. The 4.8-pF (Typical) line capacitance is suitable for a wide range of applications supporting frequencies up to 700 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 Level 2 ESD Protection

The IO pins can withstand ESD events up to ±15-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between any IO pin to ground is 4.8 pF (typical). This capacitance supports frequencies up to 700 MHz.

7.3.4 R_{DYN}

The low R_{DYN} of 0.75 Ω (typical) allows for lower clamping voltages.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of any IO pin is a minimum of ±6 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±5.5 V (minimum).

7.3.6 Ultra-Low Leakage Current

The IO pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of 2.5 V.

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Feature Description (continued)

7.3.7 Clamping Voltage

The IO pins feature an ESD clamp capable of clamping the voltage to 10 V (IO to GND) or 9 V (GND to IO) of IEC61000-4-5 surge when I_{PP} = 1 A.

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Space Saving DPW Package

The small 0.8 mm × 0.8 mm package size saves board space and makes it easy to add ESD protection.

7.4 Device Functional Modes

The TPD4E6B06 is a passive integrated circuit that triggers when voltages are above V_{BRF} or V_{BRR}. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of the TPD4E6B06 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E6B06 is a diode array type TVS. These low capacitance types of TVSs are typically used to provide a path to ground for dissipating ESD events on hi speed signal lines between a human interface connector and a system. During high voltage ESD strikes, the device clamps to a safe voltage level to protect the system.

The typical application of the TPD4E6B06 is to be placed in between the connector and the system. The low capacitance of the TPD4E6B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

8.2 Typical Application

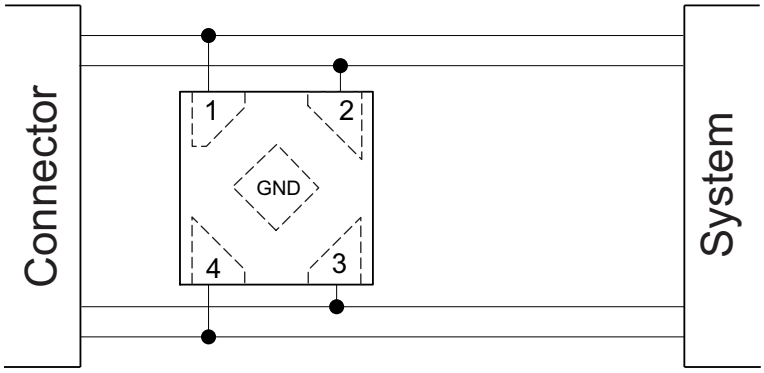


Figure 10. Protecting Data Lines

8.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on data lines	–5.5 V to 5.5 V
Operating frequency	Up to 700 MHz

8.2.2 Detailed Design Procedure

The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range

The TPD4E6B06 has 4 protection channels for signal lines. Any I/O supports a signal range of –5.5 V to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E6B06 has 4.8 pF of capacitance (Typical), supporting up to 700 MHz frequencies.

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8.2.3 Application Curve

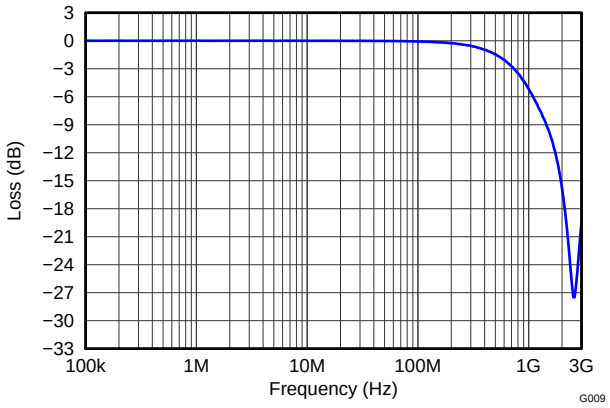


Figure 11. Insertion Loss (Any IO to GND)

9 Power Supply Recommendations

The TPD4E6B06 is a passive TVS diode-based ESD protection device, so there is no need to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

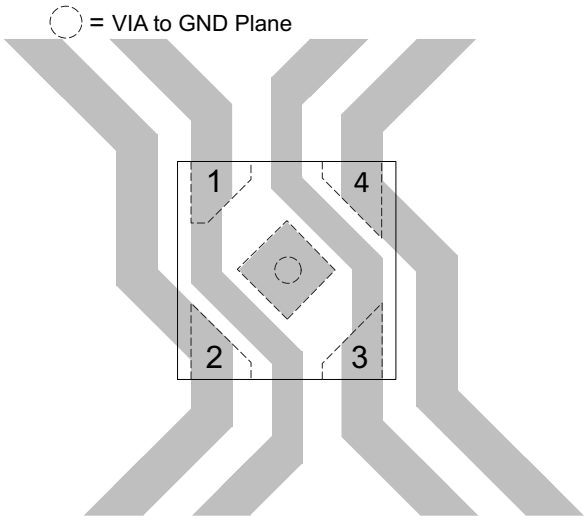


Figure 12. Single Layer Routing

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Layout Examples (continued)

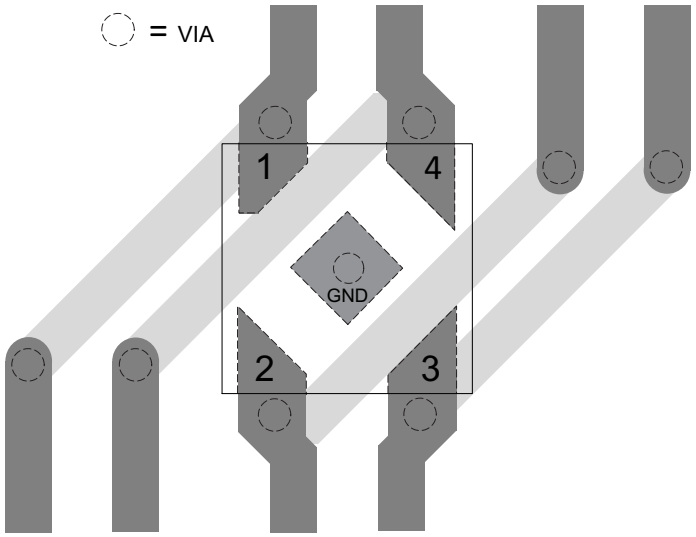


Figure 13. Double Layer Routing

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Reading and Understanding an ESD Protection Datasheet*
- *ESD Layout Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

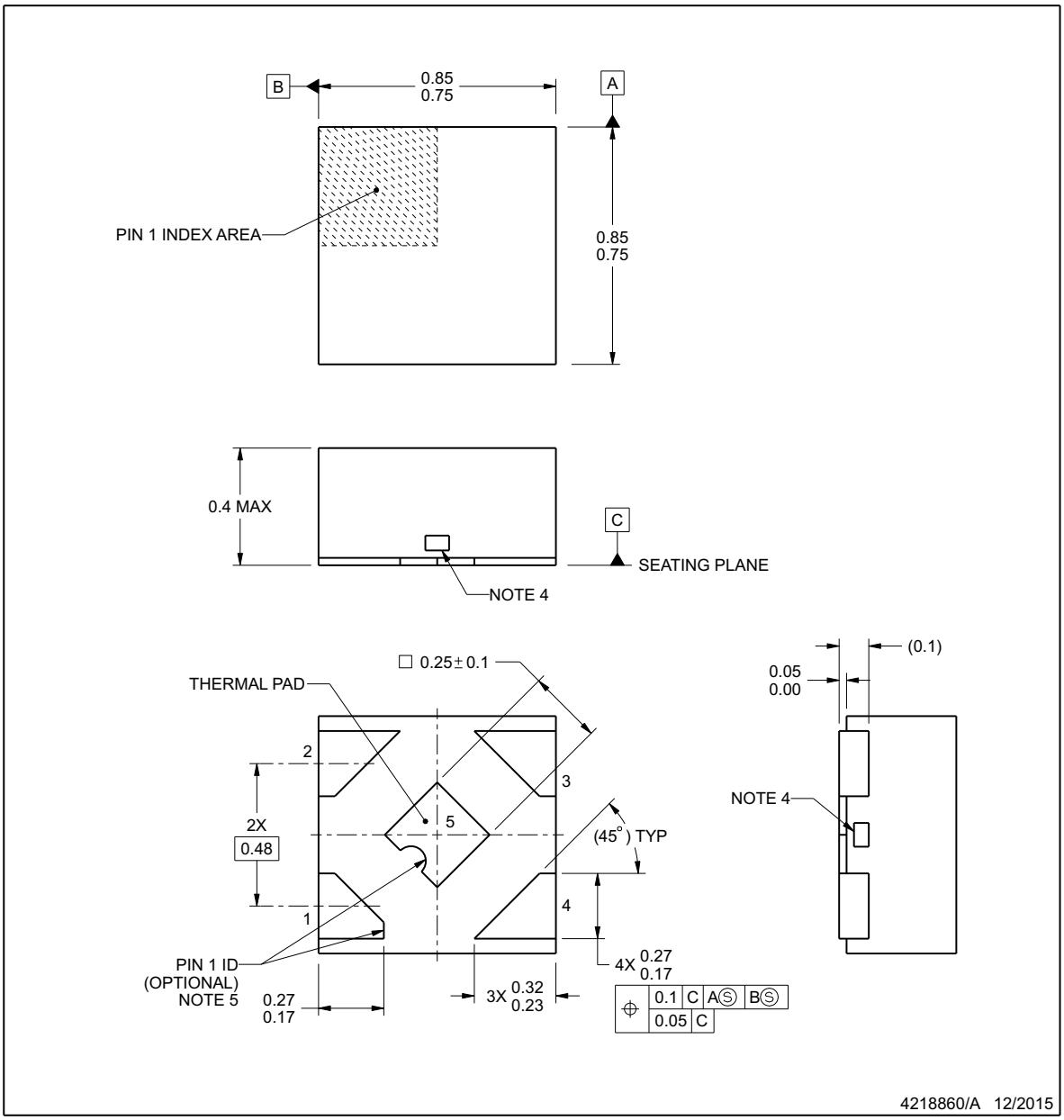
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PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

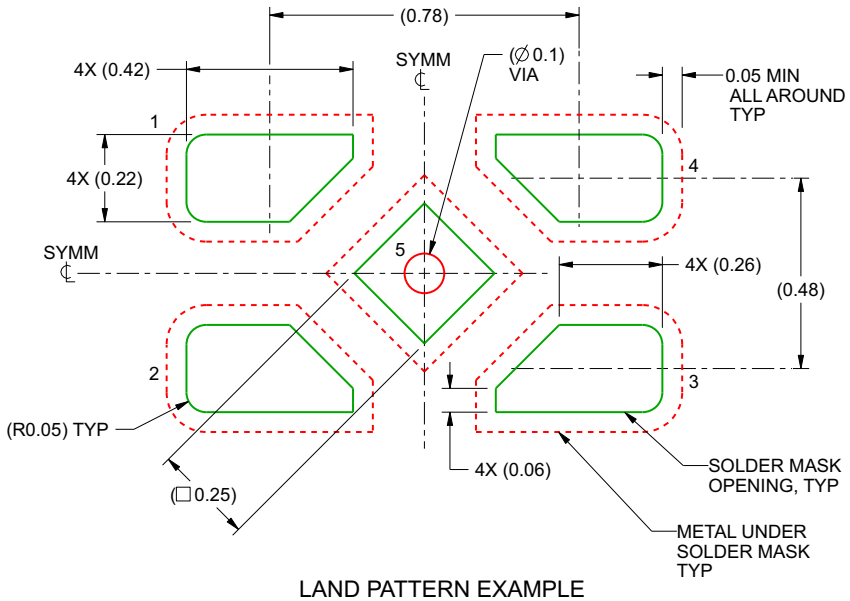
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EXAMPLE BOARD LAYOUT

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4218860/A 12/2015

NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

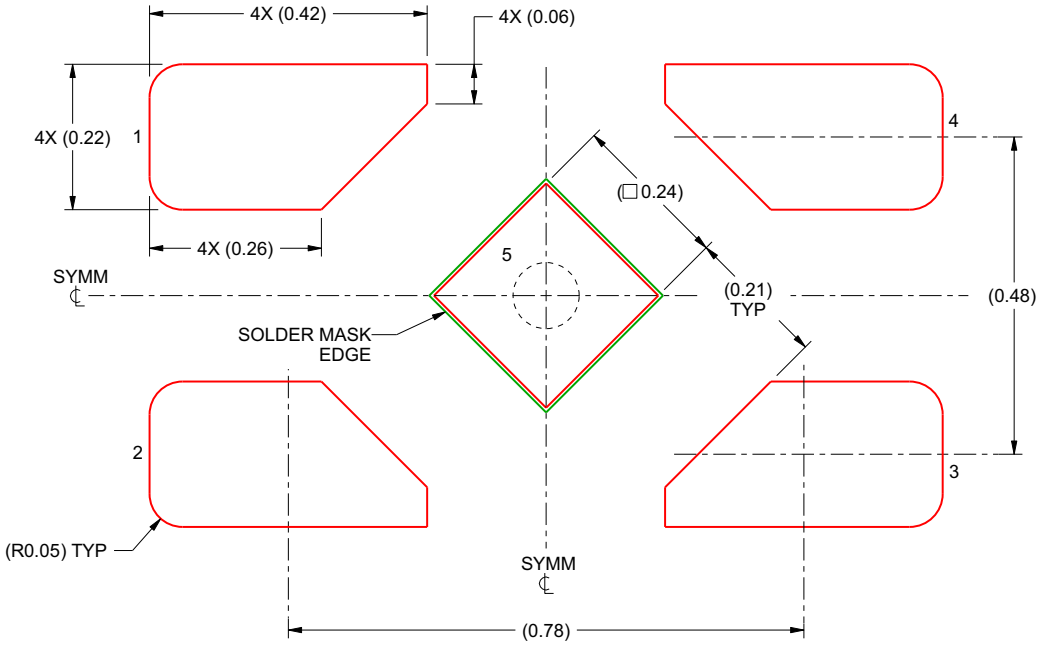
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EXAMPLE STENCIL DESIGN

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4218860/A 12/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E6B06DPWR	ACTIVE	X2SON	DPW	4	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1, B5) B2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

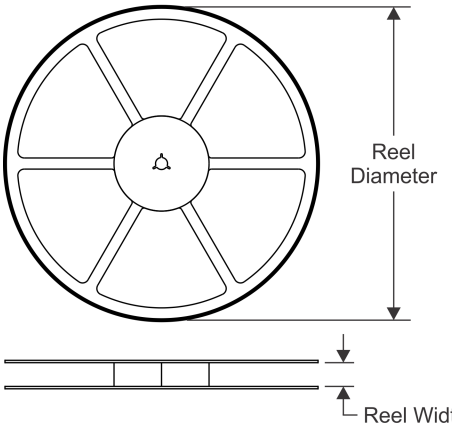
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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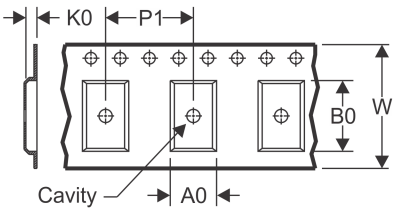
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

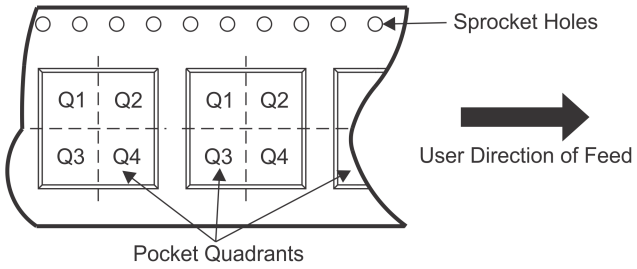


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

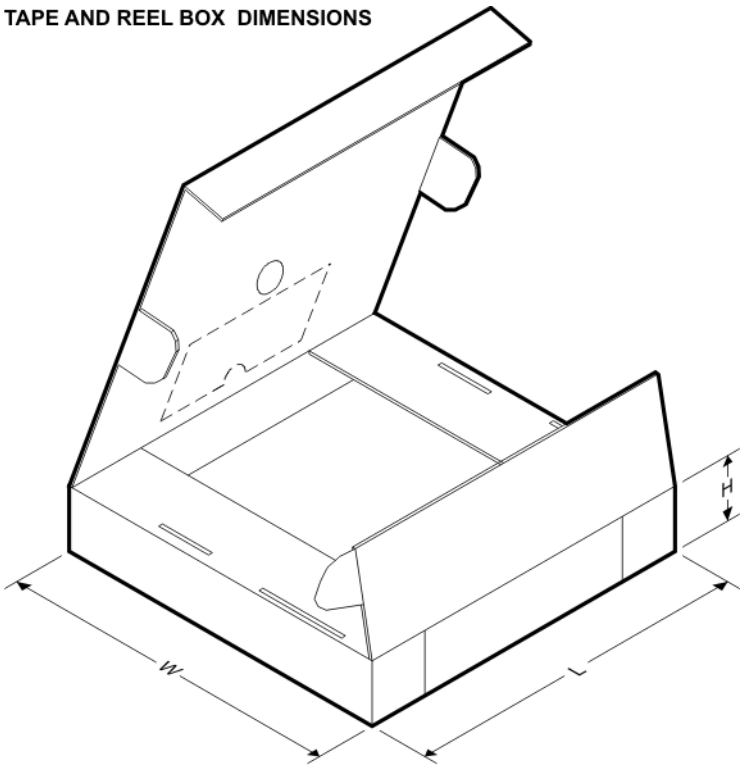
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E6B06DPWR	X2SON	DPW	4	3000	180.0	9.5	0.94	0.94	0.5	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E6B06DPWR	X2SON	DPW	4	3000	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPW 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

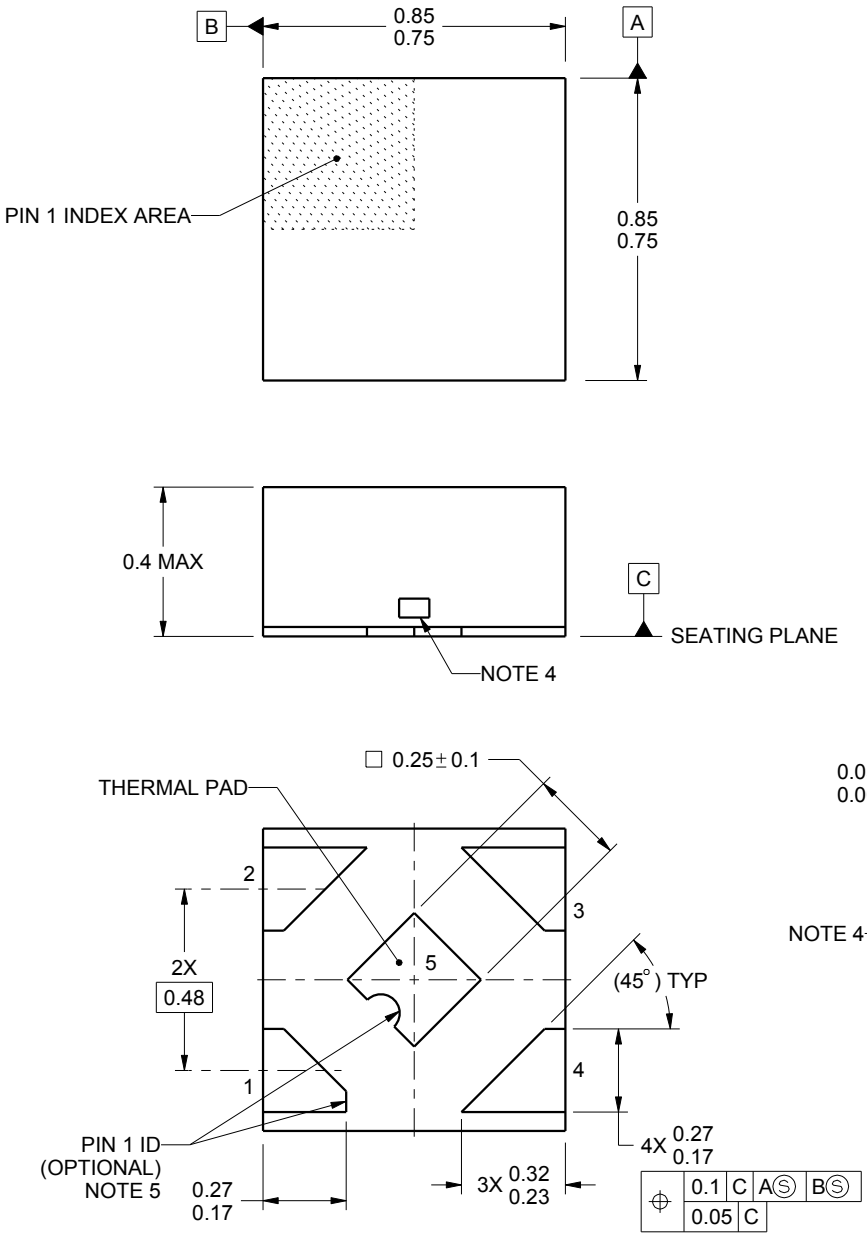
4211218-2/D

PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

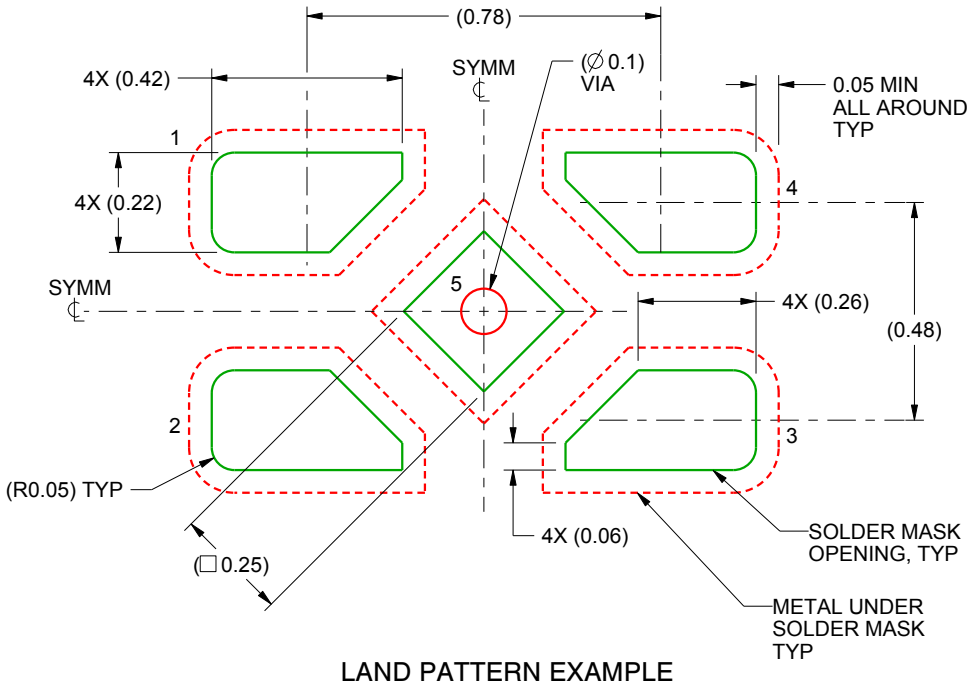
PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

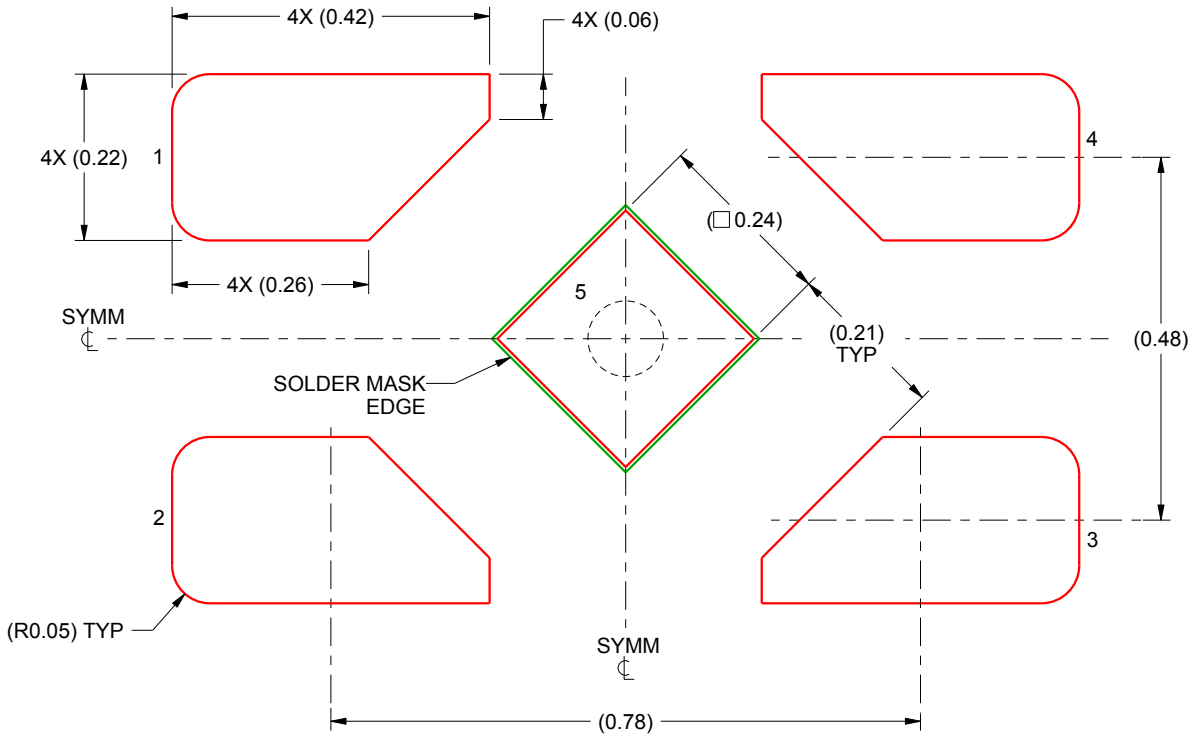


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

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NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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