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Power System Basis Chip with High Speed CAN transceiver

33907_08

POWER SYSTEM BASIS CHIP



AE SUFFIX (PB-FREE)
98ASA00173D
48-PIN LQFP-EP

The 33907_8 devices are multi-output, power supply, integrated circuit, including HSCAN transceiver, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low power mode are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over wide input voltages and output current ranges.

The 33907_8 includes enhanced safety features, with multiple fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level.

The built-in enhanced high speed CAN interface fulfills the ISO11898-2 and -5 standards. Local and bus failure diagnostics, protection, and fail-safe operation mode are provided. This device is powered by SMARTMOS technology.

Features

- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost or standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply, 1.2 V or 3.3 V delivering up to 1.5 A
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA). 5.0 V or 3.3 V
- Linear voltage regulator dedicated to auxiliary functions, or to a sensor supply (VCCA tracker or independent 5.0 V / 3.3 V)
- Multiple wake-up sources in low power mode: CAN and/or IOs
- Battery voltage sensing & MUX output terminal
- Enhanced safety block associated with fail-safe outputs
- Six configurable I/Os

Applications

- Electrical power steering
- Engine management
- Battery management
- Active suspension
- Gear box
- Transmission
- Electrical Vehicle (EV), Hybrid Electrical Vehicle (HEV)
- Advanced driver assistance systems

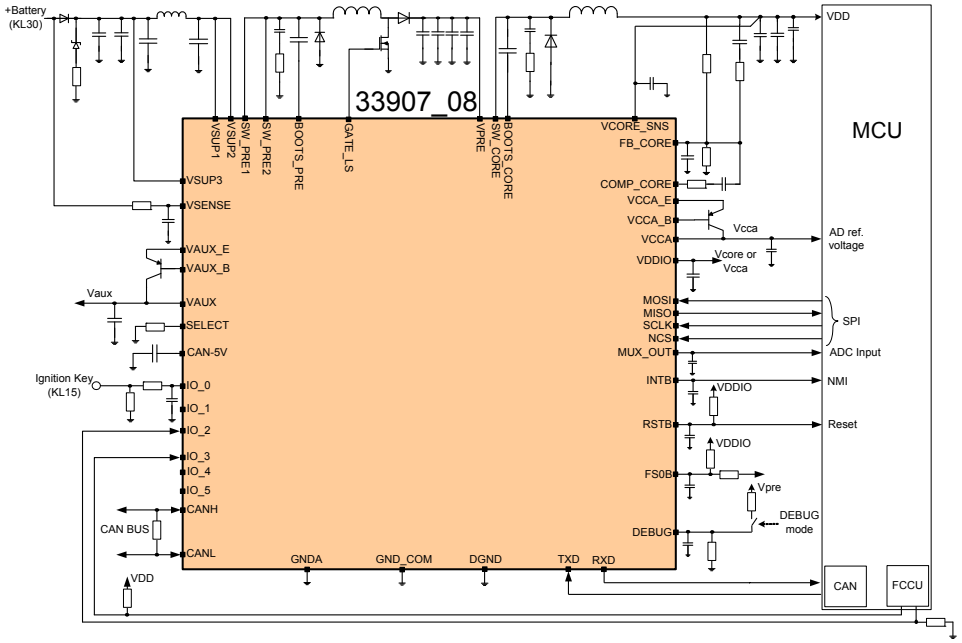


Figure 1. Simplified Application Diagram - Buck Boost Configuration

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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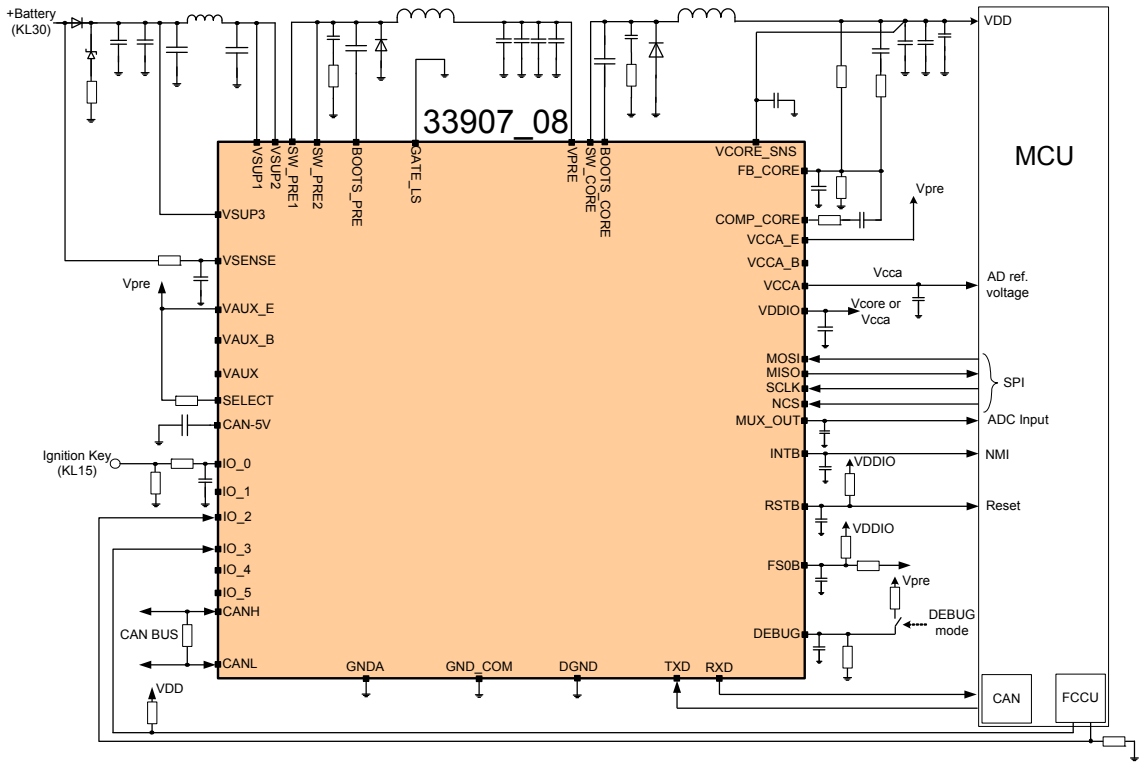


Figure 2. Simplified Application Diagram - Buck Configuration, V_{AUX} not used, V_{CCA} = 100 mA

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1 Orderable Parts

Table 1. Orderable Part Variations

Part Number [1]	V_{CORE}	Temperature (T_A)	Package
MC33907AE	VCORE Output Current Capability in Normal Mode Page 12	-40 to 125 °C	48-pin LQFP exposed pad
MC33908AE			

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

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2 Internal Block Diagram

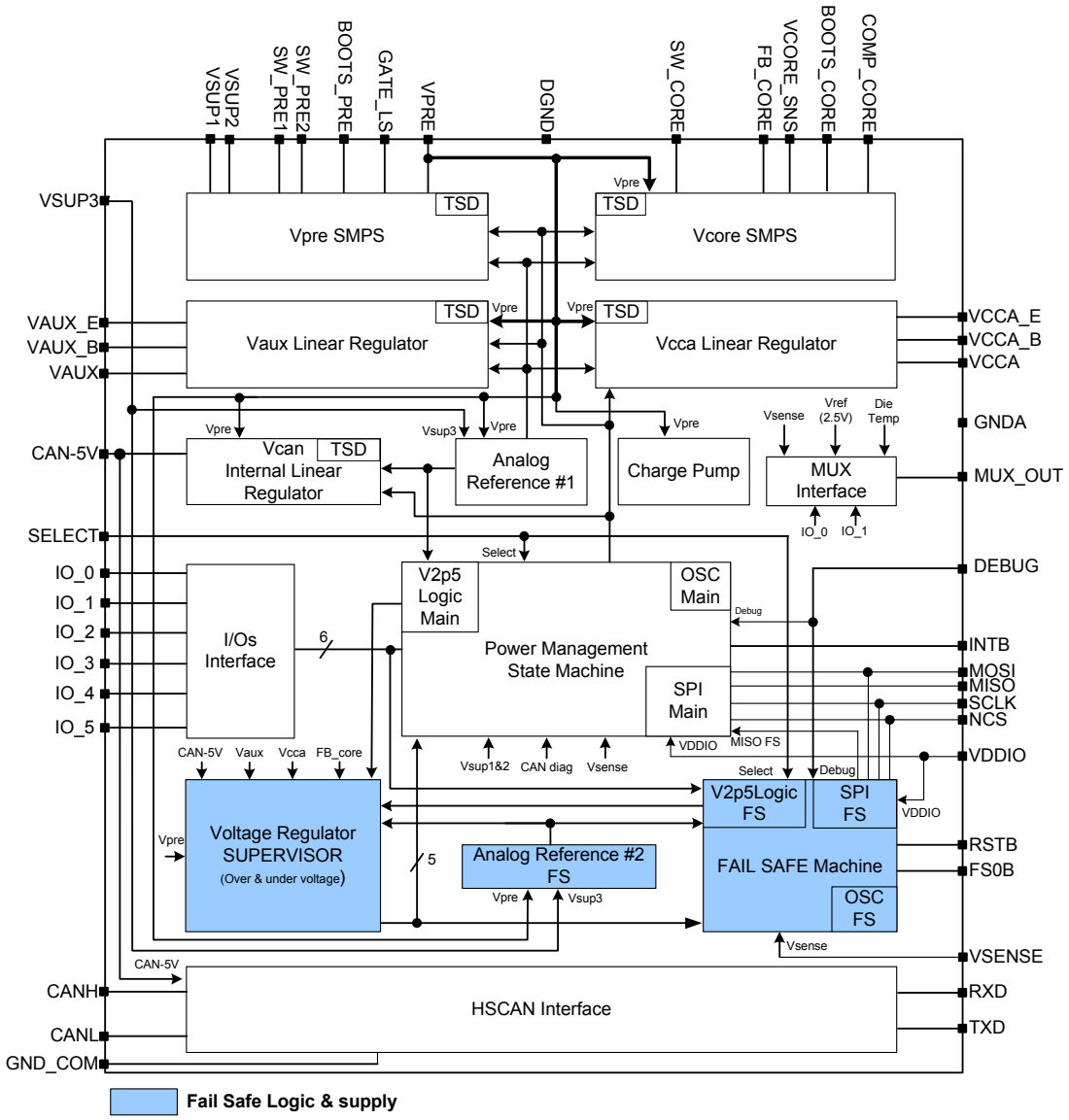


Figure 3. MC33907_08 Simplified Internal Block Diagram

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3 Pin connections

3.1 Pinout Diagram for 33907_8

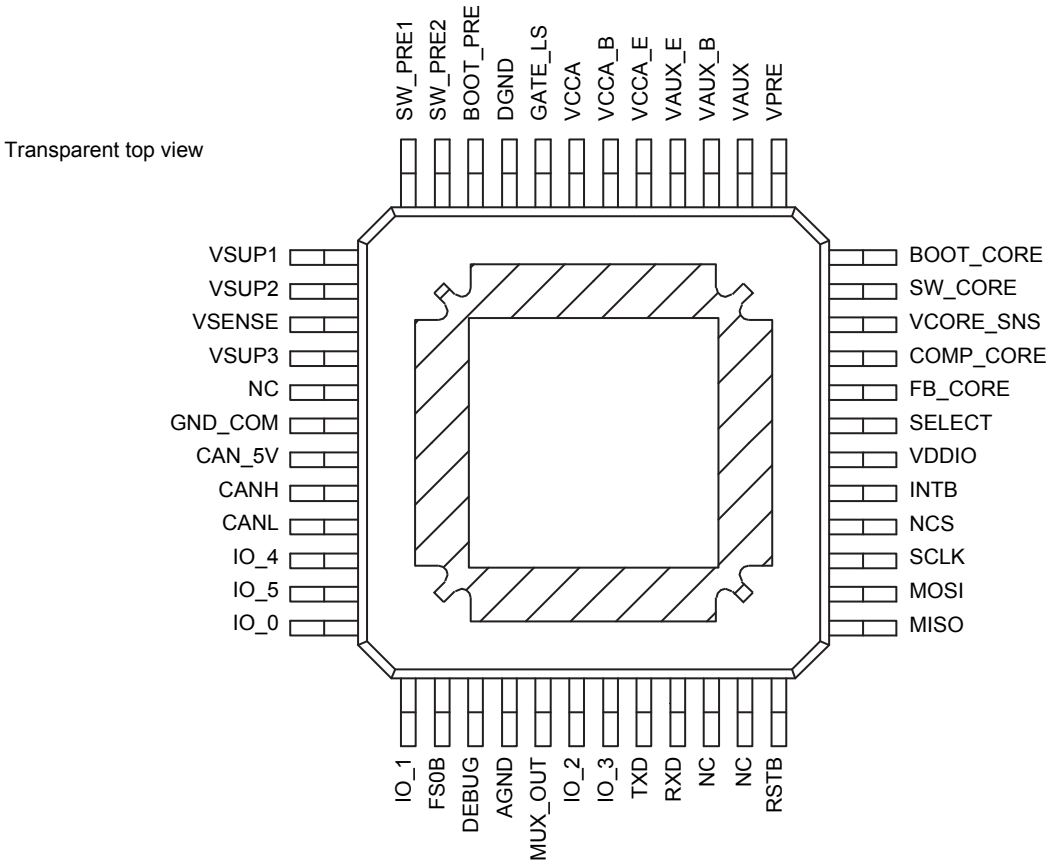


Figure 4. 33907_8 Pinout

3.2 Pin Definitions

A functional description of each pin can be found in the functional pin description section beginning on page 25.

Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Also protected by the external reverse battery protection diode used for VSUP1
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Also protected by the external reverse battery protection diode used for VSUP1. Shall be connected between the reverse protection diode and the input PI filter.
5, 22, 23	NC	N/A	Not connected. Pins must be left open.

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Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
6	GND_COM	GROUND	Dedicated ground for CAN
7	CAN_5V	A_OUT	Output voltage for the embedded CAN interface
8	CANH	A_IN/OUT	HSCAN output High
9	CANL	A_IN/OUT	HSCAN output Low
10 11	IO_4:5	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition **Output gate driver:** Can drive a logic level low side NMOS transistor. Controlled by the SPI.
12 13	IO_0:1	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output terminal **Digital input:** Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition
14	FS0B	D_OUT	Output of the safety block (active low). The pin is asserted low at startup and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital INPUT**: Pin status can be read through the SPI. Can be used to monitor error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on a rising or falling edge, or on a transition.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the HSCAN bus
21	RXD	D_OUT	Receiver output which reports the state of the HSCAN bus to the MCU
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master Input Slave Output
26	MOSI	D_IN	SPI bus. Master Output Slave Input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	No Chip Select (Active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_IN	Compensation network. Output of the error amplifier.
34	VCORE_SNS	A_IN	Vcore output voltage sense
35	SW_CORE	A_IN	VCORE switching point
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive

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Table 2. 33907_8 Pin Definition

Pin	Pin Name	Type	Definition
37	VPRE	A_OUT	VPRE output voltage
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low side MOSFET gate drive for “Non-inverting Buck-boost” configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_IN	Second pre-regulator switching point
48	SW_PRE1	A_IN	Pre-regulator switching point

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4 General Product Characteristics

4.1 Maximum Ratings

Table 3. Maximum Ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit	Notes
ELECTRICAL RATINGS				
DC Voltage at Power Supply Pins	$V_{SUP1/2/3}$	-1.0 to 40	V	
DC voltage between VSUP1, 2, and VSUP3 ($V_{SUP1,2} > V_{SUP3}$)	$V_{SUP1/2/3}$	0.0 to 4.0	V	
DC Voltage at Battery Sense Pin	V_{SENSE}	-14 to 40	V	
DC Voltage at SW_PRE1 and SW_PRE2 Pins	$V_{SW}1, 2$	-1.0 to 40	V	
DC Voltage at VPRE Pin	V_{PRE}	-0.3 to 8	V	
DC Voltage at Gate_LS pin	V_{GATE_LS}	-0.3 to 8	V	
DC Voltage at BOOT_PRE pin	V_{BOOT_PRE}	-1.0 to 50	V	
DC Voltage at SW_CORE pin	V_{SW_CORE}	-1.0 to 8.0	V	
DC Voltage at VCORE_SNS pin	V_{CORE_SNS}	0.0 to 8.0	V	
DC Voltage at BOOT_CORE pin	V_{BOOT_CORE}	0.0 to 15	V	
DC Voltage at FB_CORE pin	V_{FB_CORE}	-0.3 to 2.5	V	
DC Voltage at COMP_CORE pin	V_{COMP_CORE}	-0.3 to 2.5	V	
DC Voltage at VAUX_E, VAUX_B pin	$V_{AUX_E,B}$	-0.3 to 40	V	
DC Voltage at VAUX pin	V_{AUX}	-2.0 to 40	V	
DC Voltage at VCCA_B, VCCA_E pin	$V_{CCA_B,E}$	-0.3 to 8.0	V	
DC Voltage at VCCA pin	V_{CCA}	-0.3 to 8.0	V	
DC Voltage at VDDIO	V_{DDIO}	-0.3 to 8.0	V	
DC Voltage at FS0B (with ext R mandatory)	V_{FS0}	-0.3 to 40	V	
DC Voltage at DEBUG	V_{DEBUG}	-0.3 to 40	V	
DC Voltage at IO_0:1; 4:5 (with ext R = 5.1 kΩ in series mandatory)	$V_{IO_0,1,4,5}$	-0.3 to 40	V	
DC Voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3	V_{DIG}	-0.3 to V_{DDIO}+0.3	V	
DC Voltage at SELECT	V_{SELECT}	-0.3 to 8.0	V	
DC Voltage on CANL, CANH	V_{BUS_CAN}	-27 to 40	V	
DC voltage on CAN_5 V	V_{CAN_5V}	-0.3 to 8.0	V	
IOs maximum current capability	$I_{_IO}$	-5.0 to 5.0	mA	

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Table 3. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit	Notes
ESD Voltage				
Human Body Model (JESD22/A114) - 100 pF, 1.5 kΩ				
• All pins	$V_{ESD-HBM1}$	±2.0	kV	
• VSUP1, VSUP2, VSUP3, VSENSE, IO_0:1, IO_4:5, FS0B , DEBUG	$V_{ESD-HBM2}$	±3.5	kV	
• VAUX versus AGND	$V_{ESD-HBM3}$	±4.0	kV	
• CANH, CANL	$V_{ESD-HBM4}$	±6.0	kV	
Charge Device Model (JESD22/C101):				
• All Pins	$V_{ESD-CDM1}$	±500	V	
• Corner Pins	$V_{ESD-CDM2}$	±750	V	
System level ESD (Gun Test)				
• VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B				
330 Ω / 150 pF Unpowered According to IEC61000-4-2:	$V_{ESD-GUN1}$	±8.0	kV	
330 Ω / 150 pF Unpowered According to OEM LIN, CAN, FLexray Conformance	$V_{ESD-GUN2}$	±8.0	kV	
2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	$V_{ESD-GUN3}$	±8.0	kV	
2.0 kΩ / 330 pF Powered According to ISO10605.2008	$V_{ESD-GUN4}$	±8.0	kV	
• CANH, CANL				
330 Ω / 150 pF Unpowered According to IEC61000-4-2:	$V_{ESD-GUN5}$	±15	kV	
330 Ω / 150 pF Unpowered According to OEM LIN, CAN, FLexray Conformance	$V_{ESD-GUN6}$	±12	kV	
2.0 kΩ / 150 pF Unpowered According to ISO10605.2008	$V_{ESD-GUN7}$	±15	kV	
2.0 kΩ / 330 pF Powered According to ISO10605.2008	$V_{ESD-GUN8}$	±15	kV	
THERMAL RATINGS				
Ambient Temperature	T_A	-40 to 125	°C	
Junction Temperature	T_J	-40 to 150	°C	
Storage Temperature	T_{STG}	-55 to 150	°C	
THERMAL RESISTANCE				
Thermal resistance junction to ambient	$R_{\theta JA}$	32	°C/W	(2)
Thermal resistance junction to Case Top	$R_{\theta JCTOP}$	23	°C/W	(3)
Thermal resistance junction to Case Bottom	$R_{\theta JCBOTTOM}$	1.3	°C/W	(4)

Notes

2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
4. Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

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4.2 Static Electrical Characteristics

Table 4. Operating Range

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
POWER SUPPLY						
I_{SUP}	Power Supply Current in Normal Mode (Vsup > Vsup_uv_7)	2.0	–	13.0	mA	
I_{SUP_LPOFF1}	Power Supply Current in LPOFF (14 V, @ T_A = 25 °C)	–	32	–	µA	
I_{SUP_LPOFF2}	Power Supply Current in LPOFF (18 V, @ T_A = 80 °C)	–	42	60	µA	
V_{SNS_UV}	Power Supply Undervoltage Warning	–	8.5	–	V	
$V_{SNS_UV_HYST}$	Power Supply Undervoltage Hysteresis	0.1	–	–	V	
$V_{SUP_UV_7}$	Power Supply Undervoltage Lockout (power-up)	7.0	–	8.2	V	
$V_{SUP_UV_5}$	Power Supply Undervoltage Lockout (power-up)	–	–	5.6	V	
$V_{SUP_UV_L}$	Power Supply Undervoltage Lockout (falling - Boost config.)	–	–	2.7	V	
$V_{SUP_UV_L_B}$	Power Supply Undervoltage Lockout (falling - Buck config.)	–	–	4.6	V	
$V_{SUP_UV_HYST}$	Power Supply Undervoltage Lockout Hysteresis	–	0.1	–	V	(5)
V_{PRE} VOLTAGE PRE-REGULATOR						
V_{PRE}	V_{PRE} Output Voltage • Buck mode (V_{SUP} > Vsup_uv_7) • Buck mode ($V_{SUP_UV_7} \geq V_{SUP} \geq 4.6$ V) • Boost mode ($V_{SUP} \geq 2.7$ V)	 6.25 $V_{PRE_UV_4P3}$ 6.0	 – V_{SUP} - R_{DSON_PRE} * I_{PRE} –	 6.75 – 7.0	V	
I_{PRE}	V_{PRE} Maximum Output Current Capability • Buck or Boost with V_{SUP} > $V_{SUP_UV_7}$ • Buck with $V_{SUP_UV_7} \geq V_{SUP} \geq 4.6$ V • Boost with $V_{SUP_UV_7} \geq V_{SUP} \geq 6.0$ V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 2.0 0.5 2.0 1.0 0.3	 – 2.0 – – –	 – – – – –	A	(5)
I_{PRE_LPOFF}	V_{PRE} Maximum Output Current Capability in LPOFF at low Vsup voltage • Buck with $V_{SUP_UV_7} \geq V_{SUP} \geq 4.6$ V • Boost with $V_{SUP_UV_7} \geq V_{SUP} \geq 6.0$ V • Boost with 6.0 V ≥ V_{SUP} ≥ 4.0 V • Boost with 4.0 V ≥ V_{SUP} ≥ 2.7 V	 0.050 2.0 1.0 0.3	 – – – –	 – – – –	A	(5)
I_{PRE_LIM}	V_{PRE} Output Current Limitation with Vsup ≤ 28V	3.5	–	–	A	
I_{PRE_OC}	V_{PRE} Overcurrent Detection Threshold (in buck mode only) with $V_{SUP} \leq 28$ V	5.0	–	–	A	
V_{PRE_UV}	V_{PRE} Undervoltage Detection Threshold (Falling)	5.5	–	6.0	V	
$V_{PRE_UV_HYST}$	V_{PRE} Undervoltage Hysteresis	0.05	–	0.15	V	(5)
$V_{PRE_UV_4P3}$	V_{PRE} Shut-off Threshold (Falling - buck mode)	4.2	–	4.5	V	

Notes
5. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{PRE} VOLTAGE PRE-REGULATOR (CONTINUED)						
$V_{PRE_UV_4P3_HYST}$	V_{PRE} Shut-off Hysteresis	0.05	–	0.15	V	(6)
R_{DSON_PRE}	V_{PRE} Pass Transistor On Resistance with $V_{SUP} \leq 28$ V	–	–	200	mΩ	
L_{IR_VPRE}	V_{PRE} Line Regulation	–	20	–	mV	(6)
LOR_{VPRE_BUCK}	V_{PRE} Load Regulation for C_{OUT} = 57 µF I_{PRE} from 50 mA to 2.0 A - Buck mode	–	100	–	mV	(6)
LOR_{VPRE_BOOST}	V_{PRE} Load Regulation for C_{OUT} = 57 µF I_{PRE} from 50 mA to 2.0 A - Boost mode	–	500	–	mV	(6)
$V_{PRE_LL_H}$ $V_{PRE_LL_L}$	V_{PRE} Pulse Skipping Thresholds	– –	200 180	– –	mV	
T_{WARN_PRE}	V_{PRE} Thermal Warning Threshold	–	125	–	°C	
T_{SD_PRE}	V_{PRE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD_PRE_HYST}$	V_{PRE} Thermal Shutdown Hysteresis	–	10	–	°C	(6)
V_{SUP_IPFF}	I_{PFF} Input Voltage detection	18	–	24	V	
$V_{SUP_IPFF_HYST}$	I_{PFF} Input Voltage hysteresis	0.2	–	–	V	
$I_{PRE_IPFF_PK}$	I_{PFF} High Side Peak current detection with $V_{SUP} \leq 28$ V	1.7	–	–	A	
$V_{G_LS_OH}$	LS Gate driver High output voltage (I_{OUT} = 50 mA)	V_{PRE}-1	–	V_{PRE}	V	
$V_{G_LS_OL}$	LS Gate driver Low Level (I_{OUT} = 50 mA)	–	–	0.5	V	
V_{CORE} VOLTAGE REGULATOR						
V_{CORE_FB}	V_{CORE} Feedback Input Voltage	0.784	0.8	0.816	V	
I_{CORE}	V_{CORE} Output Current Capability in Normal Mode • MC33907 • MC33908	 – –	 – –	 0.8 1.5	A	
$I_{CORE_LIM_10}$ $I_{CORE_LIM_20}$	V_{CORE} Output Current Limitation • MC33907 • MC33908	 1.0 1.8	 – –	 2.0 3.5	A	
R_{DSON_CORE}	V_{CORE} Pass Transistor On Resistance	–	–	200	mΩ	
$LOR_{VCORE_1.2}$	V_{CORE} Transient Load regulation - 1.2 V range	-60	–	60	mV	(6), (7)
$LOR_{VCORE_3.3}$	V_{CORE} Transient Load regulation - 3.3 V range	-100	–	100	mV	(6), (7)
T_{WARN_CORE}	V_{CORE} Thermal Warning Threshold	–	125	–	°C	
T_{SD_CORE}	V_{CORE} Thermal Shutdown Threshold	160	–	–	°C	
$T_{SD_CORE_HYST}$	V_{CORE} Thermal Shutdown Hysteresis	–	10	–	°C	(6)

Notes

6. Guaranteed by design.
7. C_{OUT} = 40 µF, I_{CORE} = 10 mA to 1.5 A, $dI_{CORE}/dt \leq 2.0$ A/µs

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCA} VOLTAGE REGULATOR						
V_{CCA}	V_{CCA} Output Voltage • 5.0 V config. with Internal ballast at 100 mA • 5.0 V config with external ballast at 200 mA • 5.0 V config with external ballast at 300 mA • 3.3 V config with Internal ballast at 100 mA • 3.3 V config with external ballast at 200 mA • 3.3 V config with external ballast at 300 mA	 4.95 4.9 4.85 3.2505 3.234 3.201	 5.0 5.0 5.0 3.3 3.3 3.3	 5.05 5.1 5.15 3.3495 3.366 3.399	V	 (8) (8)
I_{CCA_IN}	V_{CCA} Output Current (int. MOSFET)	–	–	100	mA	
I_{CCA_OUT}	V_{CCA} Output Current (external PNP)	–	–	300	mA	
$I_{CCA_LIM_INT}$	V_{CCA} Output Current Limitation (int. MOSFET)	100	–	675	mA	
$I_{CCA_LIM_OUT}$	V_{CCA} Output Current Limitation (external PNP)	300	–	675	mA	
$I_{CCA_LIM_FB}$	V_{CCA} Output Current Limitation Foldback	80	–	200	mA	
$V_{CCA_LIM_FB}$	V_{CCA} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{CCA_LIM_HYST}$	V_{CCA} Output Voltage Foldback Hysteresis	0.07	–	0.3	V	
$I_{CCA_BASE_SC}$	V_{CCA} Base Current Capability (internal pull-up)	–	20	30	mA	
$I_{CCA_BASE_SK}$	V_{CCA} Base Current Capability (Current sink)	20	65	–	mA	
T_{WARN_CCA}	V_{CCA} Thermal Warning Threshold (int. ballast only)	–	125	–	°C	
TSD_{CCA}	V_{CCA} Thermal Shutdown Threshold (int. ballast only)	160	–	–	°C	
TSD_{CCA_HYST}	V_{CCA} Thermal Shutdown Hysteresis	–	10	–	°C	(9)
$LORT_{VCCA}$	V_{CCA} Transient Load Regulation • I_{CCA} = 10 mA to 100 mA (internal MOSFET) • I_{CCA} = 10 mA to 300 mA (external ballast)	–	–	1.0	%	(9)

Notes
8. External PNP gain within 150 to 450
9. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
VAUX VOLTAGE REGULATOR						
V_{AUX_5}	V_{AUX} Output Voltage (5.0 V configuration)	4.85	5.0	5.15	V	
V_{AUX_33}	V_{AUX} Output Voltage (3.3 V configuration)	3.2	3.3	3.4	V	
V_{AUX_TRK}	V_{AUX} Tracking Error (V_{AUX_5} and V_{AUX_33})	-15	–	+15	mV	
I_{AUX_OUT}	V_{AUX} Output Current	–	–	300	mA	
I_{AUX_LIM}	V_{AUX} Output Current Limitation	300	–	700	mA	
$I_{AUX_LIM_FB}$	V_{AUX} Output Current Limitation Foldback	100	–	530	mA	
$V_{AUX_LIM_FB}$	V_{AUX} Output Voltage Foldback Threshold	0.5	–	1.1	V	
$V_{AUX_LIM_HYST}$	V_{AUX} Output Voltage Foldback Hysteresis	0.05	–	0.3	V	
$I_{AUX_BASE_SC}$ $I_{AUX_BASE_SK}$	V_{AUX} Base Current Capability	– 7.0	– –	-7.0 –	mA	
TSD_{AUX}	V_{AUX} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{AUX_HYST}	V_{AUX} Thermal Shutdown Hysteresis	–	10	–	°C	(10)
LOR_{VAUX}	V_{AUX} Static Load Regulation (I_{AUX_OUT} = 10 to 300 mA)	–	15	–	mV	(10)
$LORT_{VAUX}$	V_{AUX} Transient Load Regulation • I_{AUX_OUT} = 10 mA to 300 mA	–	–	1.0	%	(10)
5V-CAN VOLTAGE REGULATOR						
V_{CAN}	V_{CAN} Output Voltage V_{SUP} > 6.0 V in Buck mode V_{SUP} > $V_{SUP_UV_L}$ in Boost mode	4.8	5.0	5.2	V	
I_{CAN_OUT}	V_{CAN} Output Current	–	–	100	mA	
I_{CAN_LIM}	V_{CAN} Output Current Limitation	100	–	250	mA	
TSD_{CAN}	V_{CAN} Thermal Shutdown Threshold	160	–	–	°C	
TSD_{CAN_HYST}	V_{CAN} Thermal Shutdown Hysteresis	–	10	–	°C	(10)
V_{CAN_UV}	V_{CAN} Undervoltage Detection Threshold	4.25	–	4.8	V	
$V_{CAN_UV_HYST}$	V_{CAN} Undervoltage Hysteresis	0.07	–	0.22	V	
V_{CAN_OV}	V_{CAN} Overvoltage Detection Threshold	5.2	–	5.55	V	
$V_{CAN_OV_HYST}$	V_{CAN} Overvoltage Hysteresis	0.07	–	0.22	V	
LOR_{VCAN}	V_{CAN} Load Regulation (from 0 to 50 mA)	–	100	–	mV	(10)

Notes
10. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
FAIL-SAFE MACHINE VOLTAGE SUPERVISOR						
V_{PRE_OV}	V_{PRE} Overvoltage Detection Threshold	7.2	–	8.0	V	
$V_{PRE_OV_HYST}$	V_{PRE} Overvoltage Hysteresis	–	0.1	–	V	(11)
$V_{CORE_FB_UV}$	V_{CORE} FB Undervoltage Detection Threshold	0.67	–	0.773	V	
$V_{CORE_FB_UV_D}$	V_{CORE} FB Undervoltage Detection Threshold - Degraded mode	0.45	–	0.58	V	
$V_{CORE_FB_UV_HYST}$	V_{CORE} FB Undervoltage Hysteresis	10	–	27	mV	(11)
$V_{CORE_FB_OV}$	V_{CORE} FB Overvoltage Detection Threshold	0.84	–	0.905	V	
$V_{CORE_FB_OV_HYST}$	V_{CORE} FB Overvoltage Hysteresis	10	–	30	mV	(11)
I_{PD_CORE}	V_{CORE} Internal Pull-down Current	5.0	12	25	mA	
$V_{CCA_UV_5}$	V_{CCA} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{CCA_UV_5D}$	V_{CCA} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{CCA_UV_33}$	V_{CCA} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{CCA_UV_HYST}$	V_{CCA} Undervoltage Hysteresis	–	0.07	–	V	(11)
$V_{CCA_OV_5}$	V_{CCA} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{CCA_OV_33}$	V_{CCA} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{CCA_OV_HYST}$	V_{CCA} Overvoltage Hysteresis	–	0.15	–	V	(11)
R_{PD_CCA}	V_{CCA} Internal Pull-down Resistor (enabled when V_{CCA} is switched off)	50	–	160	Ω	
$V_{AUX_UV_5}$	V_{AUX} Undervoltage Detection Threshold (5.0 V config)	4.5	–	4.75	V	
$V_{AUX_UV_5D}$	V_{AUX} Undervoltage Detection Threshold (Degraded 5.0 V)	3.0	–	3.2	V	
$V_{AUX_UV_33}$	V_{AUX} Undervoltage Detection Threshold (3.3 V config)	3.0	–	3.2	V	
$V_{AUX_UV_HYST}$	V_{AUX} Undervoltage Hysteresis	–	0.07	–	V	(11)
$V_{AUX_OV_5}$	V_{AUX} Overvoltage Detection Threshold (5.0 V config)	5.25	–	5.5	V	
$V_{AUX_OV_33}$	V_{AUX} Overvoltage Detection Threshold (3.3 V config)	3.4	–	3.6	V	
$V_{AUX_OV_HYST}$	V_{AUX} Overvoltage Hysteresis	–	0.07	–	V	(11)
R_{PD_AUX}	V_{AUX} Internal Pull-down Resistor	50	–	170	Ω	

Notes
11. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
FAIL-SAFE OUTPUTS						
V_{RSTB_OL}	Reset Low Output Level (I_RSTB = 2.0 mA and 2.0 V < V_{SUP} < 40 V)	–	–	0.5	V	(12)
I_{RSTB_LIM}	Reset Output Current Limitation	12	–	25	mA	
V_{RSTB_IL}	External Reset Detection Threshold (falling)	1.0	–		V	
V_{RSTB_IH}	External Reset Detection Threshold (rising)	–	–	2.0	V	
$V_{RSTB_IN_HYST}$	External Reset Input Hysteresis	0.2	–	–	V	
V_{FS0B_OL}	FS0B low Output Level (I_FS0b = 2.0 mA)	–	–	0.5	V	
I_{FS0B_LK}	FS0B Input Current Leakage (V_{FS0B} = 28 V)	–	–	1.0	µA	
I_{FS0B_LIM}	FS0B Output Current Limitation	6.0	–	12	mA	
MULTI-PURPOSE IOS						
ANALOG INPUT						
$V_{IO_ANA_WD}$	Measurable Input Voltage (wide range)	3.0	–	19	V	
$V_{IO_ANA_TG}$	Measurable Input Voltage (tight range)	3.0	–	9.0	V	
$I_{IO_IN_ANA}$	Input Current	–	–	100	µA	
DIGITAL INPUT						
V_{IO_IH}	High Input Voltage Detection Threshold (IO_0:1, IO_4:5) • Min Limit = 2.7 V at V_{SUP} = 40 V	2.6	–	–	V	
V_{IO23_IH}	High Input Voltage Detection Threshold (IO_2, IO_3)	2.0	–	–	V	
V_{IO_IL}	Digital Low Input Level (IO_0:1; IO_4:5)	–	–	2.1	V	
V_{IO_HYST}	Input Voltage Hysteresis (IO_0:1, IO_4:5)	50	120	500	mV	(13)
V_{IO23_IL}	Digital Low Input Level (IO_2, IO_3)	–	–	0.9	V	
V_{IO23_HYST}	Input Voltage Hysteresis (IO_2, IO_3)	200	450	700	mV	(13)
$I_{IO_IN_0:1}$	Input Current for IO_0:1	-5.0	–	100	µA	
$I_{IO_IN_2:5}$	Input Current for IO_2:5	-5.0	–	5.0	µA	
$I_{IO_IN_LPOFF}$	Input Current for IO_0:5 in LPOFF	-1.0	–	1.0	µA	
OUTPUT GATE DRIVER						
V_{IO_OH}	High Output Level at I_{IO_OUT} = -2.5 mA	V_{PRE} - 1.5	–	V_{PRE}	V	
V_{IO_OL}	Low Output Level at I_{IO_OUT} = +2.5 mA	0.0	–	1.0	V	
$V_{IO_OUT_SK}$ $V_{IO_OUT_SC}$	Output Current Capability	2.5 –	– –	– -2.5	mA	

Notes

12. For V_{SUP} < 2.0 V, all supplies are already off and external pull-up on RSTB (e.g V_{CORE} or V_{CCA}) pulls the line down.
13. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
ANALOG MULTIPLEXER						
V_{AMUX_ACC}	Voltage Sense Accuracy (V_{SNS}, IO_0, IO_1) using 5.1 kΩ resistor	-5.0	–	5.0	%	(14)
$V_{AMUX_WD_5}$	Divider Ratio (wide input voltage range) at V_{DDIO} = 5.0 V	–	5.0	–		
$V_{AMUX_WD_3P3}$	Divider Ratio (wide input voltage range) at V_{DDIO} = 3.3 V	–	7.0	–		
$V_{AMUX_TG_5}$	Divider Ratio (tight input voltage range) at V_{DDIO} = 5.0 V	–	2.0	–		
$V_{AMUX_TG_3P3}$	Divider Ratio (tight input voltage range) at V_{DDIO} = 3.3 V	–	3.0	–		
V_{AMUX_REF1}	Internal Voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V	
V_{AMUX_REF2}	Internal Voltage Reference with $V_{SUP} \leq$ 6.0 V or $V_{SUP} \geq$ 19 V	2.468	2.5	2.532	V	
$V_{AMUX_TP_CO}$	Internal Temperature Sensor Coefficient	–	9.9	–	mV/°C	
V_{AMUX_TP}	Temperature Sensor mux_output Voltage (at T_J = 165 °C)	2.08	2.15	2.22	V	(15)
INTERRUPT						
V_{INTB_OL}	Low output level (I_{INT} = 2.5mA)	–	–	0.5	V	
R_{PU_INT}	Internal pull-up resistor (connected to VDDIO)	–	10	–	KΩ	
I_{INT_LK}	Input leakage current	–	–	1	µA	
CAN TRANSCEIVER						
CAN LOGIC INPUT PIN (TXD)						
V_{TXD_IH}	TXD High Input Threshold	0.7 x V_{DDIO}	–	–	V	
V_{TXD_IL}	TXD Low Input Threshold	–	–	0.3 x V_{DDIO}	V	
$TXD_{PULL-UP}$	TXD Main Device Pull-up	20	33	50	KΩ	
TXD_{LK}	TXD Input Leakage Current, V_{TXD} = V_{DDIO}	-1.0	–	1.0	µA	
CAN LOGIC OUTPUT PIN (RXD)						
V_{RXD_OL1}	Low Level Output Voltage (I_{RXD} = 250 µA)	–	–	0.4	V	
V_{RXD_OL2}	Low Level Output Voltage (I_{RXD} = 1.5 mA)	–	–	0.9	V	
$VOUT_{HIGH}$	High Level Output Voltage (I_{RXD} = -250 µA, V_{DDIO} = 3.0 V to 5.5 V)	V_{DDIO} - 0.4V	–	–	V	

Notes

14. If a higher resistor value than recommended is used, the accuracy degrades.
15. Guaranteed by design.

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CAN OUTPUT PINS (CANH, CANL)						
DIFF_COM_MODE	Differential Input Comparator Common Mode Range	-12	–	12	V	
$V_{IN_DIFF_SLEEP}$	Differential Input Voltage Threshold in Sleep Mode	0.5	–	0.9	V	
V_{IN_HYST}	Differential Input Hysteresis (in Tx, Rx mode)	50	–	–	mV	
R_{IN_CHCL}	CANH, CANL Input Resistance	5.0	–	50	kΩ	
R_{IN_DIFF}	CAN Differential Input Resistance	10	–	100	kΩ	
R_{IN_MATCH}	Input Resistance Matching	-3.0	–	3.0	%	
V_{CANH}	CANH Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 2.75 2.0	 – 2.5	 4.5 3.0	V	
V_{CANL}	CANL Output Voltage (45 Ω < R_{BUS} < 65 Ω) • TX dominant state • TX recessive state	 0.5 2.0	 – 2.5	 2.25 3.0	V	
V_{OH}-V_{OL}	Differential Output Voltage • TX dominant state (45 Ω < R_{BUS} < 65 Ω) • TX recessive state	 1.5 -50	 2.0 0.0	 3.0 50	 V mV	
$I_{CANL\text{-}SK}$	CANL Sink Current Under Short-circuit Condition (V_{CANL} ≤ 12 V, CANL driver ON, TXD low)	40	–	100	mA	
$I_{CANH\text{-}SC}$	CANH Source Current Under Short-circuit Condition (V_{CANH} = -2.0 V, CANH driver ON, TXD low)	-100	–	-40	mA	
$R_{INSLEEP}$	CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode	5.0	–	50	kΩ	
V_{CANLP}	CANL, CANH Output Voltage in Sleep Modes. No Termination load.	-0.1	0.0	0.1	V	
I_{CAN}	CANH, CANL Input Current, Device Unsupplied, V_{SUP} and V_{IO} connected to GND • V_{CANH}, V_{CANL} = 5.0 V	 -10	 –	 10	µA	
T_{OT}	Overtemperature Detection	160	–	–	°C	
T_{HYST}	Overtemperature Hysteresis	-10	–	+20	°C	
DIGITAL INTERFACE						
$MISO_H$	High Output Level on MISO (I_{MISO} = 1.5 mA)	V_{DDIO} - 0.4	–	–	V	
$MISO_L$	Low Output Level on MISO (I_{MISO} = 2.0 mA)	–	–	0.4	V	
I_{MISO}	Tri-state Leakage Current (V_{DDIO} = 5.0 V)	-5.0	–	5.0	µA	
V_{DDIO}	Supply Voltage for MISO Output Buffer	3.0	–	5.5	V	
SPI_{LK}	SCLK,NCS,MOSI Input Current	-1.0	–	1.0	µA	
V_{SPI_IH}	SCLK,NCS,MOSI High Input Threshold	2.0	–	–	V	
V_{SPI_IL}	SCLK,NCS,MOSI Low Input Threshold	–	–	0.8	V	
R_{SPI}	NCS,MOSI Internal Pull-up (pull-up to VDDIO)	200	400	800	KΩ	

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Table 4. Operating Range (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
DEBUG						
V_{DEBUG_IL}	Low Input Voltage Threshold	2.1	2.35	2.6	V	
V_{DEBUG_IH}	High Input Voltage Threshold	4.35	4.6	4.97	V	
I_{DEBUG_LK}	Input Leakage Current	-10	–	10	µA	

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4.3 Dynamic Electrical Characteristics

Table 5. Dynamic Electrical Characteristics

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
DIGITAL INTERFACE TIMING						
f_{SPI}	SPI Operation Frequency (50% DC)	0.5	–	8.0	MHz	
t_{MISO_TRANS}	MISO Transition Speed, 20 - 80% • V_{DDIO} = 5.0 V, C_{LOAD} = 50 pF • V_{DDIO} = 5.0 V, C_{LOAD} = 150 pF	 5.0 5.0	 – –	 30 50	ns	
t_{CLH}	Minimum Time SCLK = HIGH	62	–	-	ns	
t_{CLL}	Minimum Time SCLK = LOW	62	–	-	ns	
t_{PCLD}	Propagation Delay (SCLK to data at 10% of MISO rising edge)	–	–	30	ns	
t_{CSDV}	NCS = LOW to Data at MISO Active	–	–	75	ns	
t_{SCLCH}	SCLK Low Before NCS Low (setup time SCLK to NCS change H/L)	75	–	–	ns	
t_{HCLCL}	SCLK Change L/H after NCS = low	75	–	–	ns	
t_{SCLD}	SDI Input Setup Time (SCLK change H/L after MOSI data valid)	40	–	–	ns	
t_{HCLD}	SDI Input Hold Time (MOSI data hold after SCLK change H/L)	40	–	–	ns	
t_{SCLCL}	SCLK Low Before NCS High	100	–	–	ns	
t_{HCLCH}	SCLK High After NCS High	100	–	–	ns	
t_{PCHD}	NCS L/H to MISO at High-impedance	–	–	75	ns	
t_{ONNCS}	NCS Min. High Time	500	–	–	ns	
t_{NCS_MIN}	NCS Filter Time	10	–	40	ns	

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Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes

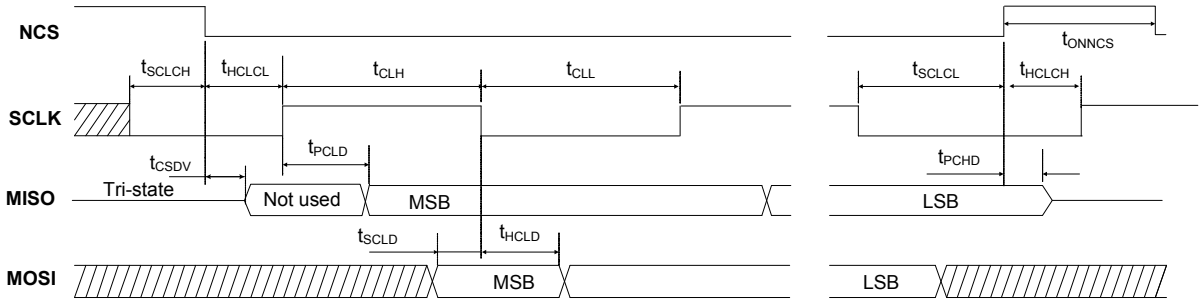


Figure 5. SPI Timing Diagram

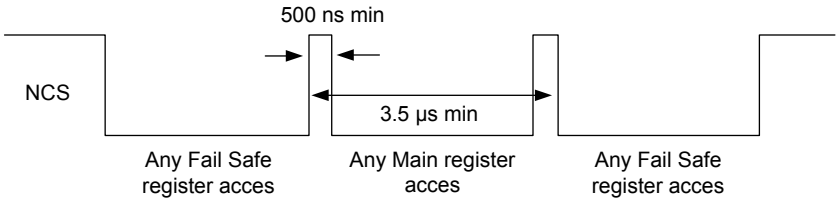


Figure 6. Register Access Restriction

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Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
CAN DYNAMIC CHARACTERISTICS						
t_{DOUT}	TXD Dominant State Timeout	0.8	–	5.0	ms	
t_{DOM}	Bus Dominant Clamping Detection	0.8	–	5.0	ms	
t_{LOOP}	Propagation Loop Delay TXD to RXD • R_{LOAD} = 120 Ω, C between CANH and CANL = 100 pF, C at RxD < 15 pF	–	–	255	ns	
t_{1PWU}	Single Pulse Wake-up Time	0.5	–	5.0	µs	
t_{3PWU}	Multiple Pulse Wake-up Time	0.5	–	1.0	µs	
t_{3PTO1}	Multiple Pulse Wake-up Timeout (120 µs bit selection)	110	120	–	µs	
t_{3PTO2}	Multiple Pulse Wake-up Timeout (360µs bit selection)	350	360	–	µs	
t_{CAN_READY}	Delay to enable CAN by SPI Command (NCS rising edge) to CAN to Transmit (device in normal mode and CAN interface in TxRx mode)	–	–	100	µs	(16)
FAIL-SAFE STATE MACHINE						
OSC_{FSSM}	Oscillator	400	–	500	kHz	
CLK_{FS_MIN}	Fail-safe Oscillator Monitoring	150	–	–	kHz	
t_{IC_ERR}	IO_0:5 Filter Time	4.0	–	20	µs	
t_{ACK_FS}	Acknowledgement Counter (used for IC error handling IO_1 and IO_5)	7.0	–	9.7	ms	
T_DFS_recovery	IO_0 filter time to recover from deep reset and fail state	0.8	–	1.3	ms	
FAIL-SAFE OUTPUT						
t_{RSTB_FB}	RSTB feedback filter time	8.0	–	15	µs	
t_{FSOB_FB}	FS0B feedback filter time	8.0	–	15	µs	
t_{RSTB_BLK}	RSTB feedback blanking time	180	–	320	µs	
t_{FSOB_BLK}	FS0B feedback blanking time	180	–	320	µs	
t_{RSTB_POR}	Reset delay time (after a Power On Reset or from LPOFF)	12	15.9	23.6	ms	
t_{RSTB_LG}	Reset duration (long pulse)	8.0	–	10	ms	
t_{RSTB_ST}	Reset duration (short pulse)	1.0	–	1.3	ms	
t_{RSTB_IN}	External Reset delay time	8.0	–	15	µs	
$T_{_FS_FB}$	RSTB, FS0B Feedback Filter Time	8.0	–	15	µs	
$T_{_DIAG_SC}$	Fail-safe Output Diagnostic Counter (FS0B)	550	–	800	µs	
VSUP VOLTAGE SUPPLY						
DV_{SUP}/DT	Supply Voltage Slew Rate	-2.0	–	2.0	V/µs	

Notes

16. For proper CAN operation, TXD must be set to high level before CAN being enabled by SPI, and must remain high for at least T_{CAN_READY}

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Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{PRE} VOLTAGE PRE-REGULATOR						
f_{SW_PRE}	V_{PRE} Switching Frequency	418	440	462	kHz	
t_{SW_PRE}	V_{SW_PRE} On and Off Switching Time	–	–	30	ns	(17)
t_{PRE_SOFT}	V_{PRE} Soft Start Duration (C_{OUT} ≤ 100 µF)	500	–	700	µs	
$t_{PRE_BLK_LIM}$	V_{PRE} Current Limitation Blanking Time	200	–	600	ns	
t_{IPRE_OC}	V_{PRE} Overcurrent Filtering Time	30	–	120	ns	(17)
t_{PRE_UV}	V_{PRE} Undervoltage Filtering Time	20	–	40	µs	
$t_{PRE_UV_4p3}$	Vpre Shut-off Filtering Time	3.0	–	6.0	µs	
$d_{IPRE/DT}$	V_{PRE} Load Regulation Variation	–	–	25	A/ms	(17)
t_{PRE_WARN}	V_{PRE} Thermal Warning Filtering Time	30	–	40	µs	
t_{PRE_TSD}	V_{PRE} Thermal Detection Filtering Time	1.3	–	–	µs	
t_{VSUP_IPFF}	I_{PFF} Input Voltage Filtering Time	1.0	–	4.0	µs	
t_{IPRE_IPFF}	I_{PFF} High Side Peak Current Filter Time	100	–	300	ns	
$t_{LS_RISE/FALL}$	LS Gate Voltage Switching Time (I_{OUT} = 300 mA)	–	–	50	ns	
V_{SENSE} VOLTAGE REGULATOR						
t_{VSNS_UV}	V_{SNS} Undervoltage Filtering Time	1.0	–	3.0	µs	
V_{CORE} VOLTAGE REGULATOR						
$t_{CORE_BLK_LIM}$	V_{CORE} Current Limitation Blanking Time	20	–	40	ns	
f_{SW_CORE}	V_{CORE} Switching Frequency	2.28	2.4	2.52	MHz	
t_{SW_CORE}	V_{SW_CORE} On and Off Switching Time	6.0	–	12	ns	
V_{CORE_SOFT}	V_{CORE} Soft Start (C_{OUT} = 100 µF max)	–	–	10	V/ms	
t_{CORE_WARN}	V_{CORE} Thermal Warning Filtering Time	30	–	40	µs	
t_{CORE_TSD}	V_{CORE} Thermal Detection Filtering Time	0.5	–	–	µs	
V_{CCA} VOLTAGE REGULATOR						
t_{CCA_LIM}	V_{CCA} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{CCA_LIM_OFF1}$ $t_{CCA_LIM_OFF2}$	V_{CCA} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{CCA_WARN}	V_{CCA} Thermal Warning Filtering Time	30	–	40	µs	
t_{CCA_TSD}	V_{CCA} Thermal Detection Filter Time (int. MOSFET)	1.5	–	–	µs	
dI_{LOAD}/dt	V_{CCA} Load Transient	–	2.0	–	A/ms	(17)
V_{CCA_SOFT}	V_{CCA} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	

Notes

17. Guaranteed by characterization.

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Table 5. Dynamic Electrical Characteristics (continued)

T_{CASE} = -40 to 125 °C, unless otherwise specified. V_{SUP} = $V_{SUP_UV_L}$ to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V < V_{SUP} < 40 V, thermal dissipation must be considered (Figure 22).

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{AUX} VOLTAGE REGULATOR						
t_{AUX_LIM}	V_{AUX} Output Current Limitation Filter Time	1.0	–	3.0	µs	
$t_{AUX_LIM_OFF1}$ $t_{AUX_LIM_OFF2}$	V_{AUX} Output Current Limitation Duration	10 50	– –	– –	ms	
t_{AUX_TSD}	V_{AUX} Thermal Detection Filter Time	1.5	–	–	µs	
dI_{AUX}/dt	V_{AUX} Load Transient	–	2.0	–	A/ms	(18)
V_{AUX_SOFT}	V_{AUX} Soft Start (5.0 V and 3.3 V)	–	–	50	V/ms	
5V-CAN VOLTAGE REGULATOR						
t_{CAN_LIM}	Output Current Limitation Filter Time	2.0	–	4.0	µs	
t_{CAN_TSD}	V_{CAN} Thermal Detection Filter Time	1.0	–	–	µs	
t_{CAN_UV}	V_{CAN} Undervoltage Filtering Time	4.0	–	6.0	µs	
t_{CAN_OV}	V_{CAN} Overvoltage Filtering Time	100	–	200	µs	
dI_{CAN}/dt	V_{CAN} Load Transient	–	100	–	A/ms	(18)
FAIL-SAFE MACHINE VOLTAGE SUPERVISOR						
t_{PRE_OV}	V_{PRE} Overvoltage Filtering Time	128	–	234	µs	
t_{CORE_UV}	V_{CORE} FB Undervoltage Filtering Time	4.0	–	10	µs	
t_{CORE_OV}	V_{CORE} FB Overvoltage Filtering Time	128	–	234	µs	
t_{CCA_UV}	V_{CCA} Undervoltage Filtering Time	4.0	–	10	µs	
t_{CCA_OV}	V_{CCA} Overvoltage Filtering Time	128	–	234	µs	
t_{AUX_UV}	V_{AUX} Undervoltage Filtering Time	4.0	–	10	µs	
t_{AUX_OV}	V_{AUX} Overvoltage Filtering Time	128	–	234	µs	
MULTI-PURPOSE IOS						
DIGITAL INPUT						
F_{IO_IN}	Digital Input Frequency Range	0.0	–	100	kHz	
ANALOG MULTIPLEXER						
t_{MUX_READY}	SPI Selection to Data Ready to be Sampled on Mux_out • V_{DDIO} = 5.0 V, C_{MUX_OUT} = 1.0 nF	–	–	10	µs	
INTERRUPT						
t_{INTB_LG}	INTB Pulse Duration (long)	100	–	–	µs	
t_{INTB_ST}	INTB Pulse Duration (short)	25	–	–	µs	
FUNCTIONAL SATE MACHINE						
t_{WU_GEN}	General Wake-up Signal Deglitch Time (for IO wu signal)	50	70	90	µs	

Notes

18. Guaranteed by characterization.

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5 Functional Description

5.1 Introduction

The 33907_8 is the third generation of the System Basis Chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN interface, external ICs such as sensors, and accurate reference voltage for A to D converters.
- Built in enhanced high speed CAN interface (ISO11898-2 and -5), with local and bus failure diagnostic, Protection and Fail-safe operation mode.
- Low power mode, with ultra low current consumption.
- Various wake-up capabilities
- Enhanced safety features with multiple fail-safe outputs and scheme.

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5.2 Functional Pin Description

5.2.1 Power Supply(VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the inputs pins for internal supply dedicated to SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO7637 pulses.

5.2.2 VSENSE Input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX-OUT pin. VSENSE pin is robust against ISO7637 pulse.

5.2.3 VCORE Output (1.2 V, 3.3 V)

On 33907 and 33908 product versions, the VCORE block is an SMPS regulator. The main difference between both versions is the current capability of the V_{CORE} regulator.

On 33907 and 33908 product versions, the voltage regulator is a step down DC-DC converter operating in voltage control mode. The output voltage is selectable (1.2 V or 3.3 V) through an external resistor divider connected between V_{CORE} and the feedback pin (FB_Core) (Figure 1). The stability of the converter is done externally, by using the COMP_Core pin.

5.2.4 VAUX OUTPUT, 5.0 V, 3.3 V Selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints.

The VAUX output voltage regulator can be used as “sensor supply” (external ECU supply) or “auxiliary supply” (local ECU supply).

Overcurrent, overvoltage, and undervoltage detectors are provided.

V_{AUX} can be turned ON or OFF (if not configured as safety critical) via a SPI command. V_{AUX} overcurrent and overvoltage information disables V_{AUX}, reported in the dedicated register, and generates an Interrupt.

V_{AUX} is enabled by default.

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5.2.5 VCCA Output, 5.0 V or 3.3 V Selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal ballast transistor delivering very good accuracy (+/- 1% for 5 V configuration and +/- 1.5% for 3.3 V configuration), with a limited current capability (100 mA) for an Analog to Digital converter, or with an external PNP transistor, giving higher current capability with lower output voltage accuracy when using a local ECU supply.

Overcurrent, overvoltage, and undervoltage detectors are provided.

VCCA can be turned ON or OFF (if not configured as safety critical) via a SPI command. V_{CCA} overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt.

VCCA is enabled by default.

5.2.6 SELECT Input (VCCA, VAUX Voltage Configuration)

VCCA and VAUX output voltage configurations are set by connecting an external resistor between SELECT pin and Ground.

According to the value of this resistor, the voltage of VCCA and VAUX are configured after each Power On Reset, and after a wake-up event when device is in LPOFF. Information latches until the next hardware configuration read.

Regulator voltage values can be read on the dedicated register via the SPI.

Table 6. V_{CCA}/V_{AUX} Voltage Selection

V_{CCA}(V)	V_{AUX}(V)	R Select	Recommended value
3.3	3.3	<7.0 KΩ	5.1 KΩ ±5.0%
5.0	5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
3.3	5.0	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	3.3	45.9 << 56.1 KΩ	51 KΩ ±5.0%

When V_{AUX} is not used, the output V_{CCA} voltage configuration is set using an external resistor connected between the SELECT and the VPRE pin.

Table 7. V_{CCA} Voltage Selection (V_{AUX} not used)

V_{CCA}(V)	R select	Recommended Value
3.3	<7.0 KΩ	5.1 KΩ ±5.0%
	21.6 << 26.2 KΩ	24 KΩ ±5.0%
5.0	10.8 << 13.2 KΩ	12 KΩ ±5.0%
	45.9 << 56.1 KΩ	51 KΩ ±5.0%

5.2.7 Debug Input (Entering In Debug Mode)

The DEBUG pin allows the product to enter Debug mode.

To activate the Debug mode, voltage applied to the DEBUG pin must be within the V_{DEBUG_IL} and V_{DEBUG_IH} range at startup. If the voltage applied to DEBUG pin is out of these limits, before V_{CORE} ramp-up, the device settles into Normal mode.

When the Debug mode is activated, the FS0B output is asserted low at startup.

As soon as the FS0B is released to “high” via SPI (Good WD answer and FS_OUT writing) this pin is never activated whatever the fault is reported.

In debug mode, any errors from watchdog are ignored (No reset and No fail-safe), even if the whole functionality of the watchdog is kept ON (Seed, LFSR, Wd_refresh counter, WD error counter). This allows an easy debug of the hardware and software routines (i.e. SPI commands).

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When the Debug mode is activated, the CAN transceiver is set to Normal operation mode. This allows communication with the MCU, in case SPI communication is not available (case of MCU not programmed).

To exit Debug mode, the pin must be tied to ground through an external pull-down resistor. A Power On Reset occurs.

5.2.8 5 V-CAN Voltage Regulator

5 V-CAN voltage regulator is a linear regulator fully dedicated to the internal HSCAN interface. An external capacitor is required.

Overcurrent, overvoltage, and undervoltage detectors are provided. During overvoltage, the 5 V-CAN regulator switches off. Information is reported in the dedicated register and this generates an Interrupt. The 5 V-CAN regulator is enabled by default.

5.2.9 Multiplexer Output Mux_out

The MUX_OUT pin (Figure 7) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX_OUT is selected via the SPI, from one of the following parameters:

- V_{SENSE}
- VIO_O
- VIO_1
- Internal 2.5 V reference
- Die temperature sensor T (°C) = Vmux_Out * 165 / 2.15

Voltage range at MUX_OUT is from GND to VDDIO (3.3 V or 5.0 V)

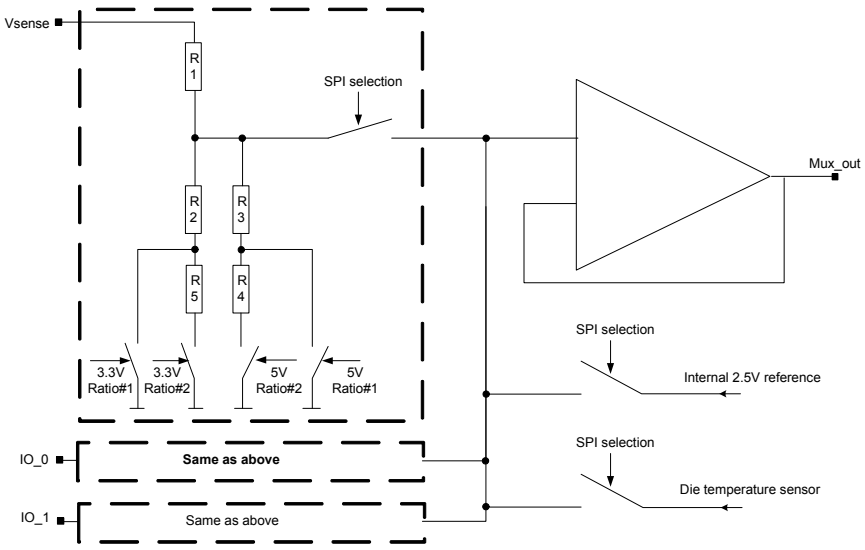


Figure 7. Simplified Analog Multiplexer Block Diagram

5.2.10 CANH, CANL, RXD, TXD

These are the pins of the high speed CAN physical interface.

The CAN interface is connected to the MCU via the RXD and TXD pins.

The HSCAN also exhibits wake-up capability with a very low current consumption.

5.2.11 INTERRUPT (INTB)

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase.

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5.2.12 I/O pins (I/O_0:I/O_6)

The 33907_8 includes six multi-purpose I/Os (I/O_0 to I/O_5).

I/O_0, I/O_1, I/O_4, and I/O_5 are load dump proof and robust against ISO7637 pulses. An external serial resistor must be connected to those pins. I/O_2 and I/O_3 are not load dump proof.

Table 8. I/Os Configuration

I/0 Number	Analog Input	Digital Input	Wake-up Capability	Output Gate Driver
IO_0	X	X	X	
IO_1	X	X	X	
IO_2		X	X	
IO_3		X	X	
IO_4		X	X	X
IO_5		X	X	X

- IO_0:1 are selectable as follows:
  Analog input (load dump proof) sent to the MCU through the MUX_OUT pin.
  Wake-up input on the rising or falling edge or based on the previous state.
  Digital input (logic level) sent to the MCU through the SPI.
  Safety purpose: Digital input (logic level) to perform an IC error monitoring (both IO_0 AND IO_1 are used if configured as safety inputs).
- IO_2:3 are selectable as follows:
  Digital input (logic level) sent to the MCU through the SPI.
  Wake-up input (logic level) on the rising or falling edge or based on the previous state.
  Safety purpose: Digital input (logic level) to monitor MCU error signals (both IO_2 AND IO_3 are used if configured as safety inputs).
  Only bi-stable protocol is available.

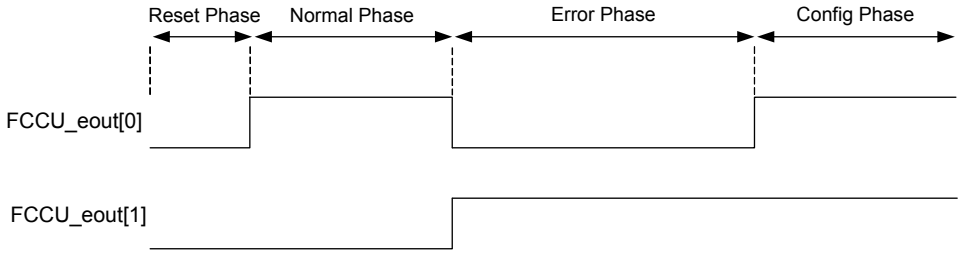


Figure 8. IO_2:3 MCU Error Monitoring: Bi-stable Protocol

- IO_4:5 are selectable as follows:
  Digital input (logic level) sent to the MCU through the SPI.
  Wake-up input (load dump proof) on rising or falling edge or based on previous state.
  Output gate driver for LS logic level MOSFET.
  Safety purpose: Digital input (logic level) to perform an IC error monitoring (both IO_4 AND IO_5 are used if configured as safety inputs).

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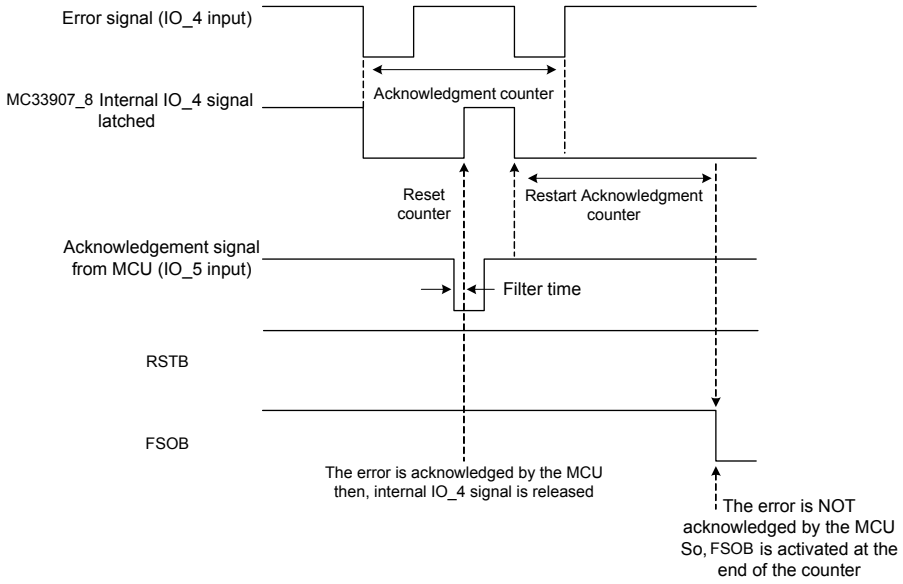


Figure 9. External Error Signal Handling

5.2.13 SAFE Output PINs (FS0B, RSTB)

FS0B is asserted low when a fault event occurs (See Faults Triggering FS0B Activation on page 42).The objective of this pin is to drive an electrical safe circuitry to deactivate the whole system and set the ECU in a protected and known state.

An external pull-up circuitry is mandatory connected to VDDIO or VSUP3. If pull-up is connected to VSUP3, the value of this pull-up must be above 10 kohm.

After each power on reset or after each wake-up event (LPOFF) the FS0B pin is asserted low. Then the MCU can decide to release the FS0B pin, when the application is ready to start.

The RSTB pin must be connected to MCU and is active low. An external pull-up resistor must be connected to VDDIO.

In default configuration, the RST delay time has three possible values depending of the mode and product configuration:

- The longest one is used automatically following a Power On Reset or when resulting from LPOFF mode (Low Power Off).
- The two reset durations are then available in the INIT_FSSM1 register, which are 1.0 ms and 10 ms. The configured duration is finally used in the normal operation when a fault occurs leading to a reset activation. The INIT_FSSM1 register is available (writing) in the INIT FS phase.

5.2.14 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the 33907_8. It can be configured as “Non-inverting Buck-boost converter” (Figure 24) or “Standard Buck converter” (Figure 23), depending of the external configuration (Low Side connection). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high side switching MOSFET is also integrated to make the current control easier.

The pre-regulator delivers a voltage output of 6.5 V, which is used internally.

Overcurrent, overvoltage, and undervoltage detectors are provided.

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6 Functional Device Operation

6.1 Mode and State Description of MAIN State Machine

The device has several operation modes. The transition and conditions to enter or leave each mode are illustrated in the functional state diagram (Figure 10). Two state machines are working in parallel. The Main state machine is in charge of the power management (V_{PRE}, V_{CORE}, V_{AUX}, V_{CCA},...) and the fail-safe state machine is in charge of all the safety aspect (WD, RSTB, FS0B,...).

6.1.1 Buck or Buck Boost Configuration

An external low side logic level MOSFET (N-type) is required to operate in “Non-inverting buck-boost converter”. The connection of the external MOSFET is detected automatically during the start-up phase.

If the low side is not connected (GATE_LS pin connected to PGND), the product is configured as a standard buck converter.

6.1.2 VPRE ON

Pre-regulator is an SMPS regulator. In this phase, the pre-regulator is switched ON and a softstart with a specified duration is started to control the V_{PRE} output capacitor charge.

6.1.3 Select Pin Configuration

This phase is detecting the required voltage level on VAUX and VCCA, according to resistor value connected between the SELECT pin and ground. If the SELECT pin is connected to V_{PRE} via the resistor, it disables the V_{AUX} regulator at start-up.

6.1.4 VCORE/VAUX/VCCA ON

In this stage, the three regulators are switched ON at the same time with a specified soft start duration.

6.1.5 INIT Main

This mode is automatically entered after the device is “Powered ON”. When RSTB is released, initialization phase starts where the device can be configured via the SPI.

During INIT phase, some registers can only be configured in this mode (refer to Table 12 and Table 13). Other registers can be written in this mode, and also in Normal mode.

Once the INIT registers configurations are complete, a last register called “INIT INT” must be configured to switch to Normal mode. Writing data in this register (even same default values), automatically locks the INIT registers, and the product switches automatically to Normal mode in the Main state machine.

6.1.6 Normal

In this mode, all device functions are available. This mode is entered by a SPI command from the INIT phase by writing in the INIT INT register.

While in Normal mode, the device can be set to Low power mode (LPOFF) using secured SPI command.

6.1.7 Low Power Mode OFF - LPOFF Sleep

Entering in Low Power mode OFF - SLEEP is only available if the product is in Normal mode by sending a secured SPI command.

In this mode, all the regulators are turned OFF and the MCU connected to V_{CORE} regulator is unsupplied.

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Once the 33907_8 is in LPOFF SLEEP, the device monitors external events to wake-up and leave the Low Power mode. The wake-up events can occur and depending of the device configuration from:

- CAN
- I/Os inputs

When a wake-up event is detected, the device starts the main state machine again by detecting the V_{PRE} configuration (BUCK or BUCK-BOOST), the wake-up source is reported to the dedicated SPI register, and the Fail-safe state machine is also restarted.

Finally, after the wake-up event, the regulators are turned ON and the MCU operation restarts, and the initialization phase is accessible again.

6.1.8 Low Power Mode OFF - LPOFF V_{PRE_UV}

LPOFF- V_{PRE_UV} is entered when the device is in the INIT or Normal mode, and if the V_{PRE} voltage level is passing the $V_{PRE_UV_L_4P3}$ threshold (4.3 V instead of 6.5 V) due to a problem on V_{PRE}.

As the device is in LPOFF, all the regulators are switched OFF. After 1.0 ms the device attempts to recover by switching ON the V_{PRE} again.

6.1.9 Low Power Mode OFF - LPOFF DEEP FS

LPOFF DEEP FS is entered during start-up if the Power On Reset of the Fail-safe machine is not rising and if the key is OFF.

in this mode, all regulators are OFF and to exit this mode, a high level on IO_0 is required (often connected to key ON key OFF signal).

LPOFF DEEP FS is also entered if the RSTB pin is asserted low within 8.0 s.

6.2 Mode and State Description of Fail-safe State Machine

6.2.1 LBIST

Included in the fail-safe machine, the Logic Built In Self Test (LBIST) verifies the correct functionality of the FSSM at start-up. The fail-safe state machine is fully checked and if an issue is reported, the device does not start and the RSTB stays low to finally go in LPOFF DEEP FS.

LBIST is run at start-up and after each wake-up event when device is in LPOFF mode.

6.2.2 Select Pin Configuration

This phase detects the required voltage level on VAUX and VCCA, according to the resistor value connected between the SELECT pin and ground, in case VAUX is used or the SELECT pin and V_{PRE}, if VAUX is not used in the application.

This mode is the equivalent mode seen in the main sate machine. Difference is in the fail-safe machine. This detection is used to internally set the UV/OV threshold on VCCA and VAUX for the voltage supervision.

6.2.3 ABIST

Included in the fail-safe machine, the Analog Built In Self Test (ABIST) verifies the correct functionality of the analog part of the device, like the voltage supervisor (overvoltage and undervoltage detection) and the fail-safe output feedback (RSTB and FS0B). The ABIST is run at start-up and after each wake-up event when device is in LPOFF mode.

6.2.4 Release RSTB

In this state, the device releases the RSTB pin.

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6.2.5 INIT FS

This mode is automatically entered after the device is “powered on” and only if Built Self Tests (Logic and Analog) have been passed successfully. This INIT FS mode starts as soon as RSTB is released (means no “Activate RST” faults are present and no external reset is requested). Faults leading to an “Activate RST” are described in Watchdog Refresh Counter.

In this mode, the device can be configured via the SPI within a maximum time of 256 ms, including first watchdog refresh.

Some registers can only be configured in this mode and is locked when leaving INIT FS mode (refer to Table 12 and Table 13).

It is recommended, to configure first the device before sending the first WD refresh.

As soon as the first good watchdog refresh is sent by the MCU, the device leaves this mode and goes into Normal WD mode.

6.2.6 Normal WD is Running

In this mode, the device is now waits for a periodic watchdog refresh, coming from the MCU within a specific configured window timing.

Configuration of the watchdog window period can be set during INIT FS phase or in this mode.

This mode is exited if there are consecutive bad watchdog refreshes, or if there is an external reset request.

6.2.7 RST Delay

When the reset pin is asserted low by the device, a delay runs, to release the RSTB, if there is no more faults present.

The reset low duration time is configurable via the SPI in the INIT_ FSSM1 register, which is accessible (writing) only in the INIT FS phase. All the sources of reset are available in the Watchdog Refresh Counter.

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6.3 Functional State Diagram

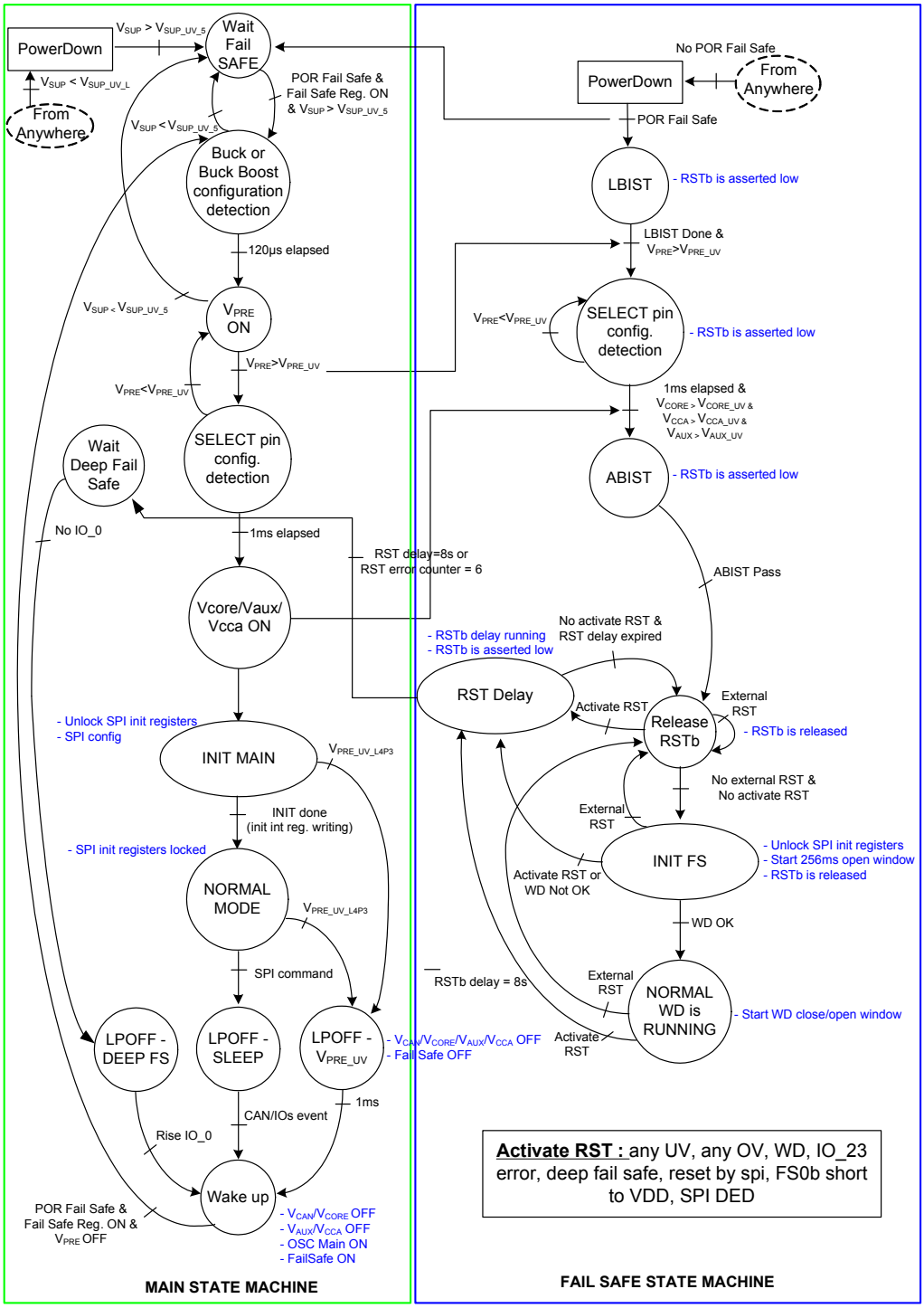


Figure 10. Simplified State Diagram

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6.4 Fail-safe Machine

To fulfill safety critical applications, the 33907_8 integrates a dedicated Fail-safe machine (FSM). The FSM is composed of three main sub-blocks: the Voltage Supervisor (VS), the Fail-safe State Machine (FSSM), and the Fail-safe Output driver (FSO).The FSM is electrically independent from the rest of the circuitry, to avoid common cause failure.

For this reason, the FSM has its own voltage regulators (analog and digital), dedicated bandgap, and its own oscillator.

Three power supply pins (VSUP 1, 2, & 3) are used to overtake a pin lift issue. The internal voltage regulators are directly connected on VSUP (one bonding wire per pin is used). Additionally, the ground connection is redundant as well to avoid any loss of ground.

All the voltages generated in the device are monitored by the voltage supervisor (under & overvoltage) due to a dedicated internal voltage reference (different from the one used for the voltage regulators). The result is reported to the MCU through the SPI and delivered to the Fail-safe state machine (FSSM) for action. The FSSM has its own voltage regulator and oscillator. All the safety relevant signals feed the FSSM, which handles the error handling and controls the fail-safe outputs.

There are two fail-safe outputs: RSTB (asserted low to reset the MCU), and FS0B (asserted low to control any fail-safe circuitry).

The Fail-safe machine is in charge of bringing and maintaining the application in a fail-safe state. Four sub fail-safe states are implemented to handle the different kinds of failures, and to give a chance for the system to come back to a normal state.

6.5 Fail-safe Machine State Diagram

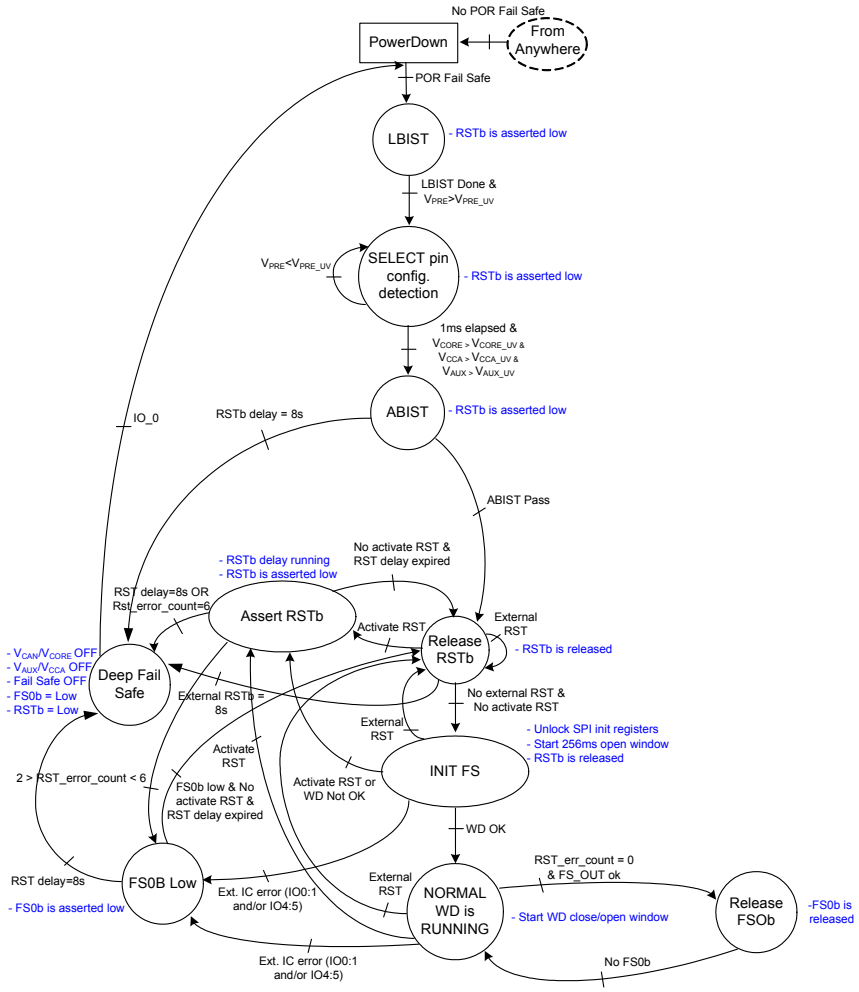


Figure 11. Simplified Fail-safe State Diagram

6.6 Watchdog Operation

A windowed watchdog is implemented in the PowerSBC and is based on "question/answer" principle. The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The error handling and watchdog operations are managed by the Fail-safe state machine. For debugging purpose, this functionality can be inhibited by setting the right voltage on the DEBUG pin at start-up.

The watchdog window duration is selectable through the SPI during the INIT FS phase or in normal mode. The following values are available: 1.0 ms, 2.0 ms, 3.0 ms, 4.0 ms, 6.0 ms, 8.0 ms, 12 ms, 16.0 ms, 24 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms. The watchdog can also be inhibited through the SPI register to allow “reprogramming” (ie.at vehicle level through CAN).

An 8-bit pseudo-random word is generated, due to a Linear Feedback Shift Register implemented in the PowerSBC. The MCU sends the seed of the LFSR during the INIT phase and then uses it to perform a pre-defined calculation. The result is sent through the SPI during the “open” watchdog window and verified by the PowerSBC. When the result is right, the LFSR is incremented and the watchdog window is restarted. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, and an INTB is generated. Any access to the WD register during the “closed” watchdog window is considered a wrong WD refresh.

6.6.1 Normal Operation (First Watchdog Refresh)

At power up, when the RSTB is released as high (after around 13 ms), the INIT phase starts for a maximum duration of 256 ms and this is considered as a fully open watchdog window. During this initialization phase the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the PowerSBC (0xB2), available in the WD_LFSR register (Table 73).

Using this LFSR, the MCU performs a simple calculation based on this formula: the result of this calculation is based on the LSFSR default value: 0x4D.

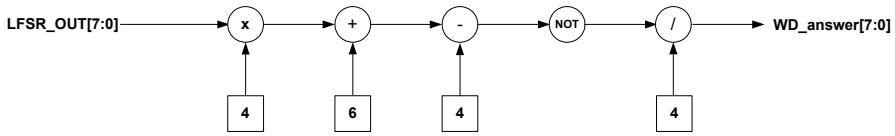


Figure 12. Watchdog Answer Calculation

The MCU sends the results in the WD answer register (Table 75).

When the watchdog is properly refreshed during the open window, the 256 ms open window is stopped and the initialization phase is finished. A new LFSR value is generated and available in the WD_LFSR register (Table 73).

If the watchdog refresh is wrong or if the watchdog is not refreshed during this 256 ms open window (INIT FS phase), the device asserts the reset low and the RSTB error counter is incremented by “1”.

After a good watchdog refresh, the device enters the Normal WD refresh mode, where open and closed windows are defined either by the configuration made during initialization phase in the watchdog window register (Table 71), or by the default value already present in this register (3.0 ms).

6.6.2 Normal Watchdog Refresh

The watchdog must be refreshed during every open window of the window period configured in the register Table 71.

Any WD refresh restarts the window. This ensures the synchronization between MCU and PowerSBC.

The duration of the “window” is selectable through the SPI with no access restriction, means the window duration can be changed in the INIT phase or Normal mode. The duty cycle of the window is set to 50% and is not modifiable.

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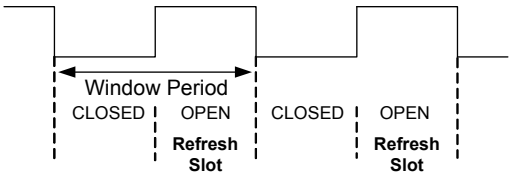


Figure 13. Windowed Watchdog

6.6.3 Watchdog in Debug Mode

When the device is in debug mode (entered via the DEBUG pin), the watchdog continues to operate, but does not affect the device operation by asserting a reset or fail-safe pins. For the user, operation appears without the watchdog. If needed and to debug the watchdog itself, the user can operate as in Normal mode and check LFSR values, the watchdog refresh counter, the watchdog error counter, and reset counter. This allows the user to debug their software and ensure a good watchdog strategy in the application.

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6.7 Wrong Watchdog Refresh Handling

Error counters and strategy are implemented in the device to manage wrong watchdog refreshes from the MCU.

According to consecutive numbers of wrong watchdog refreshes, the device can decide to assert the RSTB only, or to go in deep fail-safe mode where only a Power On Reset or a transition on IO_O helps the system to recover.

6.7.1 Watchdog error counter

The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The WD error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures that a cyclic “OK/NOK” behavior converges to a failure detection.

To allow flexibility in the application, the maximum value of this counter is configurable in the INIT_WD register, but only when device is in INIT FS mode.

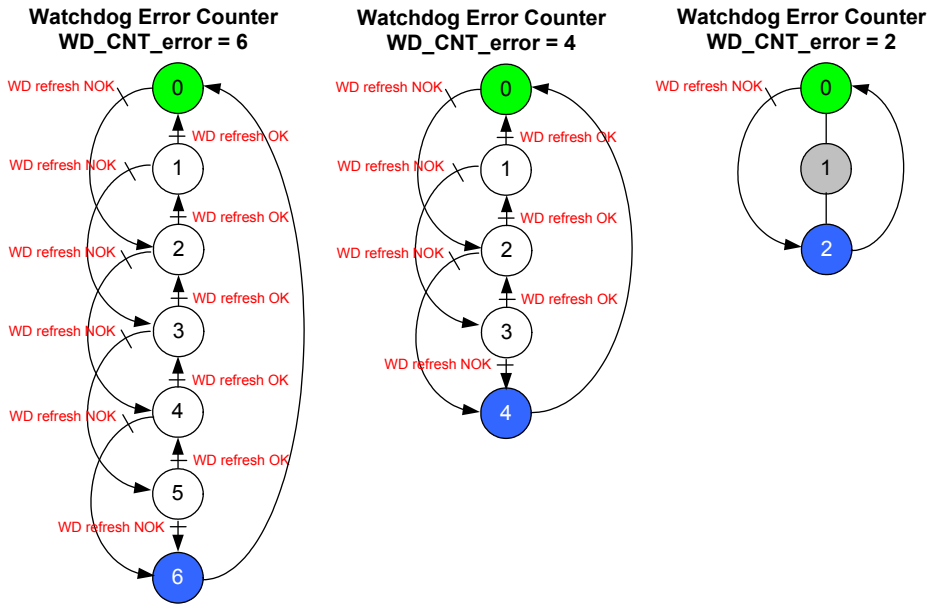


Figure 14. Watchdog Error Counter Configuration (Init_WD register, Bits WD_CNT_error_1:0)

6.7.2 Watchdog Refresh Counter

The watchdog refresh counter is used to decrement the RST error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by “1”.

Each time the watchdog refresh counter reaches “6” and if next WD refresh is also good, the RST error counter is decremented by “1” (case with WD_CNT_refresh_1:0 configured at 6).

Whatever the position is in the watchdog refresh counter, each time there is a wrong refresh watchdog, the watchdog refresh counter is reseted to “0”.

To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable in the INIT_WD register, but only when device is in INIT FS mode.

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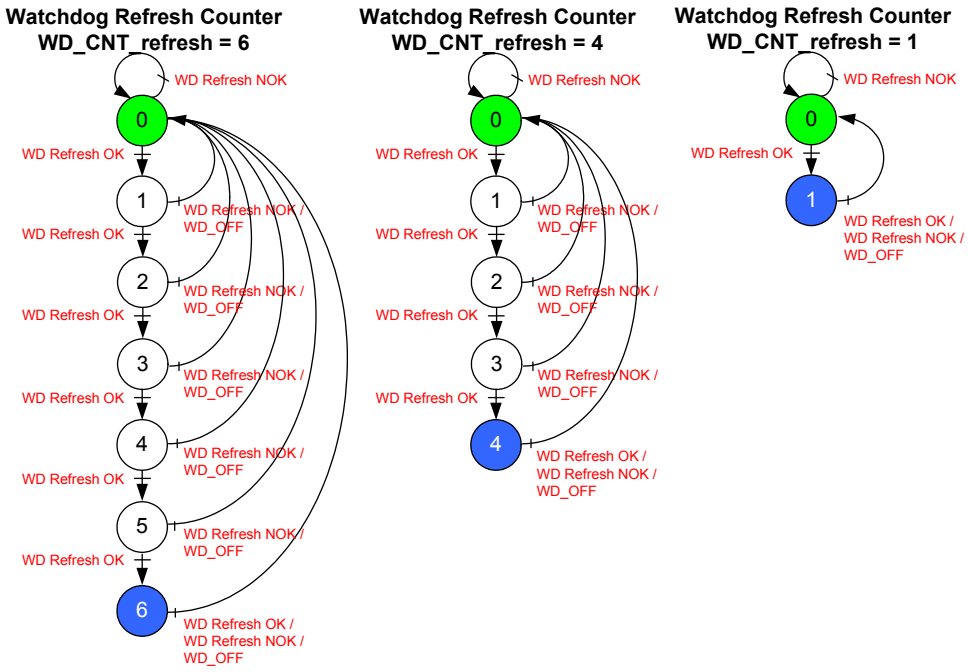


Figure 15. Watchdog Refresh Counter Configuration (Init_WD register, WD_CNT_refresh_1:0)

Table 9. Watchdog Error Table

		WINDOW	
		CLOSED	OPEN
SPI	BAD Key	WD_NOK	WD_NOK
	GOOD Key	WD_NOK	WD_OK
	None (timeout)	No_issue	WD_NOK

Any access to the watchdog register during the “closed” watchdog window is considered as a wrong watchdog refresh. Watchdog timeout, meaning no WD refresh during closed or open windows, is considered as a wrong WD refresh.

6.7.3 Reset Error Counter

The reset error counter manages the reset events and counts the number of resets occurring in the application. This counter is incremented not only for the reset linked to consecutive wrong refresh watchdogs, but also for other sources of reset (undervoltage, overvoltage, external reset).

The RST error counter is incremented by 1, each time a reset is generated.

The reset error counter has two output values (intermediate and final). The intermediate output value is used to handle the transition from reset (RSTB is asserted low) to reset and fail where RSTB and FS0B are activated. The final value is used to handle the transition from reset and fail to deep reset and fail (Deep fail-safe mode), where regulators are off, reset and FS0B are activated, and a power on reset or a transition on IO_0 is needed to recover.

The intermediate value of the reset error counter is configurable to “1” or “3” using the RSTB_err_FS bit in the INIT FSSM2 register (Table 69).

If RSTB_err_FS is set to “0”, it means the device activates FS0B when the reset error counter reaches level “3”.

If RSTB_err_FS is set to “1”, it means the device activates FS0B when the reset error counter reaches level “1”.

This configuration must be done during INIT FS phase.

The final value of the reset error counter is based on the intermediate configuration.

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- RSTB_err_FS = 0 / Intermediate = 3; Final = 6 (Figure 16). When reset error counter reaches 6, the device goes into deep reset and fails.
- RSTB_err_FS = 1 / Intermediate = 1; Final = 2 (Figure 17). When reset error counter reaches 2, the device goes into deep reset and fails.

In any condition, if the RSTB is asserted LOW for a duration longer than eight seconds, the device goes into deep reset and fails.

Conditions that leads to an incrementation of the RSTB error counter, and according to the product configuration are:

- Watchdog error counter = 6
- Watchdog refresh NOK during INIT phase or Watchdog timeout
- IO_23 error detection (FCCU)
- Undervoltage
- Overvoltage
- FS0B shorted to VDD
- SPI DED
- Reset request by the SPI
- External reset

Conditions leading to a transition go to FS, according to the product configuration are:

- IO_01/IO_23/IO_45 error detection
- Undervoltage
- Overvoltage
- Analog BIST fail
- SPI DED
- RSTB shorted to high

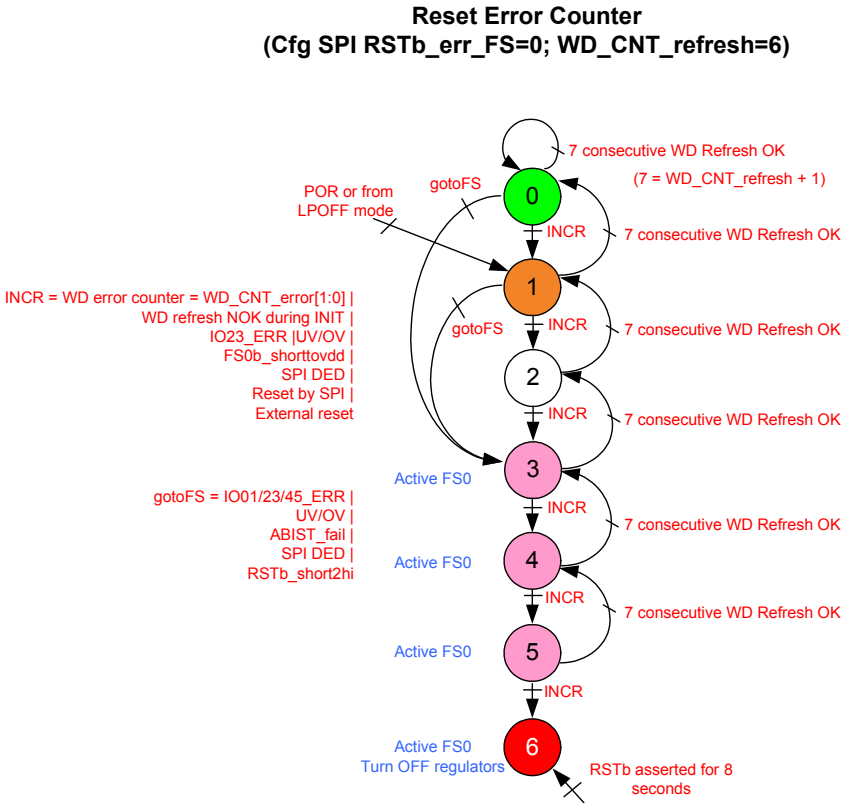


Figure 16. RSTB Error Counter (RSTB_err_FS = 0)

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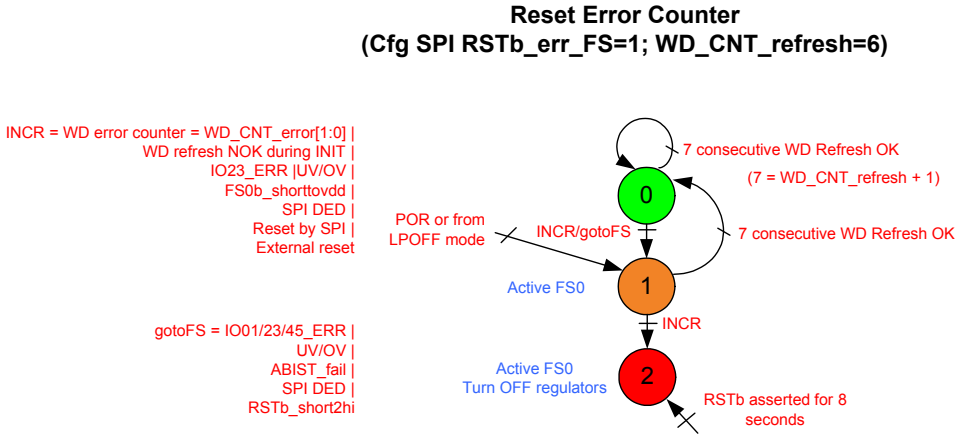


Figure 17. RSTB Error Counter(RSTb_err_FS = 1)

6.7.4 RST Error Counter at Start-up or Resuming from LPOFF Mode

At start-up or when resuming from LPOFF mode the reset error counter starts at level 1 and FS0B is asserted low. To remove activation of FS0B, the RST error counter must go back to value “0” (seven consecutive good watchdog refresh decreases the reset error counter down to 0) and a right command is sent to FS_OUT register (Figure 20).

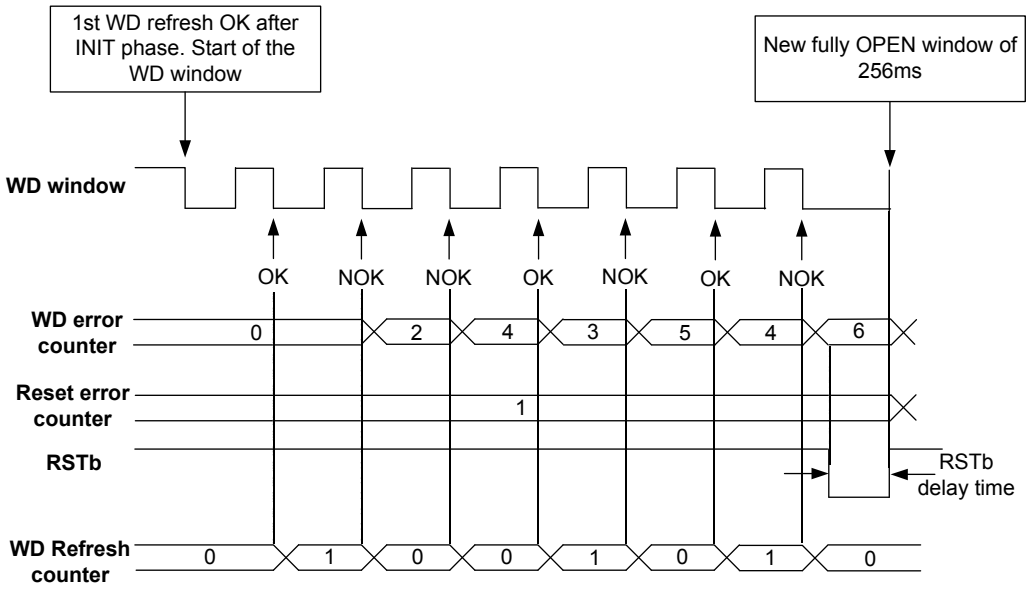


Figure 18. Example of WD Operation Generating a Reset (WD_error_cnt = 6)

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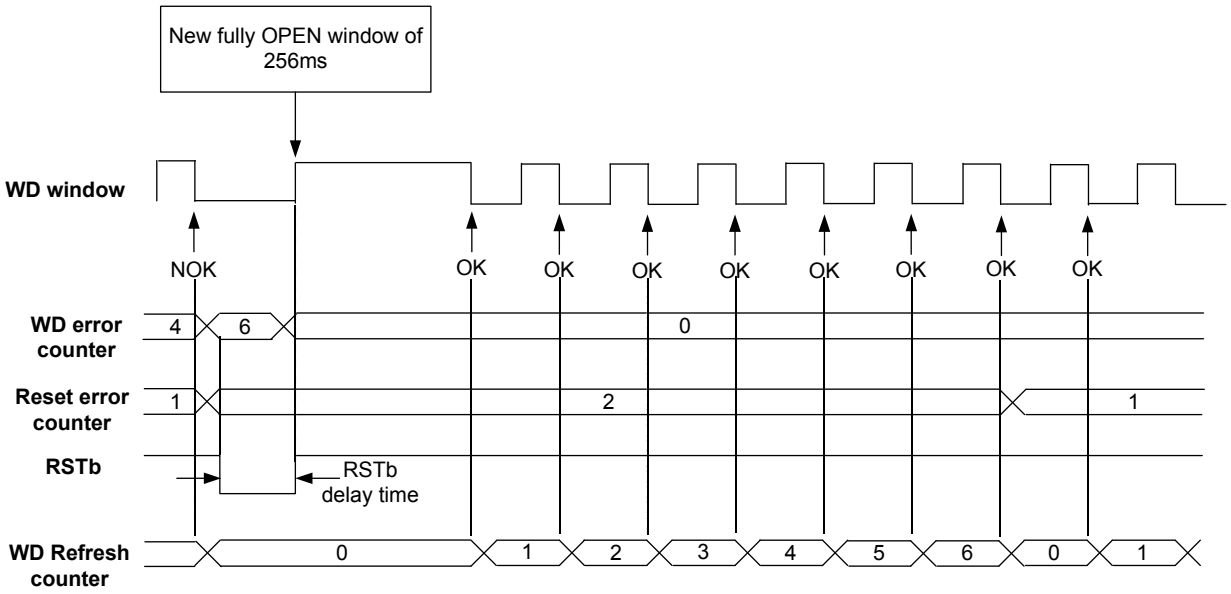


Figure 19. Example of WD Operation Leading a Decrement of the Reset Error Counter (WD_resfresh_cnt = 6)

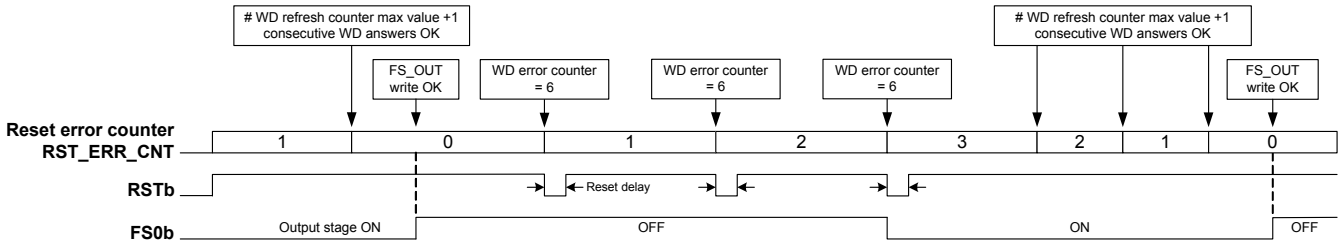


Figure 20. Reset Error Counter and FS0B DEACTIVATION Sequence (RSTB_err_FS = 0 & WD_CNT_error1:0 = 6)

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6.7.5 Fail-safe Output (FS0B) De-activation

When the fail-safe output FS0B is asserted low by the device due to a fault, some conditions must be validated before allowing the FS0B pin to be de-activated by the device.

These conditions are:

- Fault is removed
- Reset error counter must be at “0”
- FS_OUT register must be filled with the right value.

6.7.6 Faults Triggering FS0B Activation

The activation of the FS0B is clearly dependent on the product configuration, but the following items can be settled:

- IO_01/IO_23/IO_45 error detection
- Undervoltage
- Overvoltage
- Analog BIST fail (not configurable)
- SPI DED (not configurable)
- RSTB shorted to high (not configurable)
- RSTB error counter level

6.7.7 SPI DED

Some SPI registers affect some safety critical aspects of the fail-safe functions, and thus are required to be protected against SEU (Single Event Upset). Only fail-safe registers are concerned.

During INIT FS mode, access to fail-safe registers for product configuration is open. Then once the INIT FS phase is over, the Hamming circuitry is activated to protect registers content.

At this stage, if there is 1 single bit flip, the detection is made due to hamming code, and the error is corrected automatically (fully transparent for the user), and a flag is sent. If there are two errors (DED - Dual Error Detection), the detection is made due to hamming code but detected errors cannot be corrected. Flag is sent, RSTB and FS0B are activated.

6.7.8 FS_OUT Register

When fault is removed and reset error counter changes back to level “0”, a right word must be filled in the FS_OUT register. The value is dependant on the current WD_LFSR.

LSB and MSB must be swapped and negative operation per bit must be applied.

WD_LFSR_7:0=	b7	b6	b5	b4	b3	b2	b1	b0
FS_OUT_7:0 =	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$

Figure 21. FS_OUT Register Based on LFSR Value

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6.7.9 INPUT VOLTAGE RANGE

Due to the flexibility of the pre-regulator, the device can cover a wide battery input voltage range. However, a more standard voltage range can still be covered using only the Buck configuration.

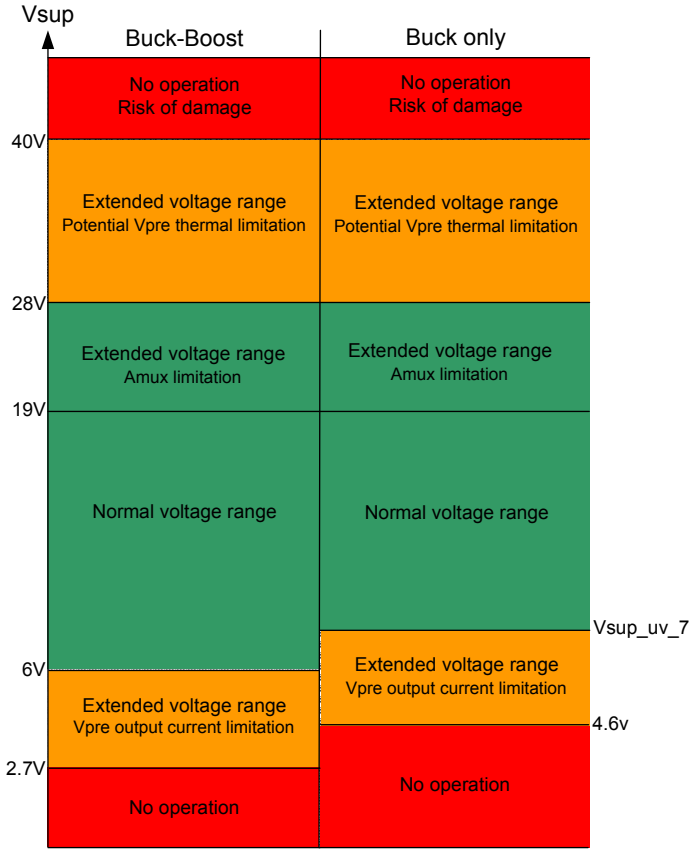


Figure 22. Input Voltage Range

- V_{SUP} > 28 V : Potential V_{PRE} thermal limitation
  RDSON, Current limitation and Overcurrent detection are specified for V_{SUP} < 28 V
- V_{SUP} < 19 V : Mux_out limitation
  IO_0 and IO_1 maximum analog input voltage range is 19 V
  Internal 2.5 V reference voltage accuracy degraded
- Buck only, V_{SUP} < $V_{SUP_UV_7}$:
  CAN communication is guaranteed for V_{SUP} > 6.0 V
  For V_{CCA} and V_{AUX} 5.0 V configuration, under voltage triggers at low V_{SUP} (refer to $V_{CCA_UV_5}$ and $V_{AUX_UV_5}$)

6.7.10 V_{pre} Voltage Pre-regulator

A highly flexible SMPS pre-regulator is implemented in the 33907_8. Depending on the input voltage requirement, the device can be configured as “Non-inverting Buck-boost converter” (Figure 24) or “Standard Buck converter” (Figure 23). An external low side MOSFET (N-type) is required to operate in “Non-inverting Buck-boost converter”. The connection of the external MOSFET is detected automatically during the start-up phase.

The converter operates in Current Control mode in any configuration. The high side switching MOSFET is integrated to make the current control easier. The PWM frequency is fixed at 440 kHz typical. The compensation network is fully integrated. The output voltage (V_{PRE}) is regulated between 6.0 V and 7.0 V.

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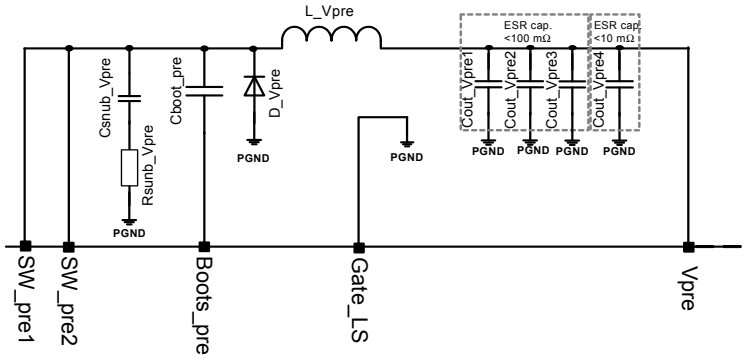


Figure 23. Pre-regulator: Buck configuration

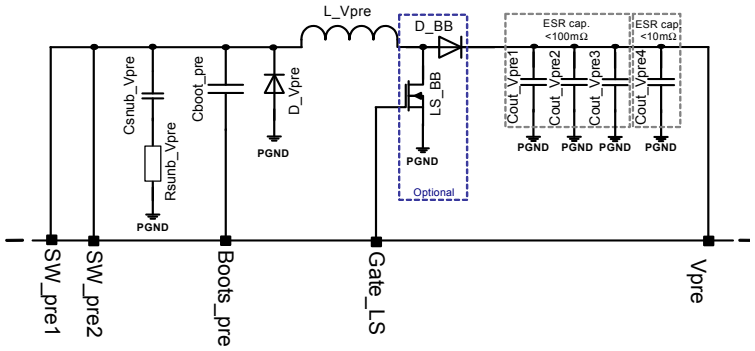


Figure 24. Pre-regulator: Buck Boost configuration

Transition between buck mode and boost mode is based on hysteresis (Figure 25).

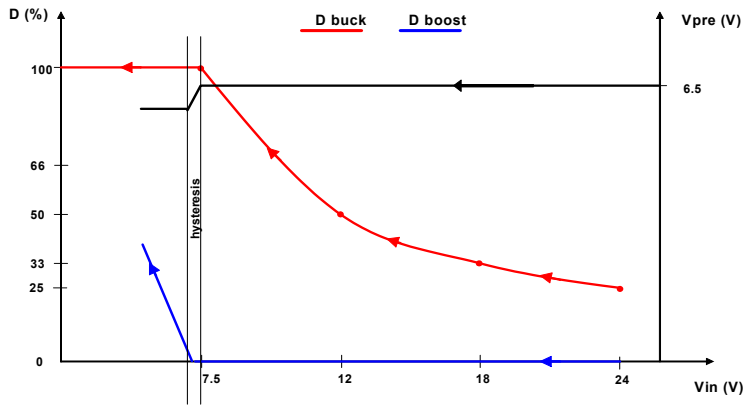


Figure 25. Transition between Buck and Boost

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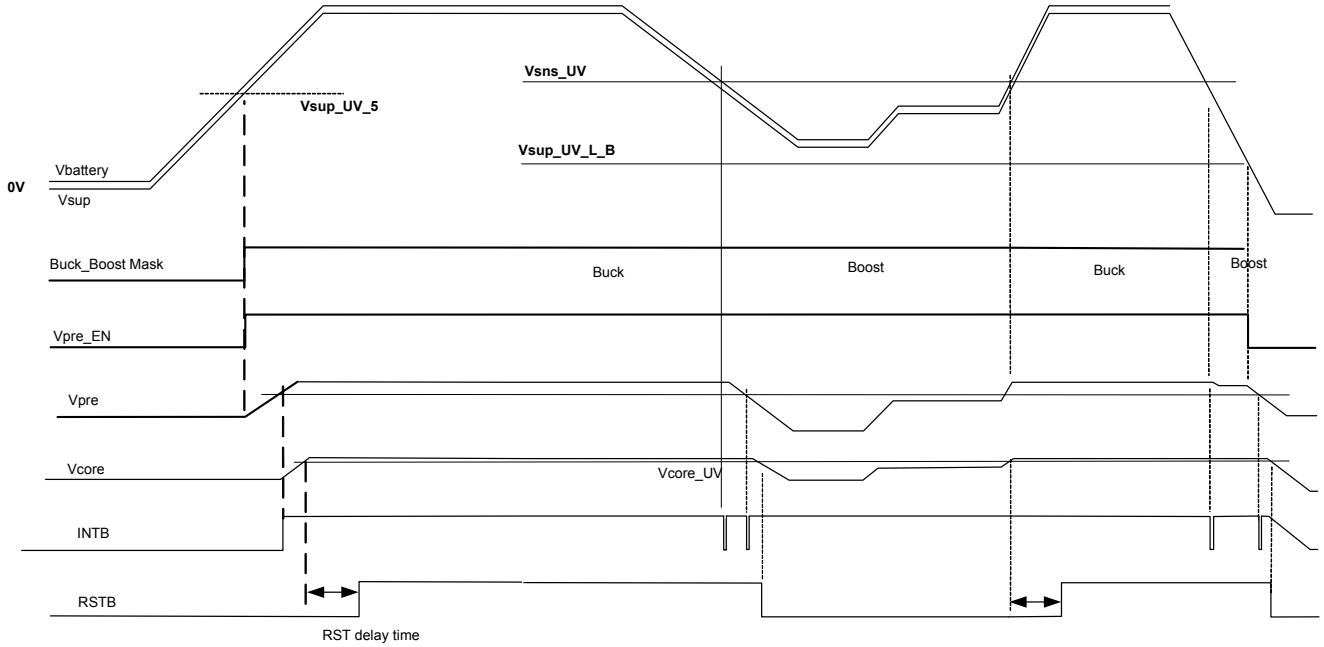


Figure 26. Buck Configuration Power-up and Power-down

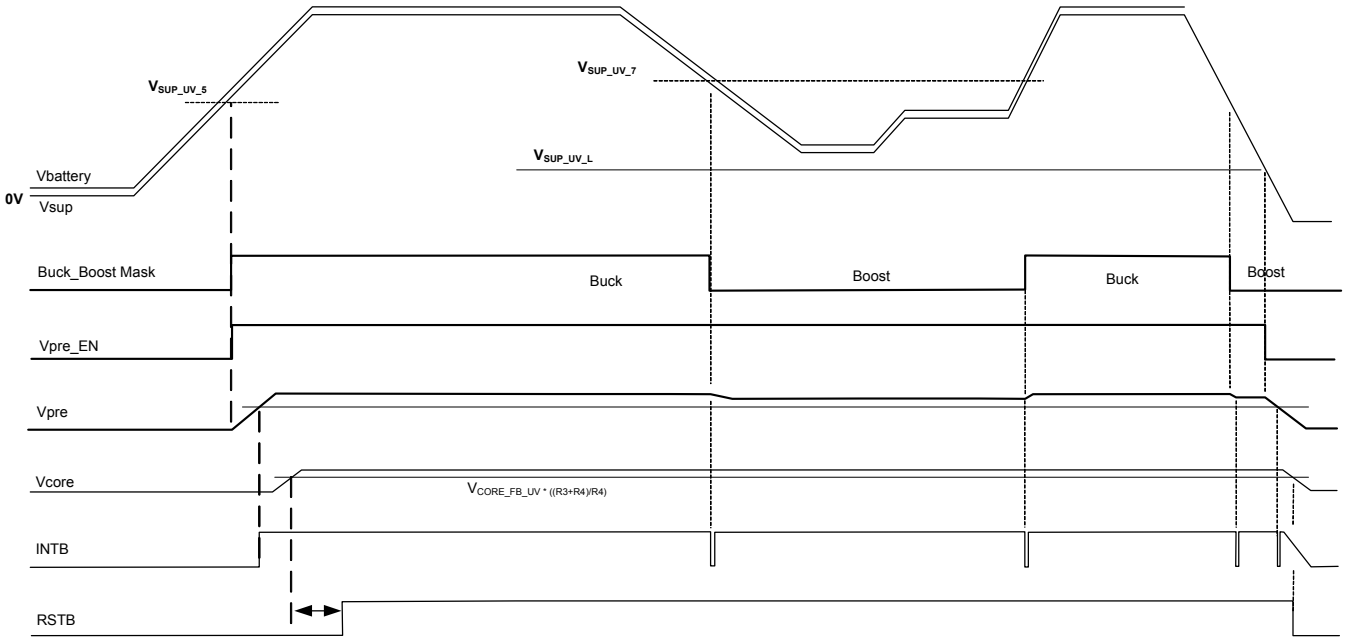


Figure 27. Buck Boost Configuration Power-up and Power-down

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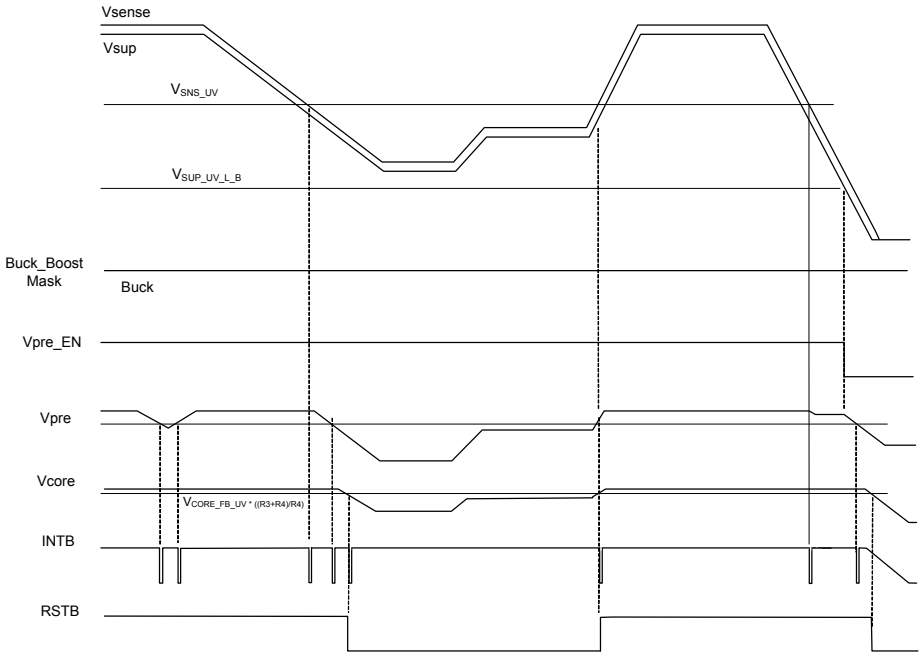


Figure 28. Behavior During a Cranking (Buck Configuration)

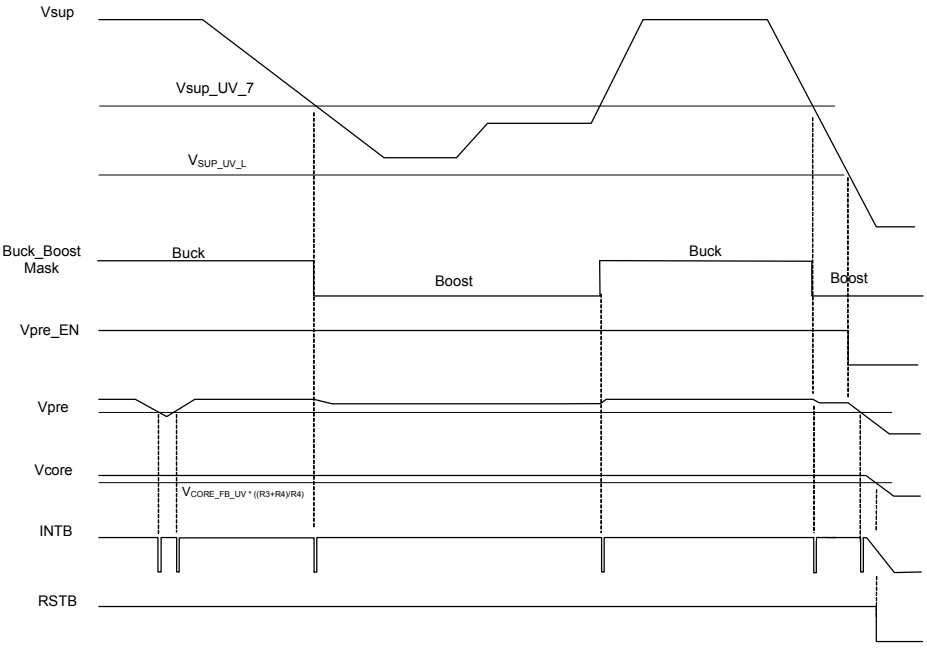


Figure 29. Behavior During a Cranking (Buck Boost Configuration)

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In order to improve the efficiency, the converter switches automatically to burst mode in light load condition. Moreover, the battery voltage sensing (V_{SENSE}) is used to manage the load dump condition. An input power feed forward function is also implemented to minimize the switching losses during the load dump.

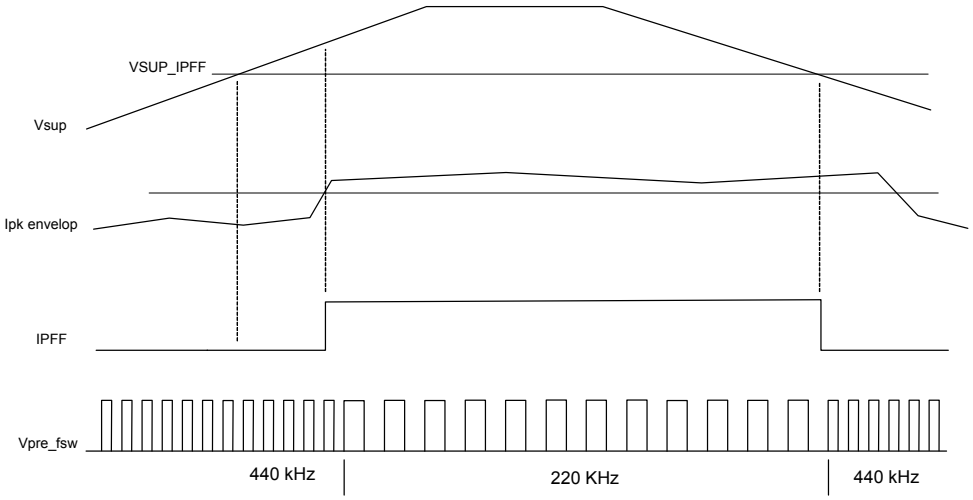


Figure 30. Input Power Feed Forward Principle

6.7.11 V_{core} Voltage Regulator

This voltage regulator is a step-down DC-DC converter operating in Voltage Control mode. The switching MOSFET is integrated. The PWM frequency is fixed at 2.4 MHz typical. The high side MOSFET is integrated in the device. The output voltage is configured for 1.2 V and 3.3 V, due to an external resistor divider connected between V_{CORE} and the feedback pin (FB-CORE) (Figure 34). The expected accuracy is ±2.0%. The output current is up to 0.8 A for the 33907 and 1.5 A for the 33908 device. The stability of the overall converter is done externally by the pin COMP_CORE.

In order to improve the efficiency, the converter switches automatically in burst mode in light load condition.

6.7.12 Charge Pump and Bootstrap

Both switching MOSFETs of V_{PRE} and V_{CORE} SMPS are driven by external bootstrap capacitors. Additionally, a charge pump is implemented to ensure 100% duty cycle for both converters. Each converter uses a 100 nF external capacitor minimum to operate properly.

6.7.13 V_{CCA} Voltage Regulator

V_{CCA} is a linear voltage regulator mainly dedicated to supply the MCU I/Os, especially the ADC. The output voltage is selectable at 5.0 V or 3.3 V. Since this output voltage can be used to supply MCU IOs, the output voltage selection is done using an external resistor connected to the SELECT pin and ground if V_{AUX} is used. When V_{AUX} is not used, the resistor is connected between the SELECT pin and V_{PRE}.

The expected accuracy is +/- 1% for 5 V configuration and +/- 1.5% for 3.3 V configuration with an output current capability at 100 mA.

An external PNP transistor is used to boost the current capability up to 300 mA. When an external PNP is used, the connection is detected automatically during the start-up sequence of the PowerSBC. In such condition, the internal pass transistor is switched OFF and all the current is driven through the external PNP to reduce the internal power dissipation. The output voltage accuracy with an external PNP is reduced to ±3.0%. The V_{CCA} output voltage is used as a reference for the Auxiliary voltage supply (V_{AUX}) when used as sensor supply output.

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6.7.14 V_{AUX} Voltage Regulator

V_{AUX} is a highly flexible linear voltage regulator either as an auxiliary supply dedicated to additional device in the ECU or as a sensor supply (i.e. outside the ECU). As an auxiliary supply, the output voltage is selectable between 5.0 V, 3.3 V. Since this voltage rail can be used to supply IOs, the selection is done with an external resistor connected between the SELECT pin and ground.

In such case, the expected accuracy is ±3.0%. The output current capability is up to 300 mA. An external PNP transistor must be used (no internal current capability).

As a sensor supply rail, the output voltage is selectable between 5.0 V and 3.3 V.

Moreover V_{CCA} can be used as reference for the sensor supply used as tracker. The selection is also done during the INIT phase and secured. The tracking accuracy is expected to be ±15 mV.

6.8 Startup Sequence

In order to provide a safe and well known startup sequence, the 33907_8 includes an undervoltage lock-out. This undervoltage lock-out is only applicable when the device is under a Power-On-Reset condition, which means the initial condition is V_{SUP} < $V_{SUP_UV_L}$ (i.e. below 2.7 V max). In all the other conditions (i.e. LPOFF), the device is able to operate (and therefore to (re)start) down to $V_{SUP_UV_L}$. The other different voltage rails automatically start, as described in the following figure.

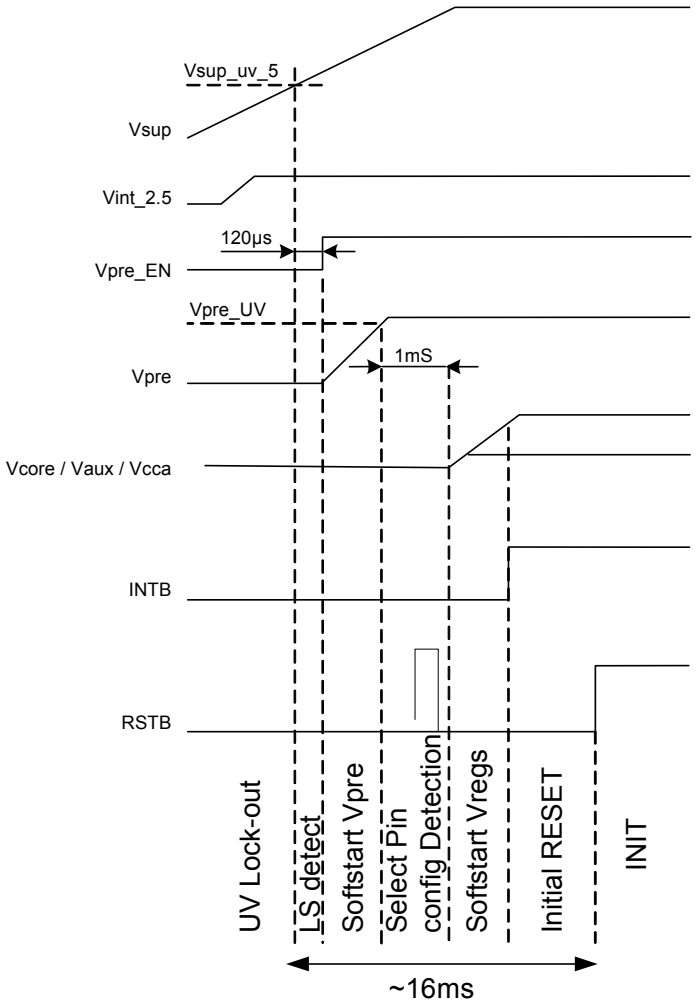


Figure 31. Start-up Scheme

The final value of V_{AUX} and V_{CCA} depends on the hardware configuration (resistor values on the SELECT pin).

It takes around 13 ms to release the RSTB. RSTB can be pulled low after those 13 ms by the MCU, if it is not ready to run after power up.

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7 Serial Peripheral Interface

7.1 High Level Overview

7.1.1 SPI

The device is using a 16 bits SPI, with the following arrangement:

MOSI, Master Out Slave In bits:

- Bit 15 read/write
- Bit 14 Main or fail-safe register target
- bit 13 to 9 (A4 to A0) to select the register address. Bit 8 is a parity bit in write mode, Next bit (=0) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0(Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

Figure 32 is an overview of the SPI implementation.

7.1.2 Parity Bit 8 Calculation:

The parity is used for write to register command (bit 15,14 = 01). It is calculated based on the number of logic ones contained in bits 15-9,7-0 sequence (this is the whole 16 bits of the write command except bit 8).

Bit 8 must be set to 0 if the number of 1 is odd.

Bit 8 must be set to 1 if the number of 1 is even.

7.1.3 Device Status on MISO

When a write operation is performed to store data or control bit into the device, MISO pin reports a 16 bit fixed device status composed of 2 bytes: Device Fixed Status (bits 15 to 8) + extended Device Status (bits 7 to 0). In a read operation, MISO reports the fixed device status (bits 15 to 8), and the next 8 bits are content of the selected register. A standard serial peripheral interface (SPI) is integrated to allow bi-directional communication between the 33907_8 and the MCU. The SPI is used for configuration and diagnostic purposes.

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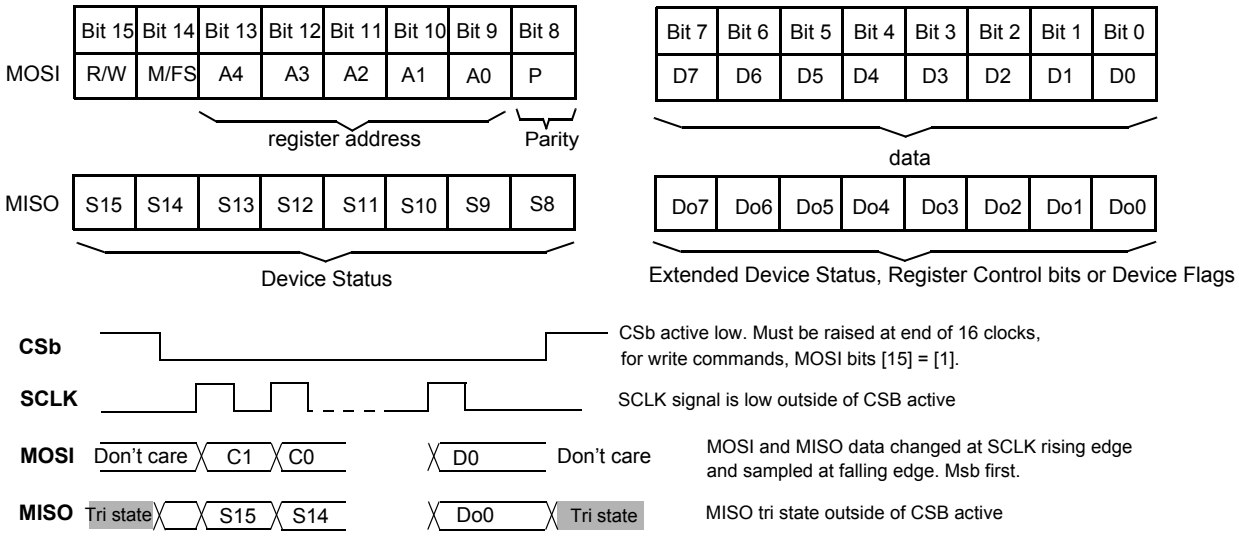


Figure 32. SPI Overview

The device contains several registers. Their address is coded on 7 bits (bits 15 to 9). Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior. Every register can also be read back in order to ensure that its content (default setting or value previously written) is correct.

7.1.4 Register Description

Although the minimum time between two NCS low sequences is defined by t_{ONNCS} (Figure 33), two consecutive accesses to the fail-safe registers must be done with a 3.5 µs minimum NCS high time in between.

Although the minimum time between two fail-safe registers accesses is 3.5 µs, some SPI accesses to the main registers can be done in between (Figure 34)

7.2 Detail Operation

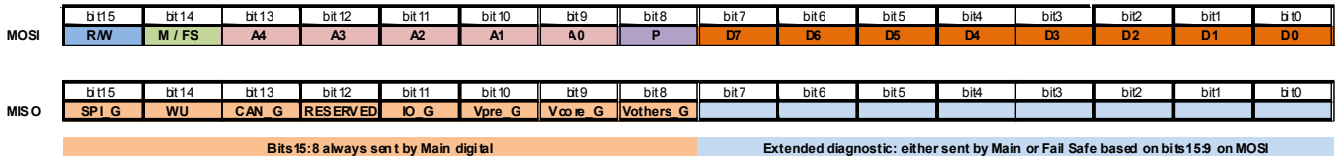


Figure 33. MOSI / MISO SPI Command Organization

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Table 10. MOSI Bits Description

R / W	Description	Set if it is a READ or WRITE Command
	0	READ
	1	WRITE
M / FS	Description	Split the addresses between Fail-safe State machine and Main Logic
	0	Main
	1	Fail-safe
A4:0	Description	Set the address to Read or Write
	0	See Register Mapping
	1	
P	Description	Parity bit (only use in Write mode). Set to 0 in Read mode
	0	Number of “1” (bit15:9 and bit 7:0) is odd
	1	Number of “1” (bit15:9) and bit 7:0) is even
D7:0	Description	Data in Write mode. Shall be set to 00h in Read mode
	0	See register details
	1	

Table 11. MISO Bits Description

SPI_G	Description	Report an error in the SPI communication
	0	NO Failure
	1	Failure
	Reset Condition	Power On Reset / When initial event cleared on read
WU	Description	Report a wake-up event. Logical OR of ALL wake-up sources
	0	NO WU event
	1	WU event
	Reset Condition	Power On Reset / When initial event cleared on read
CAN_G	Description	Report a CAN event (Diagnostic)
	0	NO event
	1	CAN event
	Reset Condition	Power On Reset / When initial event cleared on read
IO_G	Description	Report a change in IOs state
	0	NO IO transition
	1	IO transition
	Reset Condition	Power On Reset / When initial event cleared on Read
VPRE_G	Description	Report an event from Vpre-regulator and battery monitoring (Status change or failure)
	0	NO event
	1	Event occurred
	Reset Condition	Power On Reset / When initial event cleared on Read

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Table 11. MISO Bits Description (continued)

VCORE_G	Description	Report an event from V_{CORE} regulator (Status change or failure)
	0	NO event
	1	Event occurred
	Reset Condition	Power On Reset / When initial event cleared on Read
VOTHERS_G	Description	Report an event from V_{CCA}, V_{AUX}, or V_{CAN} regulators (Status change or failure)
	0	NO event
	1	Event occurred
	Reset Condition	Power On Reset / When initial event cleared on Read

7.2.1 Register Address Table

Table 12 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for main logic.

Table 12. Register Mapping of Main Logic

	Address								
Register	**FS/M**	**A4**	**A3**	**A2**	**A1**	**A0**	**Hex**	**Write description**	**Table Ref**
NOT USED	0	0	0	0	0	0	#0(00h)	N/A	N/A
INIT Vreg 1	0	0	0	0	0	1	#1(01h)	Write during INIT phase then read only	Table 15
INIT Vreg2	0	0	0	0	1	0	#2(02h)	Write during INIT phase then read only	Table 17
INIT CAN	0	0	0	0	1	1	#3(03h)	Write during INIT phase then read only	Table 19
INIT IO_WU1	0	0	0	1	0	0	#4(04h)	Write during INIT phase then read only	Table 21
INIT IO_WU2	0	0	0	1	0	1	#5(05h)	Write during INIT phase then read only	Table 23
INIT INT	0	0	0	1	1	0	#6(06h)	Write during INIT phase then read only	Table 25
NOT USED	0	0	0	1	1	1	#7(07h)	N/A	N/A
HW Config	0	0	1	0	0	0	#8(08h)	Read only	Table 27
WU source	0	0	1	0	0	1	#9(09h)	Read only	Table 29
NOT USED	0	0	1	0	1	0	#10(0Ah)	N/A	N/A
IO_input	0	0	1	0	1	1	#11(0Bh)	Read only	Table 31
Status Vreg#1	0	0	1	1	0	0	#12(0Ch)	Read only	Table 33
Status Vreg#2	0	0	1	1	0	1	#13(0Dh)	Read only	Table 35
Diag Vreg#1	0	0	1	1	1	0	#14(0Eh)	Read only	Table 37
Diag Vreg#2	0	0	1	1	1	1	#15(0Fh)	Read only	Table 39
Diag Vreg#3	0	1	0	0	0	0	#16(10h)	Read only	Table 41
Diag CAN1	0	1	0	0	0	1	#17(11h)	Read only	Table 43
Diag CAN2	0	1	0	0	1	0	#18(12h)	Read only	Table 45
Diag SPI	0	1	0	0	1	1	#19(13h)	Read only	Table 48
NOT USED	0	1	0	1	0	0	#20(14h)	N/A	N/A

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Table 12. Register Mapping of Main Logic

	Address							
Register	**FS/M**	**A4**	**A3**	**A2**	**A1**	**A0**	**Hex**	**Write description**	**Table Ref**
MODE	0	1	0	1	0	1	#21(15h)	Write during Normal and Read	Table 50
Vreg_mode	0	1	0	1	1	0	#22(16h)	Write during Normal and Read	Table 52
IO_OUT/AMUX	0	1	0	1	1	1	#23(17h)	Write during Normal and Read	Table 54
CAN Mode	0	1	1	0	0	0	#24(18h)	Write during Normal and Read	Table 56
CAN Mode 2	0	1	1	0	0	1	#25(19h)	Write during Normal and Read	Table 58

Table 13 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for Main logic

Table 13. Register Mapping of Fail-safe Logic

	Address							
Register	**FS/M**	**A4**	**A3**	**A2**	**A1**	**A0**	**Hex**	**Write description**	**Table Ref**
INIT Supervisor#1	1	0	0	0	0	1	#33(21h)	Write during INIT phase then Read only	Table 60
INIT Supervisor#2	1	0	0	0	1	0	#34(22h)	Write during INIT phase then Read only	Table 62
INIT Supervisor#3	1	0	0	0	1	1	#35(23h)	Write during INIT phase then Read only	Table 64
INIT FSSM#1	1	0	0	1	0	0	#36(24h)	Write during INIT phase then Read only	Table 66
INIT FSSM#2	1	0	0	1	0	1	#37(25h)	Write during INIT phase then Read only	Table 68
WD_Window	1	0	0	1	1	0	#38(26h)	Write (No restriction) and Read	Table 70
WD_LFSR	1	0	0	1	1	1	#39(27h)	Write (No restriction) and Read	Table 72
WD_answer	1	0	1	0	0	0	#40(28h)	Write (No restriction) and Read	Table 74
FS_OUT	1	0	1	0	0	1	#41(29h)	Write (No restriction)	Table 76
RSTb request	1	0	1	0	1	0	#42(2Ah)	Write (No restriction)	Table 78
INIT WD	1	0	1	0	1	1	#43(2Bh)	Write during INIT phase then Read only	Table 80
Diag FS1	1	0	1	1	0	0	#44(2Ch)	Read only	Table 82
WD_Counter	1	0	1	1	0	1	#45(2Dh)	Read only	Table 84
Diag_FS2	1	0	1	1	1	0	#46(2Eh)	Read only	Table 86

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7.2.2 Secured SPI Command

Some SPI commands must be secured to avoid unwanted change of the critical bits.
In the fail-safe machine and in the main state machine, the secured bits are calculated from the data bits sent as follows:

Table 14. Secured SPI

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data 3	Data 2	Data 1	Data 0	Secure 3	Secure2	Secure 1	Secure 0

- Secure 3 = NOT(Bit5)
- Secure 2 = NOT(Bit4)
- Secure 1 = Bit7
- Secure 0 = Bit6

7.3 Detail of Register Mapping

Default value of the reserved bit must be "0".

7.3.1 Init VREG 1

Table 15. INIT VREG1 Register Configuration

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	0	0	1	P	0	Reserved	Ipff_DIS	Vpre_DIS	0	0	Reserved	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Reserved	Ipff_DIS	Vpre_DIS	0	0	Reserved	0
Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	1	Ipff_DIS	Vpre_DIS	0	0	1	0

Table 16. Description and Configuration of the Bits (Default value in blue)

IPFF_DIS	Description	DISABLE the input Power Feed Forward (IPFF) function of Vpre
	0	ENABLED
	1	DISABLED
	Reset condition	Power On Reset
Vpre_DIS	Description	DISABLE Vpre SMPS (in all mode).
	0	ENABLED
	1	DISABLED
	Reset condition	Power On Reset

7.3.2 Init Vreg 2

Table 17. INIT VREG2 Register Configuration

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	0	1	0	P	0	Tcca_lim_off	Icca_lim	0	reserved	Taux_lim_off	Vaux_trk_EN	reserved
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Tcca_lim_off	Icca_lim	0	reserved	Taux_lim_off	Vaux_trk_EN	reserved

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Table 17. INIT VREG2 Register Configuration

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	Tcca_lim_off	Icca_lim	0	reserved	Taux_lim_off	Vaux_trk_EN	reserved

Table 18. INIT VREG2. Description and Configuration of the Bits (Default value in blue)

Tcca_lim_off	Description	Configure the current limitation duration before regulator is switched off. Only used for external PNP
	0	10 ms
	1	50 ms
	Reset condition	Power On Reset
Icca_lim	Description	Configure the current limitation threshold. Only available for external PNP
	0	Icca_lim_in
	1	Icca_lim_out
	Reset condition	Power On Reset
Taux_lim_off	Description	Configure the current limitation duration before regulator is switched off. Only used for external PNP
	0	10 ms
	1	50 ms
	Reset condition	Power On Reset
Vaux_trk_EN	Description	Configure Vaux regulator as a tracker
	0	No tracking. HW configuration is used
	1	Tracking enabled
	Reset condition	Power On Reset

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7.3.3 Init CAN

Table 19. INIT CAN Register Description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	0	1	1	P	0	CAN_wu_conf	Reserved	CAN_TOY	CAN_wu_TO	reserved	reserved	reserved
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	CAN_wu_conf	Reserved	CAN_TOY	CAN_wu_TO	reserved	reserved	reserved

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

Table 19. INIT CAN Register Description

MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	CAN_wu_conf	0	CAN_TOY	CAN_wu_TO	reserved	reserved	reserved

Table 20. INIT CAN. Description and Configuration of the Bits (Default value in blue)

CAN_wu_conf	Description	Define the CAN wake-up mechanism
	0	3 dominant pulses
	1	Single dominant pulse
	Reset condition	Power On Reset
CAN_TOY	Description	Configure the CAN block to be compliant with TOYOTA specification
	0	Standard CAN
	1	Toyota compliance
	Reset condition	Power On Reset
CAN_wu_to	Description	Define the CAN wake-up time-out (in case of CAN_wu_conf=0)
	0	120 µs
	1	360 µs
	Reset condition	Power On Reset

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7.3.4 INIT IO_WU1

Table 21. INIT IO_WU1 Register Description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	1	0	0	P	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU_2_1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU-2-1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0
Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_0_1	WU_0_0	WU_1_1	WU_1_0	WU-2-1	WU_2_0	INT_inh_IO_1	INT_inh_IO_0

Table 22. INIT IO_WU1. Description and Configuration of the Bits (Default value in blue)

WU_0_1:0	Description	Wake-up configuration for IO_0
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset
WU_1_1:0	Description	Wake-up configuration for IO_1
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset
WU_2_1:0	Description	Wake-up configuration for IO_2
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset
INT_inh_IO_1	Description	Inhibit the INT pulse for IO_1. IO_1 masked in IO_G. Avoid INT when used in FS
	0	INT NOT masked
	1	INT masked
	Reset condition	Power On Reset

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Table 22. INIT IO_WU1. Description and Configuration of the Bits (Default value in blue) (continued)

INT_inh_IO_0	Description	Inhibit the INT pulse for IO_0. IO_0 masked in IO_G. Avoid INT when used in FS
	0	INT NOT masked
	1	INT masked
	Reset condition	Power On Reset

7.3.5 INIT IO_WU2

Table 23. INIT IO_WU2 Register Description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	1	0	1	P	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45
Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WU_3_1	WU_3_0	WU_4_1	WU_4_0	WU_5_1	WU_5_0	INT_inh_IO_23	INT_inh_IO_45

Table 24. INIT IO_WU2. Description and Configuration of the Bits (Default value in blue)

WU_3_1:0	Description	Wake-up configuration for IO_3
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset
WU_4_1:0	Description	Wake-up configuration for IO_4
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset

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Table 24. INIT IO_WU2. Description and Configuration of the Bits (Default value in blue) (continued)

WU_5_1:0	Description	Wake-up configuration for IO_5
	0 0	NO wake-up capability
	0 1	Wake-up on rising edge only
	1 0	Wake-up on falling edge only
	1 1	Wake-up on any edge
	Reset condition	Power On Reset
INT_inh_IO_45	Description	Inhibit the INT pulse for IO_4 & IO_5. IO_4 & IO_5 masked in IO_G. Avoid INT when used in FS
	0	INT NOT masked
	1	INT masked
	Reset condition	Power On Reset
INT_inh_IO_23	Description	Inhibit the INT pulse for IO_2 & IO_3. IO_2 & IO_3 masked in IO_G. Avoid INT when used in FS
	0	INT NOT masked
	1	INT masked
	Reset condition	Power On Reset

7.3.6 INIT INT

Table 25. INIT INT Register Description

Write																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	1	0	0	0	1	1	0	P	INT_duration	reserved	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	reserved
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	INT_duration	0	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	0

Read																
	bit15	**bit14**	**bit13**	**bit12**	**bit11**	**bit10**	**bit9**	**bit8**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
MOSI	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	INT_duration	0	INT_inh_all	INT_inh_Vsns	INT_inh_Vpre	INT_inh_Vcore	INT_inh_Vothers	0

Table 26. INIT INT. Description and Configuration of the Bits (Default value in blue)

INT_duration	Description	Define the duration of the INTerrupt pulse
	0	100 µs
	1	25 µs
	Reset condition	Power On Reset

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Table 26. INIT INT. Description and Configuration of the Bits (Default value in blue) (continued)

INT_inh_all	Description	Inhibit ALL the INT
	0	All INT sources
	1	inhibit ALL INT
	Reset condition	Power On Reset
INT_inh_Vsns	Description	Inhibit the INT for V_{SNS_UV}
	0	All INT sources
	1	inhibit V_{SNS_UV}
	Reset condition	Power On Reset
INT_inh_Vpre	Description	Inhibit the INT for Vpre status event (cf. register status Vreg1)
	0	All INT sources
	1	Vpre status changed INHIBITED
	Reset condition	Power On Reset
INT_inh_Vcore	Description	Inhibit the INT for Vcore status event (cf. register status Vreg2)
	0	All INT sources
	1	Vcore status changed INHIBITED
	Reset condition	Power On Reset
INT_inh_Vothers	Description	Inhibit the INT for V_{CCA} / V_{AUX} and V_{CAN} status event (cf. register status Vreg2)
	0	All INT sources
	1	V_{CCA} / V_{AUX} / V_{CAN} status changed INHIBITED
	Reset condition	Power On Reset

7.3.7 HW Config

Table 27. HW Config Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	LS_detect	Vaux not used	Vcca_PNP_detect	Vcca_HW	Vaux_HW	x	0	DBG

Table 28. HW Config. Description and Configuration of the Bits (Default value in blue)

LS_detect	Description	Report the hardware configuration of Vpre (Buck only or Buck-Boost)
	0	Buck-Boost
	1	Buck only
	Reset condition	Power On Reset / Refresh after LPOFF
Vaux not used	Description	Report if Vaux is used
	0	Vaux is used (external PNP is assumed to be connected, Vaux can be switched OFF/ON through SPI)
	1	Vaux is not used
	Reset condition	Power On Reset / Refresh after LPOFF

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Table 28. HW Config. Description and Configuration of the Bits (Default value in blue) (continued)

Vcca_PNP_detect	Description	Report the connection of an external PNP on Vcca
	0	External PNP connected
	1	Internal MOSFET
	Reset condition	Power On Reset / Refresh after LPOFF
Vcca_HW	Description	Report the hardware configuration for Vcca
	0	3.3 V
	1	5 V
	Reset condition	Power On Reset / Refresh after LPOFF
Vaux_HW 1:0	Description	Report the hardware configuration for Vaux
	0	5 V
	1	3.3 V
	Reset condition	Power On Reset / Refresh after LPOFF
DBG	Description	Report the configuration of the DEBUG mode
	0	Normal operation
	1	DEBUG mode selected
	Reset condition	Power On Reset / Refresh after LPOFF

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WU SOURCE

Table 29. WU SOURCE Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_5_WU	IO_4_WU	IO_3_WU	IO_2_WU	IO_1_WU	IO_0_WU	Vreg_WU	Phy_WU

Table 30. WU source. Description and Configuration of the Bits (Default value in blue)

IO_5_WU	Description	Report a wake-up event from IO_5
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_4_WU	Description	Report a wake-up event from IO_4
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_3_WU	Description	Report a wake-up event from IO_3
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_2_WU	Description	Report a wake-up event from IO_2
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_1_WU	Description	Report a wake-up event from IO_1
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
IO_0_WU	Description	Report a wake-up event from IO_0
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset / Read
Phy_WU	Description	Report a wake-up event from CAN
	0	No Wake-up
	1	WU event detected
	Reset condition	Power On Reset/ Read CAN_wu

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IO INPUT

Table 31. IO INPUT Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_5	IO_4	0	IO_3	IO_2	0	IO_1	IO_0

Table 32. IO input. Description and Configuration of the Bits

IO_5	Description	Report IO_5 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_4	Description	Report IO_4 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_3	Description	Report IO_3 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_2	Description	Report IO_2 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_1	Description	Report IO_1 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset
IO_0	Description	Report IO_0 digital state in Normal mode. No update in LPOFF mode since wake-up features available
	0	Low
	1	High
	Reset condition	Power On Reset

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STATUS VREG1

Table 33. STATUS VREG1 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IpFF	Ilim_pre	Twarm_pre	BoB	Vpre_state	0	0	0

Table 34. Status Vreg1. Description and Configuration of the Bits (Default value in blue)

IpFF	Description	Input Power Feed Forward
	0	Normal Operation
	1	Ipff mode activated
	Reset condition	Power On Reset / Read
Ilim_pre	Description	Report a current limitation condition on Vpre
	0	No current limitation (Ipre_pk < Ipre_lim)
	1	Current limitation (Ipre_pk > Ipre_lim)
	Reset condition	Power On Reset / Read
Twarm_pre	Description	Report a thermal warning from Vpre
	0	No thermal warning (Tj < Twarm_pre)
	1	Thermal warning (Tj > Twarm_pre)
	Reset condition	Power On Reset / Read
BoB	Description	Report a running mode of Vpre
	0	Buck
	1	Boost
	Reset condition	Power On Reset
Vpre_state	Description	Report the activation state of Vpre SMPS
	0	SMPS OFF
	1	SMPS ON
	Reset condition	Power On Reset

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STATUS VREG2

Table 35. STATUS VREG2 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Ilim_core	Twarm_core	Vcore_state	Twarm_cca	Ilim_cca	Ilim_aux	Ilim_can	0

Table 36. Status Vreg2. Description and Configuration of the Bits (Default value in blue)

Ilim_core	Description	Report a current limitation condition on Vcore
	0	No current limitation (Icore_pk < Icore_lim)
	1	Current limitation (Icore_pk > Icore_lim)
	Reset condition	Power On Reset / Read
Twarm_core	Description	Report a thermal warning from Vcore
	0	No thermal warning (Tj < Twarm_core)
	1	Thermal warning (Tj > Twarm_core)
	Reset condition	Power On Reset / Read
Vcore_state	Description	Report the activation state of Vcore SMPS
	0	SMPS OFF
	1	SMPS ON
	Reset condition	Power On Reset
Twarm_cca	Description	Report a thermal warning from Vcca. Available only for internal pass MOSFET
	0	No thermal warning (Tj < Twarm_cca)
	1	Thermal warning (Tj > Twarm_cca)
	Reset condition	Power On Reset
Ilim_cca	Description	Report a current limitation condition on Vcca
	0	No current limitation (Icca < Icca_lim)
	1	Current limitation (Icca > Icca_lim)
	Reset condition	Power On Reset / Read
Ilim_aux	Description	Report a current limitation condition on Vaux
	0	No current limitation (Iaux < Iaux_lim)
	1	Current limitation (Iaux > Iaux_lim)
	Reset condition	Power On Reset / Read
Ilim_can	Description	Report a current limitation condition on Vcan
	0	NO current limitation (Ican < Ican_lim)
	1	Current limitation (Ican > Ican _lim)
	Reset condition	Power On Reset / Read

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DIAG VREG1

Table 37. DIAG VREG1 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Vsns_uv	Vsup_uv_7	Tsd_pre	Vpre_OV	Vpre_uv	Tsd_core	Vcore_OV	Vcore_uv

Table 38. Diag Vreg1. Description and Configuration of the Bits (Default value in blue)

Vsns_uv	Description	Detection of Vbattery below Vsns_uv
	0	Vbat > Vsns_uv
	1	Vbat < Vsns_uv
	Reset condition	Power On Reset / Read
Vsup_uv_7	Description	Detection of Vsup below Vsup_uv_7
	0	Vsup > Vsup_uv_7
	1	Vsup < Vsup_uv_7
	Reset condition	Power On Reset / Read
Tsd_pre	Description	Thermal shutdown of Vpre
	0	No TSD (Tj < Tsd_pre)
	1	TSD occurred (Tj > Tsd_pre)
	Reset condition	Power On Reset / Read
Vpre_OV	Description	Vpre overvoltage detection
	0	No overvoltage (Vpre < Vpre_ov)
	1	Overvoltage detected (Vpre> Vpre_ov)
	Reset condition	Power On Reset
Vpre_UV	Description	Vpre undervoltage detection
	0	No undervoltage (Vpre > Vpre_uv)
	1	Under voltage detected (Vpre < Vpre_uv)
	Reset condition	Power On Reset / Read
Tsd_core	Description	Thermal shutdown of Vcore
	0	No TSD (Tj < Tsd_core)
	1	TSD occurred (Tj > Tsd_core)
	Reset condition	Power On Reset / Read
Vcore_OV	Description	Vcore overvoltage detection
	0	No overvoltage (Vcore < Vcore_ov)
	1	Overvoltage detected (Vcore > Vcore_ov)
	Reset condition	Power On Reset / Read
Vcore_UV	Description	Vcore undervoltage detection
	0	No undervoltage (Vcore > Vcore_uv)
	1	Undervoltage (Vcore < Vcore_uv)
	Reset condition	Power On Reset / Read

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DIAG VREG2

Table 39. DIAG VREG2 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Tsd_Can	Vcan_OV	Vcan_uv	0	Tsd_aux	Ilim_aux_off	Vaux_OV	Vaux_uv

Table 40. Diag Vreg2. Description and Configuration of the Bits (Default value in blue)

Tsd_can	Description	Thermal shutdown of Vcan
	0	NO TSD (Tj < Tsd_can)
	1	TSD occurred (Tj > Tsd_can)
	Reset condition	Power On Reset / Read
Vcan_OV	Description	Vcan Overvoltage detection
	0	No Overvoltage (Vcan < Vcan_OV)
	1	Overvoltage detected (Vcan > Vcan_OV)
	Reset condition	Power On Reset / Read
Vcan_uv	Description	Vcan undervoltage detection
	0	No undervoltage (Vcan > Vcan_uv)
	1	Undervoltage detected (Vcan < Vcan_uv)
	Reset condition	Power On Reset / Read
Tsd_aux	Description	Thermal shutdown of Vaux
	0	No TSD (Tj < Tsd_aux)
	1	TSD occurred (Tj > Tsd_aux)
	Reset condition	Power On Reset
Ilim_aux_off	Description	Maximum current limitation duration
	0	T_limitation < Taux_lim_off
	1	T_limitation >Taux_lim_off
	Reset condition	Power On Reset / Read
Vaux_OV	Description	Vaux overvoltage detection
	0	No overvoltage (Vaux < Vaux_OV)
	1	Overvoltage detected (Vaux > Vaux_OV)
	Reset condition	Power On Reset / Read
Vaux_UV	Description	Vaux undervoltage detection
	0	No undervoltage (Vaux > Vaux_uv)
	1	undervoltage detected (Vaux < Vaux_uv)
	Reset condition	Power On Reset / Read

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DIAG VREG 3

Table 41. DIAG VREG3 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Tsd_cca	0	Ilim-cca_off	0	Vcca_OV	0	Vcca_UV	0

Table 42. Diag Vreg3. Description and Configuration of the Bits (Default value in blue)

Tsd_cca	Description	Thermal shutdown of Vcca
	0	NO TSD (Tj < Tsd_cca)
	1	TSD occurred (Tj > Tsd_cca)
	Reset condition	Power On Reset / Read
Ilim_cca_off	Description	Maximum current limitation duration. Available only when an external PNP is connected
	0	T_limitation < Tcca_lim_off
	1	T_limitation >Tcca_lim_off
	Reset condition	Power On Reset / Read
Vcca_OV	Description	Vcca overvoltage detection
	0	No overvoltage (Vcca < Vcca_OV)
	1	Overvoltage detected (Vcca > Vcca_OV)
	Reset condition	Power On Reset / Read
Vcca_UV	Description	Vcca undervoltage detection
	0	No undervoltage (Vcca > Vcca_uv)
	1	Undervoltage detected (Vcca < Vcca_uv)
	Reset condition	Power On Reset

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DIAG CAN1

Table 43. DIAG CAN1 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CANH_batt	CANH_gnd	CANL_batt	CANL_gnd	CAN_dominant	0	RXD_recessive	TXD_dominant

Table 44. Diag CAN1. Description and Configuration of the Bits (Default value in blue)

CANH_batt	Description	CANH short circuit to battery detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
CANH_gnd	Description	CANH short circuit to gnd detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
CANL_batt	Description	CANL short circuit to battery detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
CANL_gnd	Description	CANL short circuit to gnd detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
CAN_dominant	Description	CAN Bus dominant clamping detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
RXD_recessive	Description	RXD recessive clamping detection (short circuit to 5V)
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
TXD_dominant	Description	TXD dominant clamping detection (short circuit to GND)
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read

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DIAG CAN2

Table 45. DIAG CAN2 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	reserved	reserved	0	reserved	reserved	0	CAN_OT	CAN_OC

Table 46. Diag CAN2. Description and Configuration of the Bits (Default value in blue)

CAN_OT	Description	CAN overtemperature detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read
CAN_OC	Description	CAN overcurrent detection
	0	NO failure
	1	Failure detected
	Reset condition	Power On Reset / Read

Table 47. Distinguish between CAN Diagnostic and CAN Error

Register	Bit	Flag Type	Effect
DIAG CAN1	CANH_batt	Diagnostic	No impact
	CANH_gnd	Diagnostic	No impact
	CANL_batt	Diagnostic	No impact
	CANL_gnd	Diagnostic	No impact
	CAN_dominant	Error	Turn OFF CAN transceiver
	RXD_recessive	Error	Turn OFF CAN transceiver
	TXD_dominant	Error	Turn OFF CAN transceiver
DIAG CAN2	CAN_OT	Error	Turn OFF CAN transceiver
	CAN_OC	Diagnostic	No impact

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DIAG SPI

Table 48. DIAG SPI Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_err	0	SPI_clk	0	SPI_req	0	SPI_parity	0

Table 49. Diag SPI. Description and Configuration of the Bits (Default value in blue)

SPI_err	Description	Secured SPI communication check
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset / Read
SPI_CLK	Description	SCLK error detection
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or > 16)
	Reset condition	Power On Reset / Read
SPI_req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address)
	0	No error
	1	SPI violation
	Reset condition	Power On Reset / Read
SPI_parity	Description	SPI parity bit error detection
	0	Parity bit OK
	1	Parity bit error
	Reset condition	Power On Reset / Read

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MODE

Table 50. MODE Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	0	1	P	reserved	reserved	Goto_LPOFF	INT_request	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	INIT	Normal	reserved	reserved

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	INIT	Normal	reserved	reserved

Table 51. MODE. Description and Configuration of the Bits (Default value in blue)

Goto_LPOFF	Description	Configure the device in Low Power mode Vreg OFF (LPOFF)
	0	No action
	1	LPOFF mode
	Reset condition	Power On Reset
INIT	Description	Report if INIT mode of the main logic state machine is entered
	0	Not in INIT mode
	1	INIT MODE
	Reset condition	Power On Reset
Normal	Description	Report if Normal mode of the main logic state machine is entered
	0	Not in Normal mode
	1	Normal mode
	Reset condition	Power On Reset
INT_request	Description	Request for an INT pulse
	0	No Request
	1	Request for an INT pulse
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

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VREG MODE

Table 52. VREG MODE Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	reserved	reserved	reserved	reserved	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	reserved	reserved	reserved	reserved	Vcore_EN	Vcca_EN	Vaux_EN	Vcan_EN

Table 53. VREG MODE. Description and Configuration of the Bits (Default value in blue)

Vcore_EN	Description	Vcore control (Switch OFF not possible if Vcore is SAFETY critical)
	0	DISABLED
	1	ENABLED
	Reset condition	Power On Reset
Vcca_EN	Description	Vcca control (Switch OFF NOT possible if Vcca is SAFETY critical)
	0	DISABLED
	1	ENABLED
	Reset condition	Power On Reset
Vaux_EN	Description	Vaux control (Switch OFF NOT possible if Vaux is SAFETY critical)
	0	DISABLED
	1	ENABLED
	Reset condition	Power On Reset
VCAN_EN	Description	Vcan control
	0	DISABLED
	1	ENABLED
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

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IO_OUT-AMUX

Table 54. IO_OUT-AMUX Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	1	P	IO_out_4_EN	IO_out_4	IO_out_5_EN	IO_out_5	Reserved	Amux_2	Amux_1	Amux_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_out_4_EN	IO_oout_4	IO_out_5_EN	IO_out_5	Reserved	Amux_2	Amux_1	Amux_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	IO_out_4_EN	IO_oout_4	IO_out_5_EN	IO_out_5	Reserved	Amux_2	Amux_1	Amux_0

Table 55. IO_OUT-AMUX. Description and Configuration of the Bits (Default value in blue)

IO_out_4_EN	Description	Enable the output gate driver capability for IO_4
	0	High impedance (IO_4 configured as input)
	1	ENABLED (IO_4 configured as output gate driver)
	Reset condition	Power On Reset
IO_out_4	Description	Configure IO_4 output gate driver state
	0	LOW
	1	HIGH
	Reset condition	Power On Reset
IO_out_5_EN	Description	Enable the output gate driver capability for IO_5
	0	High impedance (IO_5 configured as input)
	1	ENABLED (IO_5 configured as output gate driver)
	Reset condition	Power On Reset
IO_out_5	Description	Configure IO_5 output gate driver state
	0	LOW
	1	HIGH
	Reset condition	Power On Reset
AMUX_2:0	Description	Select AMUX output
	000	Vref
	001	Vsns wide range
	010	IO_0 wide range
	011	IO_1 wide range
	100	Vsns tight range
	101	IO_0 tight range
	110	IO_1 tight range
	111	Die temp. Sense
	Reset condition	Power On Reset

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CAN MODE

Table 56. CAN MODE Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	0	0	P	CAN_mode_1	CAN_mode_0	CAN_auto_dis	reserved	reserved	reserved	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CAN_mode_1	CAN_mode_0	CAN_auto_dis	reserved	reserved	reserved	CAN_wu	reserved

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	CAN_mode_1	CAN_mode_0	CAN_auto_dis	reserved	reserved	reserved	CAN_wu	reserved

Table 57. CAN MODE. Description and Configuration of the Bits (Default value in blue)

CAN_mode_1:0	Description	Configure the CAN mode
	00	Sleep / NO wake up capability
	01	LISTEN ONLY
	10	Sleep / Wake-up capability
	11	Normal operation mode
	Reset condition	Power On Reset
CAN_auto_dis	Description	Automatic CAN Tx disable
	0	NO auto disable
	1	Reset CAN_mode from “11” to “01” on CAN over temp or TXD dominant or RXD recessive event
	Reset condition	Power On Reset
CAN_wu	Description	Report a wake up event from the CAN
	0	No wake-up
	1	wake-up detected
	Reset condition	Power On Reset / Read

Notes

19. When the device is in Normal mode, the CAN mode bits cannot be read back by the SPI when the CAN transceiver is configured in Low Power mode.
20. CAN mode is automatically configured to "sleep + wake-up capability [10]" if CAN mode was different than "sleep + no wake-up capability [00]" before the device enters in LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored.

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CAN_MODE_2

Table 58. CAN_MODE_2 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	1	0	0	1	P	reserved	reserved	reserved	Vcan_OV_Mon	secure_3	secure_2	secure_1	secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	Vcan_OV_Mon	Reserved	Reserved	Reserved

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	Reserved	Reserved	Reserved	Reserved	Vcan_OV_Mon	Reserved	Reserved	Reserved

Table 59. CAN_MODE_2. Description and Configuration of the Bits (Default value in blue)

Vcan_OV_Mon	Description	VCAN OV Monitoring
	0	OFF. Vcan OV is not monitored. Flag is ignored
	1	ON. Vcan OV flag is under monitoring. In case of OV the Vcan regulator is switched OFF.
	Reset condition	Power On Reset
Secure 3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

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INIT SUPERVISOR1

Table 60. INIT SUPERVISOR1 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	0	1	P	Vcore_ FS1	Vcore_ FS_0	Vcca_F S_1	Vcca_F S_0	secure _3	Secure _2	Secure _1	Secure _0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _Req	SPI_FS _Parity	Vcore_ FS1	Vcore_ FS_0	Vcca_F S_1	Vcca_F S_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _Req	SPI_FS _Parity	Vcore_ FS1	Vcore_ FS_0	Vcca_F S_1	Vcca_F S_0

Table 61. INIT SUPERVISOR1. Description and Configuration of the Bits (Default value in blue)

Vcore_FS1:0	Description	Vcore safety input.
	00	No effect of Vcore_OV and Vcore_uv on RSTb and FSxx
	01	Vcore_OV DOES HAVE an impact on RSTb and FSxx. Vcore_UV DOES HAVE an impact on RSTb only
	10	Vcore_OV DOES HAVE an impact on RSTb and FSxx. No effect of Vcore_UV on RSTb and FSxx
	11	Both Vcore_OV and Vcore_UV DO HAVE an impact on RSTb and FSxx
	Reset condition	Power On Reset
Vcca_FS1:0	Description	Vcca safety input.
	00	No effect of Vcca_OV and Vcca_uv on RSTb and FSxx
	01	Vcca_OV DOES HAVE an impact on RSTb and FSxx. Vcca_UV DOES HAVE an impact on RSTb only
	10	Vcca_OV DOES HAVE an impact on RSTb and FSxx. No effect of Vcca_UV on RSTb and FSxx
	11	Both Vcca_OV and Vcca_UV DO HAVE an impact on RSTb and FSxx
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

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Table 61. INIT SUPERVISOR1. Description and Configuration of the Bits (Default value in blue)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-safe logic only.
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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INIT SUPERVISOR 2

Table 62. INIT SUPERVISOR2 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	0	P	Vaux_FS1	Vaux_FS_0	0	DIS_8s	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	DIS_8s	Vaux_FS1	Vaux_FS_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	DIS_8s	Vaux_FS1	Vaux_FS_0

Table 63. INIT SUPERVISOR2. Description and Configuration of the Bits (Default value in blue)

Vaux_FS1:0	Description	Vaux safety input.
	00	No effect of Vaux_OV and Vaux_uv on RSTb and FSxx
	01	Vaux_OV DOES HAVE an impact on RSTb and FSxx. Vaux_UV DOES HAVE an impact on RSTb only
	10	Vaux_OV DOES HAVE an impact on RSTb and FSxx. No effect of Vaux_UV on RSTb and FSxx
	11	Both Vaux_OV and Vaux_UV DO HAVE an impact on RSTb and FSxx
	Reset condition	Power On Reset
DIS_8s	Description	Disable the 8s timer used to enter Deep FAILSAFE mode
	0	ENABLED
	1	DISABLED
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check, concerns Fail-safe logic only.
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

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Table 63. INIT SUPERVISOR2. Description and Configuration of the Bits (Default value in blue)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-safe Logic only
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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INIT SUPERVISOR 3

Table 64. INIT SUPERVISOR3 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	1	P	Vcore_5D	Vcca_5D	Vaux_5D	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	Vcore_5D	Vcca_5D	Vaux_5D

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	0	Vcore_5D	Vcca_5D	Vaux_5D

Table 65. INIT SUPERVISOR3. Description and Configuration of the Bits (Default value in blue)

Vcore_5D	Description	Configure the Vcore undervoltage in degraded mode. Only valid for 5V
	0	Normal 5 V undervoltage detection threshold (Vcore_uv)
	1	Degraded mode, i.e lower under voltage detection threshold applied (Vcore_uv_D)
	Reset condition	Power On Reset
Vcca_5D	Description	Configure the Vcca undervoltage in degraded mode. Only valid for 5V
	0	Normal 5 V undervoltage detection threshold (Vcca_uv_5)
	1	Degraded mode, i.e lower under voltage detection threshold applied (Vcca_uv_D)
	Reset condition	Power On Reset
Vaux_5D	Description	Configure the Vaux undervoltage in degraded mode. Only valid for 5V
	0	Normal 5 V undervoltage detection threshold (Vaux_uv_5)
	1	Degraded mode, i.e lower under voltage detection threshold applied (Vaux_uv_5D)
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check, concerns fail-safe logic only
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

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Table 65. INIT SUPERVISOR3. Description and Configuration of the Bits (Default value in blue)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-Safe Logic only
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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INIT FSSM1

Table 66. INIT FSSM1 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	0	P	IO_01_FS	0	IO_45_FS	RSTb_low	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	IO_01_FS	0	IO_45_FS	RSTb_low

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	IO_01_FS	0	IO_45_FS	RSTb_low

Table 67. INIT FSSM1. Description and Configuration of the Bits (Default value in blue)

IO_01_FS	Description	Configure the couple of IO_1:0 as safety inputs
	0	NOT SAFETY
	1	SAFETY CRITICAL
	Reset condition	Power On Reset
IO_45_FS	Description	Configure the couple of IO_5:4 as safety inputs
	0	NOT SAFETY
	1	SAFETY CRITICAL
	Reset condition	Power On Reset
RSTb_low	Description	Configure the Rstb LOW duration time
	0	10 ms
	1	1ms
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check, concerns Fail-safe logic only
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

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Table 67. INIT FSSM1. Description and Configuration of the Bits (Default value in blue)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-safe logic only
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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INIT FSSM2

Table 68. INIT FSSM2 Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	0	1	P	RSTb_ err_FS	IO_23_ FS	PS	0	Secure _3	Secure _2	Secure _1	Secure _0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _req	SPI_FS _Parity	RSTb_ err_FS	IO_23_ FS	PS	0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserv ed	IO_G	Vpre_G	Vcore_ G	Vothers _G	SPI_FS _err	SPI_FS _CLK	SPI_FS _req	SPI_FS _Parity	RSTb_ err_FS	IO_23_ FS	PS	0

Table 69. INIT FSSM2. Description and Configuration of the Bits (Default value in blue)

IO_23_FS	Description	Configure the couple of IO_3:2 as safety inputs for FCCU monitoring
	0	NOT SAFETY
	1	SAFETY CRITICAL
	Reset condition	Power On Reset
RSTb_err_FS	Description	Configure the values of the RSTb error counter
	0	intermediate=3; final=6
	1	intermediate=1; final=2
	Reset condition	Power On Reset
PS	Description	Configure the Fccu polarity
	0	Fccu_eaout_1:0 active HIGH
	1	Fccu_eaout_1:0 active LOW
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6
SPI_FS_err	Description	Secured SPI communication check, concerns Fail-safe logic only
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK_ bit
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset

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Table 69. INIT FSSM2. Description and Configuration of the Bits (Default value in blue)

SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-safe Logic only
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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WD WINDOW

Table 70. WD WINDOW Register Description

Write

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	0	P	WD_window3	WD_window2	WD_window1	WD_window0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	WD_window3	WD_window2	WD_window1	WD_window0

Read

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_req	SPI_FS_Parity	WD_window3	WD_window2	WD_window1	WD_window0

Any WRITE command to the WD_window in the Normal mode must be followed by a READ command to verify the correct change of the WD window duration

Table 71. WD Window. Description and Configuration of the Bits (Default value in blue)

WD_Window_3:0	Description	Configure the watchdog window duration. Duty cycle if set to 50%
	0000	DISABLE
	0001	1 ms
	0010	2 ms
	0011	3 ms
	0100	4 ms
	0101	6 ms
	0110	8 ms
	0111	12 ms
	1000	16 ms
	1001	24 ms
	1010	32 ms
	1011	64 ms
	1100	128 ms
	1101	256 ms
	1110	512 ms
	1111	1024 ms
	Reset condition	Power On Reset
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

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Table 71. WD Window. Description and Configuration of the Bits (Default value in blue)

SPI_FS_err	Description	Secured SPI communication check, concerns Fail-safe logic only
	0	No error
	1	Error detected in the secured bits
	Reset condition	Power On Reset
SPI_FS_CLK	Description	SCLK error detection, concerns internal error in Fail-safe logic only and external errors (at pin level) for both Main and Fail-safe logics. Other errors flagged by SPI_CLK bit.
	0	16 clock cycles during NCS low
	1	Wrong number of clock cycles (<16 or >16)
	Reset condition	Power On Reset
SPI_FS_Req	Description	Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns Fail-safe logic only
	0	No error
	1	SPI violation
	Reset condition	Power On Reset
SPI_FS_Parity	Description	SPI parity bit error detection, concerns Fail-safe logic only
	0	Parity bit OK
	1	Parity bit ERROR
	Reset condition	Power On Reset

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WD_LFSR

Table 72. WD LFSR Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	1	1	1	P	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	0	0	0	0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0

Table 73. WD LFSR. Description and Configuration of the Bits (Default value in blue)

WD_LFSR_7:0	Description	WD 8 bits LFSR value. Used to write the seed at any time
	0...	bit7:bit0: 10110010 default value at startup or after a Power on reset: 0xB2 (21)
	1...	
	Reset condition	Power On Reset

Notes

21. Value Bit7:Bit0: 1111 1111 is prohibited.

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WD ANSWER

Table 74. WD ANSWER Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	0	P	WD_answer_7	WD_answer_6	WD_answer_5	WD_answer_4	WD_answer_3	WD_answer_2	WD_answer_1	WD_answer_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb	FS0	WD	FS0_G	IO_FS_G	0	FS_ECC	FS_reg_Ecc

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb	FS0	WD	FS0_G	IO_FS_G	0	FS_ECC	FS_reg_Ecc

Table 75. WD answer. Description and Configuration of the Bits (Default value in blue)

WD_answer_7:0	Description	WD answer from the MCU
	0...	Answer = (NOT(((LFSR x 4)+6)-4))/4
	1...	
	Reset condition	Power On Reset / RSTb LOW
RSTb	Description	Report a reset event
	0	No Reset
	1	Reset occurred
	Reset condition	Power On Reset / Read
FS0b	Description	Report a fail-safe event
	0	No Fail-safe
	1	Fail safe event occurred / Also default state at power-up after LPOFF as FS0b is asserted low
	Reset condition	Power On Reset / Read
WD	Description	Report a watchdog refresh ERROR
	0	WD refresh OK
	1	WRONG WD refresh
	Reset condition	Power On Reset / Read
FS0_G	Description	Report a fail-safe output failure
	0	NO failure
	1	Failure
	Reset condition	Power On Reset / Read
IO_FS_G	Description	Report an IO monitoring error
	0	No error
	1	Error detected
	Reset condition	Power On Reset

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Table 75. WD answer. Description and Configuration of the Bits (Default value in blue)

FS_ECC	Description	Report an error code correction on Fail-safe state machine
	0	NO ECC
	1	ECC done
	Reset condition	Power On Reset / Read
FS_req_ECC	Description	Report an error code correction on Fail-safe registers
	0	NO ECC
	1	ECC done
	Reset condition	Power On Reset / Read

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FAIL-SAFE OUT (FS_OUT)

Table 76. FAIL-SAFE OUT Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	0	1	P	FS_out_7	FS_out_6	FS_out_5	FS_out_4	FS_out_3	FS_out_2	FS_out_1	FS_out_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	0	0	0	0

Table 77. Fail-Safe OUT. Description and Configuration of the Bits (Default value in blue)

FS_out_7:0	Description	Secured 8 bits word to release the FS0b
	0...	Depend on LFSR_out value and calculation
	1...	
	Reset condition	Power On Reset -> Default = 00h

RSTB REQUEST

Table 78. RSTb REQUEST register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	0	P	0	0	RSTb_request	0	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	0	0	0	0	0	0	0	0

Table 79. RSTb Request. Description and configuration of the bits (Default value in blue)

RSTb_request	Description	Request a RSTb low pulse
	0	No request
	1	Request a RSTb low pulse
	Reset condition	Power On Reset / When RSTb done
Secure3:0	Description	Secured bits based on write bits
		secured_3 = NOT(bit5) Secured_2= NOT(bit4) Secured_1=bit7 Secured_0=bit6

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INIT_WD

Table 80. INIT WD Register Description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	1	0	1	1	P	WD_CNT_refresh_1	WD_cnt_refresh_0	WD_CNT_error_1	WD_CNT_error_0	secure3	secure2	secure1	secure0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	WD_CNT_refresh_1	WD_cnt_refresh_0	WD_CNT_error_1	WD_CNT_error_0

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	SPI_FS_err	SPI_FS_CLK	SPI_FS_Req	SPI_FS_Parity	WD_CNT_refresh_1	WD_cnt_refresh_0	WD_CNT_error_1	WD_CNT_error_0

Table 81. INIT WD. Description and Configuration of the Bits (Default value in blue)

WD_CNT_error_1:0	Description	Configure the maximum value of the WD error counter
	00	6
	01	6
	10	4
	11	2
	Reset Condition	Power On Reset
WD_CNT_refresh_1:0	Description	Configure the maximum value of the WD refresh counter
	00	6
	01	6
	10	4
	11	1
	Reset Condition	Power On Reset

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DIAG FS1

Table 82. DIAG FS1 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb_ext	RSTb_diag	0	FS0b_diag_1	FS0b_diag_0	0	0	0

Table 83. Diag FS1. Description and Configuration of the Bits (Default value in blue)

RSTb_diag	Description	Report a RSTb short-circuit to HIGH
	0	NO Failure
	1	short circuit HIGH
	Reset condition	Power On Reset / Read
RSTb_ext	Description	Report an external RSTb
	0	No external RSTb
	1	external RSTb
	Reset condition	Power On Reset / Read
FS0b_diag_1:0	Description	Report a failure on FS0b
	00	No Failure
	01	Short-circuit LOW / open load
	1X	short-circuit HIGH
	Reset condition	Power On Reset / Read

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WD COUNTER

Table 84. WD COUNTER Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	WD_err_2	WD_err_1	WD_err_0	0	WD_refresh_2	WD_refresh_1	WD_refresh_0	0

Table 85. WD counter. Description and Configuration of the Bits (Default value in blue)

WD_err_2:0	Description	Report the value of the watchdog error counter
	000	From 0 to 5 (6 generates a Reset and this counter is reset to 0)
	to 110	
	Reset condition	Power On Reset
WD_refresh_2:0	Description	Report the value of the watchdog refresh counter
	000	From 0 to 6 (7 generate a decrease of the RST_err_cnt and this counter is reset to 0)
	to 111	
	Reset condition	Power On Reset

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DIAG FS2

Table 86. DIAG FS2 Register Description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU	CAN_G	Reserved	IO_G	Vpre_G	Vcore_G	Vothers_G	RSTb_err_2	RSTb_err_1	RSTb_err_0	0	IO_45_fail	IO_23_fail	0	IO_01_fail

Table 87. Diag FS1. Description and Configuration of the Bits (Default value in blue)

RSTb_err_2:0	Description	Report the value of the RSTb error counter
	000 001 … 110	Error counter is set to 1 by default
	Reset condition	Power On Reset
IO_45_fail	Description	Report an error in the IO_45 protocol
	0	NO error
	1	Error detected
	Reset condition	Power On Reset / Read
IO_23_fail	Description	Report an error in the FCCU protocol
	0	NO error
	1	Error detected
	Reset condition	Power On Reset / Read
IO_01_fail	Description	Report an error in the IO_01 protocol
	0	NO error
	1	Error detected
	Reset condition	Power On Reset / Read

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8 List of Interruptions and Description

The INTb output pin generates a low pulse when an Interrupt condition occurs. The INTb behavior as well as the pulse duration are set through SPI during INIT phase.

It is possible to mask some Interruption source (see register mapping).

Table 88. Interruptions list

Event	Description
V_{SNS_UV}	Detection of Vbattery below 8.5V
$V_{SUP_UV_7}$	Detection of V_{SUP} below 7V (after reverse current protection diode)
I_{PFF}	Input power feed forward. Based on V_{SUP} and I_{PRE_PEAK}
I_{LIM_PRE}	Pre-Regulator Current Limitation
T_{WARN_PRE}	Temperature warning on the pass transistor
BoB	Return the running state of V_{PRE} converter (Buck or Boost mode)
V_{PRE_STATE} ($V_{PRE_SMPS_EN}$)	Return the activation state of V_{PRE} DC/DC converter
V_{PRE} OV	Report a V_{PRE} overvoltage detection
V_{PRE} UV	Report a V_{PRE} under voltage detection
I_{LIM_CORE}	V_{CORE} Current limitation
T_{WARN_CORE}	Temperature warning on the pass transistor
V_{CORE_STATE} ($V_{CORE_SMPS_EN}$)	Return the activation state of V_{CORE} DC/DC converter
V_{CORE} OV	Report a V_{CORE} overvoltage detection
V_{CORE} UV	Report a V_{CORE} under voltage detection
I_{LIM_CCA}	V_{CCA} Current limitation
T_{WARN_CCA}	Temperature warning on the pass transistor (Internal Pass transistor only)
TSD_{VCCA}	Temperature shutdown of the VCCA
$I_{LIM_CCA_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
V_{CCA} OV	Report a V_{CCA} overvoltage detection
V_{CCA} UV	Report a V_{CCA} under voltage detection
I_{LIM_AUX}	V_{AUX} Current limitation
$I_{LIM_AUX_OFF}$	Current limitation maximum duration expiration. Only used when external PNP connected.
V_{AUX} OV	Report a V_{AUX} overvoltage detection
V_{AUX} UV	Report a V_{AUX} under voltage detection
TSD_{VAUX}	Temperature shutdown of the VAUX
I_{LIM_CAN}	V_{CAN} Current limitation
V_{CAN} OV	Report a V_{CAN} overvoltage detection
V_{CAN} UV	Report a V_{CAN} under voltage detection
TSD_{CAN}	Temperature shutdown on the pass transistor. Auto restart when $T_J < (TSD_{CAN} - TSD_{CAN_HYST})$.

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Table 88. Interruptions list

IO_0	Report IO_0 digital state change
IO_1	Report IO_1 digital state change
IO_2	Report IO_2 digital state change
IO_3	Report IO_3 digital state change
IO_4	Report IO_4 digital state change
IO_5	Report IO_5 digital state change
IO_0_WU	Report IO_0 WU event
IO_1_WU	Report IO_1 WU event
IO_2_WU	Report IO_2 WU event
IO_3_WU	Report IO_3 WU event
IO_4_WU	Report IO_4 WU event
IO_5_WU	Report IO_5 WU event
$CANL_{BATT}$	CANL short-circuit to battery detection
$CANL_{GND}$	CANL short-circuit to GND detection
$CANH_{BATT}$	CANH short-circuit to battery detection
$CANH_{GND}$	CANH short-circuit to GND detection
CAN_WU	Report a CAN wake-up event
CAN_OT	CAN overtemperature detection
RXD_recessive	CAN RXD recessive clamping detection (short circuit to 5 V)
TXD_dominant	CAN TXD dominant clamping detection (short circuit to GND)
CAN_dominant	CAN bus dominant clamping detection
CAN_OC	CAN overcurrent detection
INT_Request	MCU request for an Interrupt pulse
SPI_err	Secured SPI communication check
SPI_CLK	Report a wrong number of CLK pulse different than 16 during the NCS low pulse in Main state machine
SPI_Req	Invalid SPI access (Wrong write or read, write to INIT registers in normal mode, wrong address)
SPI_Parity	Report a Parity error in Main state machine

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9 Typical Applications

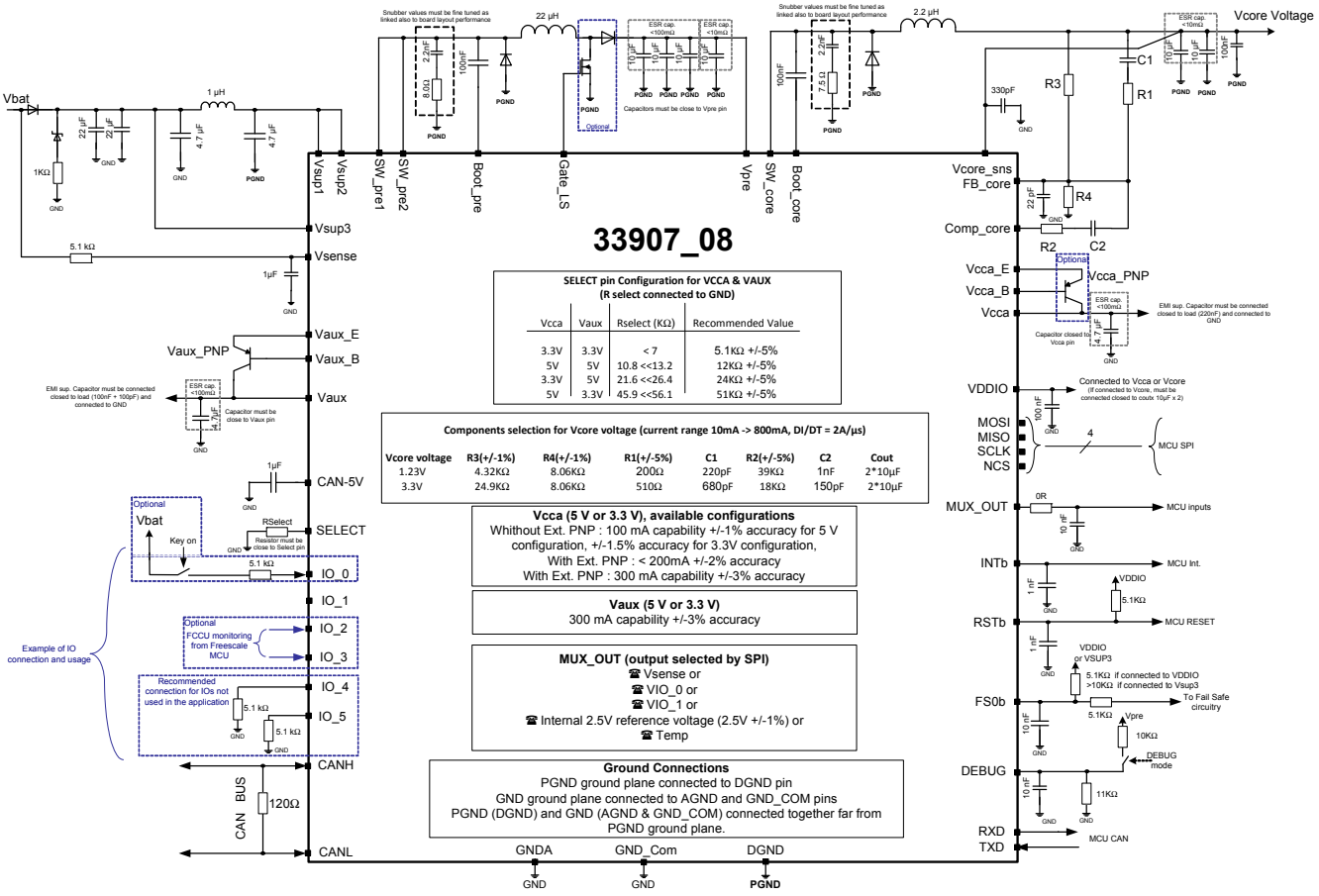


Figure 34. PowerSBC10/20 Simplified Application Schematic with Non-inverting Buck-boost Configuration

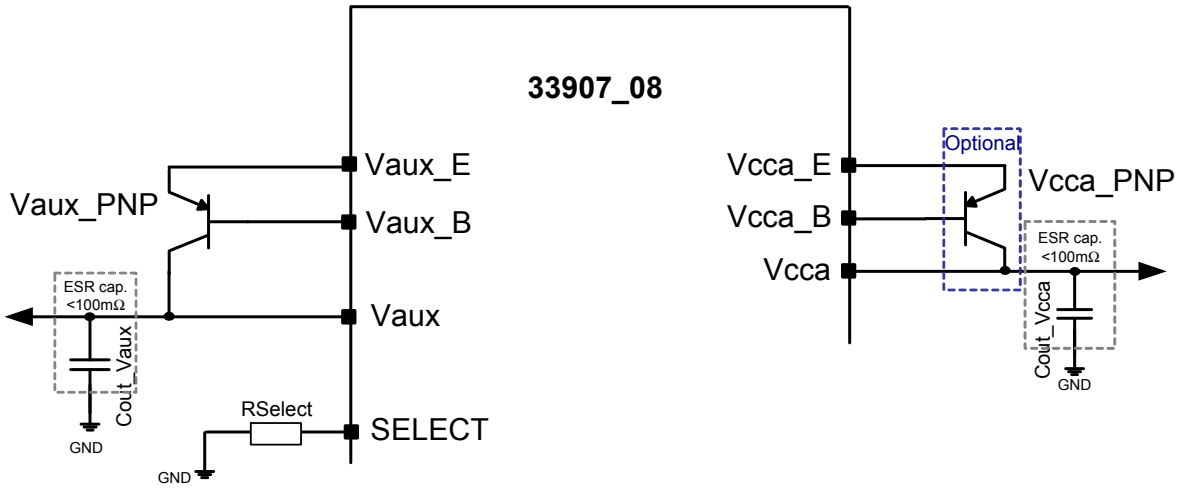


Figure 35. Vaux/Vcca Connection

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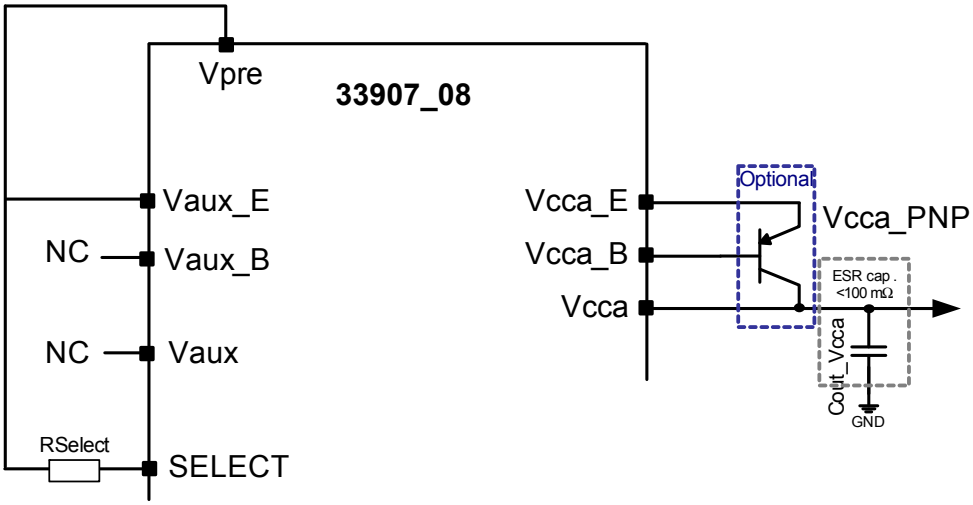


Figure 36. VCCA Connection, Vaux Not Used

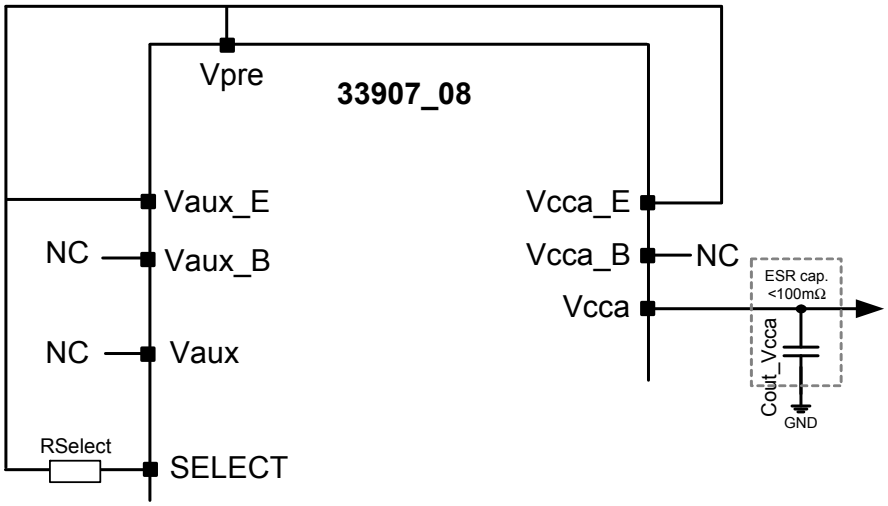


Figure 37. Vaux Not Used, Vcca Configuration up to 100 mA

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10 Packaging

10.1 Package Mechanical Dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 89. Package Mechanical Dimensions

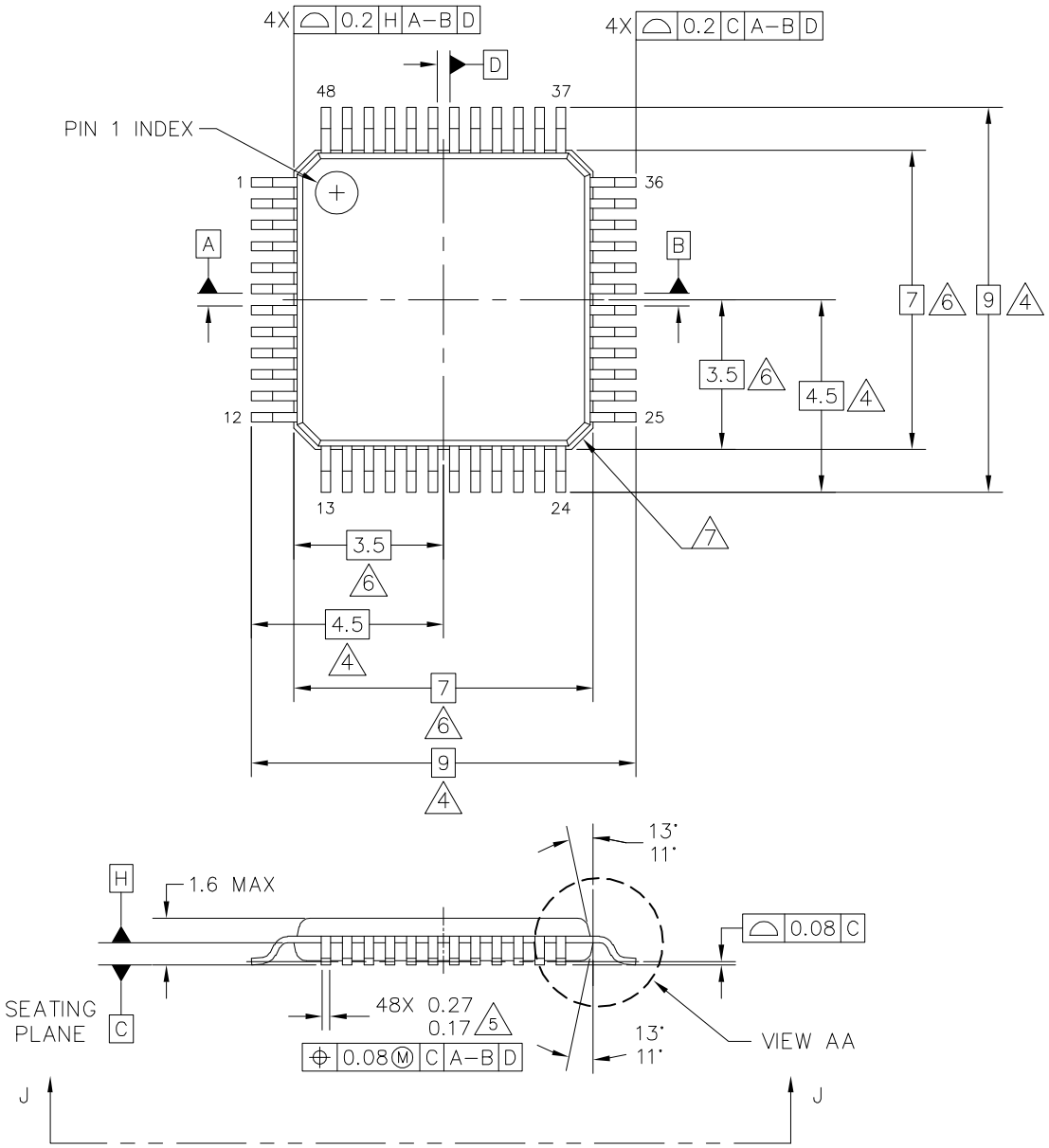
Package	Suffix	Package Outline Drawing Number
7.0 x 7.0, 48-Pin LQFP Exposed Pad, with 0.5 mm pitch, and a 4.5 x 4.5 exposed pad	AE	98ASA00173D

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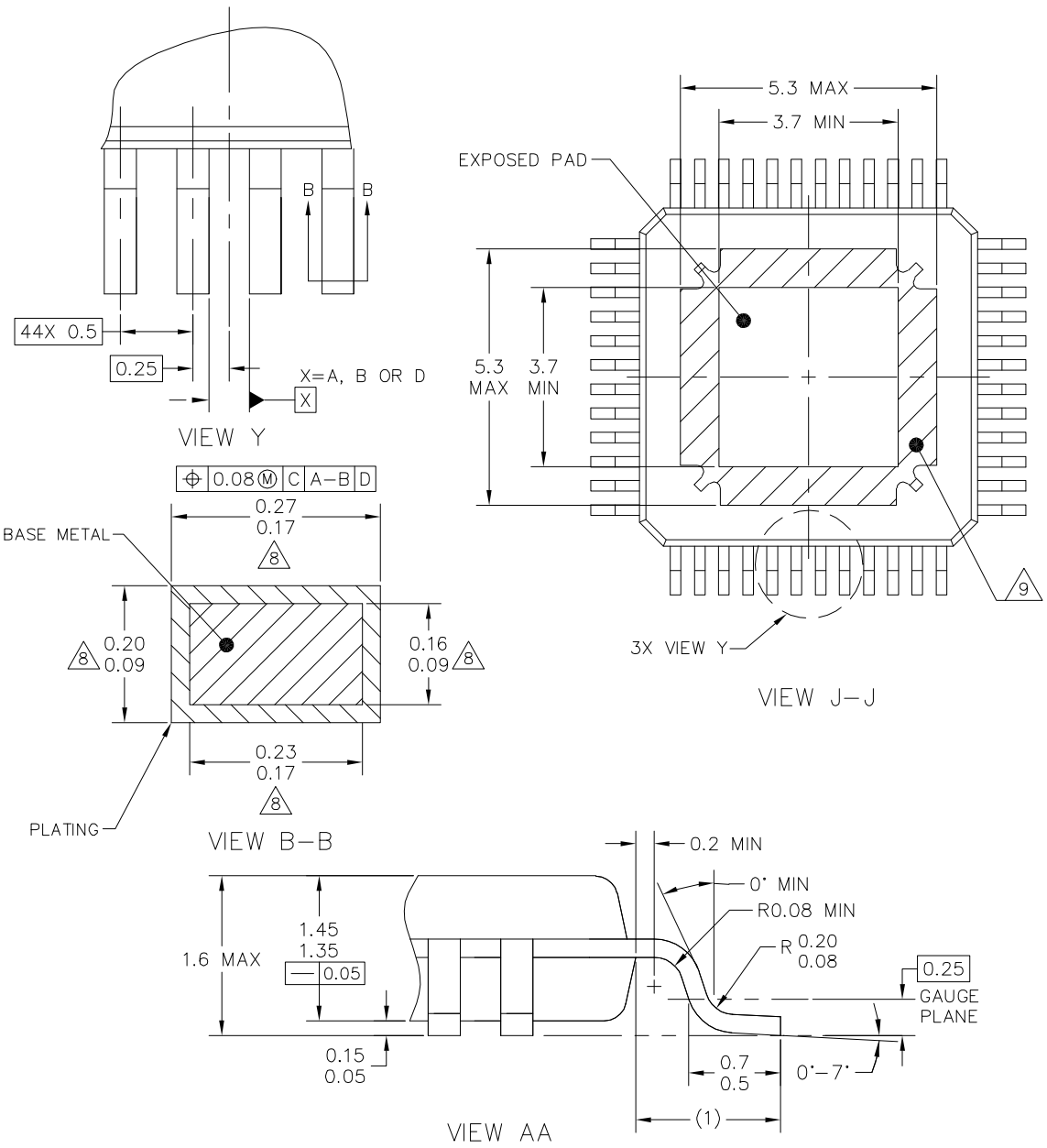
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003-02	30 JUN 2011
	STANDARD: JEDEC MS-026 BBC	

AE SUFFIX
48-PIN LQFP-EP
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TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.5X4.5 EXPOSED PAD	DOCUMENT NO: 98ASA00173D	REV: A
	CASE NUMBER: 2003-02	30 JUN 2011
	STANDARD: JEDEC MS-026 BBC	

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

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	CASE NUMBER: 2003–02	30 JUN 2011
	STANDARD: JEDEC MS–026 BBC	

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11 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	11/2013	• Initial release
2.0	12/2013	• Updated Figure 2 • Deleted Rk: IO_1 can also be used to monitor a second external resistor bridge (in parallel of the one • for VCORE output voltage set) for safety purposes from Table 2 on page 8 • Updated Gun Test in Table 3 on page 10 • Added IOs maximum current capability to Table 3 on page 10 • Updated V_{CCA} voltage in Table 4 on page 14 • Updated $V_{AUX_LIM_HYST}$ in Table 4 on page 15 • Updated $V_{CORE_FB_UV_D}$ in Table 4 on page 16 • Updated $V_{AMUX_TP_CO}$ in Table 4 on page 17 • Updated V_{SPI_IL} in Table 4 on page 18 • Deleted $V_{CORE_FB_DRIFT}$ • Deleted I_{IO_IN1} • Deleted t_{RDRIFT} • Updated t_{RSTB_POR} in Table 5 on page 22 • Added T_DFS_recovery time in Table 5 on page 22 • Updated DV_{SUP}/DT voltage in Table 5 on page 23 • Updated $t_{PRE_UV_4p3}$ in Table 5 on page 24 • Updated t_{PRE_TSD}, t_{CORE_TSD}, and t_{CCA_TSD} values in Table 5 on page 24 • Updated t_{CAN_TSD} and t_{CAN_UV} values in Table 5 on page 25 • Added a formula for temperature sensor • Deleted V_{reg_WU} from Table 30 on page 63 • Updated Figure 10, Figure 16, Figure 17, and Figure 22 • Updated Table 15, Table 16, Table 19, Table 20,Table 27, Table 28, Table 56, Table 67, Table 71, Table 75, and Table 87 • Added note (21) • Updated Figure 34, Figure 35, and Figure 36 • Added new Figure 37 • Added notes to Table 57
3.0	2/2014	• Changed to Advance Information • Changed Orderable Parts numbers 33907 and 33908 to MC • Added new reference to Table 73 in Normal Operation (First Watchdog Refresh) • Changed default in Status Vreg1. Description and Configuration of the Bits (Default value in blue) for Vpre_state, for Vcore_state in Status Vreg2. Description and Configuration of the Bits (Default value in blue), for CAN_mode_1:0 in CAN MODE. Description and Configuration of the Bits (Default value in blue), and RSTb_err_2:0 in Diag FS1. Description and Configuration of the Bits (Default value in blue) • Corected SW_PRE pin names

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