LMH0394 3G HD/SD SDI Low Power Extended Reach Adaptive Cable Equalizer

1 Features

- ST 424, ST 292, ST 344, ST 259, and DVB-ASI Compliant(1)
- Equalized Cable Lengths (Belden 1694A): 200 Meters at 2.97 Gbps, 220 Meters at 1.485 Gbps, and 400 Meters at 270 Mbps
- Ultra Low Power Consumption: 115 mW (Normal Operation)
- Power-Save Mode With Auto Sleep Control (17-mW Typical Power Consumption in Power-Save Mode)
- Designed for Crosstalk Immunity
- Output De-Emphasis to Compensate for FR4 Board Trace Losses
- Digital and Analog Programmable $MUTE_{REF}$ Threshold
- Optional SPI Register Access
- Input Data Rates: 125 Mbps to 2.97 Gbps
- Internally Terminated 100-Ω LVDS Outputs With Programmable Output Common-Mode Voltage and Swing
- Programmable Launch Amplitude Optimization
- Cable Length Indicator
- Single 2.5-V Supply Operation
- 16-pin WQFN Package
- Industrial Temperature Range: −40°C to +85°C
- Footprint Compatible with the LMH0384 and also the LMH0344, LMH0044, and LMH0074 in Pin Mode

2 Applications

- ST 424, ST 292, ST 344, and ST 259 Serial Digital Interfaces(1)
- Broadcast Video Routers, Switchers, and Distribution Amplifiers

(1) Due to SMPTE naming convention, all SMPTE Engineering Documents will be numbered as a two-letter prefix and a number. Documents and references with the same root number and year are functionally identical; for example ST 424-2006 and SMPTE 424M-2006 refer to the same document.

3 Description

The LMH0394 3-Gbps HD/SD SDI Low Power Extended Reach Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, ST 259, and DVB-ASI standards(1).

The LMH0394 provides extended cable reach with improved immunity to crosstalk and ultra low power consumption. The equalizer includes active sensing circuitry that ensures robust performance and enhanced immunity to variations in the input signal launch amplitude. The output driver offers programmable de-emphasis for up to 40” of FR4 trace losses. The LMH0394 includes power management to further reduce power consumption when no input signal is present.

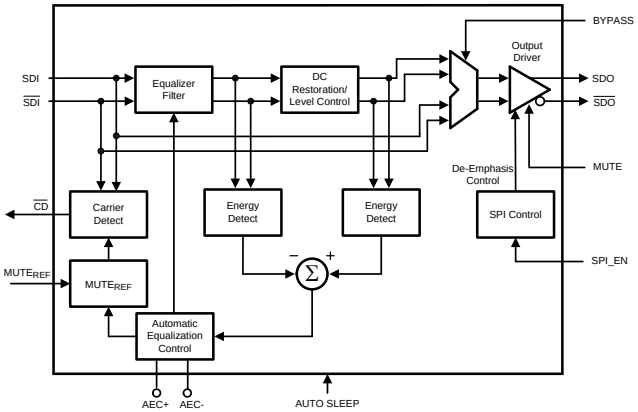
The LMH0394 supports two modes of operation. In pin mode, the LMH0394 operates with control pins to set its operating state, and is footprint compatible with the LMH0384, LMH0344, and legacy SDI equalizers. In SPI mode, an optional SPI serial interface can be used to access and configure multiple LMH0394 devices in a daisy-chain configuration. This allows users to program the output common-mode voltage and swing, output de-emphasis level, input launch amplitude, and power management settings. Users may also access a cable length indicator and all pin mode features.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0394	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

Changes from Revision L (April 2013) to Revision M **Page**

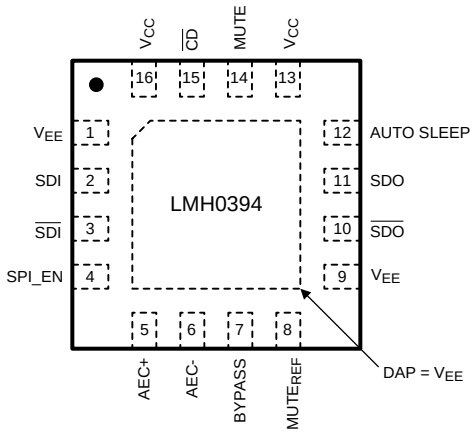
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision K (April 2013) to Revision L **Page**

- Changed layout of National Data Sheet to TI format ... 21

5 Pin Configuration and Functions

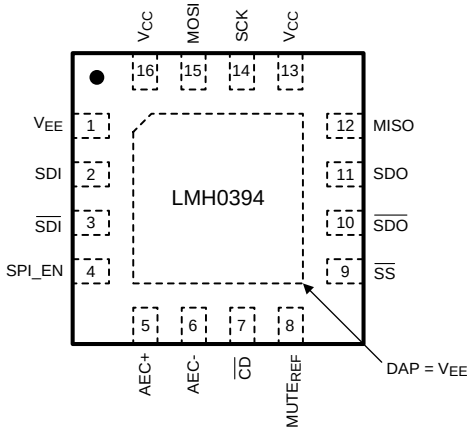
RUM Package
16-Pin WQFN (Non-SPI)
Top View



Pin Functions – Pin Mode (non-SPI) / SPI_EN = GND / LMH0344 Compatible

PIN		I/O, TYPE	DESCRIPTION
NO.	NAME		
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, Analog	Serial data true input.
3	$\overline{SDI}$	I, Analog	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1-µF) positive connection (capacitor is optional).
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1-µF) negative connection (capacitor is optional).
7	BYPASS	I, LVCMOS	Equalization bypass. This pin has an internal pull-down. H = Equalization is bypassed (no equalization occurs). L = Normal operation.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	V_{EE}	I, LVCMOS	Connect this pin to ground or drive it logic low.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	AUTO SLEEP	I, LVCMOS	Auto Sleep. AUTO SLEEP has precedence over MUTE and BYPASS. This pin has an internal pullup. H = Device will power down when no input is detected. L = Normal operation (device will not enter auto power down).
13	V_{CC}	Power	Positive power supply (+2.5 V).
14	MUTE	I, LVCMOS	Output mute. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has precedence over BYPASS. This pin has an internal pull-down. H = Outputs forced to a muted state. L = Outputs enabled.
15	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
16	V_{CC}	Power	Positive power supply (2.5 V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground). See Figure 22 for layout example.

RUM Package
16-Pin WQFN (SPI)
Top View



Pin Functions – SPI Mode / SPI_EN = V_{CC}

PIN		I/O, TYPE	DESCRIPTION
NO.	NAME		
1	V_{EE}	Ground	Negative power supply (ground).
2	SDI	I, Analog	Serial data true input.
3	$\overline{SDI}$	I, Analog	Serial data complement input.
4	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pull-down. H = SPI register access mode. L = Pin mode.
5	AEC+	I/O, Analog	AEC loop filter external capacitor (1 µF) positive connection (capacitor is optional).
6	AEC-	I/O, Analog	AEC loop filter external capacitor (1 µF) negative connection (capacitor is optional).
7	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
8	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
9	$\overline{SS}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
10	$\overline{SDO}$	O, LVDS	Serial data complement output.
11	SDO	O, LVDS	Serial data true output.
12	MISO (SPI)	O, LVCMOS	SPI Master Input / Slave Output. LMH0394 control data transmit.
13	V_{CC}	Power	Positive power supply (2.5 V).
14	SCK (SPI)	I, LVCMOS	SPI serial clock input.
15	MOSI (SPI)	I, LVCMOS	SPI Master Output / Slave Input. LMH0394 control data receive. This pin has an internal pulldown.
16	V_{CC}	Power	Positive power supply (2.5 V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground). See Figure 22 for layout example.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage		3.1	V
Input voltage (all inputs)	–0.3	V_{CC} + 0.3	V
Junction temperature		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} – V_{EE})	2.375	2.5	2.625	V
Input coupling capacitance		1		µF
Operating free-air temperature (T_A)	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH0394 RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

over supply voltage and operating temperature ranges, unless otherwise specified(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input voltage high level	Logic inputs	1.7		V_{CC}	V
V_{IL}	Input voltage low level	Logic inputs	V_{EE}		0.7	V
V_{SDI}	Input voltage swing	0m cable length(3) (SDI)	720	800	880	mV_{P-P}
V_{CMIN}	Input common-mode voltage			1.65		V
V_{SSP-P}	Differential output voltage, P-P	100-Ω load, default register settings, Figure 1(4) (SDO, $\overline{SDO}$)	500	700	900	mV_{P-P}
V_{OD}	Differential output voltage		250	350	450	mV
ΔV_{OD}	Change in magnitude of V_{OD} for complementary output states				50	mV
V_{OS}	Offset voltage		1.1	1.2	1.35	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states				50	mV
I_{OS}	Output short circuit current				30	mA
$MUTE_{REF}$	$MUTE_{REF}$ DC voltage (floating)	$MUTE_{REF}$		1.3		V
$MUTE_{RNG}$	$MUTE_{REF}$ range	$MUTE_{REF}$		0.8		V
V_{OH}	Output voltage high level	I_{OH} = -2 mA ($\overline{CD}$, MISO)	2.0			V
V_{OL}	Output voltage low level	I_{OL} = +2 mA ($\overline{CD}$, MISO)			0.2	V
I_{CC}	Supply current	Normal operation(5)		45	65	mA
		Power-save mode		7	10	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = 2.5 V and T_A = 25°C.
(3) The LMH0394 can be optimized for different launch amplitudes through the SPI.
(4) The differential output voltage and offset voltage are adjustable through the SPI.
(5) Typical I_{CC} is measured with a 2.97 Gbps input signal.

6.6 AC Electrical Characteristics

over supply voltage and operating temperature ranges, unless otherwise specified(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BR_{MIN}	Minimum input data rate	SDI, $\overline{SDI}$		125		Mbps
BR_{MAX}	Maximum input data rate	SDI, $\overline{SDI}$			2970	Mbps
TJ_{RAW}	Jitter for various cable lengths	2.97 Gbps, Belden 1694A, 0-100 meters(2)			0.2	UI
		2.97 Gbps, Belden 1694A, 100-140 meters(2)			0.3	UI
		2.97 Gbps, Belden 1694A, 140-180 meters(2)			0.5	UI
		2.97 Gbps, Belden 1694A, 180-200 meters		0.55		UI
		1.485 Gbps, Belden 1694A, 0-200 meters(2)			0.2	UI
		1.485 Gbps, Belden 1694A, 200-220 meters		0.3		UI
		270 Mbps, Belden 1694A, 0-400 meters(2)			0.3	UI
t_R, t_F	Output rise time, fall time	SDO, $\overline{SDO}$, 20% – 80%, and 100-Ω load Figure 1(3)		90	130	ps
ΔT_{R_F}	Mismatch in rise / fall time	SDO, $\overline{SDO}$ (3)		2	15	ps
t_{OS}	Output overshoot	SDO, $\overline{SDO}$ (3)		1%	5%	
RL_{IN}	Input return loss	5 MHz - 1.5 GHz(4) SDI or $\overline{SDI}$	15			dB
		1.5 GHz - 3.0 GHz(4) SDI or $\overline{SDI}$	10			dB
R_{IN}	Input resistance	single-ended SDI or $\overline{SDI}$		1.5		kΩ
C_{IN}	Input capacitance	single-ended SDI or $\overline{SDI}$		0.7		pF

(1) Typical values are stated for V_{CC} = 2.5 V and T_A = 25°C.
(2) Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with ST RP 184, ST RP 192, and the applicable serial data transmission standard: ST 424, ST 292, or ST 259.
(3) Specification is ensured by characterization.
(4) Input return loss is dependent on board design. The LMH0394 exceeds this specification on the SD394EVK evaluation board with a return loss network consisting of a 5.6-nH inductor in parallel with a 75-Ω series resistor on the input.

6.7 SPI Interface AC Electrical Characteristics

over supply voltage and operating temperature ranges, unless otherwise specified(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Recommended Input Timing Requirements						
f_{SCK}	SCK frequency				20	MHz
t_{PH}	SCK pulse width high	See Figure 2 and Figure 3	40			% SCK period
t_{PL}	SCK pulse width low		40			% SCK period
t_{SU}	MOSI set-up time	See Figure 2 Figure 3	4			ns
t_H	MOSI hold time		4			ns
t_{SSSU}	$\overline{SS}$ set-up time	See Figure 2 and Figure 3	14			ns
t_{SSH}	$\overline{SS}$ hold time		4			ns
t_{SSOF}	$\overline{SS}$ OFF-time		1			SCK period
Switching Characteristics						
t_{ODZ}	MISO driven-to-TRI-STATE time	See Figure 3			20	ns
t_{OZD}	MISO TRI-STATE-to-driven time				10	ns
t_{OD}	MISO output delay time				15	ns

(1) Typical values are stated for V_{CC} = 2.5 V and T_A = 25°C.

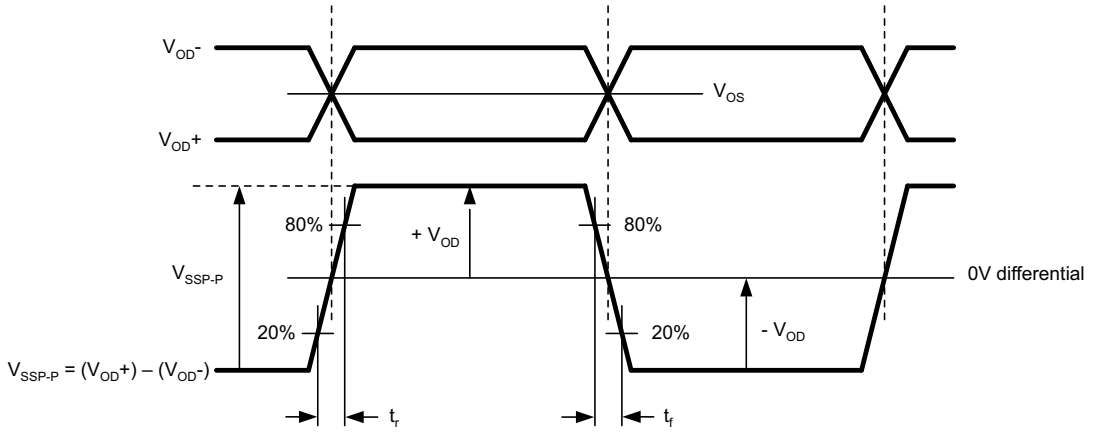


Figure 1. LVDS Output Voltage, Offset, and Timing Parameters

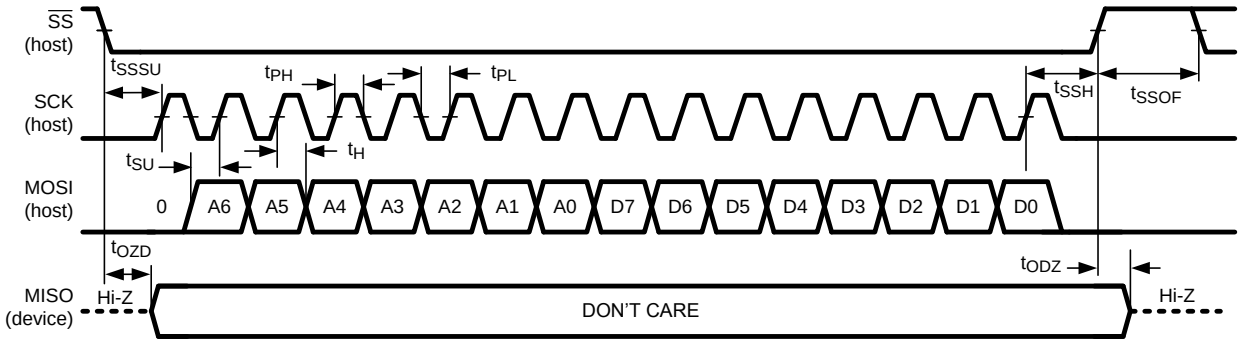


Figure 2. SPI Write

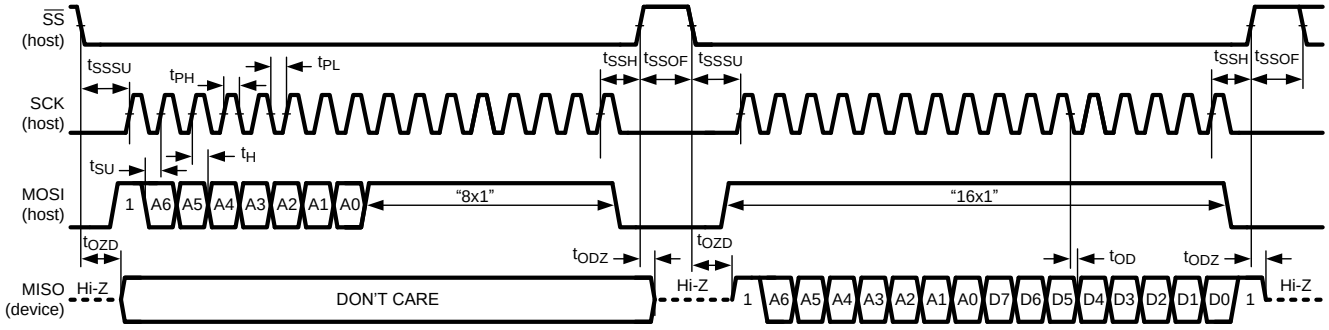


Figure 3. SPI Read

6.8 Typical Characteristics

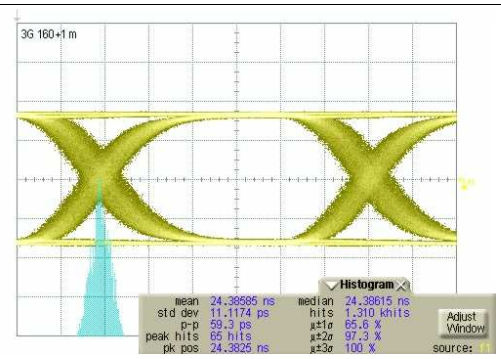


Figure 4. Differential Serial Data Output After Equalizing 161 Meters of Belden 1694A at 2.97 Gbps, PRBS10 Pattern

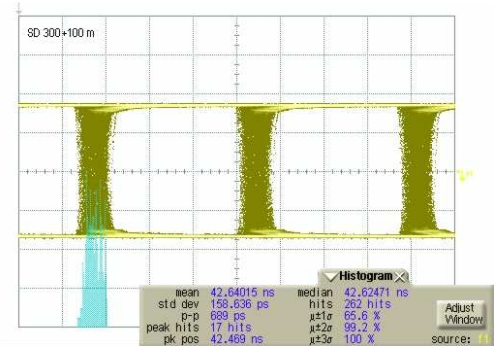


Figure 5. Differential Serial Data Output After Equalizing 400 Meters of Belden 1694A at 270 Mbps, PRBS10 Pattern

7 Detailed Description

7.1 Overview

The LMH0394 is a 3 Gbps HD/SD SDI low power extended reach adaptive cable equalizer. It is designed to equalize data transmitted over cable or any media with similar dispersive loss characteristics. The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, ST 259, and DVB-ASI standards. The LMH0394 features design enhancements including longer cable equalization, lower output jitter, configurable pin mode and SPI modes, a power-saving sleep mode, and programmable output common-mode voltage and swing. The LMH0394 implements DC restoration to correctly handle pathological data conditions.

The LMH0394 provides extended cable reach with improved immunity to crosstalk and ultra-low power consumption. The equalizer includes active sensing circuitry that ensures robust performance and enhanced immunity to variations in the input signal launch amplitude. The output driver offers programmable de-emphasis for up to 40” of FR4 trace losses. The LMH0394 includes power management to further reduce power consumption when no input signal is present.

7.2 Functional Block Diagram

The LMH0394 supports two modes of operation. In pin mode, the LMH0394 operates with control pins to set its operating state and is footprint compatible with the LMH0384, LMH0344, and legacy SDI equalizers. In SPI mode, an optional SPI serial interface can be used to access and configure multiple LMH0394 devices in a daisy-chain configuration.

This allows users to program the output common-mode voltage and swing, output de-emphasis level, input launch amplitude, and power management settings. Users may also access a cable length indicator and all pin mode features.

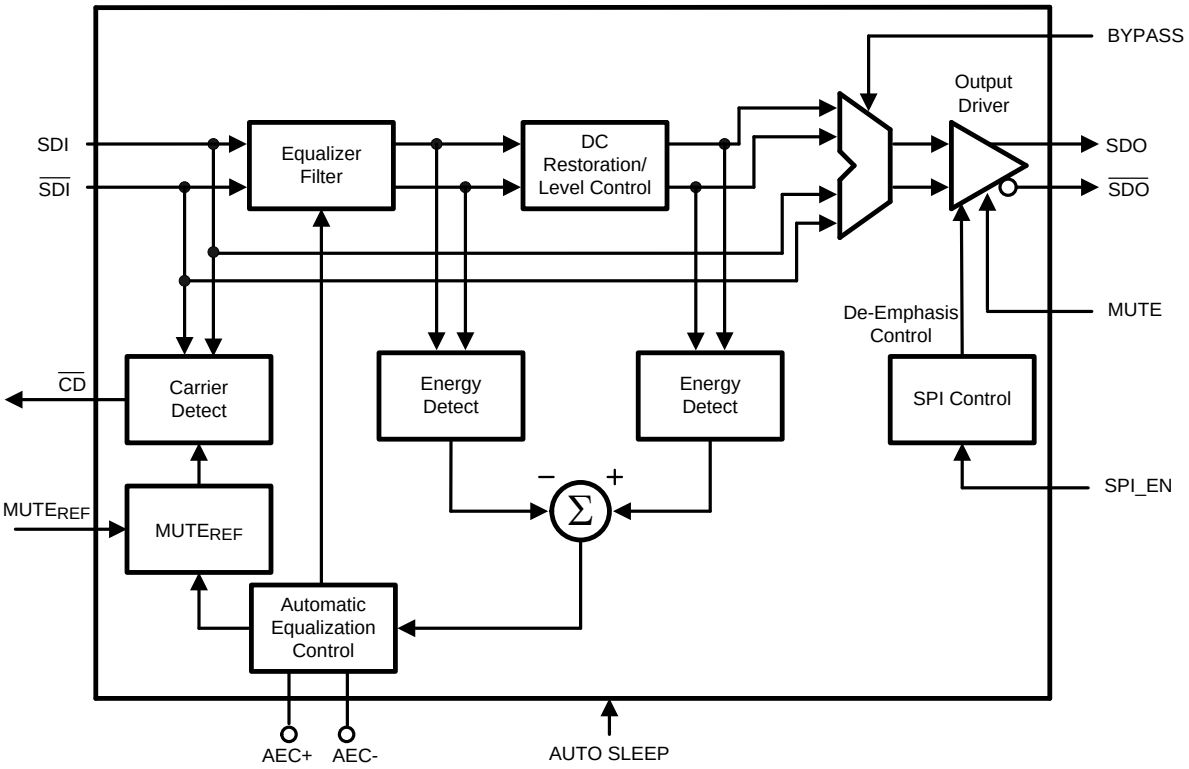


Figure 6. Functional Block Diagram (Pin Mode)

7.3 Feature Description

7.3.1 Block Description

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter.

The **Carrier Detect** block generates the carrier detect signal based on the SDI input and an adjustment from the **Mute Reference** block.

The **SPI Control** block uses the MOSI, MISO, SCK, and $\overline{SS}$ signals in SPI mode to control the SPI registers. SPI_EN selects between SPI mode and pin mode. In pin mode, SPI_EN is driven logic low.

The **Output Driver** produces SDO and $\overline{SDO}$.

7.3.2 Mute Reference ($Mute_{REF}$)

The mute reference sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. The applied voltage must be greater than the $MUTE_{REF}$ floating voltage (typically 1.3 V) in order to change the $\overline{CD}$ threshold. As the applied $MUTE_{REF}$ voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. $MUTE_{REF}$ may be left unconnected or connected to ground for normal $\overline{CD}$ operation. Optionally, the LMH0394 allows the mute reference to be set digitally through SPI register 03h.

Figure 7 shows the minimum $MUTE_{REF}$ input voltage required to force carrier detect to inactive vs. Belden 1694A cable length. The results shown are valid for Belden 1694A cable lengths of 0-200 m at 2.97 Gbps, 0-220 m at 1.485 Gbps, and 0-400 m at 270 Mbps.

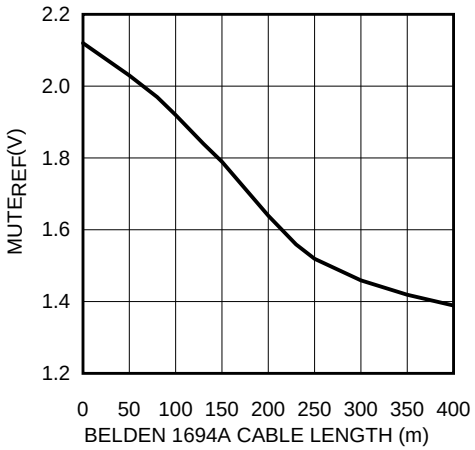


Figure 7. $MUTE_{REF}$ vs. Belden 1694A Cable Length

7.3.3 Carrier Detect ($\overline{CD}$) and Mute

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0394 input. This signal is a logical OR operation of the internal energy detector and $MUTE_{REF}$ setting (if used). The internal energy detector detects energy across different data rates. If $MUTE_{REF}$ is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0394 input. $\overline{CD}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and $\overline{SDO}$. Applying a high input to MUTE will mute the LMH0394 outputs by forcing the output to a logic 1. Applying a low input will force the outputs to be active.

Feature Description (continued)

In pin mode, $\overline{CD}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

7.3.4 Input Interfacing

The LMH0394 accepts single-ended input. The input must be AC coupled. The *Functional Block Diagram* shows the typical configuration for a single-ended input. The unused input must be properly terminated as shown in Figure 8 or Figure 9.

The LMH0394 can be optimized for different launch amplitudes through the SPI (see *Launch Amplitude Optimization* in the *SPI Register Access* section).

The LMH0394 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in ST RP 178 and RP 198, respectively.

7.3.5 Output Interfacing

SDO and $\overline{SDO}$ together are internally terminated 100-Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common-mode voltage (V_{OS}) is 1.2 V. The output common-mode voltage may be adjusted through the SPI in 200 mV increments, from 0.8 V to 1.2 V (see *Output Driver Adjustments and De-emphasis Setting* in the *SPI Register Access* section). When the output common mode is supply referenced, the common-mode voltage is about 1.35 V (for 700 mV_{P-P} differential swing). This adjustable output common-mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted through the SPI. Valid options are 400, 600, 700, or 800 mV_{P-P} (see *Output Driver Adjustments and De-emphasis Setting* in the *SPI Register Access* section).

The LMH0394 output must be DC coupled to the input of the receiving device where possible. 100-Ω differential transmission lines must be used to connect between the LMH0394 outputs and the input of the receiving device.

The LMH0394 output must not be DC coupled to CML inputs. If there are strong pullup resistors (that is, 50 Ω) at the receiving device, AC coupling must be used. The value of these AC-coupling capacitors must be large enough (typically 4.7 µF) to accommodate for the SD pathological video pattern.

Figure 8 shows an example of a DC-coupled interface between the LMH0394 and LMH0346 SDI reclocker. The differential transmission line must be terminated with a 100-Ω resistor at the receiving device as shown. The resistor should be placed as close as possible to the LMH0346 input. If desired, this network may be terminated with two 50-Ω resistors and a center-tap capacitor to ground in place of the single 100-Ω resistor.

Figure 9 shows an example of a DC-coupled interface between the LMH0394 and LMH0356 SDI reclocker. The LMH0356 inputs have internal 50-Ω terminations (100-Ω differential) to terminate the transmission line, so no additional components are required.

The LMH0394 output driver is equipped with programmable output de-emphasis to minimize inter-symbol interference caused by the loss dispersion from driving signals across PCB traces (see *Output Driver Adjustments and De-emphasis Setting* in the *SPI Register Access* section). De-emphasis works with all combinations of output common-mode voltage and output voltage swing settings to support DC coupling to the receiving device.

Feature Description (continued)

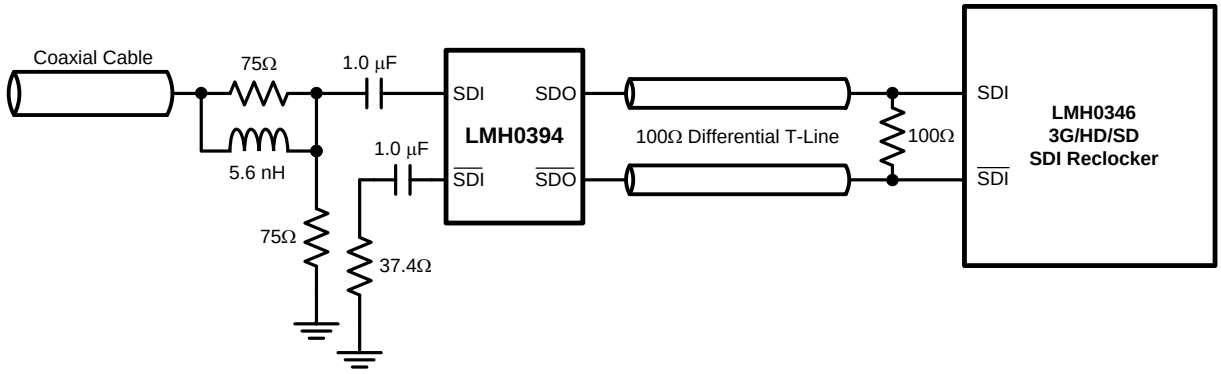


Figure 8. DC Output Interface to LMH0346 Reclocker

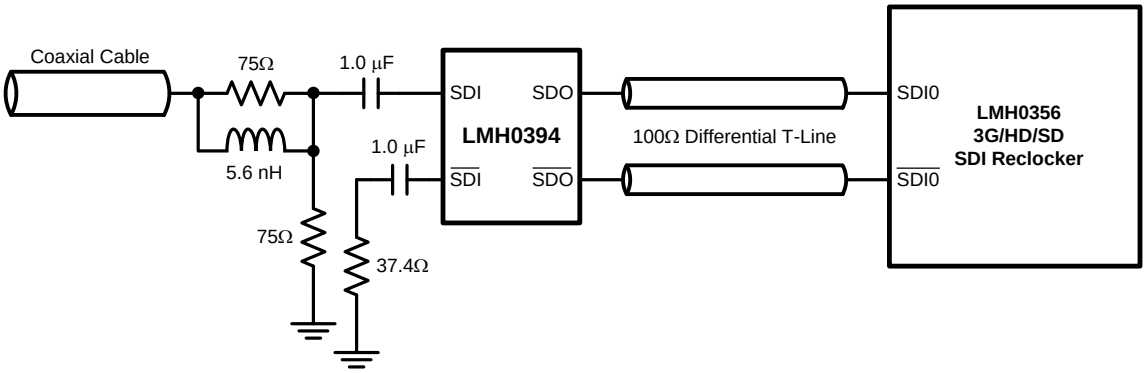


Figure 9. DC Output Interface to LMH0356 Reclocker

7.4 Device Functional Modes

The LMH0394 supports two modes of operation. In pin mode, the LMH0394 operates with control pins to set its operating state and is footprint compatible with the LMH0384, LMH0344, and legacy SDI equalizers. In SPI mode, an optional SPI serial interface can be used to access and configure multiple LMH0394 devices in a daisy-chain configuration.

7.4.1 Auto Sleep

The auto sleep mode allows the LMH0394 to power down when no input signal is detected. If the AUTO SLEEP pin is set high, the LMH0394 goes into a deep power-save mode when no signal is detected. The device powers on again once an input signal is detected. The auto sleep functionality can be turned off by setting AUTO SLEEP low or tying this pin to ground. An additional auto sleep setting available in SPI mode can be used to force the equalizer to power down regardless of whether there is an input signal or not. Auto sleep has precedence over mute and bypass modes.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and should not have any impact on the system timing requirements. The device will wake up automatically once an input signal is detected, and the delay between signal detection and full functionality of the equalizer is negligible (about 5 ms). The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

7.5 Programming

7.5.1 SPI Register Access

Setting SPI_EN high enables the optional SPI register access mode. In SPI mode, the LMH0394 provides register access to all of its features along with a cable length indicator, programmable output de-emphasis, programmable output common-mode voltage and swing, digital $MUTE_{REF}$, and launch amplitude optimization. There are eight supported 8-bit registers in the device (see Table 1). The LMH0394 supports SPI daisy-chaining among an unlimited number of LMH0394 devices. With SPI_EN set low, the device operates in pin mode and is footprint compatible with the LMH0384, LMH0344, LMH0044, and LMH0074.

7.5.1.1 SPI Transaction Overview

Each SPI transaction to a single device is 16-bits long. The transaction is initiated by driving $\overline{SS}$ low, and completed by returning $\overline{SS}$ high. The 16-bit MOSI payload consists of the read/write command (“1” for reads and “0” for writes), the seven address bits of the device register (MSB first), and the eight data bits (MSB first). The LMH0394 MOSI input data is latched on the rising edge of SCK, and the MISO output data is sourced on the falling edge of SCK.

In order to facilitate daisy-chaining, the prior SPI command, address, and data are shifted out on the MISO output as the current command, address, and data are shifted in on the MOSI input. For SPI writes, the MISO output is typically ignored as “Don't Care” data. For SPI reads, the MISO output provides the requested read data (after 16 periods of SCK). The MISO output is active when $\overline{SS}$ low, and tri-stated when $\overline{SS}$ is high.

7.5.1.2 SPI Write

The SPI write is shown in Figure 2. The SPI write is 16 bits long. The 16-bit MOSI payload consists of a “0” (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0394's MOSI input. After the SPI write, $\overline{SS}$ must return high. The prior SPI command, address, and data shifted out on the MISO output during the SPI write is shown as “Don't Care” on the MISO output in Figure 2.

7.5.1.3 SPI Read

The SPI read is shown in Figure 3. The SPI read is 32 bits long, consisting of a 16-bit read transaction followed by a 16-bit dummy read transaction to shift out the read data on the MISO output. The first 16-bit MOSI payload consists of a “1” (read command), seven address bits, and eight “1”s which are ignored. The second 16-bit MOSI payload consists of 16 “1”s which are ignored but necessary in order to shift out the requested read data on the MISO output. The $\overline{SS}$ signal is driven low, and the first 16 bits are sent to the LMH0394's MOSI input. The prior SPI command, address, and data are shifted out on the MISO output during the first 16-bit transaction, and are typically ignored (this is shown as “Don't Care” on the MISO output in Figure 3. $\overline{SS}$ must return high and then is driven low again before the second 16 bits (all “1”s) are sent to the LMH0394's MOSI input. Once again, the prior SPI command, address, and data are shifted out on the MISO output, but this data now includes the requested read data. The read data is available on the MISO output during the second 8 bits of the 16-bit dummy read transaction, as shown by D7-D0 in Figure 3.

7.5.1.4 SPI Daisy-Chain Operation

The LMH0394 SPI controller supports daisy-chaining the serial data between an unlimited number of LMH0394 devices. Each LMH0394 device is directly connected to the SCK and $\overline{SS}$ pins on the host. However, only the first LMH0394 device in the chain is connected to the host’s MOSI pin, and only the last device in the chain is connected to the host’s MISO pin. The MISO pin of each intermediate LMH0394 device in the chain is connected to the MOSI pin of the next LMH0394 device, creating a serial shift register.

This daisy-chain architecture is shown in Figure 10.

Programming (continued)

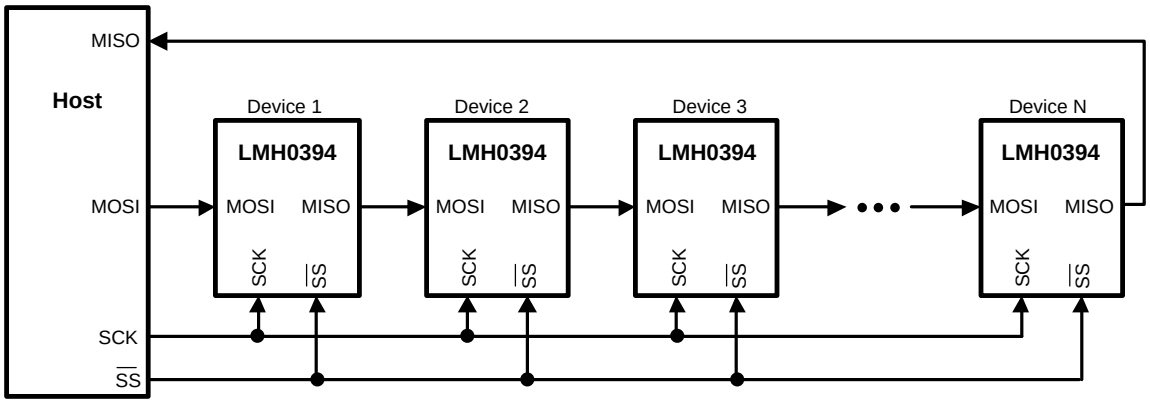


Figure 10. SPI Daisy Chain System Architecture

In a daisy-chain configuration of N LMH0394 devices, the host conceptually sees a shift register of length 16xN. Therefore the length of SPI transactions (as previously described) is 16xN bits, and $\overline{SS}$ must be asserted for 16xN clock cycles for each SPI transaction.

7.5.1.5 SPI Daisy-Chain Write

Figure 11 shows the SPI daisy-chain write for a daisy-chain of N devices. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI write data for Device N (the last device in the chain), followed by the write data for Device –1, Device –2, etc., ending with the write data for Device 1 (the first device in the chain). The 16-bit SPI write data for each device consists of a "0" (write command), seven address bits, and eight data bits. After the SPI daisy-chain write, $\overline{SS}$ must return high and then the write occurs for all devices in the daisy-chain.

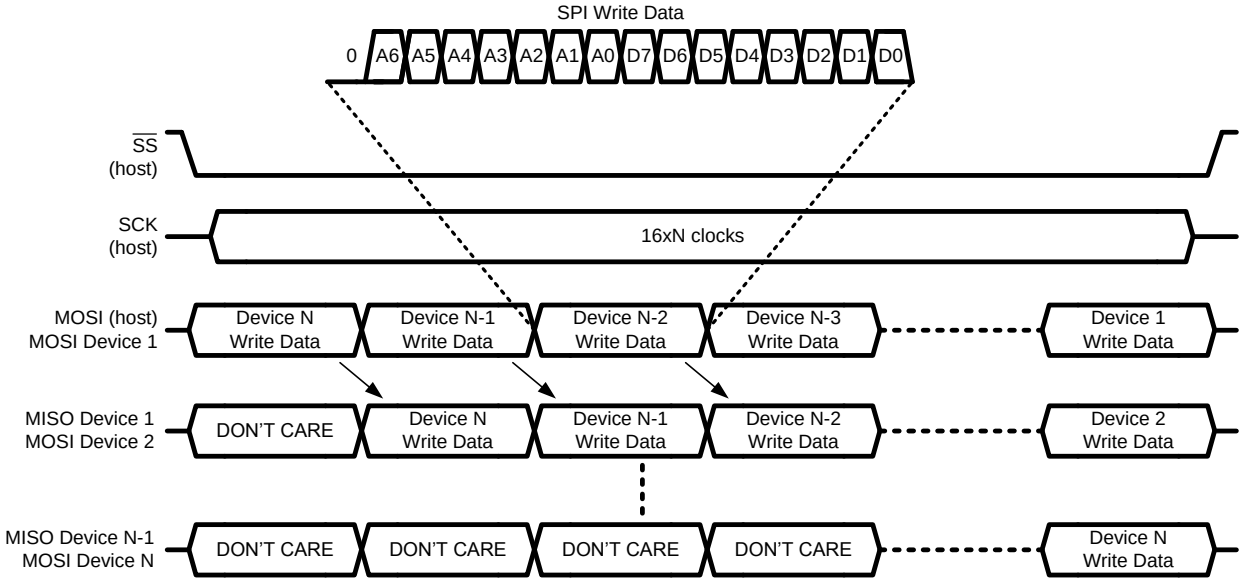


Figure 11. SPI Daisy-Chain Write

Programming (continued)

7.5.1.6 SPI Daisy-Chain Read

Figure 12 shows the SPI daisy-chain read for a daisy-chain of N devices. The SPI daisy-chain read is 32xN bits long, consisting of 16xN bits for the read transaction followed by 16xN bits for the dummy read transaction (all "1"s) to shift out the read data on the MISO output. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The first 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI read data for Device N (the last device in the chain), followed by the read data for Device –1, Device –2, etc., ending with the read data for Device 1 (the first device in the chain). The 16-bit SPI read data for each device consists of a "1" (read command), seven address bits, and eight "1"s (which are ignored). After the first 16xN bit transaction, $\overline{SS}$ must return high (to latch the data) and then is driven low again before the second 16xN bit transaction of all "1"s is sent to the MOSI input. The requested read data is shifted out on MISO starting with the data for Device N and ending with the data for Device 1. After this transaction, $\overline{SS}$ must return high.

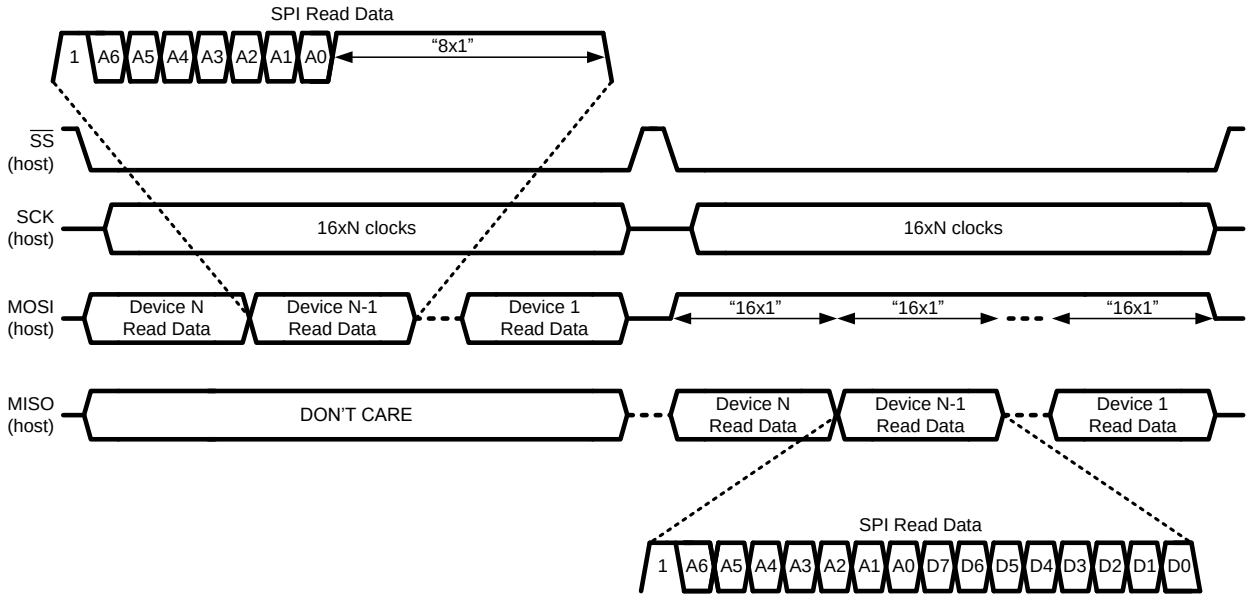


Figure 12. SPI Daisy-Chain Read

7.5.1.7 SPI Daisy-Chain Read and Write Example

The following example further clarifies LMH0394 SPI daisy-chain operation. Assume a daisy-chain of three LMH0394 devices (Device 1, Device 2, and Device 3), with Device 1 as the first device in the chain and Device 3 as the last device in the chain, as shown by the first three devices in Figure 10. Because there are three devices in the daisy-chain, each SPI transaction is 48-bits long.

This example shows an SPI operation combining SPI reads and writes in order to accomplish the following three tasks:

1. Write 0x22 to register 0x01 of Device 3 in order to set the output swing to 400 mV_{P-P}.
2. Read the contents of register 0x00 of Device 2.
3. Write 0x10 to register 0x00 of Device 1 in order to force the sleep mode.

Figure 13 shows the two 48-bit SPI transactions required to complete these tasks (the bits are shifted in left to right).

Programming (continued)

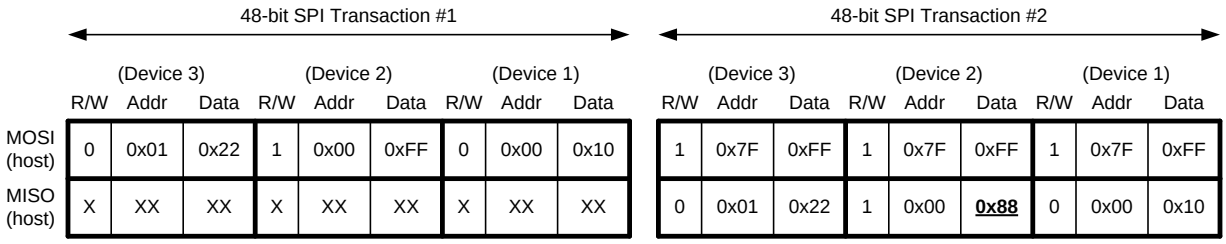


Figure 13. SPI Daisy-Chain Read and Write Example

The following occurs at the end of the first transaction:

1. Write 0x22 to register 0x01 of Device 3.
2. Latch the data from register 0x00 of Device 2.
3. Write 0x10 to register 0x00 of Device 1.

In the second transaction, three dummy reads (each consisting of 16 “1”s) are shifted in, and the read data from Device 2 (with value 0x88) appears on MISO in the 25th through 32nd clock cycles.

7.5.1.8 SPI Daisy-Chain Length Detection

A useful operation for the host may be to detect the length of the daisy-chain. This is a simple matter of shifting in a series of dummy reads with a known data value (such as 0x5A). For an SPI daisy-chain of N LMH0394 devices, the known data value will appear on the host's MISO pin after N+1 writes. Assuming a daisy-chain of three LMH0394 devices, the result of this operation is shown in Figure 14.

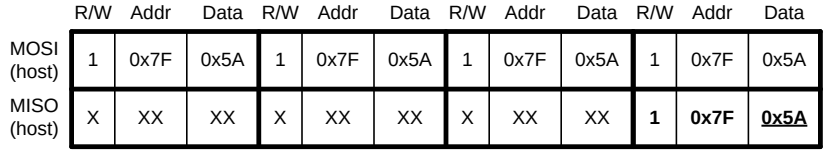


Figure 14. SPI Daisy-Chain Length Detection

7.5.1.9 Output Driver Adjustments and De-emphasis Setting

The output driver swing (amplitude), offset voltage (common-mode voltage), and de-emphasis level are adjustable through SPI register 01h.

The output swing is adjustable through bits [7:6] of SPI register 01h. The default value for these register bits is 10b for a peak to peak differential output voltage of 700 mV_{P-P}. The output swing can be set for 400 mV_{P-P}, 600 mV_{P-P}, 700 mV_{P-P}, or 800 mV_{P-P}.

The offset voltage is adjustable through bits [5:4] of SPI register 01h. The default value for these register bits is 10b for an output offset of 1.2 V. The output common-mode voltage may be adjusted in 200 mV increments, from 0.8 V to 1.2 V. It can be set to “11b” for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 1.35 V.

The output de-emphasis is turned on or off by bit 3 of SPI register 01h, and the de-emphasis level is set by bits [2:1] of SPI register 01h. The output de-emphasis level may be set for 0 dB (for driving up to 10” FR4), -3 dB (for driving 10-20” FR4), -5 dB (for driving 20-30” FR4), or -7 dB (for driving 30-40” FR4).

7.5.1.10 Launch Amplitude Optimization

The LMH0394 can compensate for attenuation of the input signal prior to the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

Programming (continued)

Bit 7 of SPI register 02h is used for the launch amplitude setting. At the default setting of “0b”, the LMH0394 operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to “1b” to optimize the LMH0394 for input signals with 6 dB of attenuation (400 mV_{P-P}).

7.5.1.11 Cable Length Indicator (CLI)

The cable length indicator (CLI) provides an indication of the length of the cable attached to input. CLI is accessible through bits [7:0] of SPI register 06h. The 8-bit setting ranges in decimal value from 0 to 247 (“00000000” to “11110111” binary), corresponding to 0 to 400 m of Belden 1694A cable. For 3G and HD input, CLI is 1.25 m per step. For SD input, CLI is 1.25 m per step, less 20 m, from 0 to 191 decimal, and 3.5 m per step from 192 to 247 decimal.

To calculate the Belden 1694A cable length (in meters) from the CLI decimal value for 3G or HD input:

$$\text{Cable Length} = \text{CLI} \times 1.25 \tag{1}$$

To calculate the Belden 1694A cable length (in meters) from the CLI decimal value for SD input:

For CLI ≤ 191,

$$\text{Cable Length} = (\text{CLI} \times 1.25) - 20$$

For CLI > 191,

$$\text{Cable Length} = ((191 \times 1.25) - 20) + ((\text{CLI} - 191) \times 3.5) \tag{2}$$

Figure 15 shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of 0-200 m at 2.97 Gbps, 0-220 m at 1.485 Gbps, and 0-400 m at 270 Mbps. Note: Given the continuous adaptive nature of the equalizer, the CLI values may vary constantly within several steps.

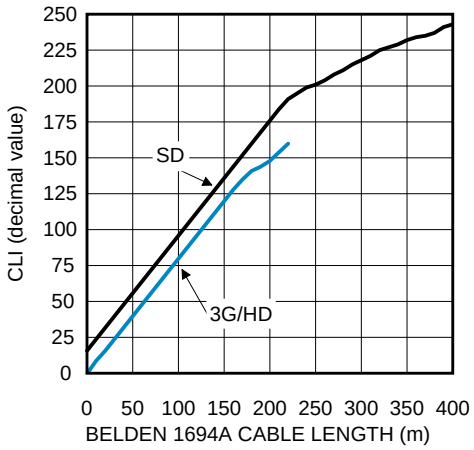


Figure 15. CLI vs. Belden 1694A Cable Length

7.6 Register Maps

Table 1. SPI Registers

Address	R/W	Name	Bits	Field	Default	Description
00h	R/W	General Control	7	Carrier Detect		Read only. 0: No carrier detected. 1: Carrier detected.
			6	Mute	0	Mute has precedence over Bypass. 0: Normal operation. 1: Outputs muted.
			5	Bypass	0	0: Normal operation. 1: Equalizer bypassed.
			4:3	Sleep Mode	01	Sleep mode control. Sleep has precedence over Mute and Bypass. 00: Disable sleep mode (force equalizer to stay enabled). 01: Sleep mode active when no input signal detected. 10: Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Reserved	0	Reserved as 0. Always write 0 to this bit.
			1	Master Reset	0	Reset registers and state machine. (This bit is self-clearing.) 0: Normal operation. 1: Reset registers and state machine.
			0	Acquisition Reset	0	Reset state machine. (This bit is self-clearing.) 0: Normal operation. 1: Reset state machine.

Register Maps (continued)

Table 1. SPI Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
01h	R/W	Output Driver	7:6	Output Swing	10	Output driver swing (V_{SSP-P}). 00: V_{SSP-P} = 400 mV_{P-P}. 01: V_{SSP-P} = 600 mV_{P-P}. 10: V_{SSP-P} = 700 mV_{P-P}. 11: V_{SSP-P} = 800 mV_{P-P}.
			5:4	Offset Voltage	10	Output driver offset voltage (common-mode voltage). 00: V_{OS} = 0.8 V. 01: V_{OS} = 1.0 V. 10: V_{OS} = 1.2 V. 11: V_{OS} referenced to positive supply.
			3	De-Emphasis	0	Output driver de-emphasis control. 0: De-emphasis disabled. 1: De-emphasis enabled.
			2:1	De-Emphasis Amplitude Level	01	Output driver de-emphasis level. 00: 0 dB (no de-emphasis). 01: -3 dB de-emphasis. 10: -5 dB de-emphasis. 11: -7 dB de-emphasis.
			0	Reserved	0	Reserved (read only).
02h	R/W	Launch Amplitude Control	7	Launch Amplitude Control	0	Launch amplitude optimization setting. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for 6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:0	Reserved	1101000	Reserved as 1101000. Always write 1101000 to these bits.

Register Maps (continued)

Table 1. SPI Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
03h	R/W	$MUTE_{REF}$	7:6	Reserved	00	Reserved as 00. Always write 00 to these bits.
			5	$MUTE_{REF}$ Mode	0	0: Use $MUTE_{REF}$ pin. 1: Use digital $MUTE_{REF}$.
			4:0	Digital $MUTE_{REF}$ Setting	11111	Digital $MUTE_{REF}$ (10m per step). 00000: Mute when cable (EQ boost) ≥ 10 m. ..... 01111: Mute when cable (EQ boost) ≥ 160 m. ..... 11111: Never mute.
04h	R	Device ID	7:6	Reserved	00	Reserved.
			5:4	EQ ID	01	00: LMH0384 device. 01: LMH0394 device. 10: LMH0395 device. 11: Reserved.
			3:0	Die Revision	0011	Die revision.
05h	R	Rate Indicator	7:6	Reserved	00	Reserved.
			5	Rate Indicator		0: SD. 1: 3G/HD.
			4:0	Reserved	11000	Reserved.
06h	R	Cable Length Indicator	7:0	Cable Length Indicator		Cable Length Indicator (CLI), with 10% accuracy. 00000000: Short cable. ..... 11110111: Maximum cable. 11111000: Reserved. ..... 11111111: Reserved.
07h	R	Launch Amplitude Indication	7:2	Launch Amplitude Indication		Indication of launch amplitude: 1% or 0.08 dB per step with 5% accuracy. 000000: Nominal -32%. ..... 011111: Nominal -1%. 100000: Nominal. 100001: Nominal +1%. ..... 111111: Nominal +31%.
			1:0	Reserved		Reserved.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH0394 3-Gbps HD/SD SDI Low Power Extended Reach Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports ST 424, ST 292, ST 344, ST 259, and DVB-ASI standards. Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation. The bypass pin allows the adaptive equalizer to be bypassed. The LMH0394 accepts single-ended input. The input must be AC coupled. The LMH0394 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in ST RP 178 and RP 198, respectively.

8.1.1 Interfacing to 3.3-V SPI

The LMH0394 may be controlled through optional SPI register access. The LMH0394 SPI pins support 2.5-V LVCMOS logic levels and are compliant with JEDEC JESD8-5 (see *DC Electrical Characteristics*). Care must be taken when interfacing the SPI pins to other voltage levels.

The 2.5-V LMH0394 SPI pins may be interfaced to a 3.3-V compliant SPI host by using a voltage divider or level translator. One implementation is a simple resistive voltage divider as shown in Figure 16.

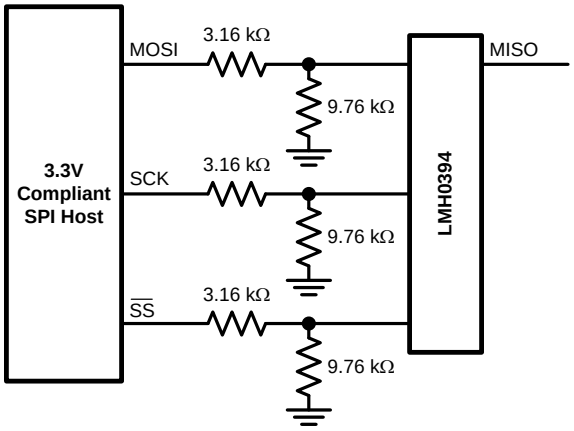


Figure 16. 3.3-V SPI Interfacing

8.1.2 Crosstalk Immunity

Single-ended SDI signals are susceptible to crosstalk and good design practices must be employed to minimize its effects. Most crosstalk originates through capacitive coupling from adjacent signals routed closely together through traces and connectors. To reduce capacitive coupling, SDI signals must be appropriately spaced apart or insulated from one another. This can be accomplished by physically isolating signal traces in the layout and by providing additional ground pins between signal traces in connectors as necessary. These techniques help to reduce crosstalk but do not eliminate it.

The LMH0394 was designed specifically with crosstalk in mind and incorporates advanced circuit design techniques that help to isolate and minimize the effects of cross-coupling in high-density system designs. The LMH0394's enhanced design results in minimal degradation in cable reach in the presence of crosstalk and overall superior immunity against cross-coupling from neighboring channels.

8.2 Typical Application

Figure 17 shows the application circuit for the LMH0394 in SPI mode. (Note: The application circuit shows an external capacitor connected between the AEC+ and AEC- pins as commonly configured in legacy equalizers. This capacitor is optional and not necessary for the LMH0394; the AEC+ and AEC- pins may be left unconnected with no change in performance.)

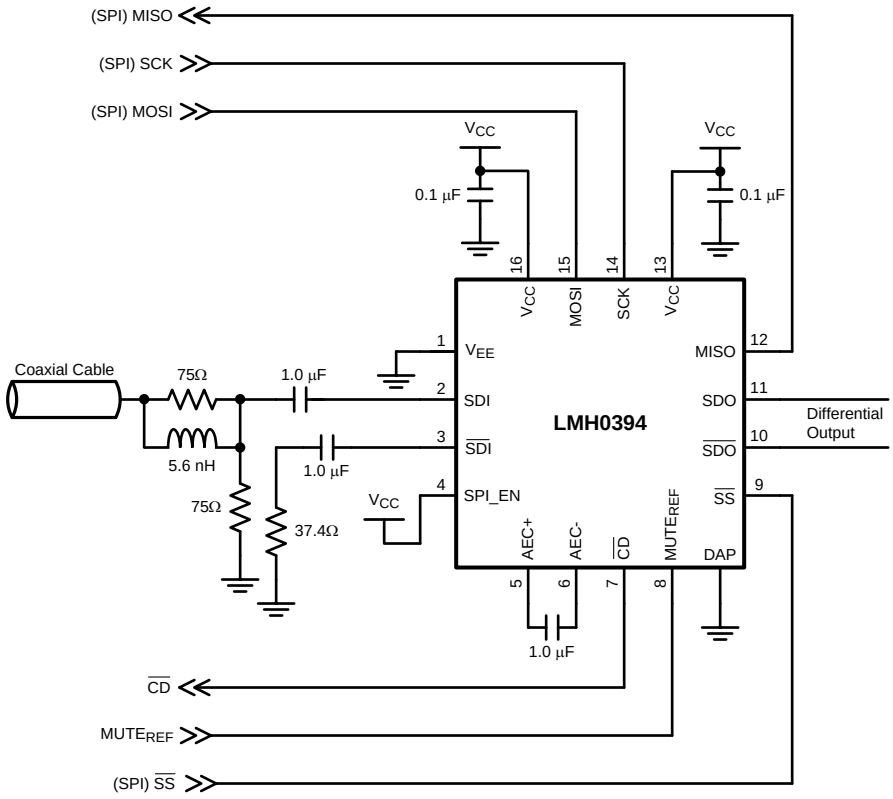


Figure 17. Application Circuit (SPI Mode)

8.2.1 Design Requirements

Table 2 lists the design parameters for the LMH0394.

Table 2. LMH0394 Design Parameters

DESIGN PARAMETER	REQUIREMENT
Input AC coupling capacitors	Required. A common type of AC coupling capacitor is 1-µF ± 10% X7R ceramic capacitor (0402 or 0201 size). Capacitors may be implemented on the PCB or in the connector.
Distance from Device to BNC	Keep this distance as short as possible.
High-Speed SDI, and $\overline{\text{SDI}}$ trace impedance	Design single-ended trace impedance with 75 Ω ± 5%
High-Speed SDO, and $\overline{\text{SDO}}$ trace impedance	Design differential trace impedance with 100 Ω ± 5%
DC Power Supply Coupling Capacitors	To minimize power supply noise, use 0.01-µF capacitors as close to the device VDD pins as possible

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

1. Maximum power draw for PCB regulator selection: Use maximum current consumption in the data sheet.
2. Closely compare schematic against typical connection diagram in the data sheet.
3. Plan out the PCB layout and component placement to minimize parasitic.
4. Consult the BNC vendor for optimum BNC landing pattern

8.2.3 Application Curves

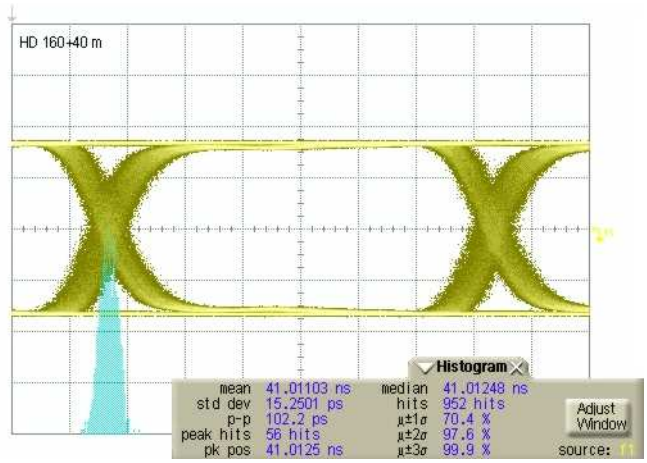


Figure 18. Differential Serial Data Output After Equalizing 200 Meters of Belden 1694A 1.485 Gbps, PRBS10

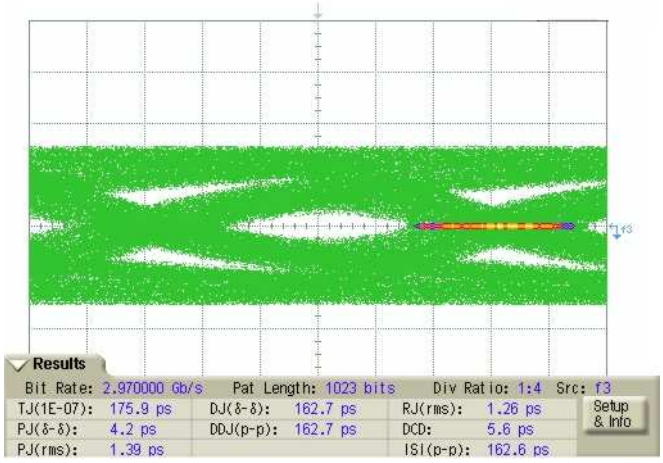


Figure 19. Differential Serial Data Output After 40 Inches FR4 With 0 dB De-Emphasis at 2.97 Gbps, PRBS10

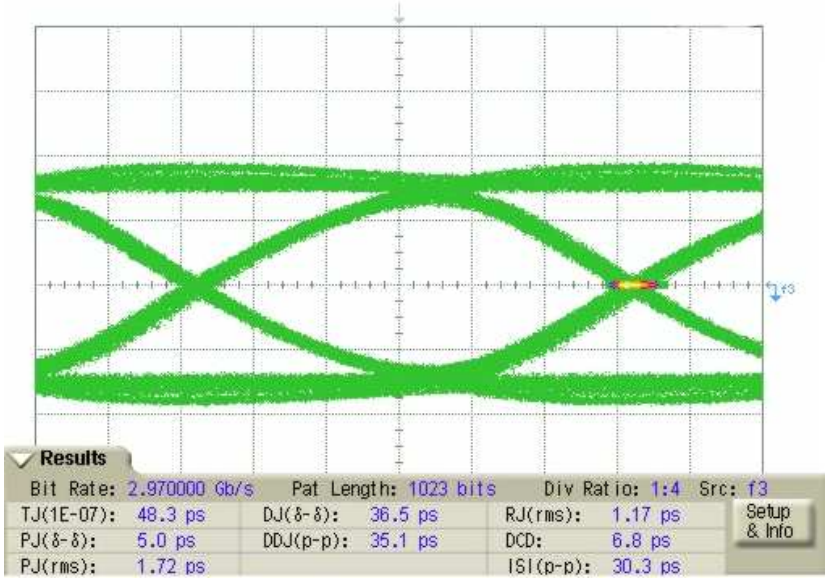


Figure 20. Differential Serial Data Output After 40 Inches FR4 With 7 dB De-Emphasis at 2.97 Gbps, PRBS10

8.3 Do's and Dont's

Pay special attention to the PCB layout for the high-speed signals. SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, and 3 Gbps data rates over coaxial cables. One of the requirements is meeting the required Return Loss. This requirement specifies how closely the port resembles 75-Ω impedance across a specified frequency band. The SMPTE specifications also defines the use of AC coupling capacitors for transporting uncompressed serial data streams with heavy low frequency content. This specification requires the use of a 1-µF AC coupling capacitor on the input of the LMH0394 to avoid low frequency bandwidth limitation.

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the recommended operating conditions in terms of DC voltage and maximum current consumption.
2. The maximum current draw for the LMH0394 is provided in the data sheet. This number can be used to calculate the maximum current the supply must provide.
3. The LMH0394 does not require any special power supply filtering, provided the recommended operating conditions are met. Use 0.01-µF capacitors as close to the device VDD pins as possible.

10 Layout

10.1 Layout Guidelines

For information on layout and soldering of the WQFN package, please refer to the following application note: *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

The ST 424, 292, and 259 standards have stringent requirements for the input return loss of receivers, which essentially specify how closely the input must resemble a 75-Ω network. Any non-idealities in the network between the BNC and the equalizer will degrade the input return loss. Care must be taken to minimize impedance discontinuities between the BNC and the equalizer to ensure that the characteristic impedance of this trace is 75 Ω. Please consider the following PCB recommendations:

- Use surface mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the equalizer.
- Select a board stack-up that supports both 75-Ω single-ended traces and 100-Ω loosely-coupled differential traces.
- Place return loss components closest to the equalizer input pins.
- Maintain symmetry on the complementary signals.
- Route 100-Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect equalizer power and ground pins to the respective power or ground planes.

10.2 Layout Example

Figure 22 and Figure 21 demonstrate the LMH0394EVM PCB layout. Ground and supply relief under the return loss passive components and pads reduces parasitic - improving return loss performance. The solder mask for the DAP is divided into four quadrants. Five via are placed such that they are in the boundary of the 4 quadrants. This is done to ensure that the via are not covered by solder mask for improving solder quality. This practice improves both thermal performance and soldering during board assembly.

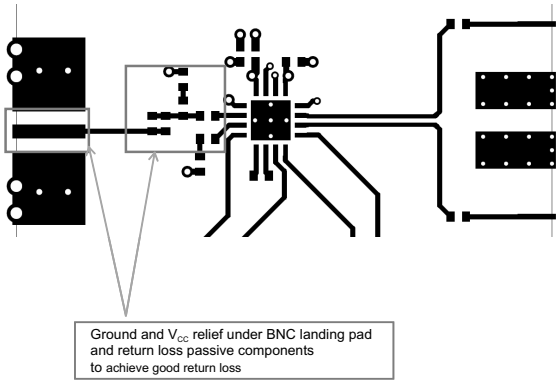


Figure 21. LMH0394EVM Top Etch Layout

Layout Example (continued)

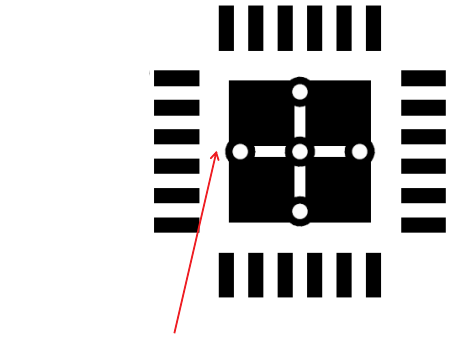


Figure 22. LMH0394EVM Top Solder Paste Mask

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

AN-1187 Leadless Leadframe Package (LLP), SNOA401.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0394SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L0394	Samples
LMH0394SQE/NOPB	ACTIVE	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L0394	Samples
LMH0394SQX/NOPB	ACTIVE	WQFN	RUM	16	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	L0394	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

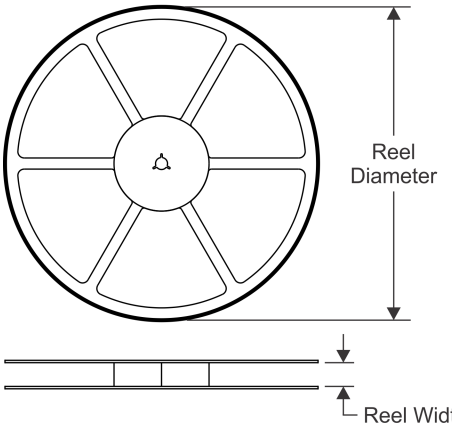
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

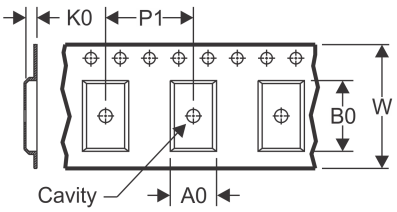
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

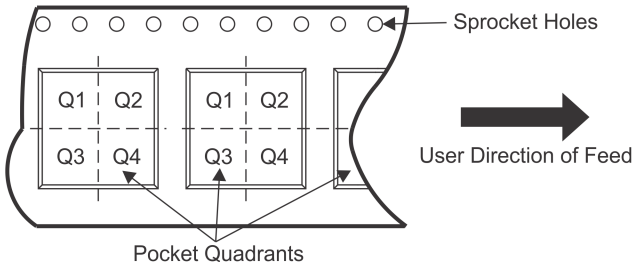


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

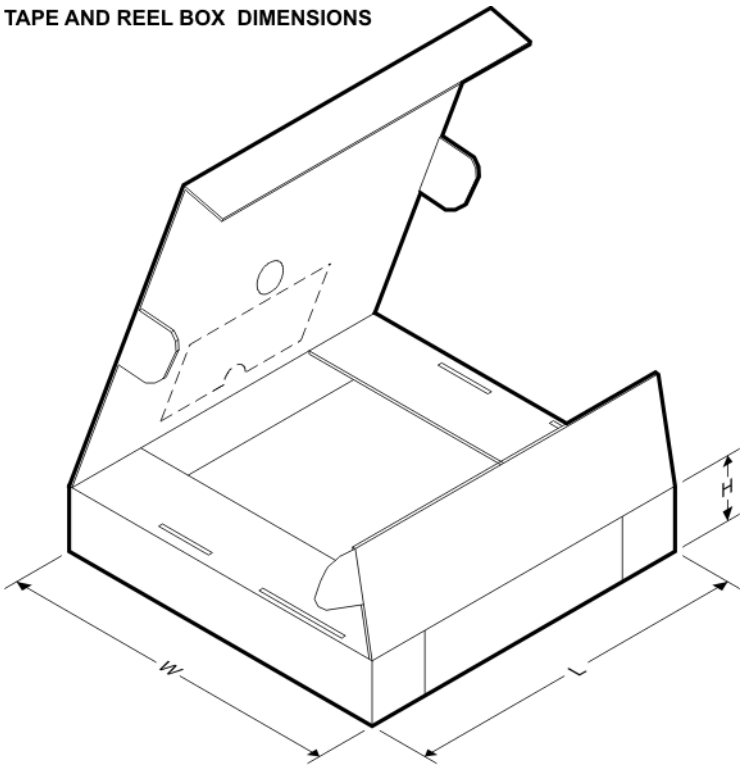
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0394SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0394SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0394SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

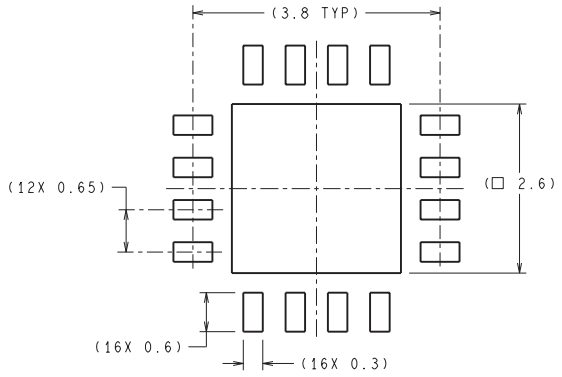
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

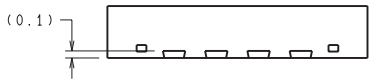
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0394SQ/NOPB	WQFN	RUM	16	1000	210.0	185.0	35.0
LMH0394SQE/NOPB	WQFN	RUM	16	250	210.0	185.0	35.0
LMH0394SQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0

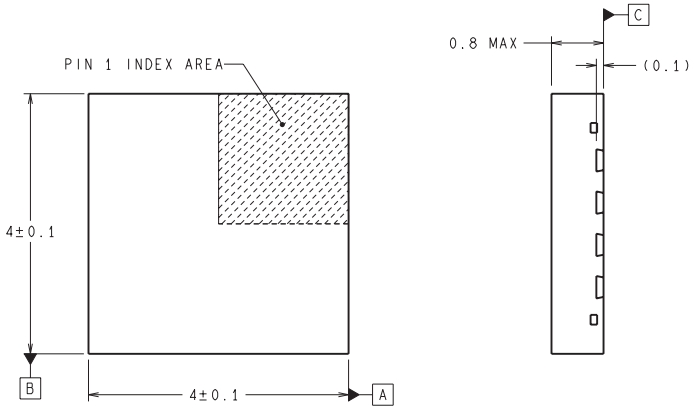
RUM0016A

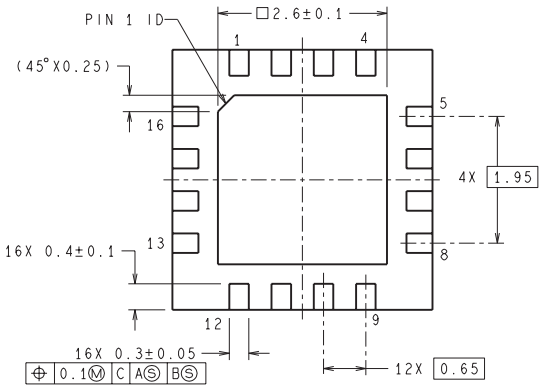


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY







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