ADS58C28 EVM

This is the user's guide for the ADS58C28 EVM Rev B. The ADS58C28 is a dual channel, 11-bit, 200MSPS analog-to-digital converter. This EVM is specifically suited for interfacing with TI's TSW1200 EVM to capture and display waveforms from the ADC. The EVM schematic, BOM, and layout files can be found in the design package in the ADS58C28 EVM product folder on www.ti.com.

1 Software Control

1.1 Installation Instructions

- Open folder named: ADS58C28_ADS42xx_Installer_vxpx (where xpx represents the latest version)
- Double-click: **setup.exe**
- Follow on-screen instructions to complete GUI installation
  - Wait for "ADS58C28/ADS42xx_ Installer" initializing screen to complete
  - Click "Next" to install files in the default destination directory
  - Select "I accept the License Agreement" and click "Next"
  - Select "Next" on the summary page
  - Wait for files to load and then click "Next"
  - Once all files are installed click "Next"
- If Windows Logo Message window appears, click "Continue Anyway"
- Once installed, launch by clicking on the ADS58C28_ADS42xx_GUI_vxpx program in Start>Texas Instruments ADCs
- When plugging in the USB cable for the first time, you will be prompted to install the USB drivers.
  - On the Welcome to the Found New Hardware Wizard window select "No, not at this time"
  - Select "Install the software automatically" button on the next window
  - Select "Continue Anyway" on the Windows Logo Message window
  - If computer can not find the drivers automatically then you can access them directly in the install directory: C:\Program Files\Texas \Instruments\ADS58C28_ADS42xx\data
  - Click "Finish" once completed

1.2 Software Operation

The software allows full programming control of the ADC device. Figure 1 shows the GUI front panel that has two register tabs: Top Level and Advanced. The Top Level tab provides an interface to the most used registers. The Advanced tab includes less used registers and provides an option to manually input address and data values.

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1.2.1 Top Level

Figure 1 shows the Top Level tab of the register user interface. Below is a brief explanation of the controls. Please refer to the ADS58C28 datasheet for more detailed explanations of the register functions as needed.

- Reset: Device reset, click this switch to reset the device.
- PND Global: Device power down, click this switch on to power down the device.
- Data format: Device output data format, click it to set 2's complement.
- LVDS_CMOS Ctrl: Select this box for LVDS or CMOS output format.
- Digital Funct Ctrl: Enable or disable three digital functions:
  - SNRb/Gain Disable – SNRBoost, gain, test patterns, and offset correction are disabled.
  - SNRb Enable Only – SNRBoost is enabled; gain, test patterns and offset correction are disabled.
  - SNRb/Gain Enable – SNRBoost, gain, test patterns, offset correction are enabled.
- Gain_chA: Set this box for gain of channel A.
- Gain_chB: Set this box for gain of channel B.
- Test Pattern: Select device test pattern.
- High Perf Mode: High performance mode enable or disable.
- High Freq Mode ChA: High frequency Mode enable for channel A.
- High Freq Mode ChB: High frequency Mode enable for channel B.
- Low Speed Mode En: Low speed mode enable or disable.
- Low Speed Mode ChA: Low speed mode for channel A.
- Low Speed Mode ChB: Low speed mode for channel B.
- LVDS Data Strength: Set the data strength from this switch.
- LVDS Clkout Strength: Set the output clock strength from this switch.
- CMOS Clk Strength: Set CMOS output clock strength from this switch.
- SNRBoost ChA: SNRBoost enable or disable for channel A.
- SNRBoost ChB: SNRBoost enable or disable for channel B.
- SNRBoost Filter ChA: Select SNRBoost filter for channel A.
- SNRBoost Filter ChB: Select SNRBoost filter for channel B.

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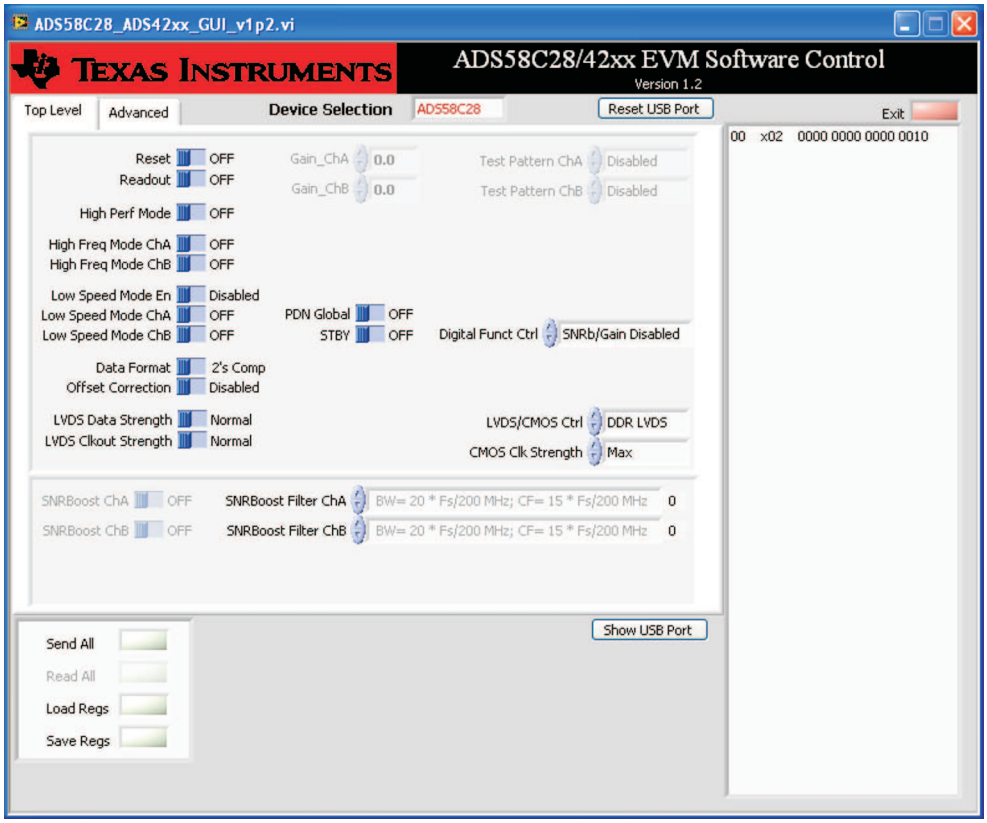


Figure 1. ADS58C28_ADS42xx_GUI Front Panel – Top Level

1.2.2 Advanced Level

Click on "Advanced" tab on the GUI to bring the advanced panel to the front. On this panel user can write address and data of any register into the address/data boxes (as shown in Figure 2, "45" is address and "4" is data). Press Enter on the key board once data is entered or click "Send All" button on the GUI to send address and data from the boxes to ADC. The address and data are shown in the display box located at right side of the panel. In addition, there is group of switches used for output offset functions, SNRBoost pin overwrite, and a group of LEDs used to designate a custom test pattern.

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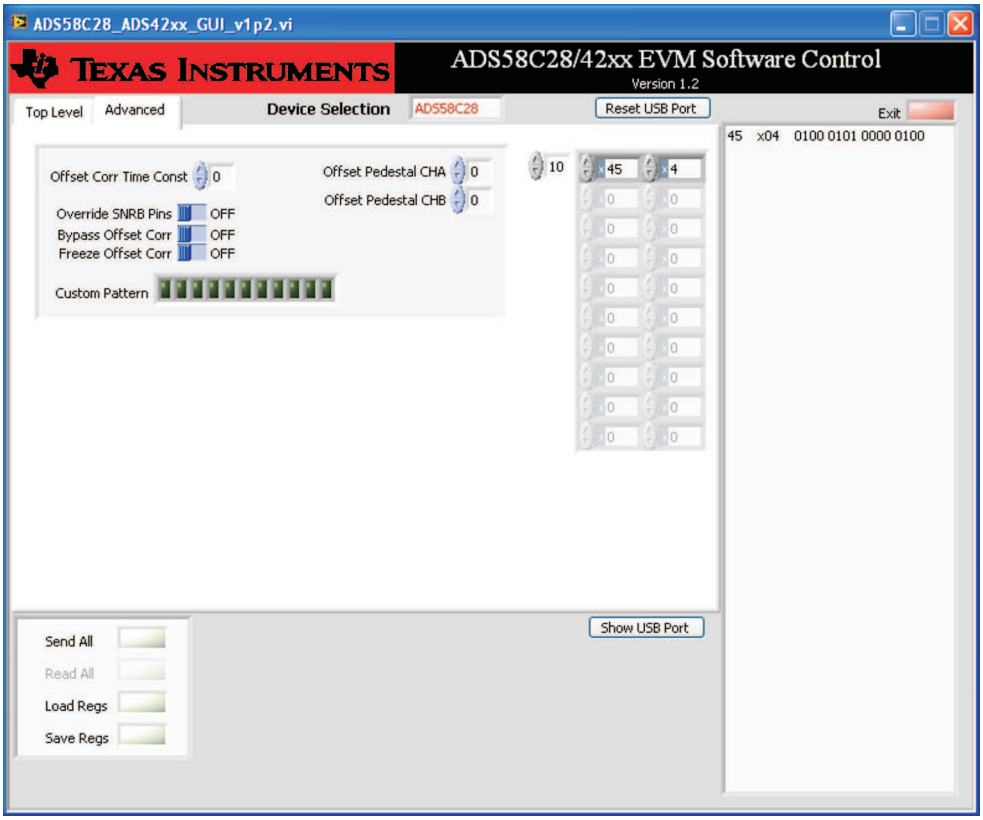


Figure 2. ADS58C28_ADS42xx_GUI – Advanced Level

1.2.3 Register Control

- Send All: Sends all the register configurations on the panel to the device
- Read All: Not active
- Save Regs: Saves the register configuration to text file
- Load Regs: Loads a register file from a text file. After load register the relative switches and selecting boxes are automatically updated.
  - Select Load Regs button.
  - Double click on the desired register file.
  - Click on Send All to ensure all of the values are loaded properly.

1.2.4 Misc Settings

- Device Selection: Select ADS58C28 for proper operation
- Reset USB: Toggle this button if the USB port is not responding. This generates a new USB handle address.
- Show USB Port: Allows user to change USB port configuration. Default setting is appropriate for the EVM RevB.
- Exit: Stops the program

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2 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

2.1 Test Block Diagram

The test set-up for general testing of the ADS58C28 with the TSW1200 capture card is shown in Figure 3.

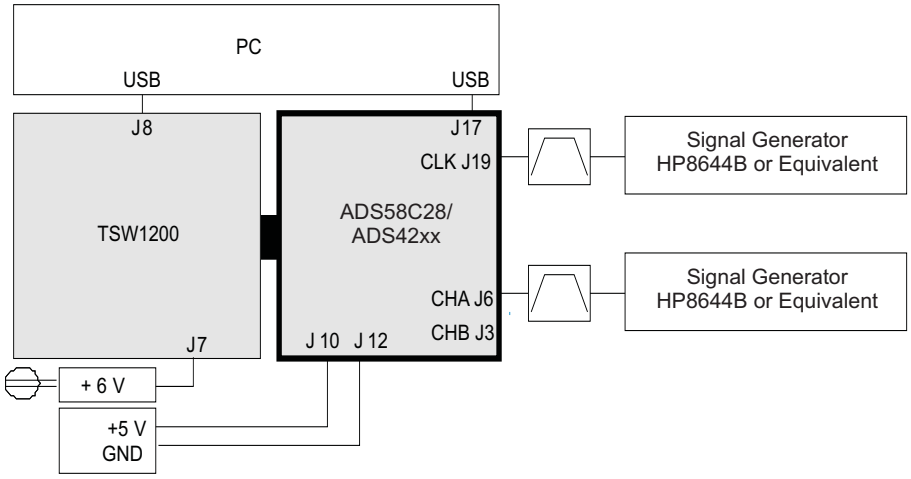


Figure 3. Test Set-up Block Diagram

2.2 Verify Board Set-up

Verify jumper settings are in the correct position as outlined in Table 1.

Table 1. Default ADS58C28/42xx EVM Rev B Jumper setting for serial interface

Jumper	Default position	Function
JP15	Short 1–2	DC supply
JP16	Short 1–2	DC supply
JP17	Short 2–3	DC supply, LDO
JP19	Short 2–3	DC supply, LDO
JP28	Short 2–3	DC supply, LDO
JP29	Short 2–3	DC supply, LDO
JP26	Open	DC supply for ext buffer
JP27	Open	DC supply for ext buffer
JP3	Short 2–3	OPA power down
JP4	Short 2–3	OPA power down
JP22	Open	SDOUT to FPGA
JP20	Short 1–2	CDC
JP21	Short 1–2	CDC
J14	Short 1–2	CDC power down
J18	Open	CDC, VCXO
JP8	Short 2–3	ADC SCLK for SPI
JP9	Short 2–3	ADC SDATA for SPI
JP10	Short 2–3	ADC SEN for SPI
JP11	Short 2–3	ADC for SPI, also reset
JP12	Short 1–2	ADC Low speed mode disable
JP13	Open	
JP14	Short 7 - 8	ADC 2's complement, DDR LVDS

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Table 1. Default ADS58C28/42xx EVM Rev B Jumper setting for serial interface (continued)

Jumper	Default position	Function
JP5	Short 1 - 2	ADC CTRL3, normal operation
JP6	Short 1 - 2	ADC CTRL2, normal operation
JP7	Short 1 - 2	ADC CTRL1, normal operation
JP 18	Short 1 - 2	Ext Buffer
JP 23	Short 1 - 2	Ext Buffer
JP 24	Short 1 - 2	Ext Buffer
JP 25	Short 1 - 2	Ext Buffer

Table 2. Parallel interface with Pin Control of ADS58C28/42xx EVM Rev B Jumper Setting

Jumper	Position	Function
JP8	Short 1 - 2	ADC SCLK for parallel control
JP9	Short 1 - 2	ADC SDATA for parallel control
JP10	Short 1 - 2	ADC SEN for parallel control
JP11	Short 1 - 2	ADC parallel control

2.3 Test Set-up Connections

- Connect ADS58C28 EVM to TSW1200 EVM
- Connect 5V power to banana jack at J10; connect ground to J12
- Connect USB cable to programming computer at J17
- Connect USB and power supply jack to TSW1200
- Connect Clock signal through appropriate BPF to J19
- Connect input signal through appropriate BPF to J6 or J3

2.4 TSW1200 Quick Start Operation

Reference the TSW1200 User's Guide for more detailed explanation of the TSW1200 set-up and operation. This document assumes the TSW1200 software is installed and functioning properly. The front panel of the TSW1200 is shown in Figure 4. The following configuration needs to be changed from the default settings

- Jumper setting on TSW1200 board
  Set J11 (2-3) High, J10 (1-2) Low for LVDS DDR data input (default)
  Set J11 (2-1) Low, J10 (1-2) Low for 1-wire serial data input
- Select ADS58C28 device name from the TI ADC Selection pull-down menu
  - If this option is not available then download the latest ADS58C28.ini file from the product folder of the TSW1200 at www.ti.com
  - Place updated *.ini files in the TSW1200 product directory located at C:\Program Files\Texas Instruments\TSW1200\ADC Files
- Select Single Tone FFT from the Test pull-down menu
- Select Data Capture Option>Capture Options>Two's Complement Mode to set data format
- Select the desired channel (i.e., Channel A or B) from the Channel Display pull-down menu
- Change ADC sampling rate to desired value (i.e., 200 MHz)
- Change input frequency to desired value (i.e., 140 MHz or other)
- Press Ctrl-Shift-I to reset the software as needed
- Verify status display in lower left has no errors
- Press Capture button to initiate a data capture

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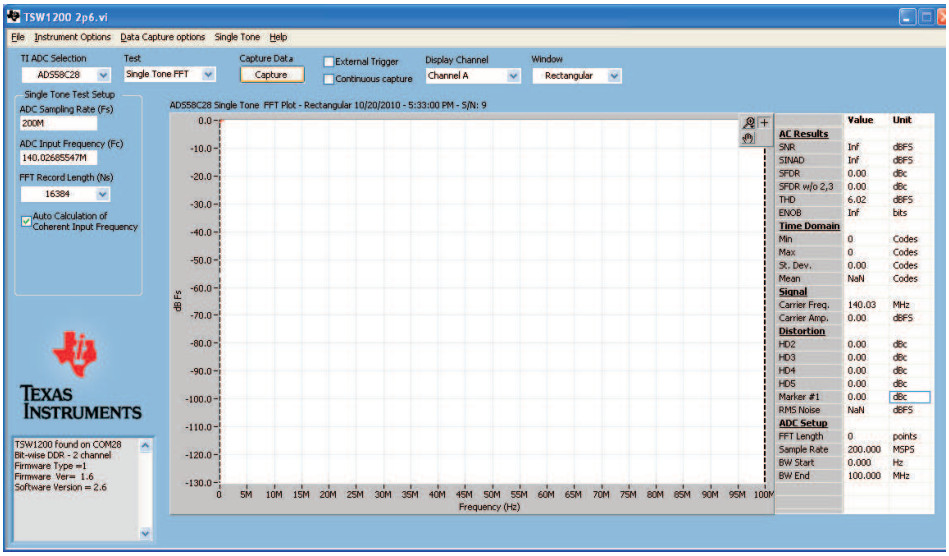


Figure 4. TSW1200 GUI

2.5 ADS58C28 Test Procedure

- Switch on 5V power supply on ADC EVM. Verify source current is about 310 mA ± 20 mA with clock and TSW1200 connected at EVM default (i.e., connected at 200MHz).
- Connect clock signal at J19 through an appropriate BPF.
  - Adjust the signal generator amplitude output 0.6Vrms to provide approximately 0.8 Vpp at J19 through a BPF with about 5 dB attenuation plus cable losses.
  - Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Connect input signal through an appropriate BPF at either J6 or J3 (Channel A or B, i.e., 140MHz).
  - Adjust frequency of generator to match the coherent frequency displayed in the TSW1200 GUI.
  - Select the proper Display Channel on the TSW1200 GUI software that corresponds to the input connection.
  - Adjust the signal generator amplitude output to achieve –1 dBFS on FFT plot at the "Carrier Amp" indicator.
  - Use a high quality, low phase noise generator for this input to ensure proper device evaluation.
- Enable SNR Boost (if desired) through either hardware or software.
  - Hardware enable by CTRL pins JP5, JP6 and JP7
    - Set Digital Funct Ctrl to "SNRb/Gain Disable"
    - Select desired SNRBoost Filter Chx register
    - Set Digital Funct Ctrl to "SNRb Enable Only"
    - Set hardware pins at jumper JP5 and JP6 to High (short 2–3), set JP7 to LOW (short 1–2) to enable SNRBoost.
    - See table 8 in SBAS509 datasheet for other hardware control options
  - Software enable by setting the GUI registers only
    - Set Digital Funct Ctrl to "SNRb/Gain Disable"
    - Set desired SNRBoost filter for Chx
    - Set Digital Funct Ctrl to "SNRb Enable Only"
    - Set Override SNRb Pins to "On" in Advanced panel
    - Set SNRBoost ChA and ChB to "On" in Top Level panel
- Initiate a capture by pressing the Capture button on the TSW1200 GUI

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2.6 ADS58C28 Performance Results

Figure 5 shows the performance results with the SNR Boost disabled at 200 MSPS clock frequency and with a 140 MHz input tone. Figure 6 shows the same set-up with SNR Boost enabled using a filter register setting of 40 (BW = 60 × Fs/184 MHz; CF = 46 × Fs/184 MHz) corresponding roughly to 60 MHz of BW for the given clocking rate. ADC calculations related to SNR and SFDR are completed over this specified bandwidth by adjusting the cursor bandwidth on the TSW1200 GUI.

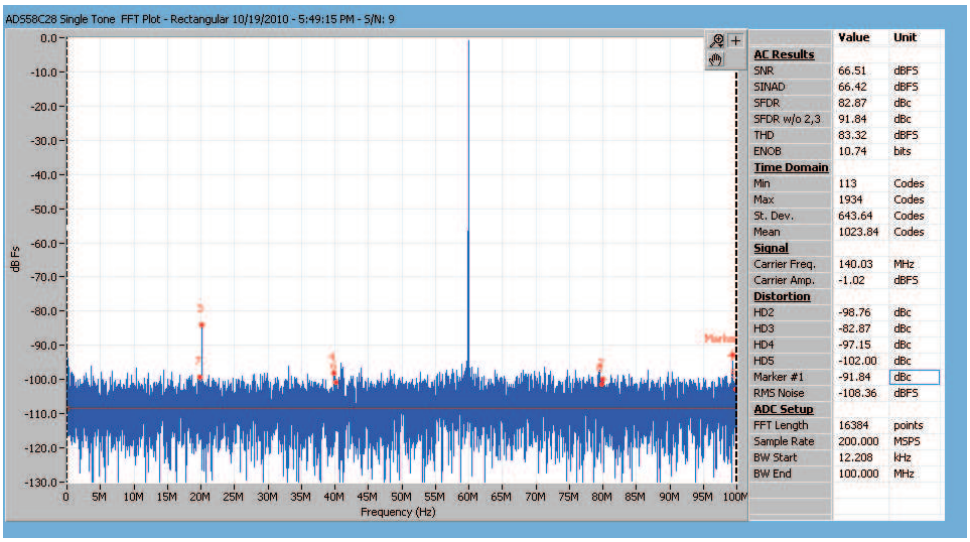


Figure 5. FFT Plot: 200 MHz Clock, 140 MHz input; SNRBOOST Disable

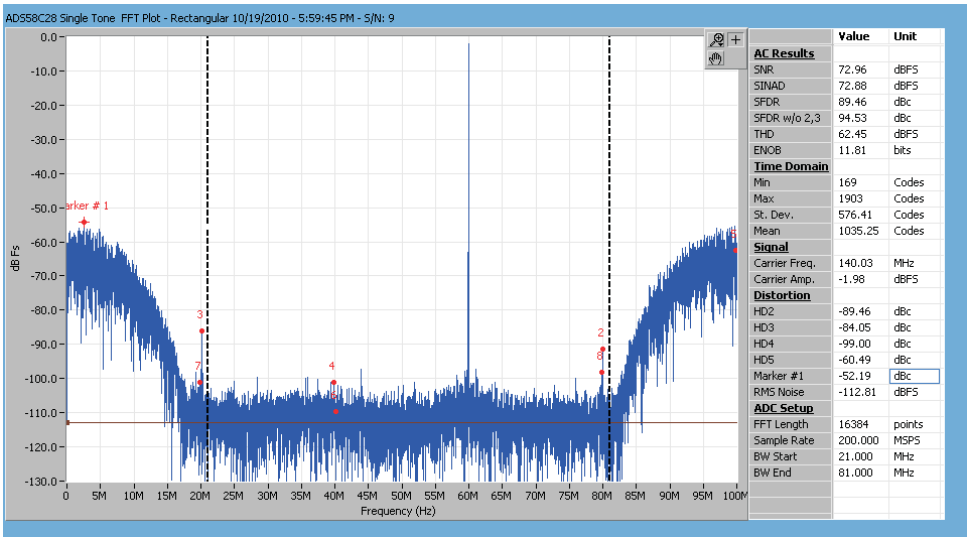


Figure 6. FFT Plot: 200 MHz clock, 140 MHz input; SNRBOOST Enabled with Filter #40 (BW 60MHz)

3 Optional Configurations

3.1 THS4509 Input Op-Amp Configuration

The default analog input configuration is transformer coupling through T1 and T2 for channel A, and T3 and T4 for channel B. The optional configuration for analog input is through an Op-Amp THS4509. The changes required to modify the transformer coupled input to the OPA-driven input are shown in Table 3.

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Table 3. Jumper Setting for Transformer-Coupled or OPA-Driven Input

Jumpers or 0 Ω	Transformer-coupled input (default)	OPA-driven input
R119	Install	Do not install
R123	Install	Do not install
R120	Do not install	install
R129	Do not install	install
R143	Install	Do not install
R141	Install	Do not install
R131	Do not install	Install
R132	Do not install	Install
R93	Install	Do not install
R94	Install	Do not install
R95	Do not install	Install
R96	Do not install	Install
R97	Install	Do not install
R98	Install	Do not install
R99	Do not install	Install
R114	Do not install	Install
SJP3	Shunt 2 - 3, default	Shunt 1-2
SJP4	Shunt 2 - 3, default	Shunt 1-2

J11 and J13 are the power supply for THS4509. An on-board layout option for a LPF or BPF is available between the amplifier and the ADC. By default the filter is bypassed to allow the user flexibility to design according to desired specifications.

3.2 On-board CDC72010 Clock

The default clock input configuration is 1:4 transformer coupling through T6. The optional configuration is through clock driver CDC72010. The changes required to modify the transformer coupled clock input to clock driver input are shown in Table 4.

Table 4. Jumper Setting for Transformer-Coupled or CDC72010 Input

Jumper	Transformer-coupled (Default)	CDC72010
J14	shunt	open
JP20	Shunt 1-2	Shunt 1-2
JP21	Shunt 1-2	Shunt 1-2
J18	open	open
R121	0 ohm	DNI
R122	DNI	0 ohm
SJP7	Short 1-2	Short 3-4
SJP6	Short 3-4	Short 5-6

The on-board layout is available for the option of VCXO and crystal BPF. The CDCE72010 comes with a default configuration (please see CDCE72010 data sheet for details about device default configuration). With a 10MHz primary reference at J19 and a 983.04 MHz VCXO on-board the CDC outputs a LVCMOS clock at U0P (pin7) at 245.76MHz. With a 491.52 MHz VCXO the CDC outputs a LVCMOS clock at U0P at 122.88MHz. The clock goes through an on-board crystal BPF (Y0) and is used as the input clock to the ADC through SJP6.

3.3 Parallel CMOS Output

The default ADC output is configured as DDR LVDS output on the EVM. The layout provides an option of 1.8V parallel CMOS output from the ADC. The changes required to modify from DDR LVDS output to parallel CMOS output are shown in Table 5.

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Table 5. Jumper/Component Setting for DDR LVDS Output and Parallel CMOS Output

Jumper/Component	DDR LVDS output	Parallel CMOS
U12 (SN74AVC16T245)	DNI	Installed
U13 (SN74AVC16T245)	DNI	Installed
RN5 to RN8	Installed	DNI
RN9 to RN12	Installed	DNI
JP26	Open	Shunt
JP27	Open	Shunt

The CMOS output data is output from the EVM board at 40-pin connectors J1 (ch A) and J2 (ch B).

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –0.3 V to 1.9 V and the output voltage range of –0.3 V to 2.1 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50° C. The EVM is designed to operate properly with certain components above 25° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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