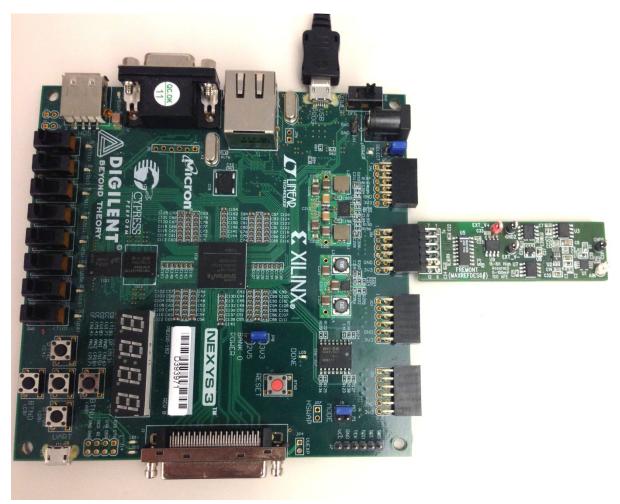


Fremont (MAXREFDES6#) Nexys 3 Quick Start Guide

Rev 0; 9/13



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Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000

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1. Required Equipment

- PC with Windows® OS with Xilinx® ISE®/SDK version 13.4 or later and two USB ports
- License for Xilinx EDK/SDK version 13.4 or later
- One +7V power supply
- One -6V power supply
- Fremont (MAXREFDES6#) board
- Nexys[™]3 development kit
- Industrial sensor or signal source

2. Overview

Below is a high-level overview of the steps required to quickly get the Fremont design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. The Fremont (MAXREFDES6#) subsystem reference design will be referred to as the Fremont throughout this document.

- 1. Connect the Fremont board to the JB1 port of a Nexys 3 development kit as shown in <u>Figure 1</u>. Ensure the connector is aligned as shown in <u>Figure 2</u>.
- 2. Connect the power supplies to the Fremont board.
- 3. Download the latest **RD6V01_00.ZIP** file located at the Fremont page.
- 4. Extract the **RD6V01_00.ZIP** file to a directory on your PC.
- 5. Open the Xilinx SDK.
- 6. Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
- 7. Open a terminal program to communicate with FPGA board.
- Use Xilinx SDK to download and run the executable file (.ELF) on the MicroBlaze[™].

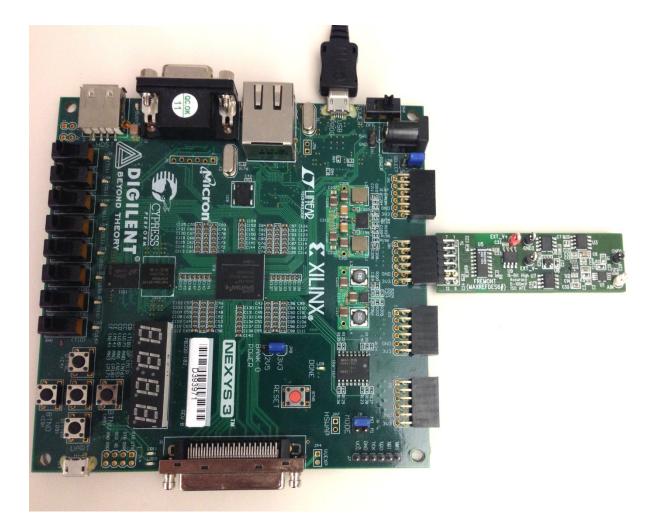


Figure 1. Fremont Board Connected to Nexys 3 Development Kit



Figure 2. Pmod[™] Connector Alignment

3. Included Files

The top level of the hardware design is a Xilinx ISE Project Navigator Project (.XISE) for Xilinx ISE version 13.4. The Verilog-based HDL design instantiates the MicroBlaze core, the support hardware required to run the MicroBlaze and the peripherals that interface to the Pmod ports. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Fremont subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

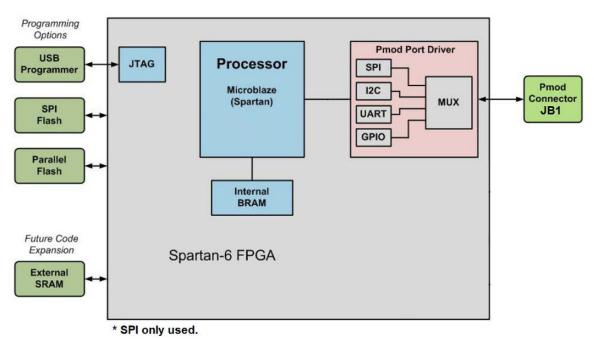


Figure 3. Block Diagram of FPGA Hardware Design

4. Procedure

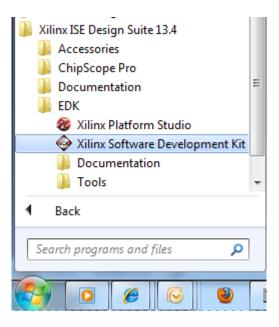
- 1. Connect the Fremont board to the JB1 port of a Nexys 3 development kit as shown in Figure 1. Power up the Nexys 3 development kit.
- Connect the +7V power supply to the EXT_V+ connector. Connect the -6V power supply to the EXT_V- connector. Connect the ground terminal of the power supplies to the GND2 connector.
- Download the latest RD6V01_00.ZIP file located at <u>www.maximintegrated.com/fremont</u>. All files available for download are available at the bottom of the page.
- 4. Extract the **RD6V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the path prior to where you extract the .ZIP file must not exceed 82 characters due to the Windows 250-character total path limitation. For example, this 90-character preceding path would be an example of a path that would be too long:

C:\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\RD6V01_00.ZIP (This path is too long.)

In addition, the Xilinx tools require the path to not contain any spaces.

C:\Do Not Use Spaces In The Path\RD6V01_00.ZIP (This path has spaces.)

For the purposes of this document, it will be **C:\designs\maxim\RD6V01_00**. See <u>Appendix A: Project Structure and Key Filenames</u> in this document for the project structure and key filenames. 5. Open the Xilinx Software Development Kit (SDK) from the Windows Start menu.



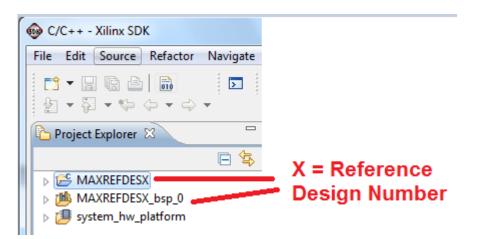
6. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is

C:\designs\maxim\RD6V01_00\RD6_NEXYS3_V01_00\Design_Files\sdkWorkspace

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse[™]-based IDE, so it will be a familiar flow for many software developers.

Workspace Launcher	×
Select a workspace	
Xilinx SDK stores your projects in a folder called a workspace. Choose a workspace folder to use for this session.	
Workspace: Enter the path from the instructio	ns <u>B</u> rowse
Use this as the default and do not ask again	OK Cancel

7. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.



8. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to

C:\designs\maxim\RD6V01_00\RD6_NEXYS3_V01_00\Design_Files\sdkWorkspace

and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

Click **Finish** to import the projects.

😥 Import	
Select Create new projects from an archive file or directory.	
Select an import source:	
type filter text	
 General Archive File Existing Projects into Workspace File System Preferences C/C++ Remote Systems Run/Debug Team 	
Cancel Cancel Cancel]

9. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).



The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected as well as an FPGA BMM (.BMM) file. Be sure to select the .BIT file and the .BMM by using the paths below.

Bitstream:

C:\designs\maxim\RD6V01_00\RD6_NEXYS3_V01_00\Design_Files\ sdkWorkspace\system_hw_platform\system.bit

BMM File:

C:\designs\maxim\RD6V01_00\RD6_NEXYS3_V01_00\Design_Files\ sdkWorkspace\system_hw_platform\system_bd.bmm Additionally, make sure **bootloop** is selected as shown, then press **Program**.

Program FPGA				×
Program FPGA Specify the bitstre	am and the ELF files that reside in BRAM m	emory		→ □ □ □
Hardware Specific	ation: path filled in auto	matically		
Bitstream: BMM File:	nter the path from the i	nstructions		Browse
Processor	ELF File to Initialize in Block RAM			
microblaze_0	bootloop	T		
?			Program	Cancel

It takes approximately 10 seconds to download the FPGA and a message box indicating **FPGA configuration complete** appears.

10. Setup of the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

The Nexys 3 utilizes the FTDI FT232 USB-UART bridge IC, so you need to install FTDI's virtual COM port (VCP) driver for their FT232 device family. Make sure to choose the driver that supports a "Virtual Com Port," also known as VCP. These may be obtained from the FTDI website (www.ftdichip.com).

Once installed, Windows assigns a previously unused COM port. Use the Windows <u>Control Panel</u> | <u>System</u> | <u>Device Manager</u> to determine the COM port number. (It will be named **USB Serial Port**). Make a note of which COM port this is. That information is needed in the next step.

Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

bits per second: 460,800;

data bits: **8**;

parity: none;

stop bits: 1;

flow control: none.

11. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the MicroBlaze using the following steps.

Right Click the mouse while the **MAXREFDES6 C** project is selected, choose the **Run As** menu, and then **Run Configurations...** menu as shown below.

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C Project Explo		New Go Into	•		🖲 Mał	
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🕫 😂 MAXREF	J	Open in New Window			1	
MAXREF	Ð	Сору	Ctrl+C		1	
b 📴 system_l	Ē	Paste	Ctrl+V		Right	Click Mouse on
	×	Delete	Delete			REFDESX C project
		Move				
		Rename	F2		Select	t Run As
	2	Import				
	4	Export			Run C	Configurations
		Build Project				
		Clean Project				
	ন্ত্রী	Refresh	F5			
		Close Project				
		Close Unrelated Projects				
		Build Configurations	•			
		Make Targets				
		Index				
		Show in Remote Systems view				
		Convert To		📮 Console 🛿 🔲 Properti	ies 🖉 1	
	۲	Format Project With Jindent Run As	+	1 Launch on Hardware		
	-	Debug As		2 Local C/C++ Application		
		Profile As		 3 Remote ARM Linux Appli 		
		Team		Run Configurations		
			· ·	Kun Configurations		

Next, double-click the mouse on the Xilinx C/C++ ELF menu.

😡 Run Configurations	Contract of the second second second	×
Create, manage, and run confi	gurations	
Image: Second state	 Configure launch settings from this dialog: Press the 'New' button to create a configuration of the selected type. Press the 'Duplicate' button to copy the selected configuration. Press the 'Delete' button to remove the selected configuration. Press the 'Filter' button to configure filtering options. Edit or view an existing configuration by selecting it. Configure launch perspective settings from the <u>Perspectives</u> preference page. 	
?		Run Close

Next, press the **Search Project** button.

💀 Run Configurations		Three Persons manager manager a	×
Create, manage, and run confi Ø Program not specified	gurations		
Yee Yee type filter text C C/C++ Application C C/C++ Remote Application Launch Group Remote ARM Linux Applicati Xilinx C/C++ ELF Xilinx C/C++ ELF Yee MAXREFDESX Debug	Name: MAXREFDESX Debug	© Disable auto build <u>Configure Workspace Settings</u>	wmmon) wse
< Ⅲ ► Filter matched 6 of 6 items		Apply	e <u>v</u> ert
?		Run	Close

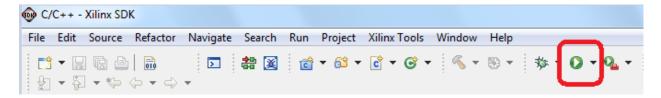
Double-click on the MAXREFDES6.elf bina	ry.
---	-----

Program Selection
Choose a <u>p</u> rogram to run:
Binaries:
MAXREFDESX.elf
Qualifier:
 microblazele - /MAXREFDESX/Debug/MAXREFDESX.elf microblazele - /MAXREFDESX/Release/MAXREFDESX.el
OK Cancel

Run Configurations	A R R R DO DO DO DO DO DO	
Create, manage, and run confi	gurations	
Yume Yume type filter text C C/C++ Application C C/C++ Remote Application Launch Group Remote ARM Linux Applicati Xilinx C/C++ ELF Xilinx C/C++ ELF Xilinx C/C++ ELF Xilinx C/C++ BLF	C/C++ Application: Debug/MAXREFDESX.elf Project: MAXREFDESX Build (if required) before launching	nection Profile Options Debugger Options Common Search Project Browse Browse
	Build configuration: Debug Enable auto build Ø Use workspace settings Zonnect process input & output to a terminal.	© Disable auto build <u>Configure Workspace Settings</u>
✓ III ▶ Filter matched 6 of 6 items		Apply Re <u>v</u> ert
?		<u>R</u> un Close

Verify the application is selected and press the **Run** button.

Once the Debug/MAXREFDES6 configuration is setup once, you just need to press the **Run** button if you ever want to run the program again.



At this point, the application will be running on the MicroBlaze and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select continuous sampling, press 0.

🍓 test - HyperTerminal	. O <mark>X</mark>
<u>File Edit View Call Transfer Help</u>	
//////////////////////////////////////	E
Connected 0:01:33 Auto detect 460800 8-N-1 SCROLL CAPS NUM Capture Print echo	

5. Code Documentation

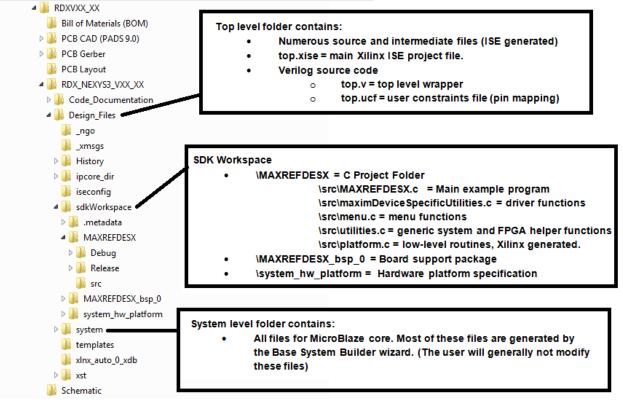
Code documentation can be found at: C:\...\RD6V01_00\RD6_NEXYS3_V01_00\Code_Documentation\

RD	RDXVXX_XX ► RDX_NEXYS3_VXX_XX ► Code_Documentation ►					
Burn	New folder					
•	Name	Date modified	Туре	Size		
	퉬 html	12/21/2012 1:03 PM	File folder			
	퉬 latex	12/21/2012 1:03 PM	File folder			
1	🖉 MainPage.html	12/6/2012 3:42 PM	HTML Document	1 KB		
	AAXREFDESX_Code_Documentation.pdf	12/13/2012 2:56 PM	Adobe Acrobat D	157 KB		

To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in pdf format with a PDF reader, open the **MAXREFDES6_Code_Documentation.pdf** file.





7. Trademarks

Eclipse is a trademark of Eclipse Foundation, Inc.

ISE is a registered trademark of Xilinx, Inc.

MicroBlaze is a trademark of Xilinx, Inc.

Nexys is a trademark of Digilent Inc.

Pmod is a trademark of Digilent Inc.

Spartan is a registered trademark of Xilinx, Inc.

Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.

Xilinx is a registered trademark and registered service mark of Xilinx, Inc.

8. Revision History

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	9/13	Initial release	—