WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFFERENTIAL AMPLIFIER

FEATURES

- **Fully Differential Architecture**
- **Common-Mode Input Range Includes the Negative Rail**
- **Minimum Gain of 2 V/V (6 dB)**
- **Bandwidth: 2 GHz**
- **Slew Rate: 6400 V/μs**
- **1% Settling Time: 2 ns**
- **HD_2: –72 dBc at 100 MHz**
- **HD_3: –79 dBc at 100 MHz**
- **OIP_2: 78 dBm at 70 MHz**
- **OIP_3: 42 dBm at 70 MHz**
- **Input Voltage Noise: 2.3 nV/$\sqrt{Hz}$ (f > 10 MHz)**
- **Noise Figure: 19.2 dB (G = 10 dB)**
- **Output Common-Mode Control**
- **5-V Power Supply Current: 39.2 mA**
- **Power-Down Capability: 0.65 mA**

APPLICATIONS

- **5-V Data-Acquisition Systems**
- **High Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

DESCRIPTION

The THS4508 is a wideband, fully-differential operational amplifier designed for single-supply 5-V data acquisition systems. It has very low noise at 2.3 nV/$\sqrt{Hz}$, and extremely low harmonic distortion of –72 dBc HD_2 and –79 dBc HD_3 at 100 MHz with 2 V_{PP}, G = 10 dB, and 1-kΩ load. Slew rate is very high at 6400 Vμs, and with settling time of 2 ns to 1% (2 V step), it is ideal for pulsed applications. It is designed for minimum gain of 6 dB, but is optimized for gain of 10 dB.

To allow for dc coupling to analog-to-digital converters (ADCs), its unique output common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The THS4508 is a high-performance amplifier that has been optimized for use in high performance, 5-V single-supply data acquisition systems. The output has been optimized for best performance with its common-mode voltages set to mid-supply, and the input has been optimized for best performance with its common-mode voltage set to 0.7 V. High performance at a low power-supply voltage is ideal for high-performance, single-supply 5-V data-acquisition systems with a minimum parts count. The combined performance of the THS4508 in a gain of 10-dB driving the ADS5500 ADC, sampling at 125 MSPS, is 82-dBc SFDR, and 68.3-dBc SNR with a –1-dBFS signal at 70 MHz.

The THS4508 is offered in a quad 16-pin leadless QFN package (RGT), and is characterized for operation over the full industrial temperature range from –40°C to +85°C.

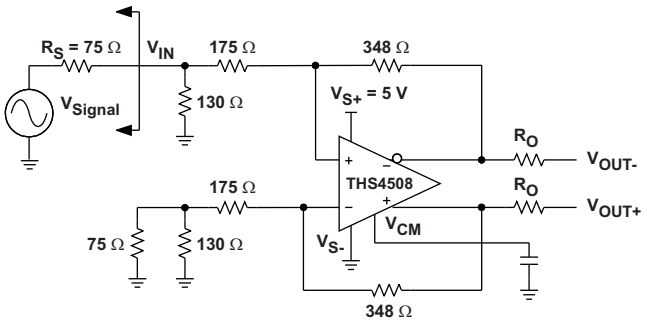


Figure 1. Video Buffer

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			UNIT
V_{SS}	Supply voltage	V_{S-} to V_{S+}	5.5 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		4 V
I_O	Output current		200 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature(2)		+150°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		+125°C
T_A	Operating free-air temperature range		–40°C to +85°C
T_{stg}	Storage temperature range		–65°C to +150°C
	ESD ratings	HBM	2000 V
		CDM	1500 V
		MM	100 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(3) The maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device. The THS4508 incorporates a (QFN) exposed thermal pad on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the QFN thermally enhanced package.

DISSIPATION RATINGS TABLE (PER PACKAGE)

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \le 25°C$	$T_A = 85°C$
RGT (16)	2.4°C/W	39.5°C/W	2.3 W	225 mW

ORDERING INFORMATION(1)

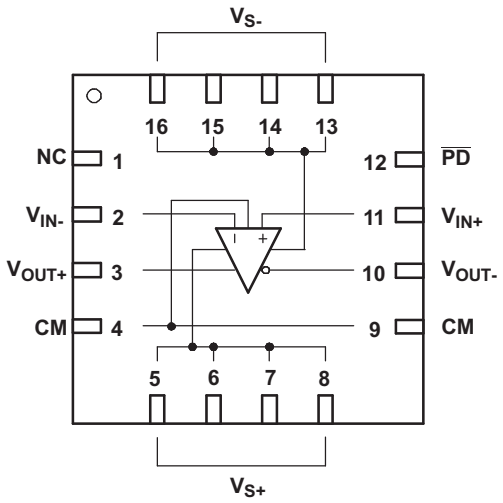
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS4508	QFN-16	RGT	–40°C to +85°C	THS4508	THS4508RGTT	Tape and Reel, 250
					THS4508RGTR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

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DEVICE INFORMATION

THS4508
(RGT PACKAGE)
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL (RGT PACKAGE)		DESCRIPTION
NO.	NAME	
1	NC	No internal connection
2	V_{IN-}	Inverting amplifier input
3	V_{OUT+}	Noninverting amplifier output
4, 9	CM	Common-mode voltage input
5–8	V_{S+}	Positive amplifier power-supply input
10	V_{OUT-}	Inverting amplifier output
11	V_{IN+}	Noninverting amplifier input
12	$\overline{PD}$	Power-down, $\overline{PD}$ = logic low puts part into low-power mode, $\overline{PD}$ = logic high or open for normal operation
13–16	V_{S-}	Negative amplifier power-supply input

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ELECTRICAL CHARACTERISTICS; $V_{S+} - V_{S-} = 5$ V:

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 10 dB, CM = open, $V_O = 2\ V_{PP}$, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ Differential, T = +25°C Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-supply.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS	TEST LEVEL (1)
AC PERFORMANCE (see Figure 44)							
Small-Signal Bandwidth	G = 6 dB, $V_O = 100\ mV_{PP}$			2		GHz	C
	G = 10 dB, $V_O = 100\ mV_{PP}$			1.7		GHz	
	G = 14 dB, $V_O = 100\ mV_{PP}$			600		MHz	
	G = 20 dB, $V_O = 100\ mV_{PP}$			300		MHz	
Gain-Bandwidth Product	G = 20 dB			3		GHz	
Bandwidth for 0.1 dB flatness	G = 10 dB, $V_O = 2\ V_{PP}$			400		MHz	
Large-Signal Bandwidth	G = 10 dB, $V_O = 2\ V_{PP}$			1.5		GHz	
Slew Rate (Differential)	V_O = 2-V Step			6400		V/µs	
Rise Time				0.5		ns	
Fall Time				0.5		ns	
Settling Time to 1%				2		ns	
Settling Time to 0.1%				12		µs	
2nd-Order Harmonic Distortion	f = 10 MHz			–104		dBc	
	f = 50 MHz			–82			
	f = 100 MHz			–69			
3rd-Order Harmonic Distortion	f = 10 MHz			–105			
	f = 50 MHz			–92			
	f = 100 MHz			–81			
2nd-Order Intermodulation Distortion	200-kHz tone spacing, $R_L = 499\ \Omega$	f_C = 70 MHz		–78		dBc	
		f_C = 140 MHz		–64			
3rd-Order Intermodulation Distortion		f_C = 70 MHz		–95			
		f_C = 140 MHz		–78			
2nd-Order Output Intercept Point	200-kHz tone spacing, $R_L = 100\ \Omega$	f_C = 70 MHz		78		dBm	
		f_C = 140 MHz		58			
3rd-Order Output Intercept Point		f_C = 70 MHz		42			
		f_C = 140 MHz		35			
1-dB Compression Point (2)	f_C = 70 MHz			12.2		dBm	
	f_C = 140 MHz			10.8			
Noise Figure	50-Ω system, 10 MHz			19.2		dB	
Input Voltage Noise	f > 10 MHz			2.3		nV/√Hz	
Input Current Noise	f > 10 MHz			2.9		pA/√Hz	
DC PERFORMANCE							
Open-Loop Voltage Gain (A_{OL})				68		dB	C
Input Offset Voltage	T_A = +25°C			1	4	mV	A
	T_A = –40°C to +85°C			1	5		
Average Offset Voltage Drift				2.3		µV/°C	B
Input Bias Current	T_A = +25°C		1.75	8	15.5	µA	A
	T_A = –40°C to +85°C			8	18.5		
Average Bias Current Drift				20		nA/°C	B
Input Offset Current	T_A = +25°C			0.5	3.6	µA	A
	T_A = –40°C to +85°C			0.5	7		
Average Offset Current Drift				7		nA/°C	B

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(2) The 1-dB compression point is measured at the load with 50-Ω double termination. Add 3 dB to refer to amplifier output.

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ELECTRICAL CHARACTERISTICS; $V_{S+} - V_{S-} = 5$ V: (continued)

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 10 dB, CM = open, $V_O = 2\ V_{PP}$, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ Differential, T = +25°C Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-supply.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS	TEST LEVEL (1)
INPUT							
Common-Mode Input Range High				2.3		V	B
Common-Mode Input Range Low				–0.3			
Common-Mode Rejection Ratio				90		dB	B
Differential Input Impedance				18.2 || 2.2		MΩ || pF	C
Common-Mode Input Impedance				3.8 || 2.5		MΩ || pF	C
OUTPUT							
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	T_A = +25°C	3.7	3.8		V	A
		T_A = –40°C to +85°C	3.6	3.8			
Minimum Output Voltage Low		T_A = +25°C		1.2	1.3		
		T_A = –40°C to +85°C		1.2	1.4		
Differential Output Voltage Swing	T_A = +25°C		4.8	5.2		V	A
	T_A = –40°C to +85°C		4.4	5.2			
Differential Output Current Drive	$R_L = 10\ \Omega$			96		mA	C
Output Balance Error	V_O = 100 mV, f = 1 MHz			–43		dB	C
Closed-Loop Output Impedance	f = 1 MHz			0.3		Ω	C
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-Signal Bandwidth				700		MHz	C
Slew Rate				110		V/µs	
Gain				1		V/V	
Output Common-Mode Offset from CM input	1.25 V < CM < 3.5 V			5		mV	
CM Input Bias Current	1.25 V < CM < 3.5 V			±40		µA	
CM Input Voltage Range				1.25 to 3.75		V	
CM Input Impedance				32 || 1.5		kΩ || pF	
CM Default Voltage				2.5		V	
POWER SUPPLY							
Specified Operating Voltage			3.75 (3)	5	5.25	V	C
Maximum Quiescent Current	T_A = +25°C			39.2	42.5	mA	A
	T_A = –40°C to +85°C			39.2	43.5		
Minimum Quiescent Current	T_A = +25°C		35.9	39.2			
	T_A = –40°C to +85°C		35	39.2			
Power-Supply Rejection (±PSRR)	To differential output			90		dB	C
POWER-DOWN	Referenced to V_{S-}						
Enable Voltage Threshold	Device assured *on* above 2.1 V			> 2.1		V	C
Disable Voltage Threshold	Device assured *off* below 0.7 V			< 0.7			
Power-Down Quiescent Current	T_A = +25°C			0.65	0.9	mA	A
	T_A = –40°C to +85°C			0.65	1		
Input Bias Current	$\overline{PD} = V_{S-}$			100		µA	C
Input Impedance				50 || 2		kΩ || pF	
Turn-on Time Delay	Measured to output on			55		ns	
Turn-off Time Delay	Measured to output off			10		µs	

(3) See the *Application Information* section of this data sheet for device operation with full supply voltages less than 5 V.

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TYPICAL CHARACTERISTICS

TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 10 dB, CM = open, $V_O = 2\ V_{PP}$, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

Small-Signal Frequency Response			Figure 2
Large Signal Frequency Response			Figure 3
Harmonic Distortion	HD_2, G = 6 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 4
	HD_3, G = 6 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 5
	HD_2, G = 10 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 6
	HD_3, G = 10 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 7
	HD_2, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 8
	HD_3, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 9
	HD_2, G = 10 dB	vs Output voltage	Figure 10
	HD_3, G = 10 dB	vs Output voltage	Figure 11
	HD_2, G = 10 dB	vs CM input voltage	Figure 12
	HD_3, G = 10 dB	vs CM input voltage	Figure 13
Intermodulation Distortion	IMD_2, G = 6 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 14
	IMD_3, G = 6 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 15
	IMD_2, G = 10 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 16
	IMD_3, G = 10 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 17
	IMD_2, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 18
	IMD_3, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 19
Output Intercept Point	OIP_2	vs Frequency	Figure 20
	OIP_3	vs Frequency	Figure 21
S-Parameters		vs Frequency	Figure 22
Transition Rate		vs Output Voltage	Figure 23
Transient Response			Figure 24
Settling Time			Figure 25
0.1 dB Flatness			Figure 26
Rejection Ratio		vs Frequency	Figure 27
Output Impedance		vs Frequency	Figure 28
Overdrive Recovery			Figure 29
Output Voltage Swing		vs Load Resistance	Figure 30
Turn-Off Time			Figure 31
Turn-On Time			Figure 32
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 33
Open Loop Gain		vs Frequency	Figure 34
Input Referred Noise		vs Frequency	Figure 35
Noise Figure		vs Frequency	Figure 36
Quiescent Current		vs Supply Voltage	Figure 37
Output Balance Error		vs Frequency	Figure 38
CM Input Impedance		vs Frequency	Figure 39
CM Small-Signal Frequency Response			Figure 40
CM Input Bias Current		vs CM Input Voltage	Figure 41
Differential Output Offset Voltage		vs CM Input Voltage	Figure 42
Output Common-Mode Offset		vs CM Input Voltage	Figure 43

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TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 10 dB, CM = open, $V_O = 2\ V_{PP}$, $R_F = 349\ \Omega$, $R_L = 200\ \Omega$ Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

SMALL-SIGNAL FREQUENCY RESPONSE

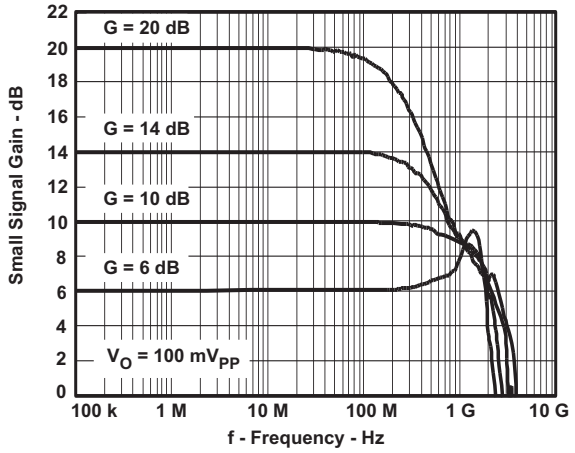


Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

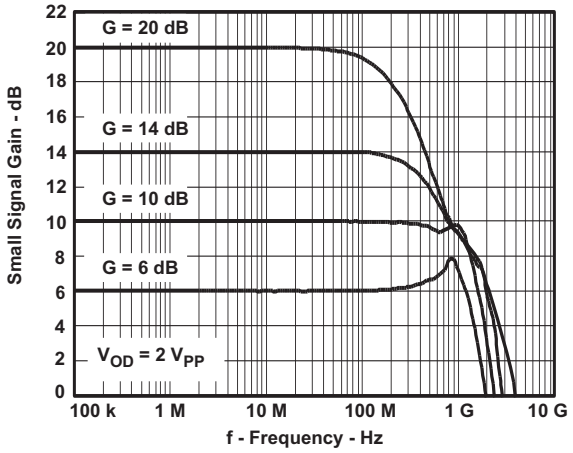


Figure 3.

HD_2 vs FREQUENCY

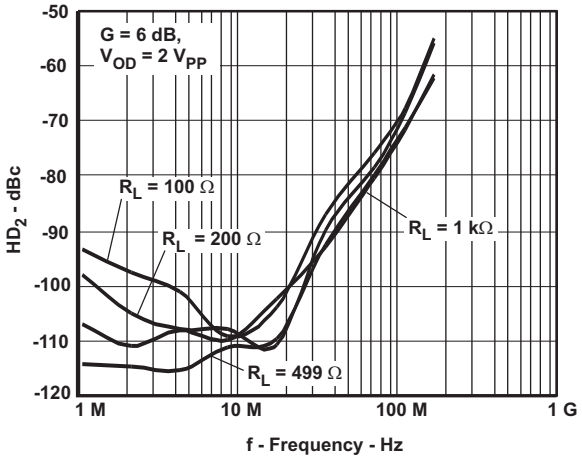


Figure 4.

HD_3 vs FREQUENCY

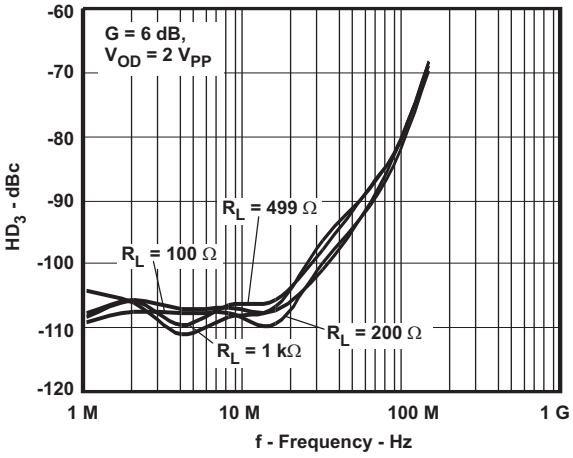


Figure 5.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

HD_2 vs FREQUENCY

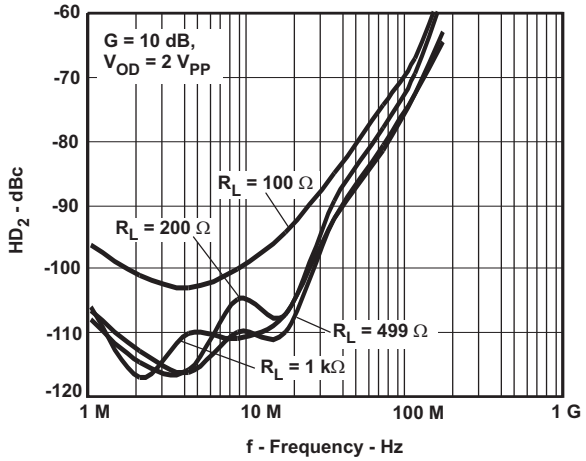


Figure 6.

HD_3 vs FREQUENCY

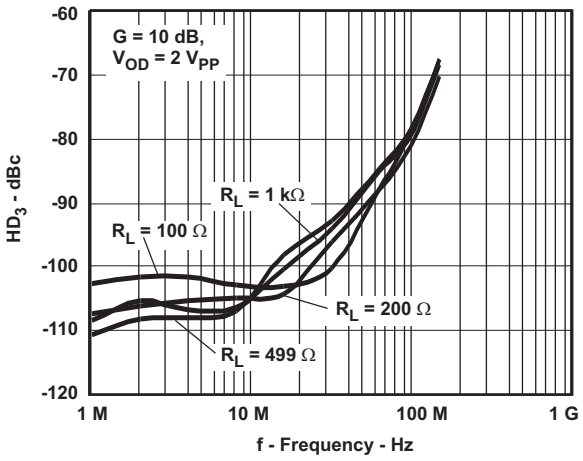


Figure 7.

HD_2 vs FREQUENCY

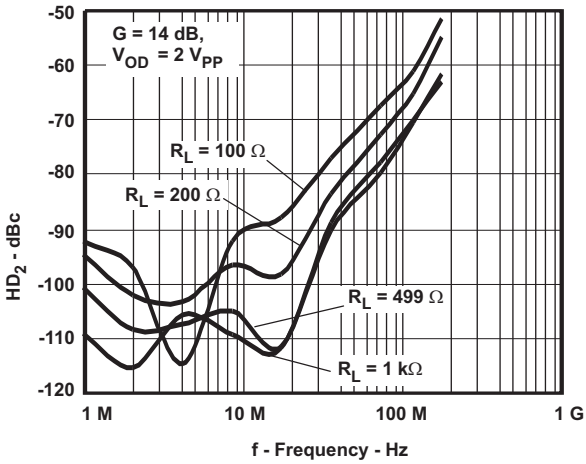


Figure 8.

HD_3 vs FREQUENCY

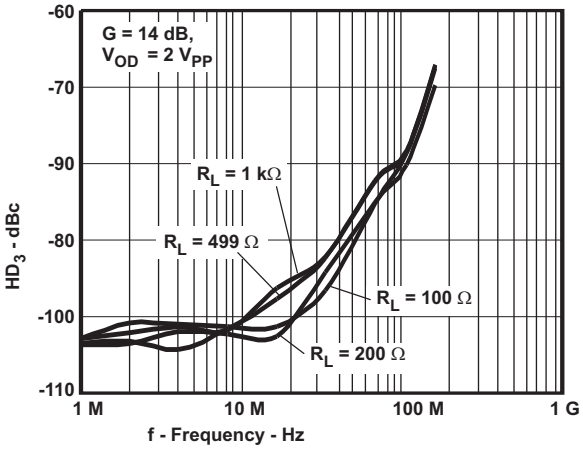


Figure 9.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

HD_2 vs OUTPUT VOLTAGE

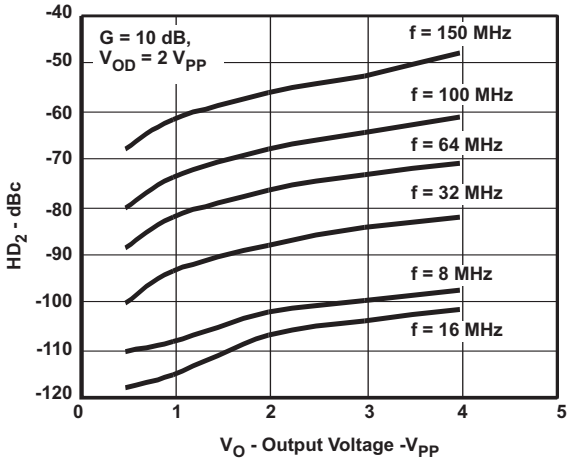


Figure 10.

HD_3 vs OUTPUT VOLTAGE

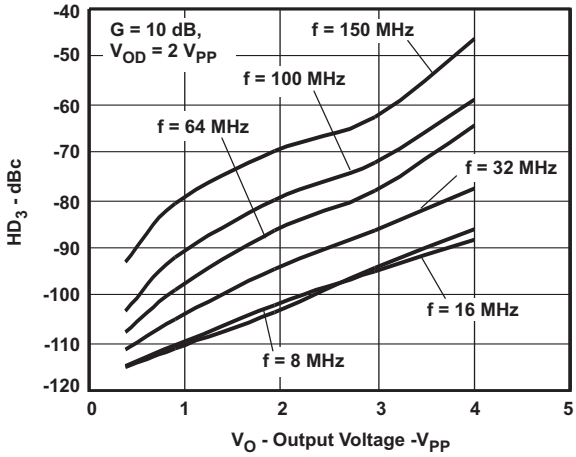


Figure 11.

HD_2 vs CM OUTPUT VOLTAGE

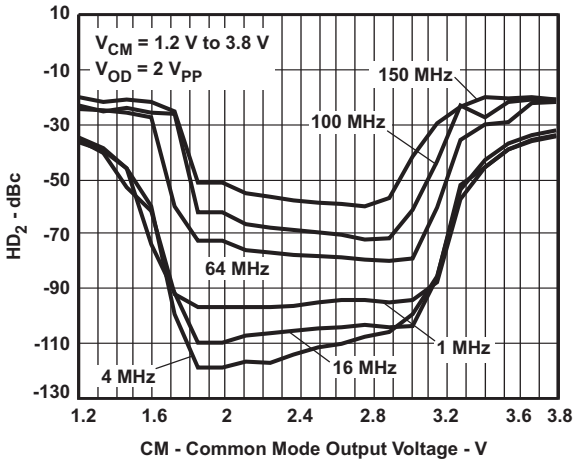


Figure 12.

HD_3 vs CM OUTPUT VOLTAGE

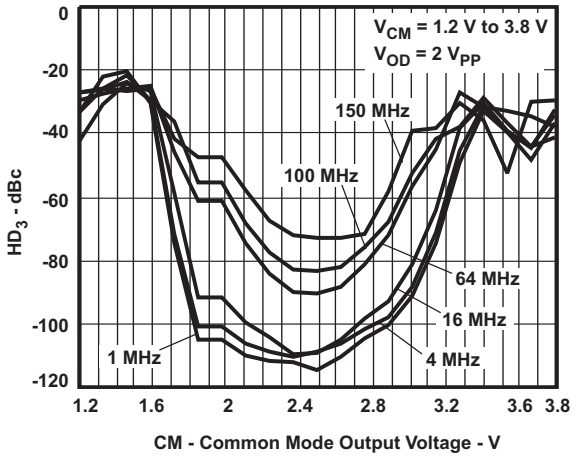


Figure 13.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

IMD$_2$ vs FREQUENCY

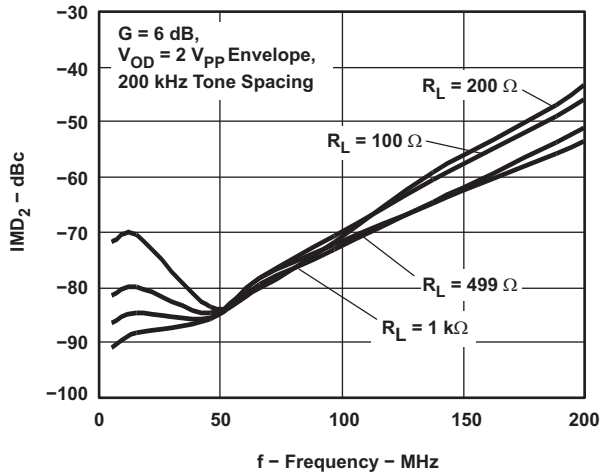


Figure 14.

IMD$_3$ vs FREQUENCY

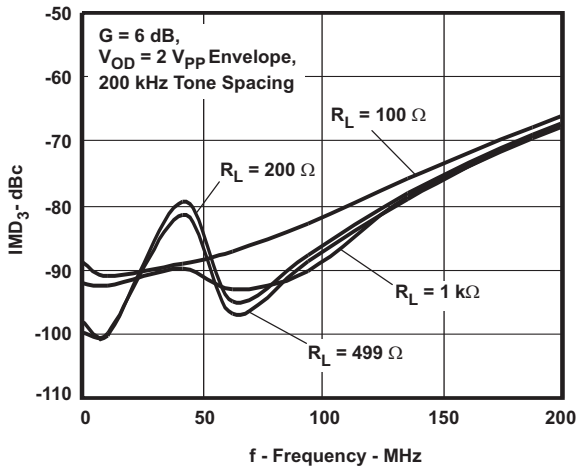


Figure 15.

IMD$_2$ vs FREQUENCY

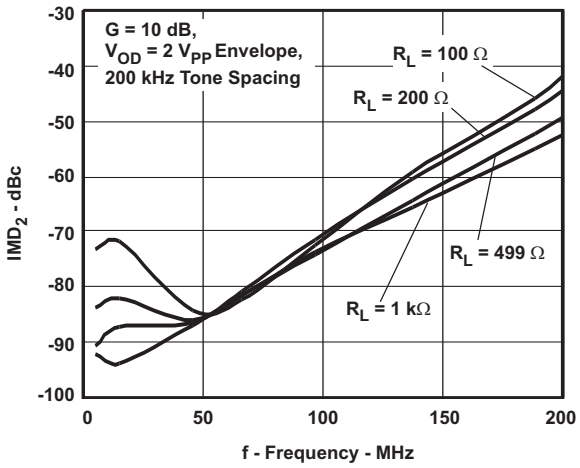


Figure 16.

IMD$_3$ vs FREQUENCY

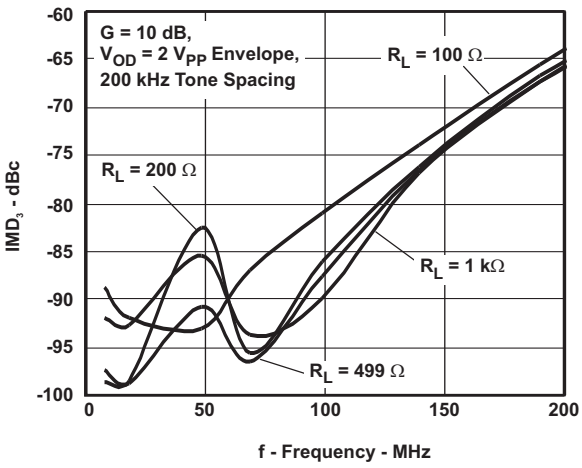


Figure 17.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

IMD_2 vs FREQUENCY

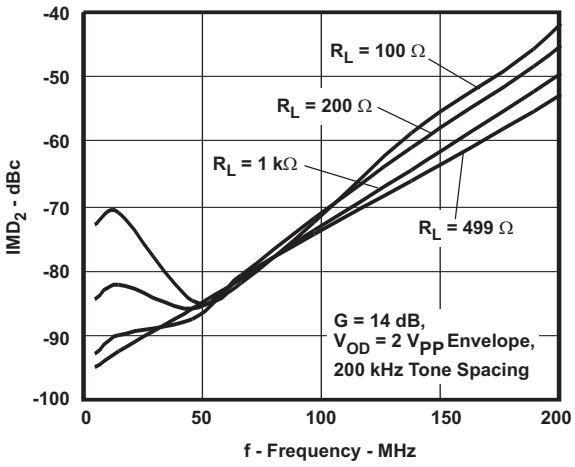


Figure 18.

IMD_3 vs FREQUENCY

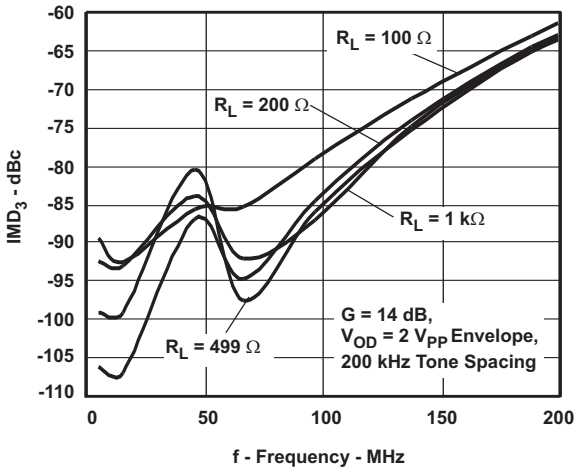


Figure 19.

OIP_2 vs FREQUENCY

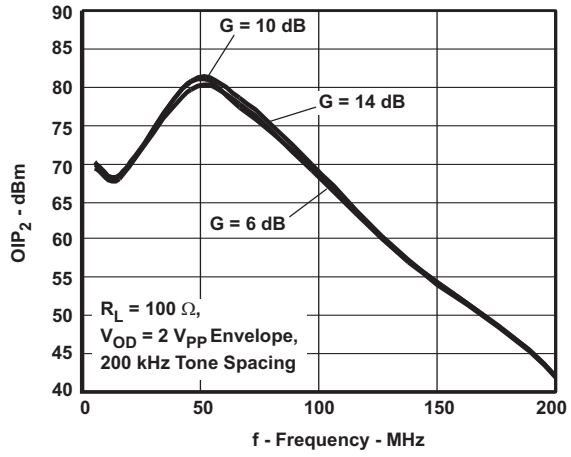


Figure 20.

OIP_3 vs FREQUENCY

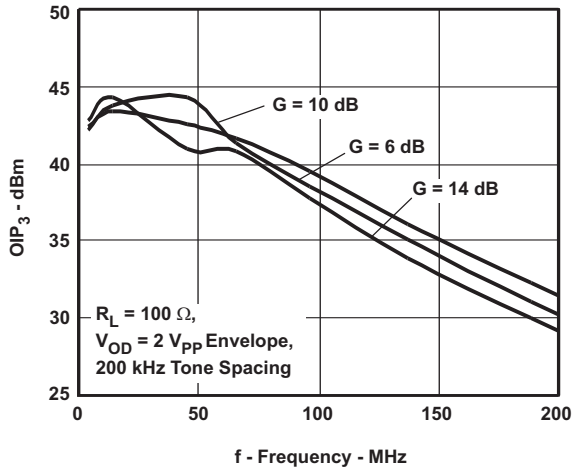


Figure 21.

Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

S-PARAMETERS vs FREQUENCY

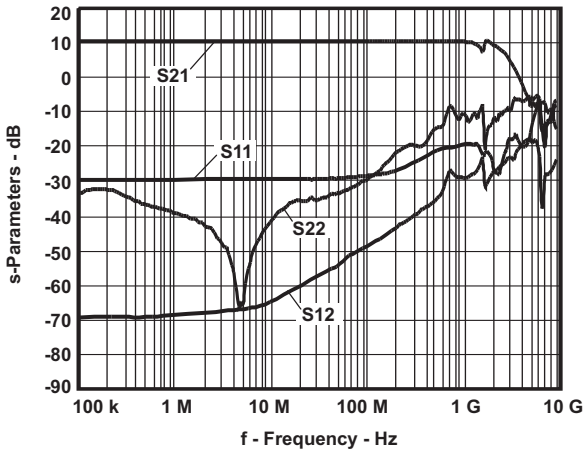


Figure 22.

TRANSITION RATE vs OUTPUT VOLTAGE

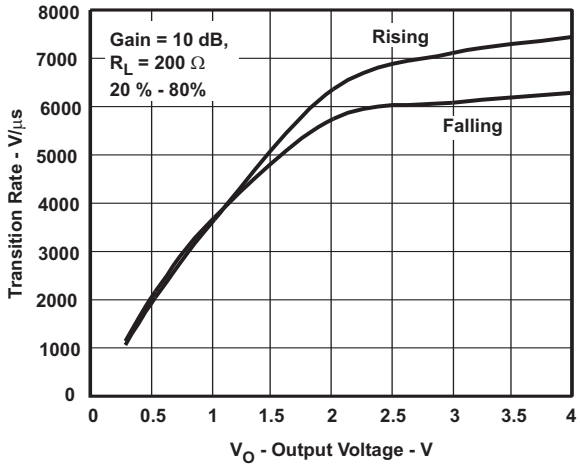


Figure 23.

TRANSIENT RESPONSE

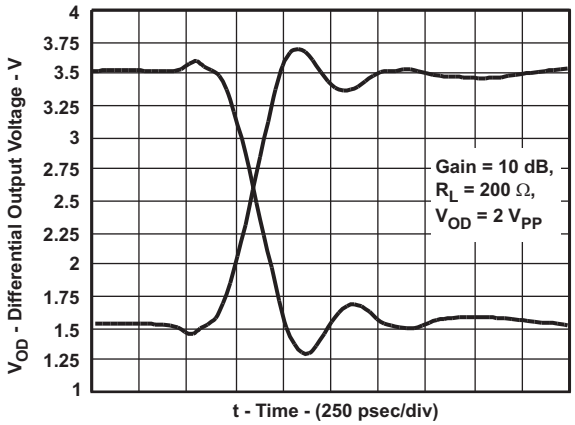


Figure 24.

SETTLING TIME

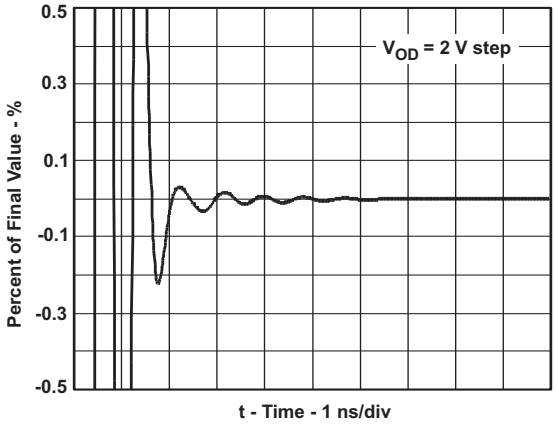


Figure 25.

0.1-dB FLATNESS

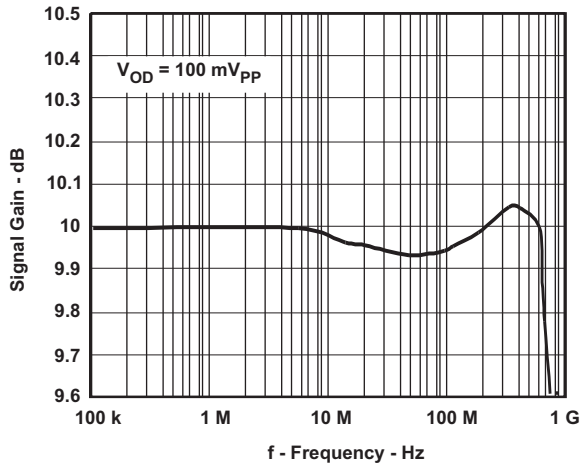


Figure 26.

REJECTION RATIO vs FREQUENCY

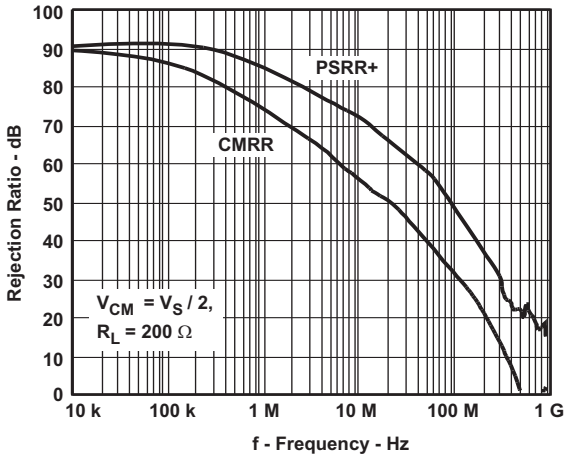


Figure 27.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

OUTPUT IMPEDANCE vs FREQUENCY

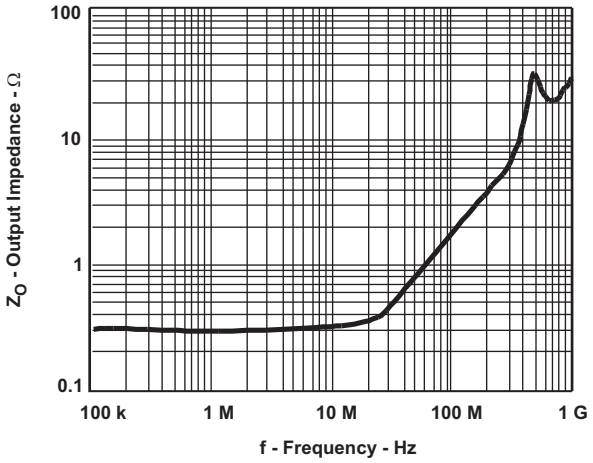


Figure 28.

OVERDRIVE RECOVERY

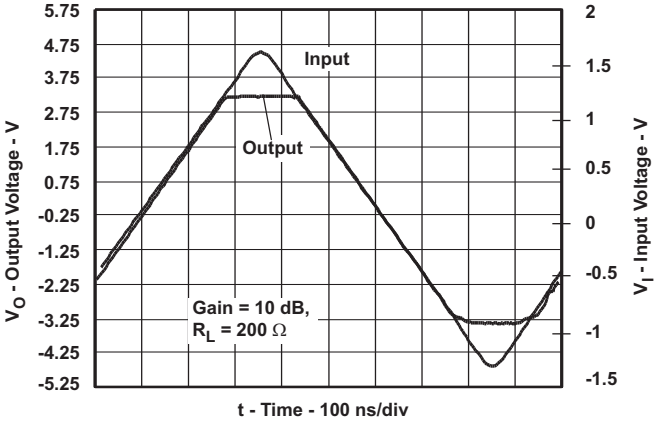


Figure 29.

V_{OD} SWING vs LOAD RESISTANCE

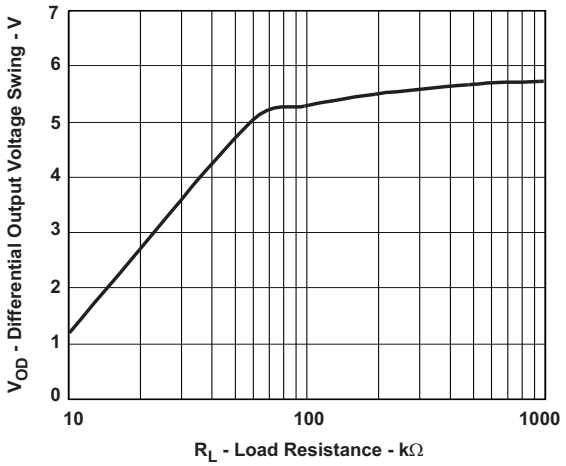


Figure 30.

TURN-OFF TIME

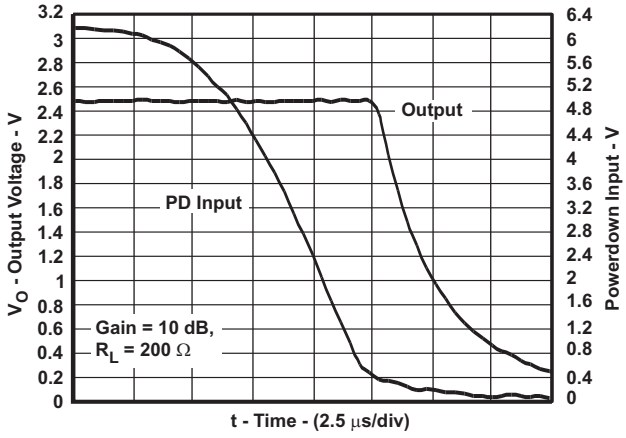


Figure 31.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

TURN-ON TIME

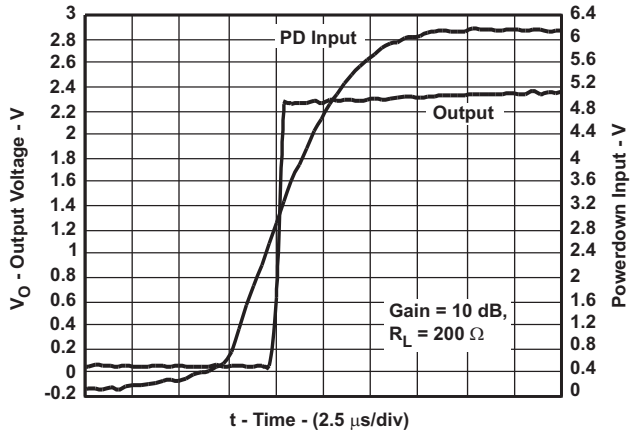


Figure 32.

INPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

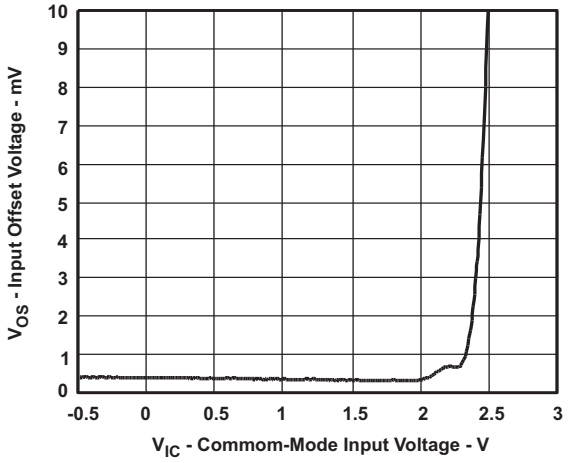


Figure 33.

OPEN LOOP GAIN AND PHASE vs FREQUENCY

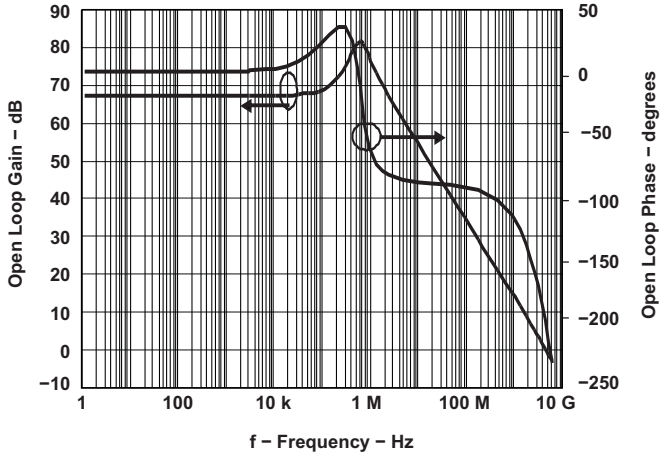


Figure 34.

INPUT-REFERRED NOISE vs FREQUENCY

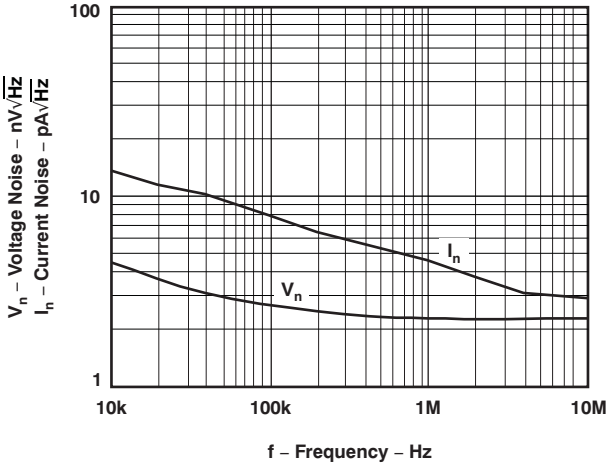


Figure 35.

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Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

NOISE FIGURE vs FREQUENCY

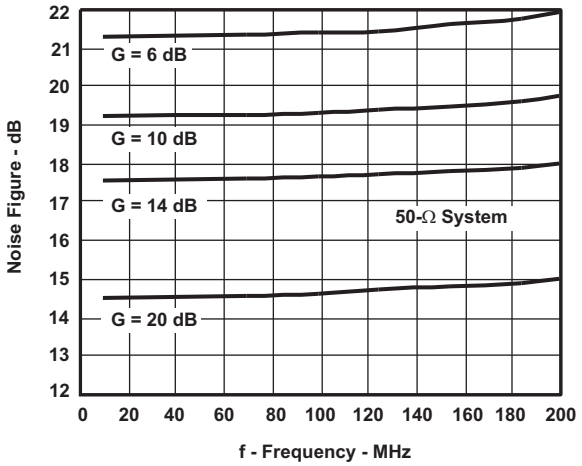


Figure 36.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

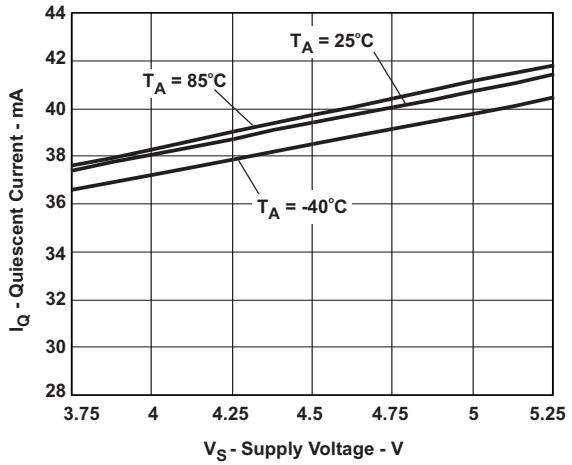


Figure 37.

OUTPUT BALANCE ERROR vs FREQUENCY

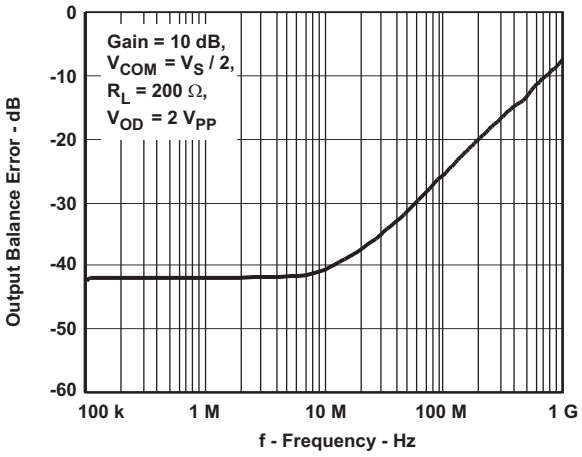


Figure 38.

CM INPUT IMPEDANCE vs FREQUENCY

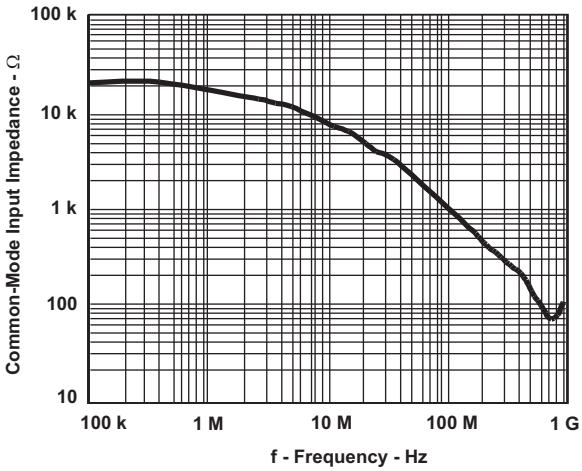


Figure 39.

Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, G = 10 dB, CM = open, V_O = 2 V_{PP}, R_F = 349 Ω, R_L = 200 Ω Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Midrail

CM SMALL-SIGNAL FREQUENCY RESPONSE

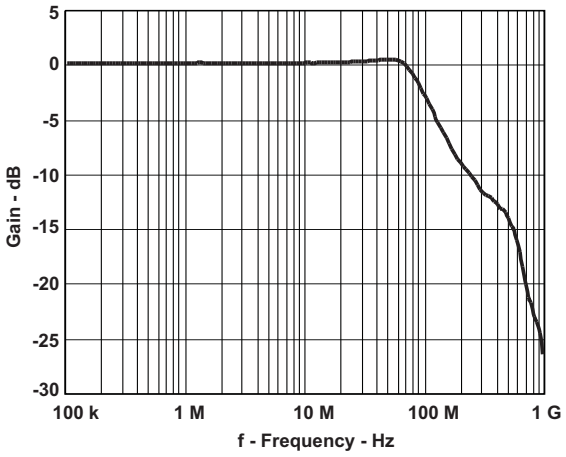


Figure 40.

CM BIAS CURRENT vs CM INPUT VOLTAGE

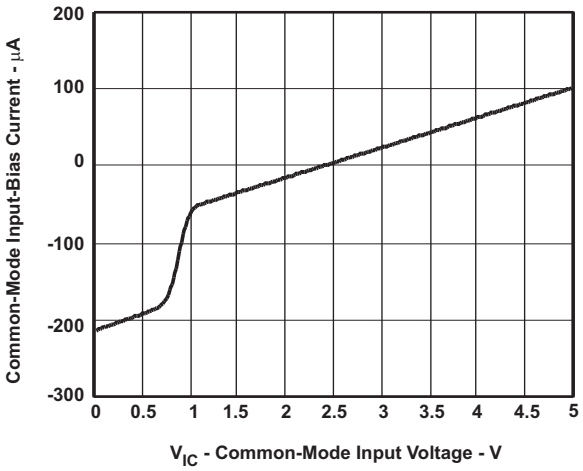


Figure 41.

V_{OD} OFFSET VOLTAGE vs CM INPUT VOLTAGE

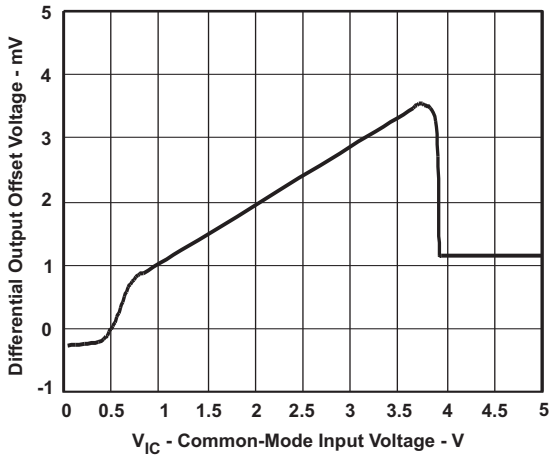


Figure 42.

V_{OC} OFFSET VOLTAGE vs CM INPUT VOLTAGE

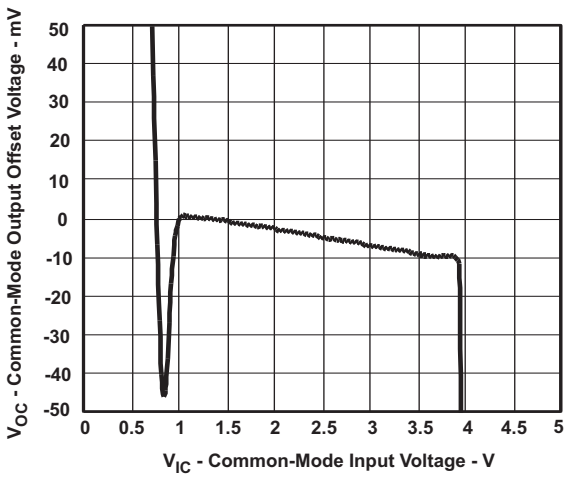


Figure 43.

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TEST CIRCUITS

The THS4508 is tested with the following test circuits built on the EVM. For simplicity, the power supply decoupling is not shown—see the layout in the *Application Information* section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac-coupled 50-Ω sources, and a 0.22-µF capacitor and a 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

Note the gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten.
100 Ω	25 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note the total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 45, the signal will see slightly more loss, and these numbers will be approximate.

Frequency Response

The circuit shown in Figure 44 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100-Ω resistor. The gain is referred to the amplifier output by adding back the 6-dB loss due to the voltage divider on the output.

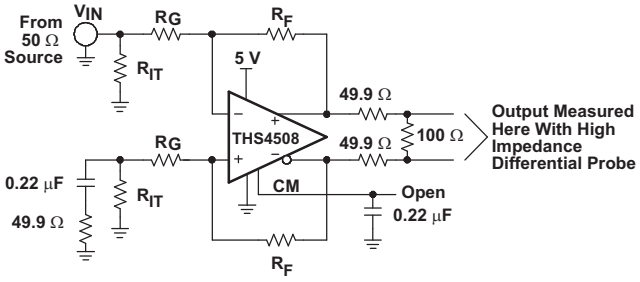


Figure 44. Frequency Response Test Circuit

Distortion and 1 db Compression

The circuit shown in Figure 45 is used to measure harmonic distortion, intermodulation distortion, and 1-db compression point of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

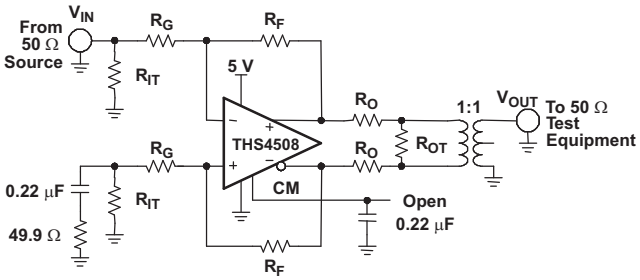


Figure 45. Distortion Test Circuit

The 1-dB compression point is measured with a spectrum analyzer with 50-Ω double termination or 100-Ω termination as shown in Table 2. The input power is increased until the output is 1 dB lower than expected. The number reported in the table data is the power delivered to the spectrum analyzer input. Add 3 dB to refer to the amplifier output.

S-Parameter, Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in Figure 46 is used to measure s-parameters, slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier output.

Because S_{21} is measured single-ended at the load with 50-Ω double termination, add 12 dB to refer to the amplifier output as a differential signal.

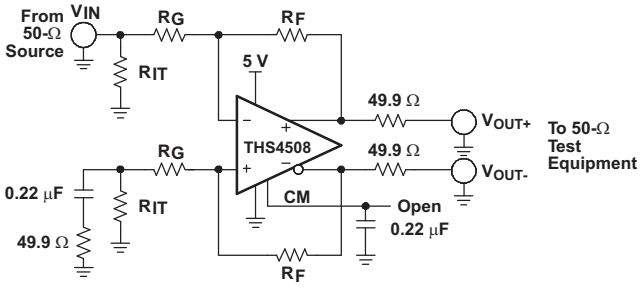


Figure 46. S-Parameter, SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Off Test Circuit

CM Input

The circuit shown in Figure 47 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or V_{OUT-} with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

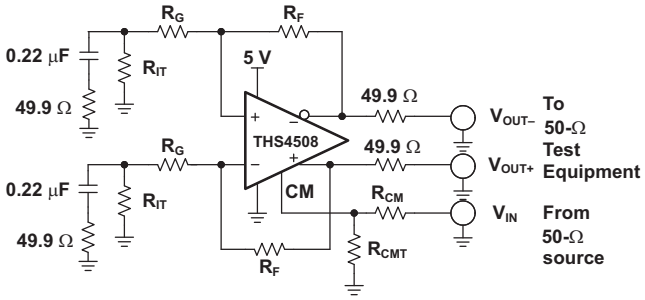


Figure 47. CM Input Test Circuit

CMRR and PSRR

The circuit shown in Figure 48 is used to measure the CMRR and PSRR of V_{S+} and V_{S-}. The input is switched appropriately to match the test being performed.

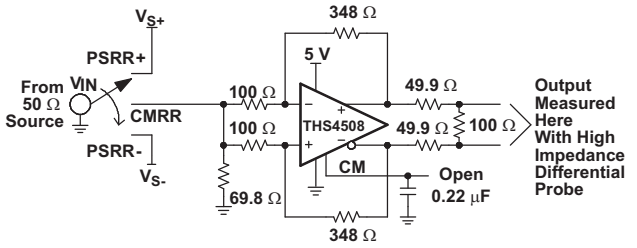


Figure 48. CMRR and PSRR Test Circuit

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APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4508. For simplicity, power-supply decoupling capacitors are not shown in these diagrams. For more detail on the use and operation of fully differential operational amplifiers, refer to application report *Fully-Differential Amplifiers* (SLOA054) , available for download at the TI web site.

Differential Input to Differential Output Amplifier

The THS4508 is a fully differential operational amplifier, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 49 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

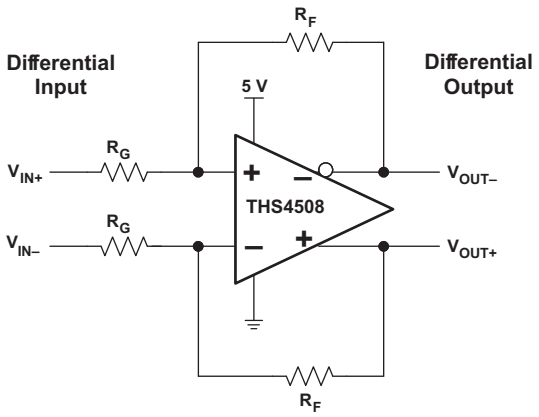


Figure 49. Differential Input to Differential Output Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output Amplifier

The THS4508 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 50 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

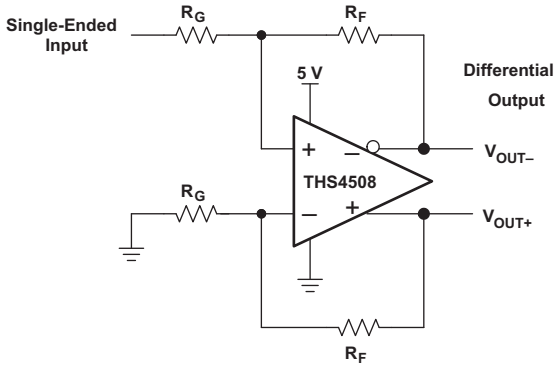


Figure 50. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-model voltage of a fully differential operational amplifier is the voltage at the (+) and (–) input pins of the operational amplifier.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the operational amplifier. Assuming the operational amplifier is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin determines the input common-mode voltage of the operational amplifier.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the operational amplifier, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the operational amplifier increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 51 is representative of the CM input. The internal CM circuit has about 700 MHz of –3-dB bandwidth, which

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is required for best performance, but it is intended to be a dc-bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where V_{CM} is the voltage applied to the CM pin, and V_{S+} ranges from 3.75 V to 5 V, and V_{S-} is 0 V (ground).

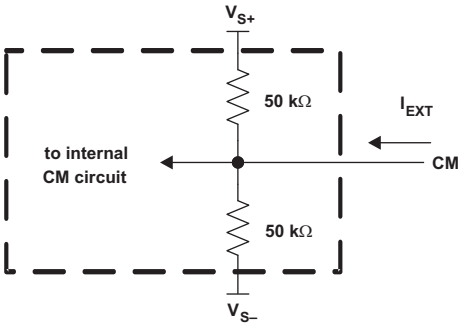


Figure 51. CM Input Circuit

Device Operation with Single Power Supplies Less than 5 V

The THS4508 is optimized to work in systems using a 5-V single supply, and the characterization data presented in this data sheet were taken with 5-V single-supply inputs. For ac-coupled systems or dc-coupled systems operating with supplies less than 5 V and greater than 3.75 V, the amplifier input common-mode range is maximized by adding pull-down resistors at the device inputs. The pull-down resistors provide additional loading at the input, and lower the common-mode voltage that is fed back into the device input through resistor R_F. Figure 52 shows the circuit configuration for this mode of operation where R_{PD} is added to the dc-coupled circuit to avoid violating the V_{ICR} of the operational amplifier. Note R_S and R_{IT} are added to the alternate input from the signal input to balance the amplifier. One resistor that is equal to the combined value $R_I = R_G + R_S \parallel R_{IT}$ can be placed at the alternate input.

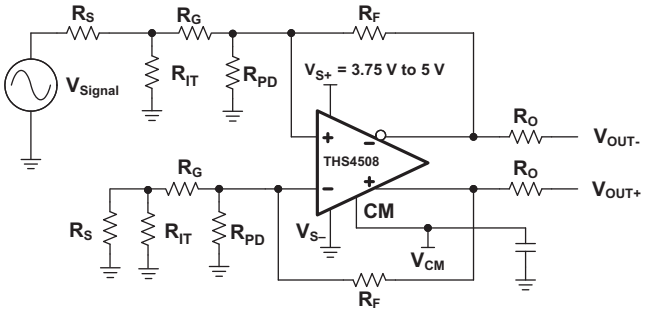


Figure 52. THS4508 DC-Coupled Single-Source Supply Range From 3.75 V to 5 V With R_{PD} Used To Set V_{IC}

Note that in Figure 52, the source is referenced to ground as is the input termination resistor R_{IT}. The proper value of resistance to add can be calculated from Equation 3:

$$R_{PD} = \frac{1}{\frac{1}{R_F}\left[\frac{1.6}{\frac{V_{S+}}{2} - 1.6}\right] - \frac{1}{R_I}} \quad (3)$$

where $R_I = R_G + R_S \parallel R_{IT}$.

V_{S+} is the power-supply voltage, R_F is the feedback resistance, R_G is the gain-setting resistance, R_S is the signal source resistance, and R_{IT} is the termination resistance.

Table 3 is a modification of Table 1 to add the proper values with R_{PD} assuming V_{S+} = 3.75 V, a dc-coupled 50-Ω source impedance, and setting the output common-mode voltage to mid-supply.

Table 3. R_{PD} Values for Various Gains, V_{S+} = 3.75 V, DC-Coupled Signal Source

Gain	R_F	R_G	R_{IT}	R_{PD}
6 dB	348 Ω	169 Ω	64.9 Ω	86.6 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	110 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	158 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	226 Ω

If the signal originates from an ac-coupled 50-Ω source (see Figure 53), the equivalent dc-source resistance is an open circuit and $R_I = R_G + R_{IT}$. Table 4 is a modification of Table 1 to add the proper values with R_{PD} assuming V_{S+} = 3.75 V, an ac-coupled 50-Ω source impedance, and setting the output common-mode voltage to mid-supply.

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Table 4. R_{PD} Values for Various Gains, V_{S+} = 3.75 V, AC-Coupled Signal Source

Gain	R_F	R_G	R_{IT}	R_{PD}
6 dB	348 Ω	169 Ω	64.9 Ω	80.6 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	90.9 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	90.9 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	77.6 Ω

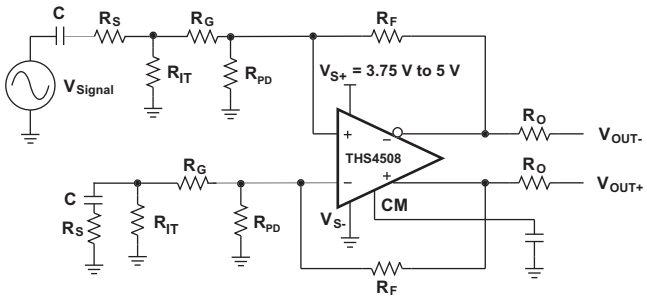


Figure 53. THS4508 AC-Coupled Single-Source Supply Range From 3.75 V to 5 V With R_{PD} Used To Set V_{IC}

Video Buffer

Figure 54 shows a possible application of the THS4508 as a dc-coupled video buffer with a gain of 2. Figure 55 shows a plot of the Y' signal originating from a HDTV 720p video system. The input signal includes a 3-level sync (minimum level at –0.3 V), and the portion of the video signal with maximum amplitude of 0.7 V. Although the buffer draws its power from a 5-V single-ended power supply, internal level shifters allow the buffer to support input signals which are as much as –0.3 V below ground. This allows maximum design flexibility while maintaining a minimum parts count. Figure 56 shows the differential output of the buffer. Note that the dc-coupled amplifier can introduce a dc offset on a signal applied at its input

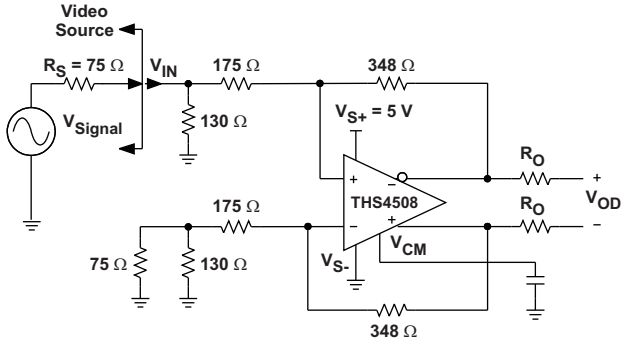


Figure 54. Single-Supply Video Buffer, Gain = 2

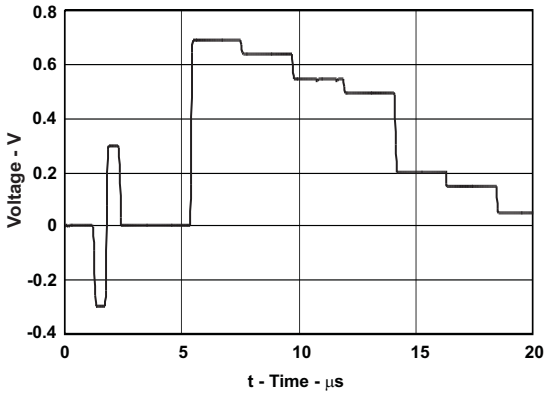


Figure 55. Y' Signal With 3-Level Sync and Video Signal

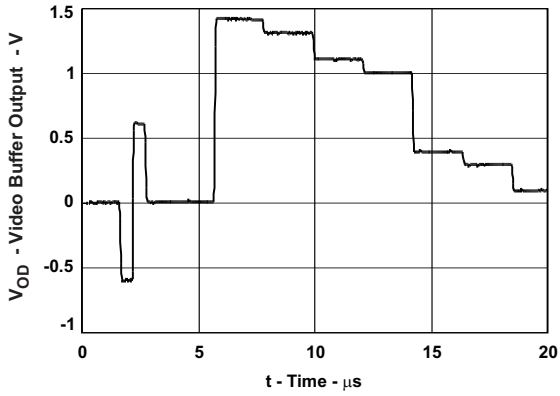


Figure 56. Video Buffer Differential Output Signal

THS4508 + ADS5500 Combined Performance

The THS4508 is designed to be a high-performance drive amplifier for high-performance data converters such as the ADS5500 14-bit 125-MSPS ADC. Figure 57 shows a circuit combining the two devices, and Figure 58 shows the combined SNR and SFDR performance versus frequency with –1 dBFS input signal level sampling at 125 MSPS. The THS4508 amplifier circuit provides 10 dB of gain, and converts the single-ended input signal to a differential output signal. The default common-mode output of the THS4508 (2.5 V) is not compatible with the required common-mode input of the ADS5500 (1.55 V), so dc-blocking capacitors are added (0.22 µF). Note that a biasing circuit (not shown in Figure 57) is needed to provide the required common-mode, dc-input for the ADS5500. The 100-Ω resistors and 2.7-pF capacitor between the THS4508 outputs and ADS5500 inputs along with the input capacitance of the ADS5500 limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50-Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal

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source. Input termination is accomplished via the 69.8-Ω resistor and 0.22-µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor is inserted to ground across the 69.8-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See Table 1 for component values to set proper 50-Ω termination for other common gains.

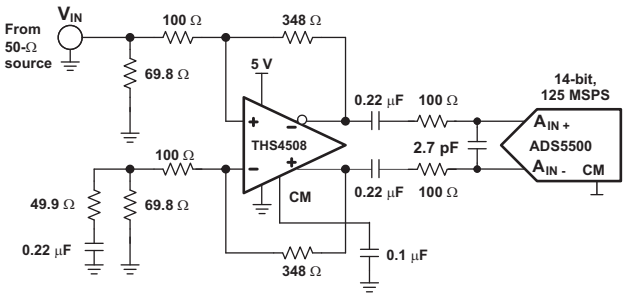


Figure 57. THS4508 + ADS5500 Circuit

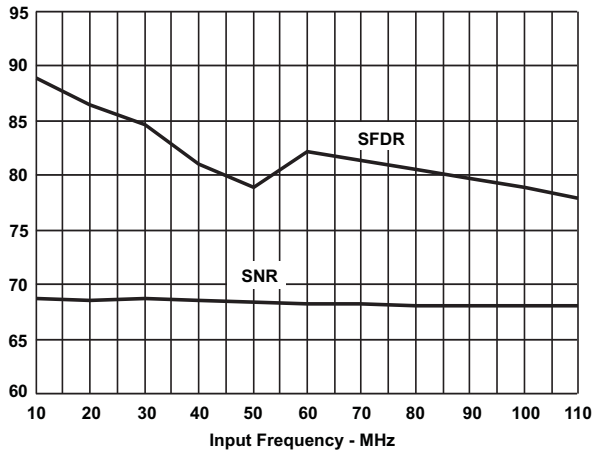


Figure 58. THS4508 + ADS5500 SFDR and SNR Performance versus Frequency

THS4508 + ADS5424 Combined Performance

Figure 59 shows the THS4508 driving the ADS5424 ADC, and Figure 60 shows the combined SNR and SFDR performance versus frequency with –1 dBFS input signal level and sampling at 80 MSPS.

As before, the THS4508 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4508 + ADS5500 circuit.

The 225-Ω resistors and 2.7-pF capacitor between the THS4508 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100 MHz (–3 dB).

When the THS4508 is operated from a single power supply with V_{S+} = 5 V and $V_{S–}$ = ground, the 2.5-V output common-mode voltage is compatible with the recommended value of the ADS5424 input common-mode voltage (2.4 V).

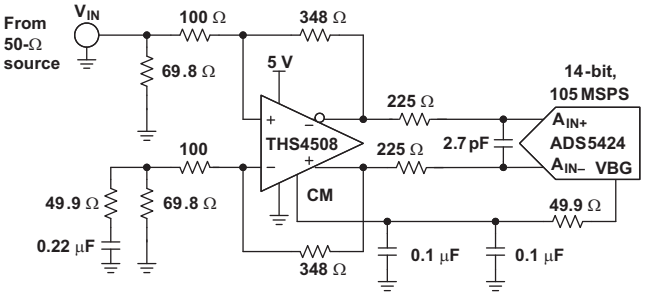


Figure 59. THS4508 + ADS5424 Circuit

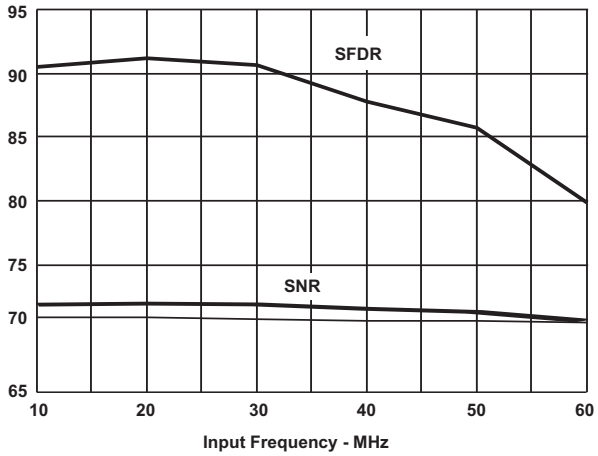


Figure 60. THS4508 + ADS5424 SFDR and SNR Performance vs Frequency

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Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the operational amplifier circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10-μF and two 0.1-μF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1-μF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4508 recommended printed circuit board (PCB) footprint is shown in Figure 61.

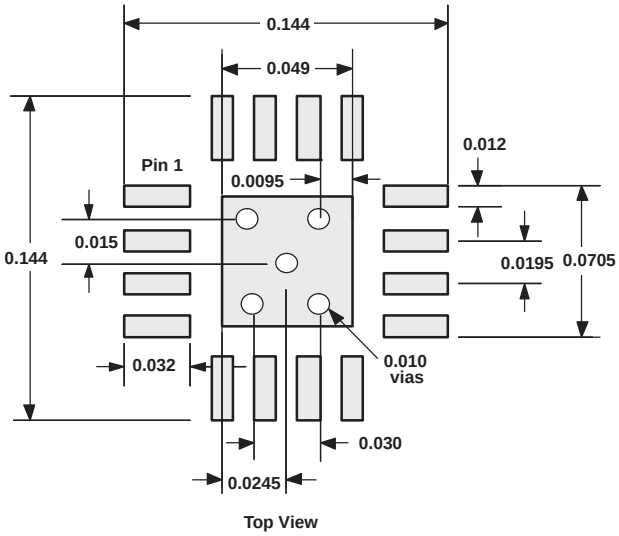


Figure 61. QFN Etch and Via Pattern

THS4508 EVM

Figure 62 is the THS4508 EVAL1 EVM schematic. Layers 1 through 4 of the PCB are shown in Figure 63 through Figure 66 , and Table 5 lists the bill of material for the EVM as supplied from TI.

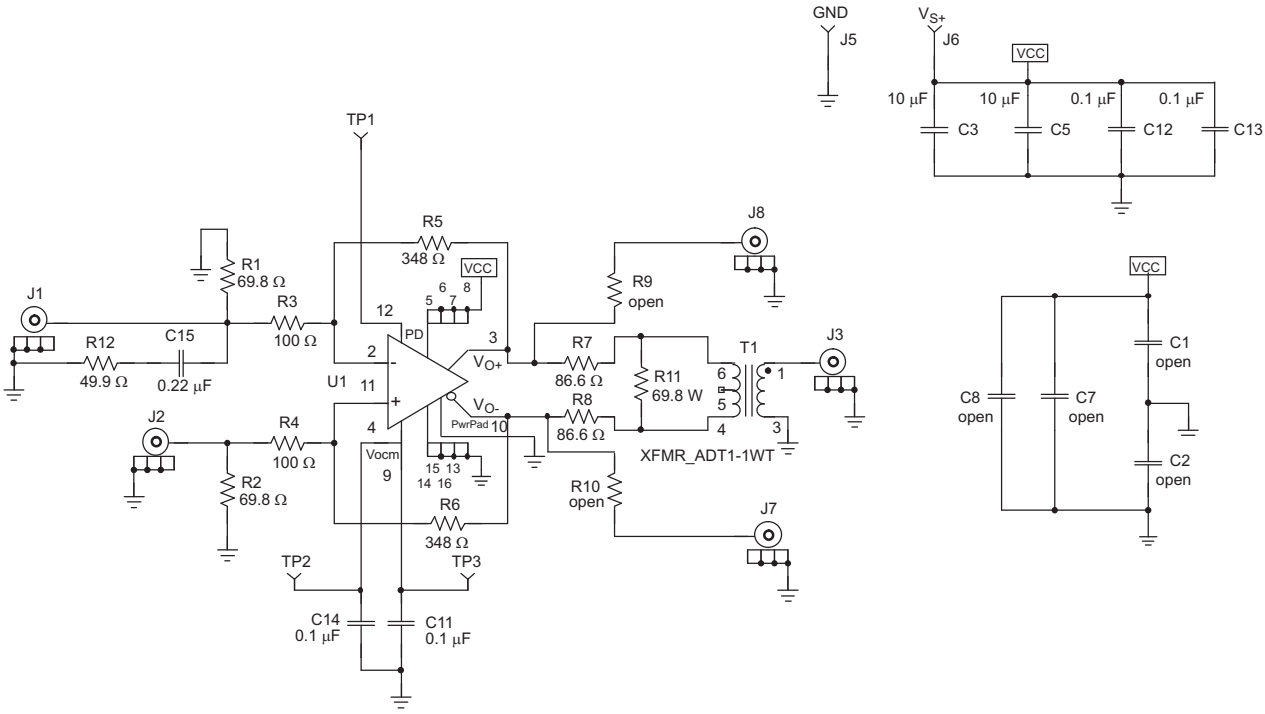


Figure 62. THS4508 EVAL1 EVM Schematic

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Table 5. THS4508RGT EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER(1)
1	CAP, 10.0 F, Ceramic, X5R, 6.3V	0805	C3, C5	2	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10V	0402	C11, C12, C13, C14	4	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 µF, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8, C9, C10	6	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
8	Resistor, 69.8 Ω, 1/16W, 1%	0402	R1, R2, R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 100 Ω, 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP1000F
11	Resistor, 348 Ω, 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Resistor, 0 Ω, 5%	0805	C4, C6	2	(KOA) RK73Z2ATTD
13	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, banana receptance, 0.25" diameter hole		J5, J6	2	(HH SMITH) 101
15	OPEN		J1, J7, J8	3	
16	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
17	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
18	IC, THS4508		U1	1	(TI) THS4508RGT
19	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
20	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
21	Printed circuit board			1	(TI) EDGE# 6468901

(1) The manufacturer's part numbers were used for tesr purposes only.

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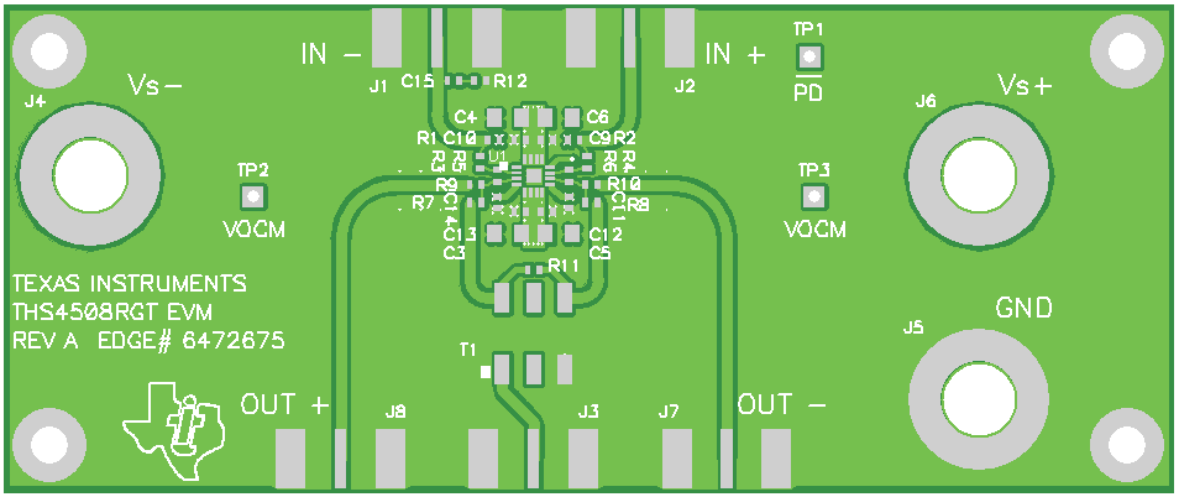


Figure 63. THS4508 EVM Top Layer

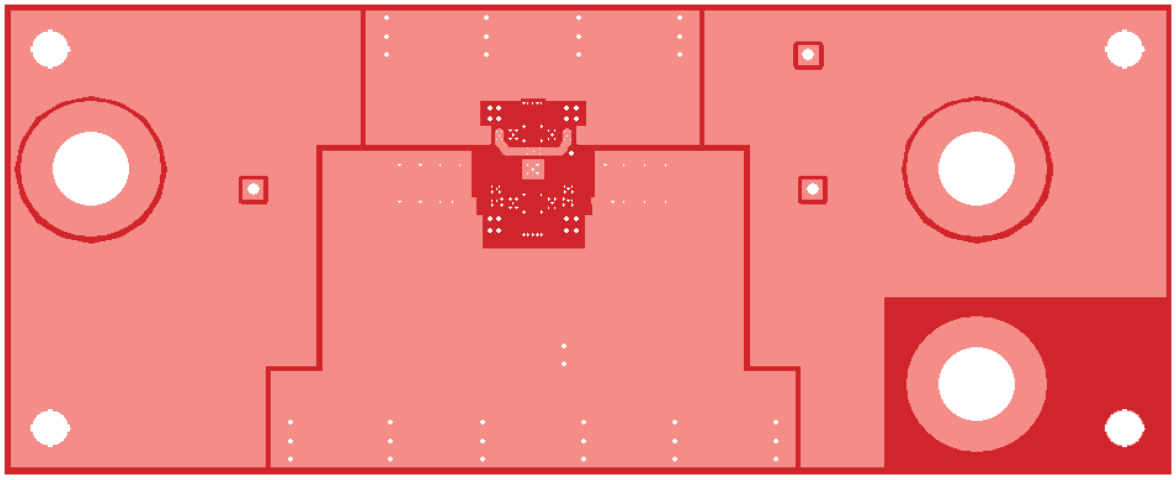


Figure 64. THS4508 EVM Layer 1

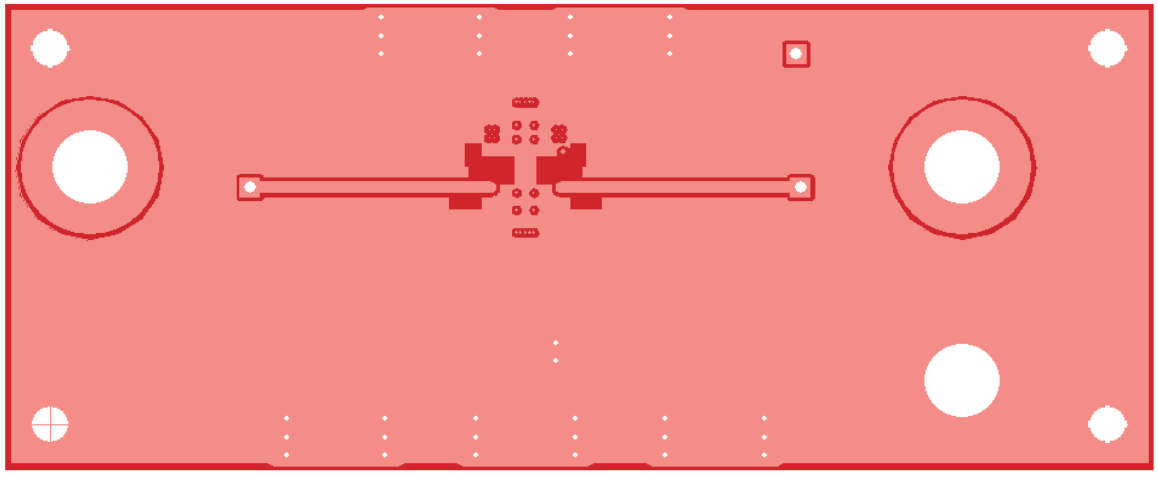


Figure 65. THS4508 EVM Layer 2

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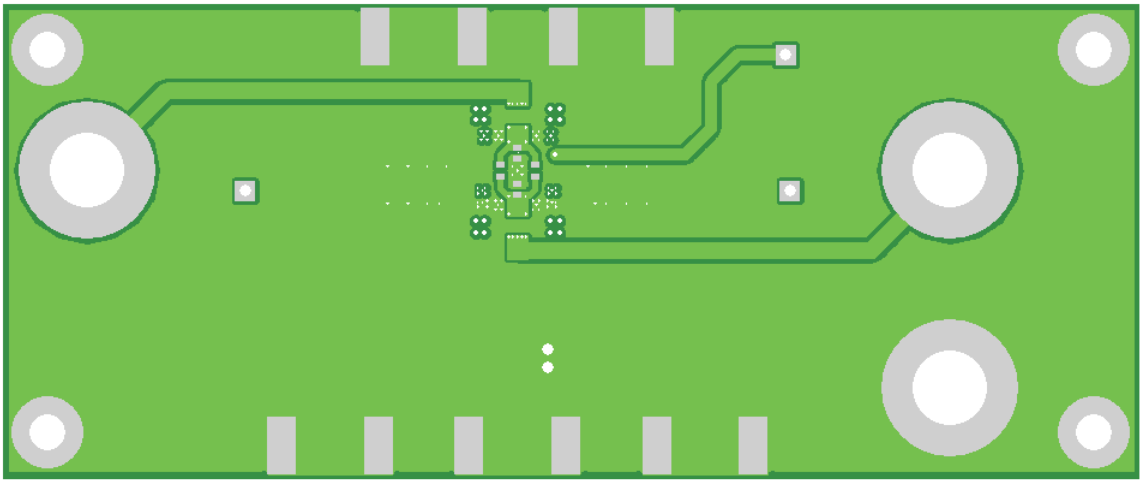


Figure 66. THS4508 EVM Bottom Layer

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the table provided below.

Input Range, V_{S+} to V_{S-}	3.0 V to 6.0 V
Input Range, V_I	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}
Output Range, V_O	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30°C. The EVM is designed to operate properly with certain components above +50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments Post Office Box 655303 Dallas, Texas 75265

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Revision History

Changes from Revision D (May 2007) to Revision E	Page
• Added *Ordering Information* table	2
• Changed Figure 35; corrected x-axis scale values	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4508RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4508	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

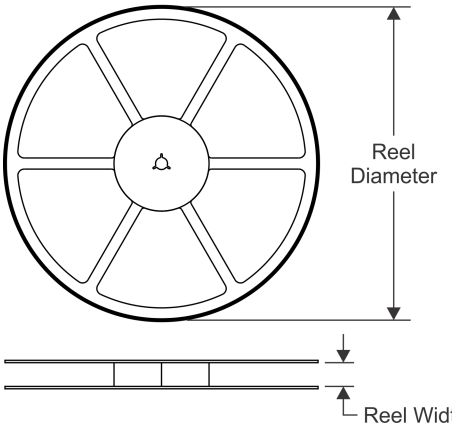
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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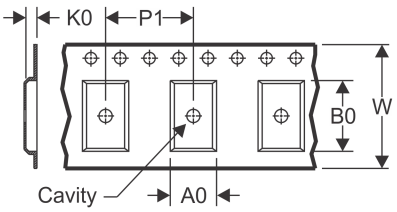
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

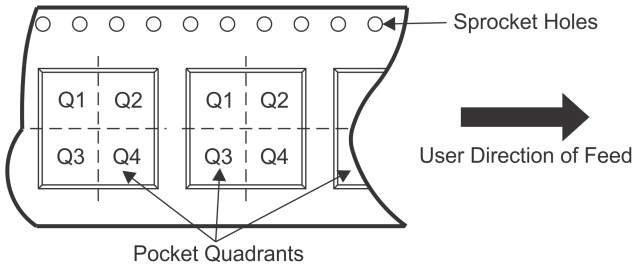


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

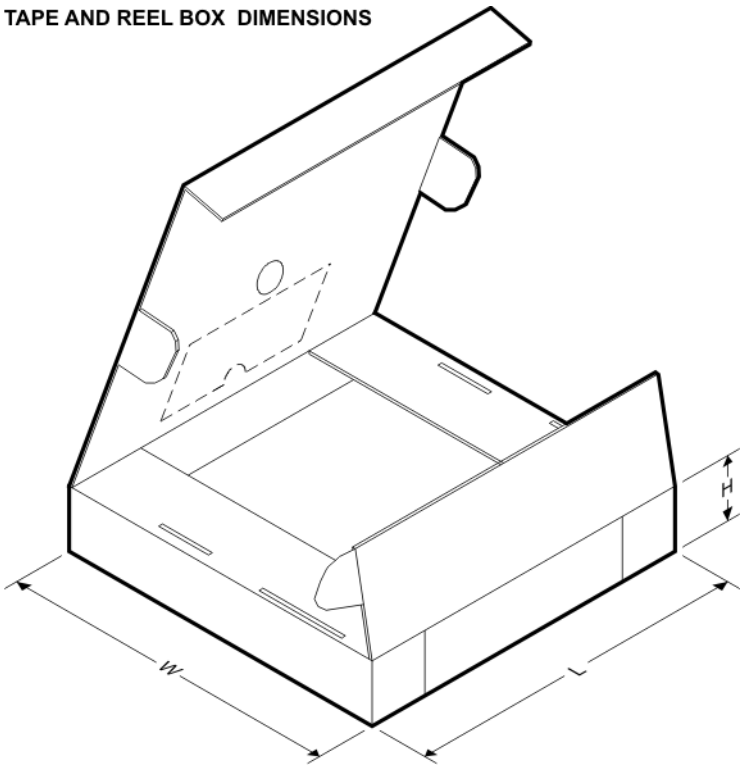
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4508RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

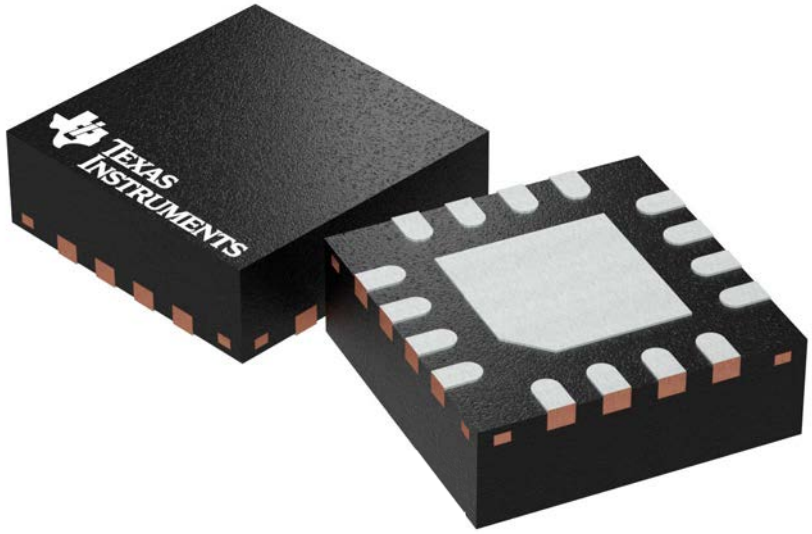


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4508RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



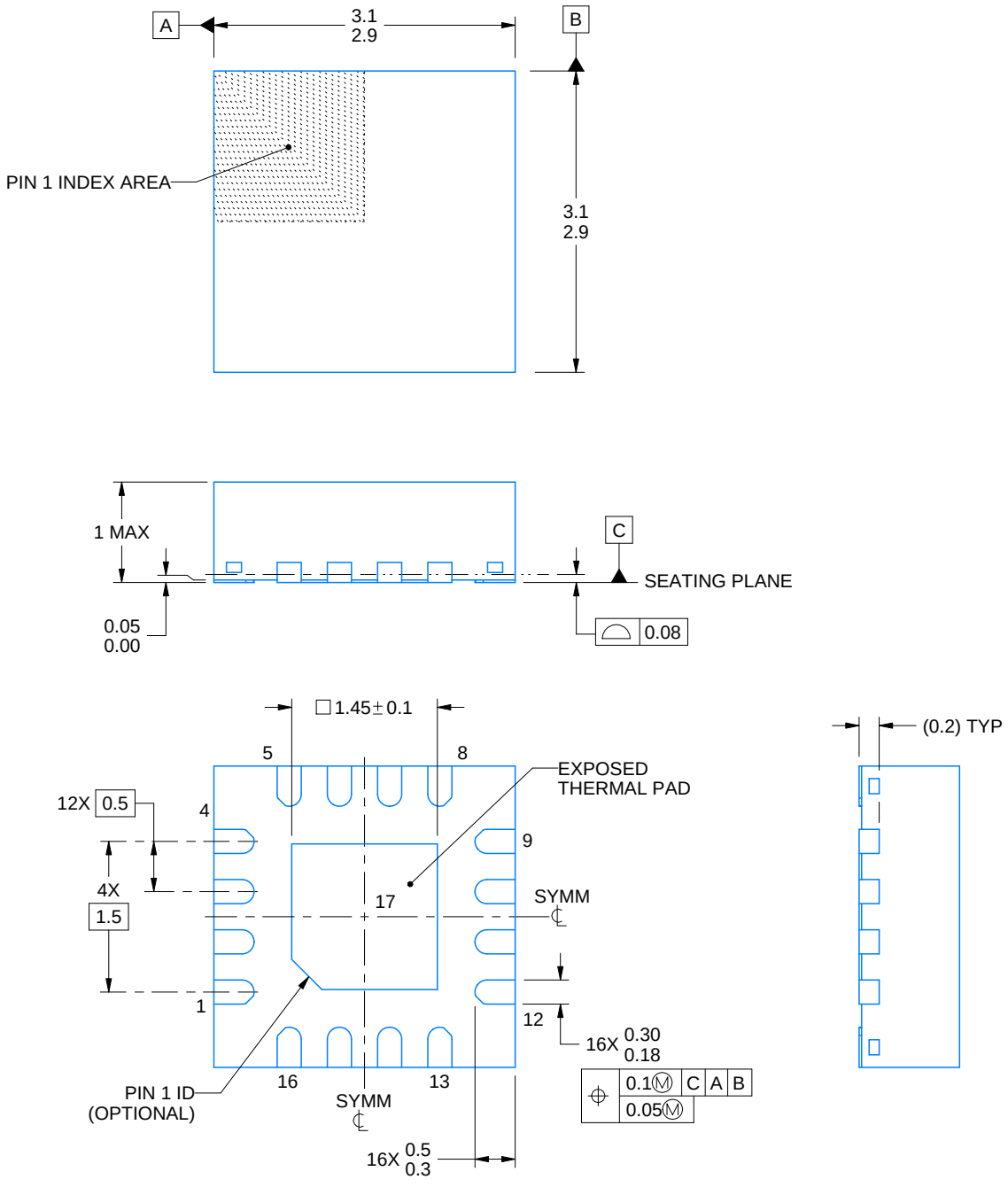
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

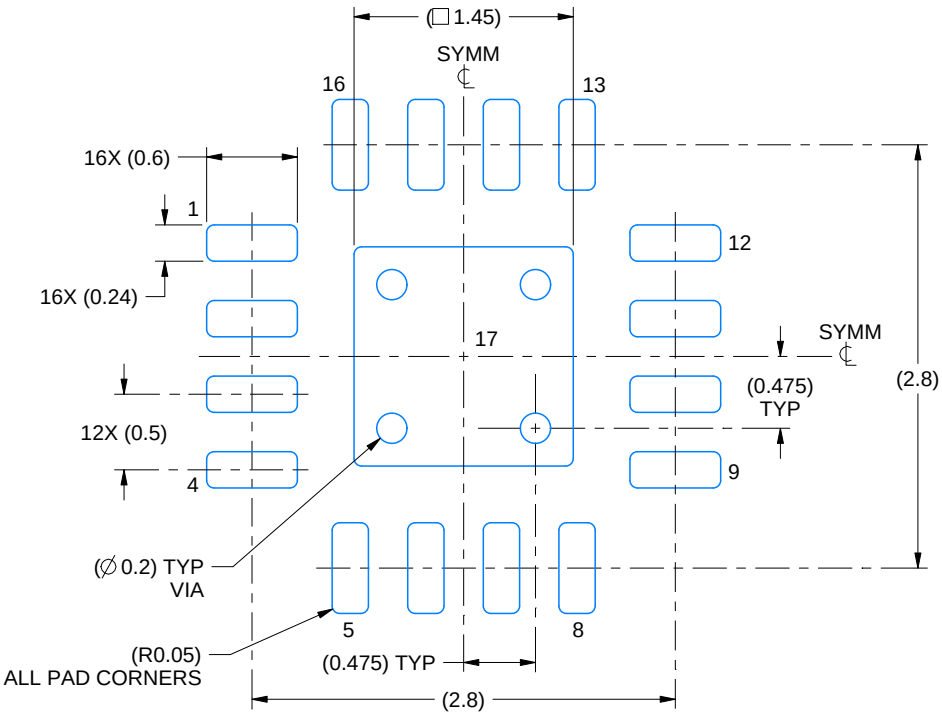
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

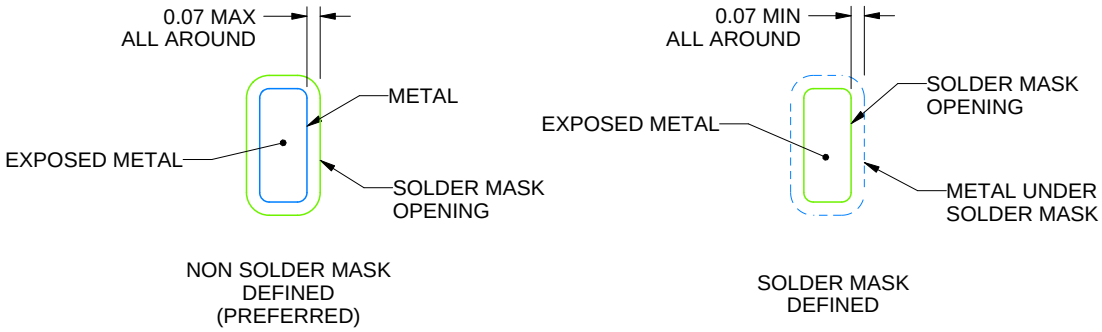


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

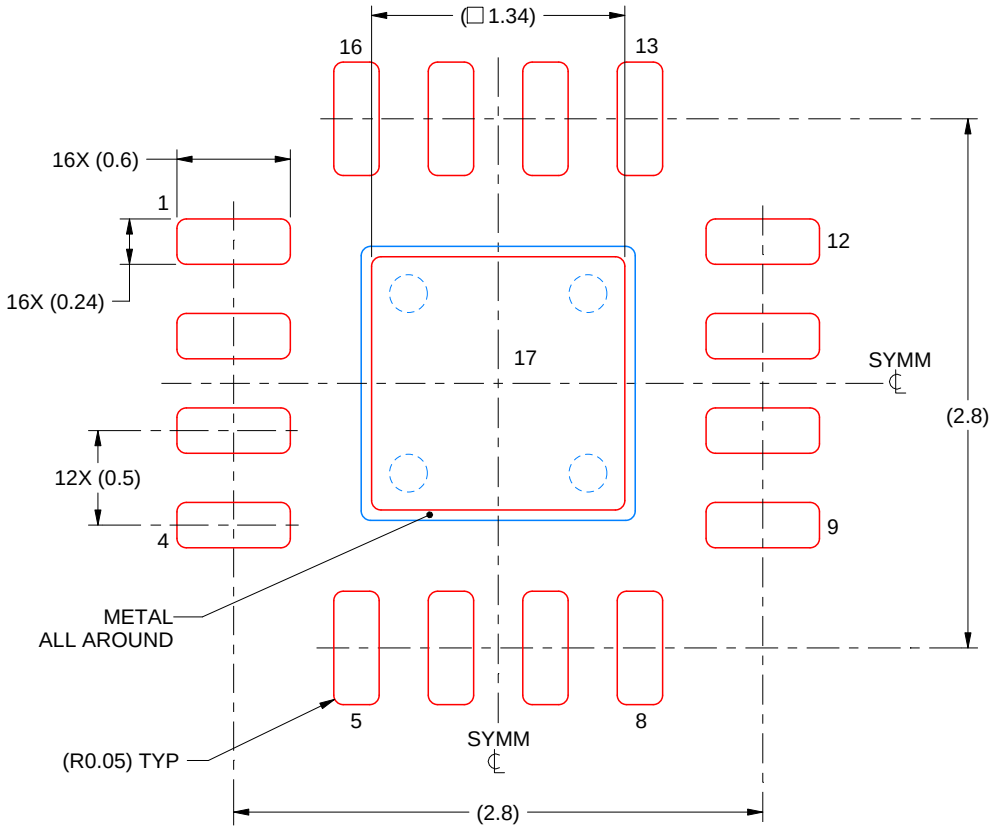


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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