MCP2517FD

MCP2517FD Silicon Errata and Data Sheet Clarification

The functionality of the MCP2517FD device is described in the device Data Sheet (DS20005688**B**), except for the anomalies described below.

1. Module: SPI Module

TX MAB underflow/RX MAB overflow due to long delays between SPI bytes

The SPI Interface can block the CAN FD Controller module from accessing RAM in between SPI bytes and between the last byte and the rising edge of the nCS line during an SPI READ or SPI READ CRC instruction while accessing RAM.

If the CAN FD Controller module is blocked for more than TSPIMAXDLY, a TX MAB underflow or an RX MAB overflow can occur.

Work around

Keep the delay between two SPI bytes and between the last SPI byte and the rising edge of nCS shorter than TSPIMAXDLY; see Figure 1.

The maximum allowed delay between two bytes depends on which CAN message frame is transmitted and on the selected Nominal Bit Time (NBT) and Data Bit Time (DBT). Table 1 lists TSPIMAXDLY for the worst-case scenarios.

For example: TSPIMAXDLY is 8.5 µs for a CAN FD frame at 500 kbps/2 Mbps. In comparison, an SPI byte takes 0.67 µs at 12 MHz SCK. A delay of 10 times the duration of one SPI byte could cause a TX MAB underflow. It is highly unlikely for an MCU application to introduce such a long delay, but this error could occur when running an operation system like Linux on a slower MPU.

In case of a TX MAB underflow, the device will notify the application by setting SERRIF and MODIF and by transitioning to Restricted Operation or Listen Only mode (depending on CiCON.SERR2LOM). After the application requests Normal mode, the CAN FD Controller module will automatically attempt to retransmit the message that caused the TX MAB underflow. It is not necessary to reset the device.

In case of an RX MAB overflow, the device will notify the application by setting SERRIF. The device will remain in Normal mode. The message that caused the RX MAB overflow will be discarded.

FIGURE 1: MAXIMUM DELAY BETWEEN SPI BYTES

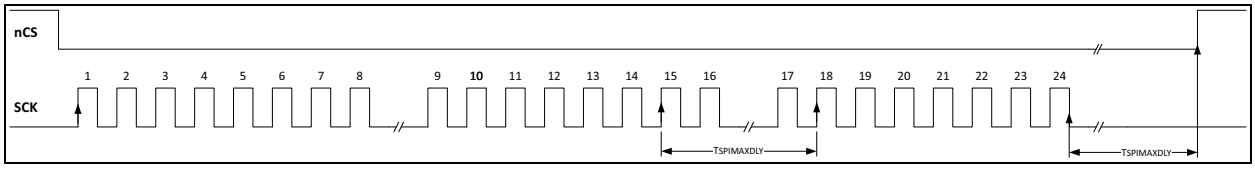

TABLE 1: WORST-CASE SCENARIOS

Scenario	Frame Format	TSPIMAXDLY
1	CAN Base Frame	5 NBT
2	CAN FD Control Field	3 NBT + 5 DBT
3	CAN FD Data Phase	32 DBT

2. Module: SPI Module

Incorrect CRC for certain READ_CRC commands

It is possible that there is a mismatch between the transmitted CRC and the actual CRC for the transmitted data when data is updated at a specific time during the SPI READ_CRC command. In these cases the transmitted CRC is wrong. The data transmitted is correct.

Fix/Work Around:

If a CRC mismatch occurs, reissue the READ_CRC command.

Only bits 7/15/23/31 of the following registers can be affected:

- CiTXIF
- CiRXIF
- CiCON
- CiTBC
- CiINT
- CiRXOVIF
- CiTXATIF
- CiTXREQ
- CiTREC
- CiBDIAG0
- CiBDIAG1
- CiTXQSTA
- CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31. In these cases, the registers CiTXIF, CiRXIF, CiRXOVIF, CiTXATIF and CiTX-REQ are not affected.

Bit 31 of RAM reads with CRC could also be affected. This can be avoided by reading from a received FIFO only after the message has been loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

Data Sheet Clarifications:

In the MCP2517FD Data Sheet (DS20005688**B**), the following clarifications and corrections should be noted:

a) None to report at this time.

APPENDIX A: REVISION HISTORY

Rev. B Document (July 2019)

- Updated **Section 1. Module: "SPI Module"**.
- Updated Figure 1.
- Added **Section 2. Module: "SPI Module"**: Incorrect CRC for certain READ_CRC commands.

Rev. A Document (May 2018)

- Initial release of this document.

NOTES:

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ISBN: 978-1-5224-4720-7

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