TPS7A6050QKTT EVM

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1 Introduction

The Texas Instruments TPS7A6050QKTT EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A6050QKTT Linear Regulator.

The EVM contains one Linear Regulator (see Table 1).

Table 1. Device and Package Configurations

REGULATOR	IC	PACKAGE
U1	TPS7A6050QKTTRQ1	KTT-5

2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS7A6050QKTT EVM.

2.1 Input/Output Connector Descriptions

VBAT is the protected power input for the regulator. The test point provides a power (Vbat) connection and a reverse battery protection diode to allow the user to power the EVM.

GND is the ground return for the regulator. The EVM provides three GND test points to allow the user to power the EVM, connect the load and attach an oscilloscope ground lead.

VIN is a power test point. The test point allows the user to measure the input voltage after the reverse battery protection diode. The user can also apply power to the regulator through this test point.

VOUT is power output for the regulator. The test point provides a connection to attach a load to the EVM.

DLY is a test point to monitor the charging of the delay capacitor.

nRST is a test point to monitor the reset flag. The reset flag is an active low, open drain output that will remain low when the output voltage is below the power-on reset threshold of approximately 4.65 V.

DELAY is the jumper used to set the delay time to hold the nRST pin low after the supply has exceeded the programmed power-on reset threshold voltage of approximately 4.65 V. The jumper capacitors allow the reset delay to be set to four set points. The user can set a specific delay time by changing one of the delay capacitors – C5, C6 or C7. The capacitor value can be set using this equation.

$$t_{POR} = \frac{CDLY * 3}{10^{-6}}$$

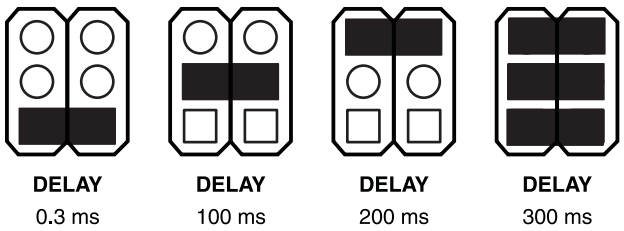


Figure 1. Reset Delay Time Settings

2.2 Setup

The input voltage range for the converter is 5.3 V to 40 V. The EVM can support up to 300 mA of load current.

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2.3 Operation

The TPS7A6050QKTT will power-up after the V_{BAT} voltage has exceeded the Power-On Reset threshold. The DELAY jumper should be configured for the desired nRST delay time.

In this configuration, the device will power up when power is applied.

The PCB offers footprints for the TPS7A6050QKTTQ1 or the TPS7A6050QKVUQ1 device.

3 Board Layout

Figure 2, Figure 3, and Figure 4 show the board layout for the TPS7A6050QKTT EVM PWB. The EVM offers capacitors and a jumper to program the nRST delay time.

The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 2 oz copper planes on the top and bottom to dissipate heat.

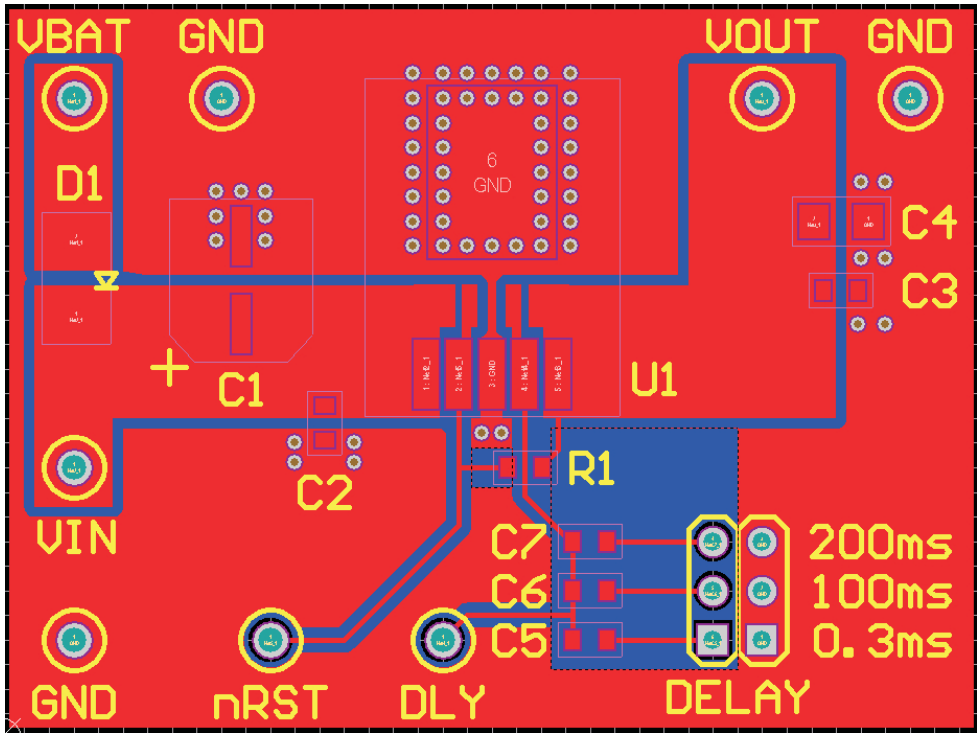


Figure 2. Top Assembly Layer

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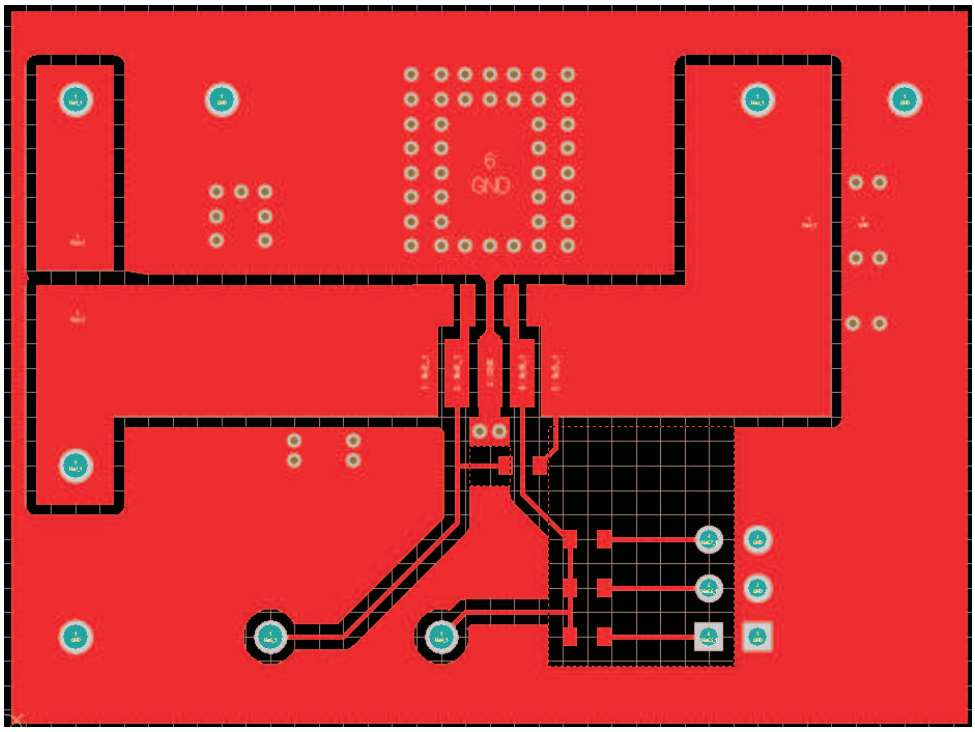


Figure 3. Top Layer Routing

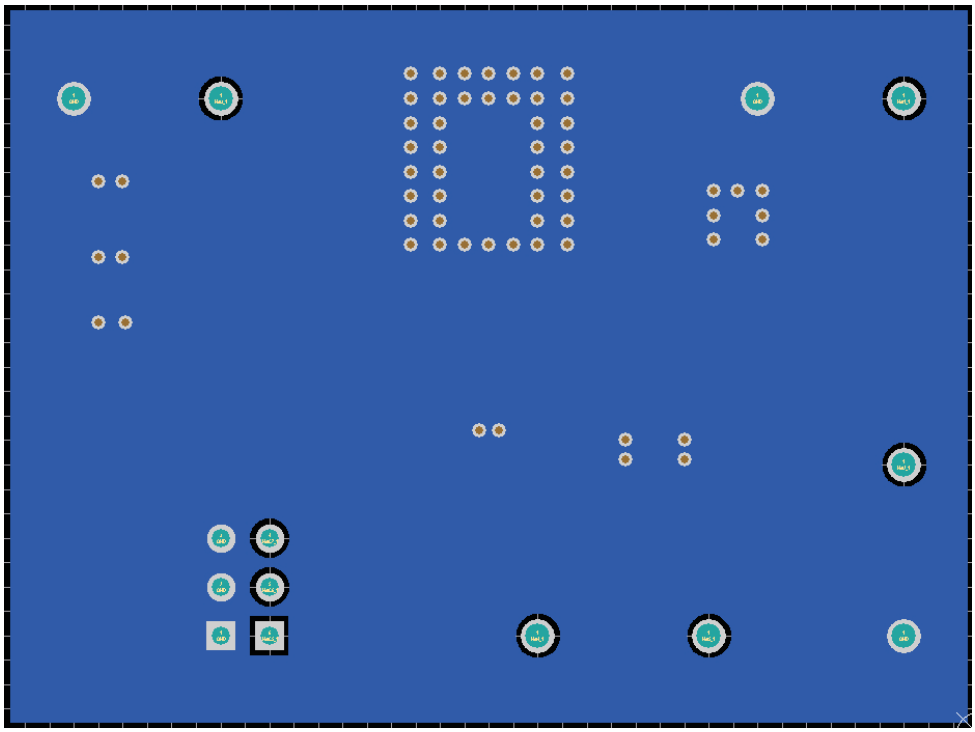


Figure 4. Bottom Layer Routing

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4 Schematic and Bill of Materials

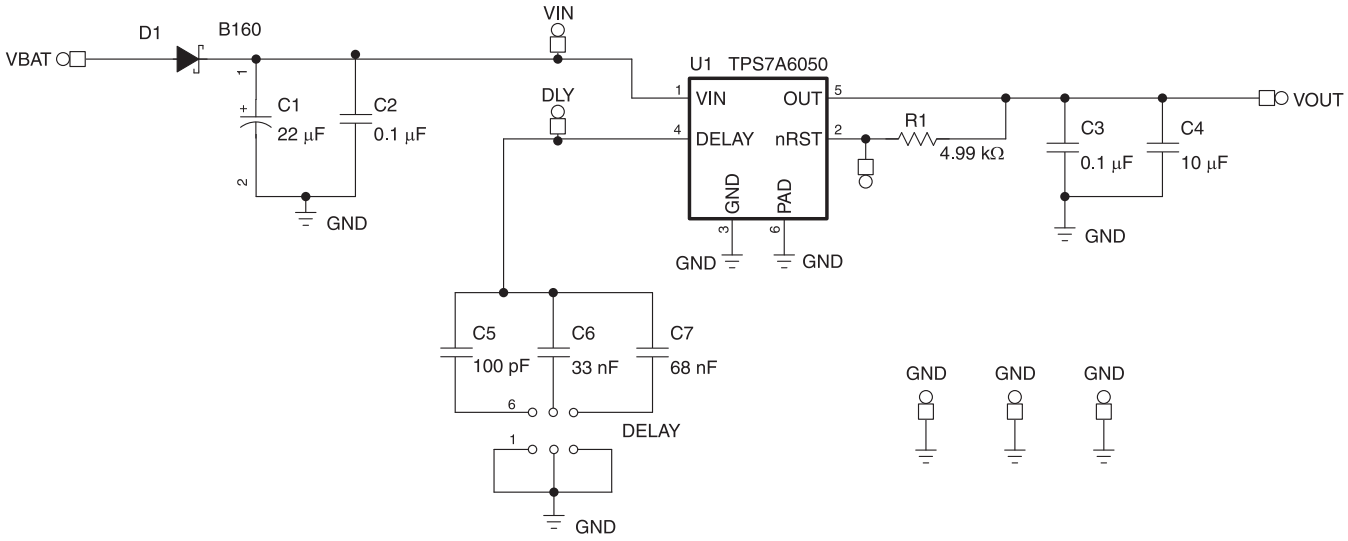


Figure 5. TPS7A6050QKTT EVM Schematic

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Table 2. TPS7A6050QKTT Bill of Materials

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C1	Capacitor, electrolytic, 22 µF, 50 V	6.3mm x 5.8mm	Panasonic	EEV-FK1H220P
2	C2, C3	Capacitor, ceramic, 0.1 µF, 50 V, 10%	603	muRata	GCM188R71H104KA57
1	C4	Capacitor, ceramic, 10 µF, 16 V, 10%	1206	muRata	GRM31CR71C106KAC7
1	C5	Capacitor, ceramic, 100 pF, 50 V, 5%	603	muRata	GCM1885C1H101JA16
1	C6	Capacitor, ceramic, 33 nF, 50 V, 10%	603	muRata	GRM188R71H333KA61
1	C7	Capacitor, ceramic, 68 nF, 50 V, 10%	603	muRata	GRM188R71H683KA93
1	D1	Diode, Schottky, 1 A, 60 V	SMA	Diodes	B160-13-F
8	DLY, GND (x3), nRST, VBAT, VIN, VOUT	Test point, 52-mil	0.052	Kobiconn	151-103-RC
1	DELAY	Header, 6-pin, 100-mil spacing, (36-pin strip)	0.100 x 3	Sullins	PEC03DAAN
3	DELAY	Connector jumper, shorting, 100-mil spacing	0.1	Sullins	SPC02SYAN
1	R1	Resistor, chip, 4.99-kΩ, 1/10W, 1%	603	Yageo	RC0603FR-074K99L
1	U1	IC, TPS7A6050QKTTQ1		TI	TPS7A6050QKTTQ1
	-	PCB, 2-inch x 1.5-inch x 0.062		Any	TPS7A60xx, REV A

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 5.3 V to 40 V and the output voltage 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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