MAX77874

16A High-Performance Quad-Phase Buck Regulator for Multicore CPU and GPU Processors

General Description

The MAX77874 is a quad-phase, high-current, step-down buck regulator for CPU and GPU multicore processors. Proprietary IP provides industry-leading transient response, output voltage accuracy, high efficiency, and miniature PCB footprint.

The output voltage is I²C programmable from 0.25V to 1.30V in 5mV steps. Output current capability is 16A. Rotational phase spreading ensures high efficiency and low ripple at light loads with seamless operation across all varying loads. Turbo skip mode combines the same transient response of forced-PWM mode with light load efficiency similar to Skip mode. Soft-start and DVS ramp rates are I²C programmable and controlled through dedicated logic inputs.

The MAX77874 is offered in a 48-bump, 0.35mm pitch WLP array and is specified over the -40°C to +85°C temperature range.

***Ordering Information* appears and *Benefits and Features* continued at end of data sheet.**

Applications

- Smartphones, Tablets, Ultrabooks
- DSLR, Mirrorless, Action Cameras
- Gaming, Drones, Robots, Virtual Reality
- AI, Machine Vision, Embedded Microprocessors

Benefits and Features

- Operating Range
  - V_{IN}: 2.7V to 4.8V
  - V_{OUT}: 0.25V to 1.30V in 5mV Steps
  - I_{OUT}: Up to 16A
- Fast Load-Transient Response
  - 25mV Droop in FPWM and Turbo-Skip Modes
  - 40mV Droop in Skip Mode
  - Conditions: $3.7V_{IN}$, $0.9V_{OUT}$, 200mA to 9.2A
- Tight V_{OUT} Accuracy
  - 0.28% (max) Initial Accuracy at $0.9V_{OUT}$
  - 1.5% (max) Over Line/Temperature
  - $3mV_{P-P}$ (typ) Ripple at All Loads

Simplified Block Diagram for 16A Multiphase Buck for Multicore Processors

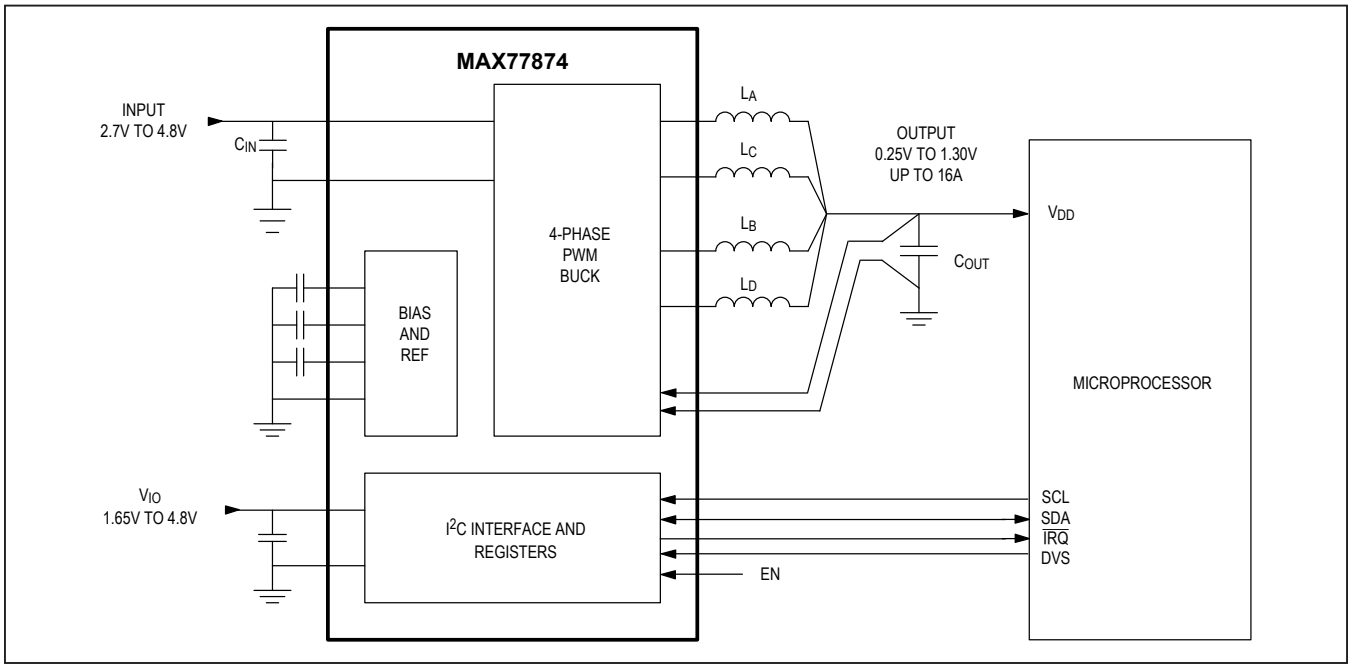


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Absolute Maximum Ratings

PG_, AGND_, SNS- to AGND ..... -0.3V to +0.3V
EN, DVS, SDA, SCL, $\overline{IRQ}$ to AGND ..... -0.3V to V_{IO} + 0.3V
IN_, LX_ to PG_ ..... -0.3V to +5.5V
V_{DD_ANA} to AGND ..... -0.3V to +1.85V
SNS+ to AGND ..... -0.3V to V_{CC} + 0.3V
V_{DD_DIG} to AGND ..... -0.3V to +1.85V
V_{CC}, V_{IO} to AGND ..... -0.3V to +5.5V
V_{PP} to AGND ..... -0.3V to +8V
LX_ Current (Note 1) ..... $4.3A_{RMS}$
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LX_ has internal clamping diodes to PG_ and IN_. Applications that forward bias these diodes should take care not to exceed the power dissipation limits of the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W482B2+1
Outline Number	**21-0784**
Land Pattern Number	**Refer to Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	57°C/W
Junction to Case (θ_{JC})	

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40°C to +85°C, typical values at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_{CC} Falling UVLO Threshold	V_{UVLO_F}		2.5	2.6	2.7	V
V_{CC} Rising UVLO Threshold	V_{UVLO_R}		2.7	2.8	2.9	V
V_{CC} Falling UVLO Threshold Delay Time	t_{UVLO_F}	V_{CC} falling, 20mV overdrive		20		µs
V_{CC} Operating Voltage Range	V_{CC}		2.7		4.8	V
Shutdown Supply Current	I_{SHDN}	BUCK0EN[0] = 0, V_{IO} = 0V, V_{IN} = V_{CC} = V_{PP} = 4.8V, T_A = +25°C		0.2	5	µA
Shutdown Supply Current (Note 1)	I_{SHDN}	BUCK0EN[0] = 0, V_{VIO} = 0V, V_{IN} = V_{CC} = V_{PP} = 4.8V, T_A = +85°C		1		µA

Electrical Characteristics (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40°C to +85°C, typical values at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Disable Supply Current	$I_{DISABLE}$	BUCK0EN[0] = 0, V_{IO} = 1.8V, V_{IN} = V_{CC} = V_{PP} = 4.8V, T_A = +25°C		14	30	µA
Disable Supply Current (Note 1)	$I_{DISABLE}$	BUCK0EN[0] = 0, V_{IO} = 1.8V, V_{IN} = V_{CC} = V_{PP} = 4.8V, T_A = +85°C		25		µA
Skip Mode Quiescent Supply Curernt	$I_{Q,SKIP}$	BUCK0EN[0] = 1, TURBO[0] = 0, FPWMEN[0] = 0, V_{OUT} = 0.9V, no load, no switching, includes current through SNS+ and SNS- internal dividers		275	550	µA
Turbo Skip Mode Quiescent Supply Current	$I_{Q,TURBOSKIP}$	BUCK0EN[0] = 1, TURBO[0] = 1, FPWMEN[0] = 0, V_{OUT} = 0.9V, no load, no switching, includes current through SNS+ and SNS- internal dividers		475	900	µA
V_{PP} Input Current	I_{VPP}	V_{PP} = V_{CC}, T_A = +25°C		0.03	1	µA
		V_{PP} = V_{CC}, T_A = -40°C to +85°C		0.1		µA
V_{IO} Input Voltage Range	V_{IO}		1.65	1.8	4.8	V
V_{IO} Static Supply Current	$I_{VIO,STATIC}$	f_{SCL} = f_{SDA} = 0Hz, SCL and SDA pulled high, EN = GND, BUCK0EN[0] = 0, ENPD_EN[0] = 0		0.2	1	µA
V_{IO} Dynamic Supply Current	$I_{VIO,DYN}$	f_{SCL} = f_{SDA} = 1MHz		10		µA
V_{CC} Dynamic Supply Current	I_{CC}	f_{SCL} = f_{SDA} = 1MHz		30		µA
V_{DD_DIG} AND V_{DD_ANA} SUPPLIES						
V_{DD_DIG} Output Voltage	V_{DD_DIG}			1.575		V
V_{DD_ANA} Output Voltage	V_{DD_ANA}			1.575		V
V_{DD_ANA} and V_{DD_DIG} Enable Time	t_{CE}	V_{DD_ANA} and V_{DD_DIG} ready time from V_{CC} rising edge		200		µs
GPIO/I/O LOGIC PINS						
EN Pulldown Resistance	$R_{PD,EN}$		200	400	800	kΩ
EN, DVS Input Logic High Threshold	$V_{IH,EN}V_{IH,DVS}$		0.7 x V_{IO}			V
EN, DVS Input Logic Low Threshold	$V_{IL,EN}V_{IL,DVS}$				0.3 x V_{IO}	V
EN, DVS, $\overline{IRQ}$ Logic Input Leakage Current	$I_{LK,EN}I_{LK,DVS}I_{LK,\overline{IRQ}}$	V_{IO} = 1.8V, T_A = +25°C	-1		+1	µA
		V_{IO} = 1.8V, T_A = -40°C to +85°C		0.1		
$\overline{POK}$ Threshold Falling		V_{OUT} = 0.9V	607.5	675	741.5	mV
$\overline{POK}$ Threshold Rising		V_{OUT} = 0.9V	648	720	792	mV
$\overline{POK}$ Threshold Hysteresis		V_{OUT} = 0.9V	39	46	52	mV
$\overline{IRQ}$ Output Voltage Low	$V_{OL,\overline{IRQ}}$	I_{SINK} = 10mA		0.2	0.4	V

Electrical Characteristics (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40°C to +85°C, typical values at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL MONITORS						
Thermal Alarm 1	T_{J120}	T_J rising, 5°C hysteresis		+120		°C
Thermal Alarm 2	T_{J140}	T_J rising, 5°C hysteresis		+140		°C
Thermal Shutdown Temperature	T_{JSHDN}	T_J rising, 15°C hysteresis		+165		°C

Electrical Characteristics—Quad Phase Core Buck Regulator

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40°C to +85°C, typical values at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}	8-bit resolution, 5mV/LSB	0.25		1.3	V
Output Voltage Range End-Point Error		V_{OUT} = 0.25V and 1.3V, I_{OUT} = 0mA, FPWMEN[0] = 1, T_A = +25°C	-10	±1	+10	mV
DC OUTPUT VOLTAGE ACCURACY						
Initial Output Voltage Accuracy		I_{OUT} = 0mA, FPWMEN[0] = 1, T_A = +25°C	-2.5		+2.5	mV
Output Voltage Accuracy, FPWM Mode		I_{OUT} = 0mA, TURBO[0] = 0, FPWMEN[0] = 1, T_A = -5°C to +85°C	-5		+5	mV
		I_{OUT} = 0mA, TURBO[0] = 0, FPWMEN[0] = 1, T_A = -40°C to +85°C	-13	±1.75	+10	
Output Voltage Accuracy, Turbo Skip Mode		I_{OUT} = 0mA, TURBO[0] = 1,FPWMEN[0] = 0, excludes output voltage ripple		±2.5		mV
Output Voltage Accuracy, Skip Mode		I_{OUT} = 0mA, TURBO[0] = 0, FPWMEN[0] = 0, excludes output voltage ripple		±2.5		mV
Load Regulation		FPWMEN[0] = 1, I_{OUT} = 0 to 16A		0.1		mV/A
Line Regulation		V_{IN} = 2.5V to 4.8V, I_{OUT} = 0mA, FPWMEN[0] = 1	-0.3		+0.3	mV/V
SWITCH RATINGS						
Maximum Output Current	$I_{OUT,MAX}$	Per phase, RMS rating	4000			mA
PMOS Current Limit	I_{LIMP}	Per phase	4.750	5.275	5.800	A
NMOS Valley Current Limit	I_{VALLEY}	Per phase	3.819	4.244	4.669	A
NMOS Negative Current Limit	I_{LIMN}	Per phase	-1800	-1500	-1200	mA
Zero-Crossing Current Threshold	I_{ZX}	DC tested	+50	+115	+170	mA
Zero-Crossing Comparator Propagation Delay	t_{PD_ZX}			20		ns
Switching Frequency	f_{SW}	FPWM mode, no load, T_A = +25°C	1.9	2.0	2.1	MHz

Electrical Characteristics—Quad Phase Core Buck Regulator (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40°C to +85°C, typical values at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX_ Leakage Current	I_{LKG_LX}	$V_{LX_}$ = 0V or 4.8V, T_A = +25°C		0.1	1	µA
		$V_{LX_}$ = 0V or 4.8V, T_A = -40°C to +85°C (Note 1)		1		
Main Switch On-Resistance	R_{DSON_MS}	$I_{LX_}$ = 190mA		65		mΩ
Synchronous Rectifier On-Resistance	R_{DSON_SR}	$I_{LX_}$ = -190mA		16		mΩ
ACTIVE DISCHARGE						
LX_ Active Discharge Resistance	R_{LX_AD}	BUCK0EN[0] = 0, BUCK0ADEN[0] = 1, resistance from LX_ to PG_, per phase		100	140	Ω
RAMP RATES						
Startup Ramp Rate		BUCK0SSR[1:0] = 0b00, WARMSTART[0] = 1	4.5	5	5.5	mV/µs
		BUCK0SSR[1:0] = 0b01, WARMSTART[0] = 1	9	10	11	
		BUCK0SSR[1:0] = 0b10, WARMSTART[0] = 1	18	20	22	
		BUCK0SSR[1:0] = 0b11, WARMSTART[0] = 1	36	40	44	
Cold Startup Ramp Rate		WARMSTART[0] = 0	1.125	1.25	1.375	mV/µs
DVS Ramp Rate		BUCK0RSR[1:0] = 0b00	4.5	5	5.5	mV/µs
		BUCK0RSR[1:0] = 0b01	9	10	11	
		BUCK0RSR[1:0] = 0b10	18	20	22	
		BUCK0RSR[1:0] = 0b11	36	40	44	
DVS Ramp Delay		Measured from DVS rising edge to first LX pulse		1.5		µs
Startup Ramp Delay		Measured from EN rising edge to first LX pulse		50	200	µs
SNS+ AND SNS- FEEDBACK INPUTS						
SNS+ Input Impedance	$R_{IN,SNS+}$		75	120	160	kΩ
SNS- Input Impedance	$R_{IN,SNS-}$		75	120	160	kΩ

I²C Electrical Characteristics

V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40ºC to +85ºC, typical values are at T_A = +25ºC, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.8V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.8V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V

I²C Electrical Characteristics (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40ºC to +85ºC, typical values are at T_A = +25ºC, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL} (Note 1)	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 2)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 100pF) (Note 2)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{rCL1}	T_A = +25°C	10		80	ns
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns

I²C Electrical Characteristics (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, V_{OUT} = 0.9V, C_{VDD_ANA} = 1µF, C_{VDD_DIG} = 1µF, C_{VCC} = 1µF, T_A = -40ºC to +85ºC, typical values are at T_A = +25ºC, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (Note 2)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		80	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

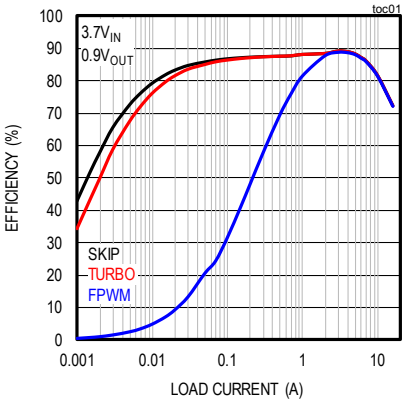
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 2: Guaranteed by design. Not production tested.

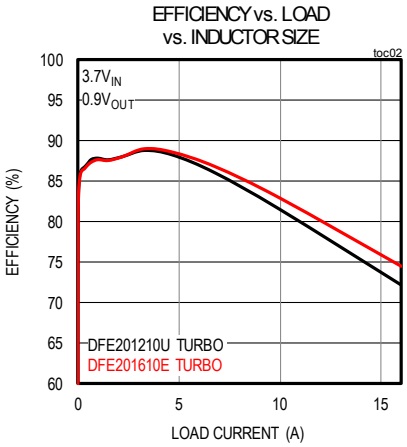
Typical Operating Characteristics

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

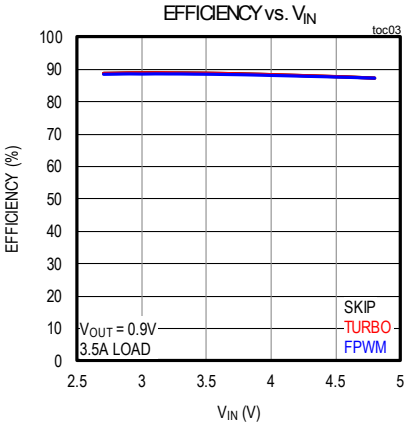
EFFICIENCY vs. LOAD



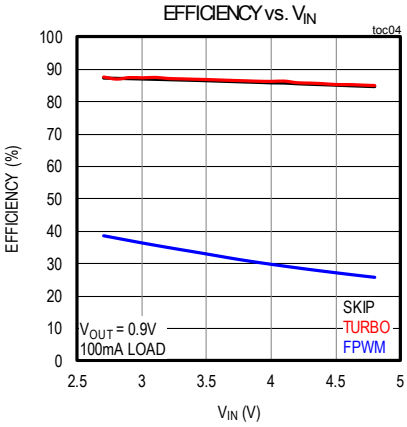
EFFICIENCY vs. LOAD vs. INDUCTOR SIZE



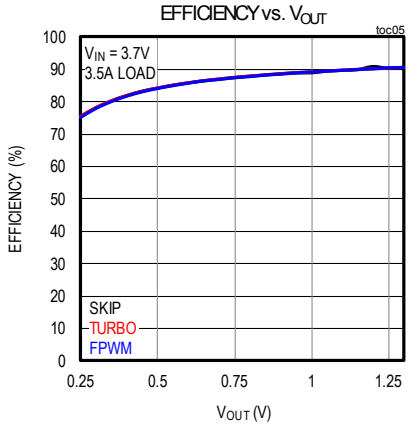
EFFICIENCY vs. V_{IN}



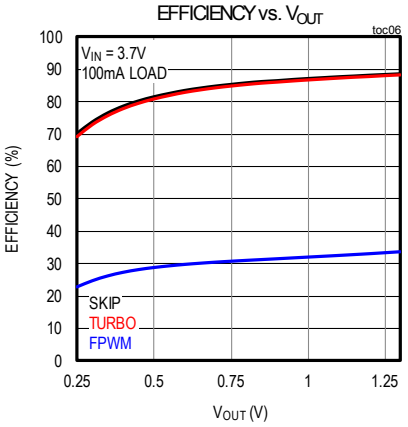
EFFICIENCY vs. V_{IN}



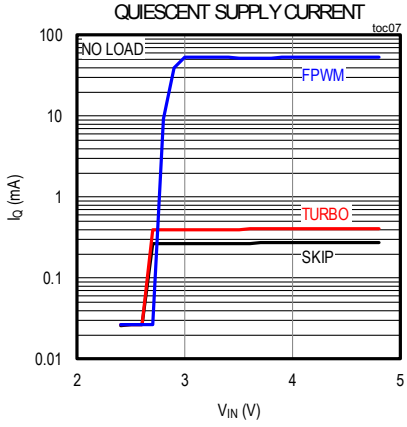
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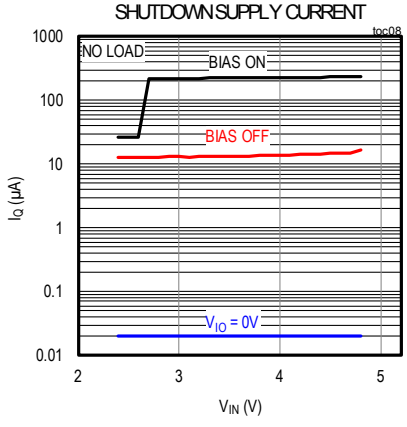
EFFICIENCY vs. V_{OUT}



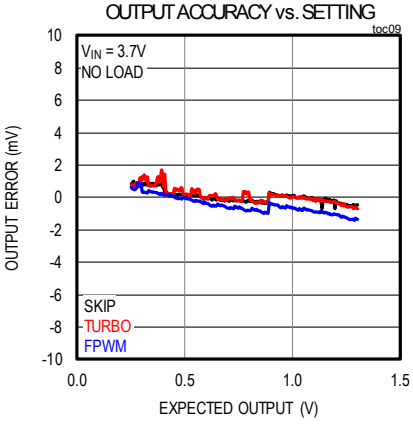
QUIESCENT SUPPLY CURRENT



SHUTDOWN SUPPLY CURRENT



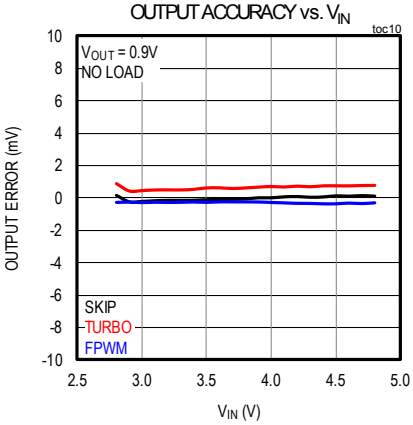
OUTPUT ACCURACY vs. SETTING



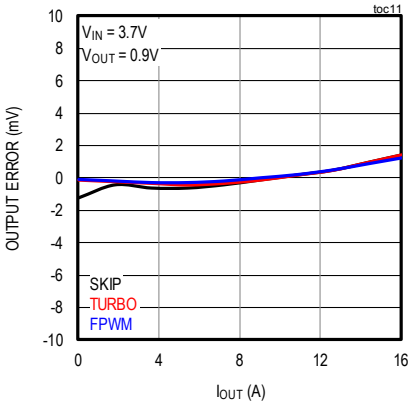
Typical Operating Characteristics (continued)

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

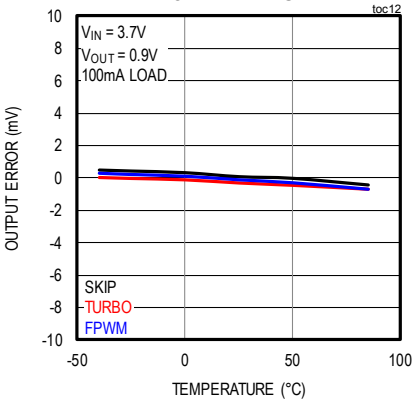
OUTPUT ACCURACY vs. V_{IN}



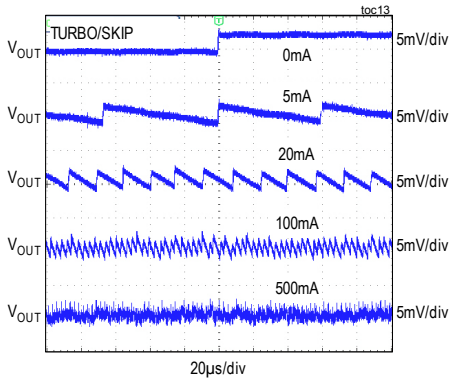
OUTPUT ACCURACY vs. DC LOAD



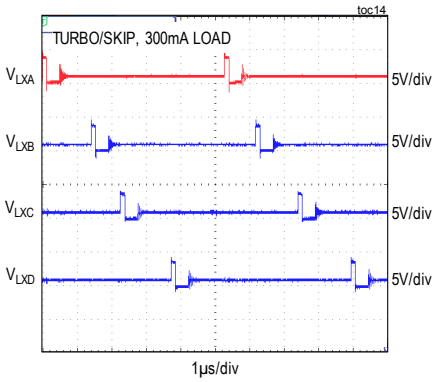
OUTPUT ACCURACY vs. TEMPERATURE



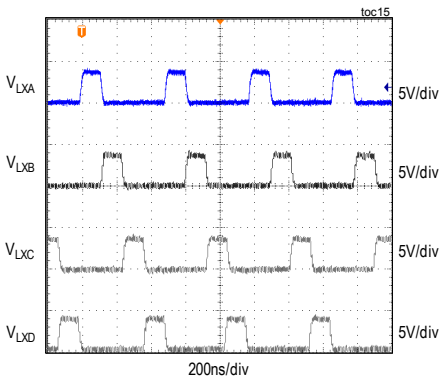
OUTPUT VOLTAGE RIPPLE



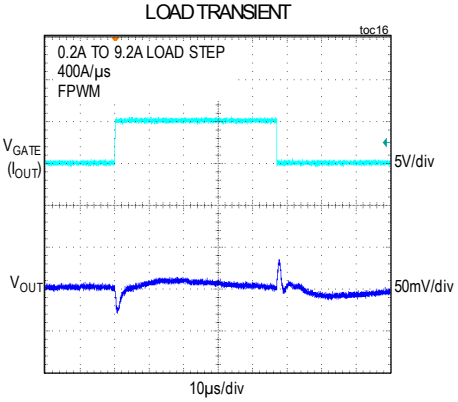
LIGHT-LOAD PHASE SPREADING



FPWM PHASE MATCHING



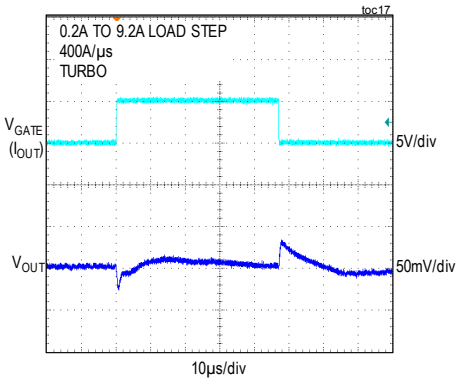
LOAD TRANSIENT



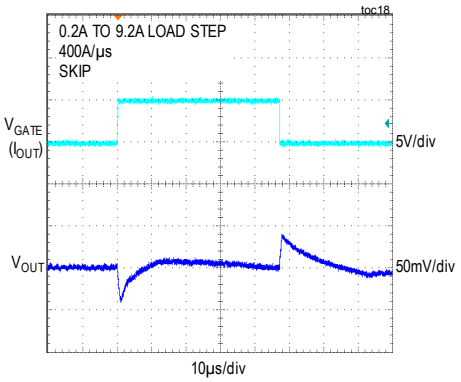
Typical Operating Characteristics (continued)

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

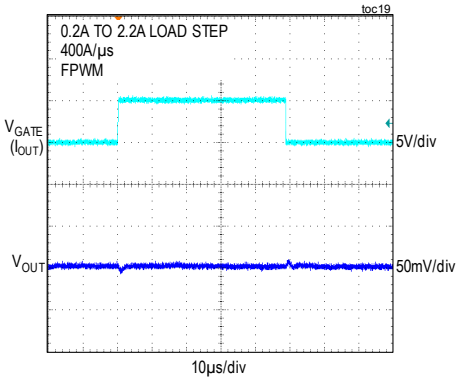
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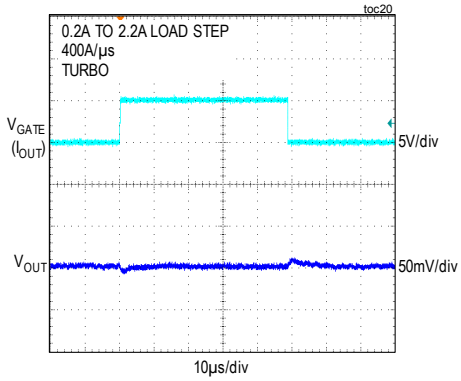
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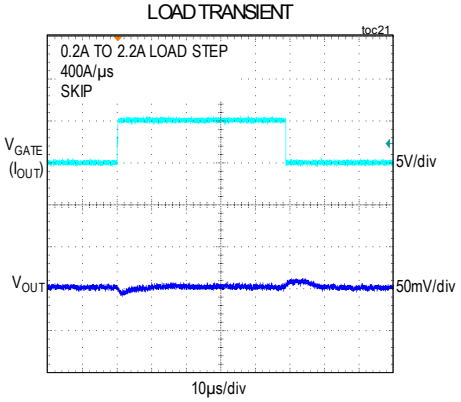
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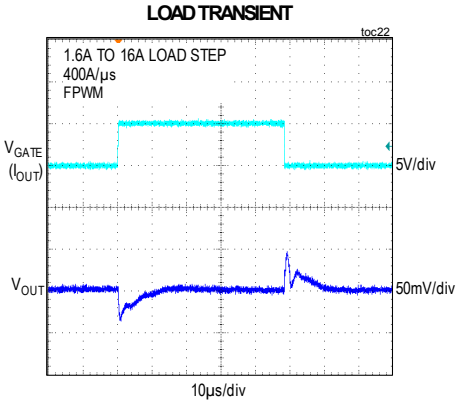
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LOAD TRANSIENT



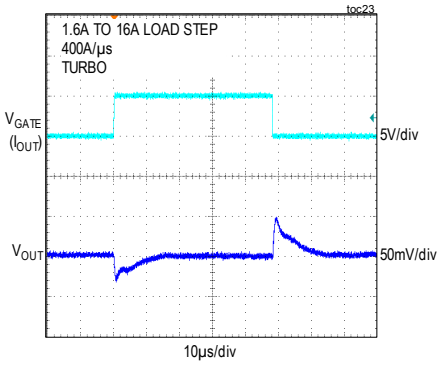
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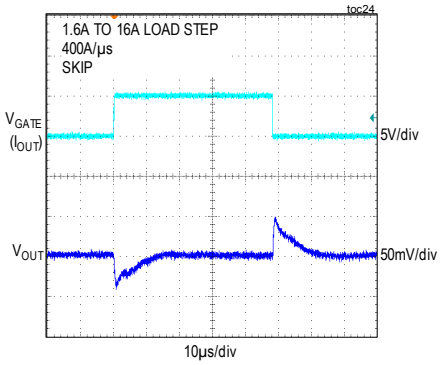
Typical Operating Characteristics (continued)

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

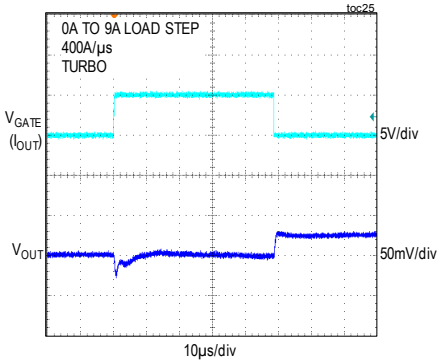
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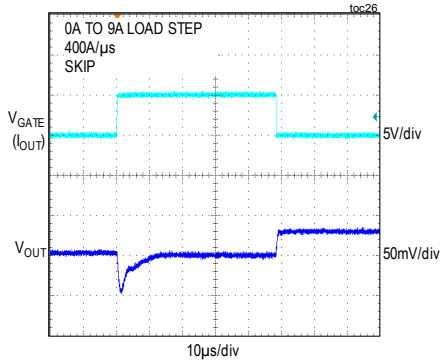
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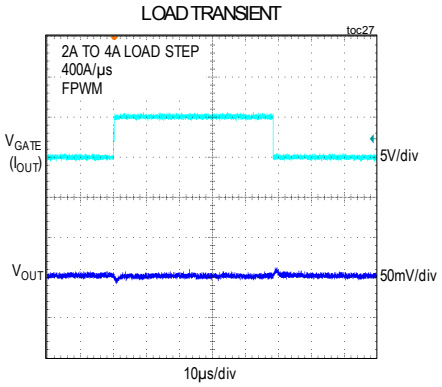
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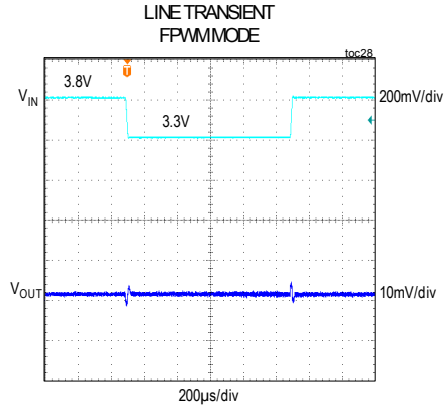
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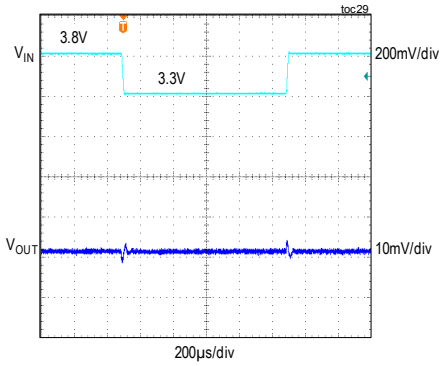
LINE TRANSIENT
FPWM MODE



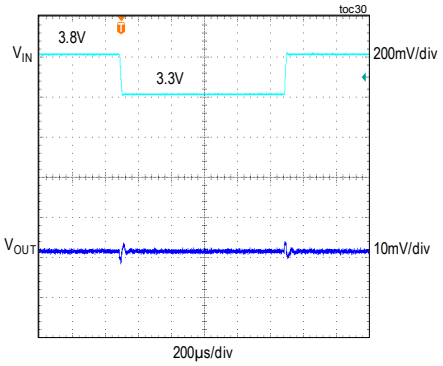
Typical Operating Characteristics (continued)

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

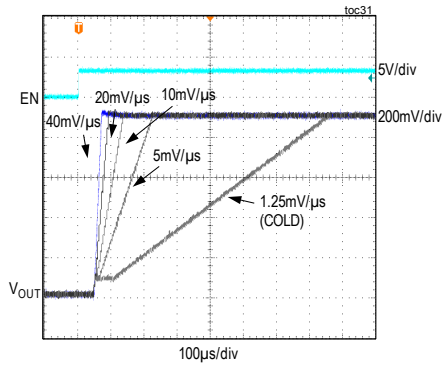
LINE TRANSIENT
TURBO MODE



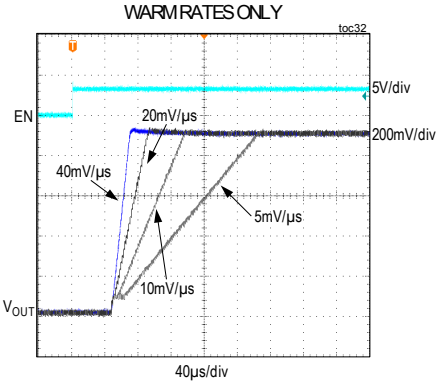
LINE TRANSIENT
SKIP MODE



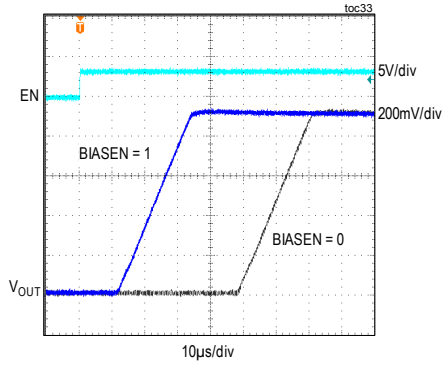
REGULATOR SOFT-START RATES



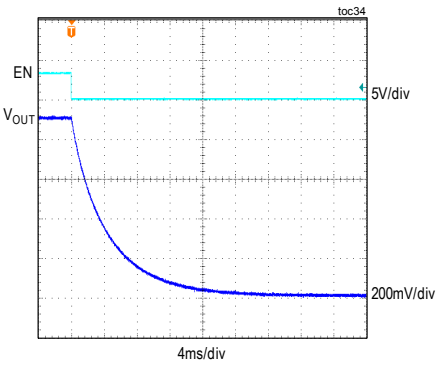
REGULATOR SOFT-START RATES
WARM RATES ONLY



REGULATOR ENABLE vs. BIAS STATUS



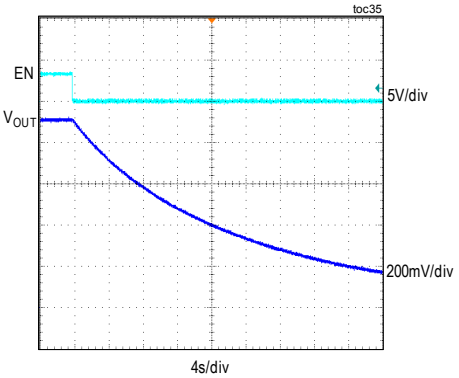
REGULATOR SHUTDOWN
ACTIVE DISCHARGE ENABLED



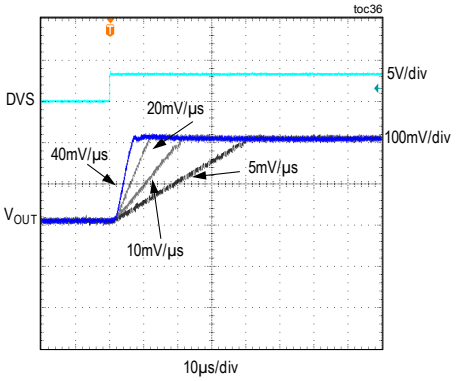
Typical Operating Characteristics (continued)

(Figure 12, V_{IN} = 3.7V, V_{OUT} = 0.9V, V_{IO} = 1.8V, L = TOKO DFE201210U-R24M ,T_A = +25°C, unless otherwise noted.)

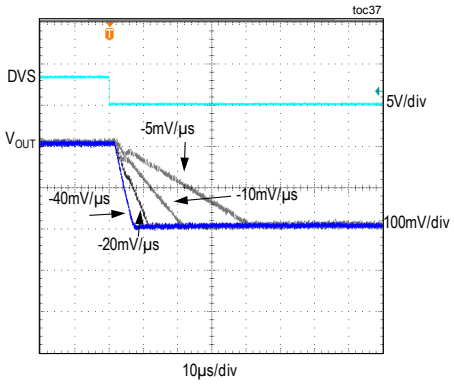
REGULATOR SHUTDOWN
ACTIVE DISCHARGE DISABLED



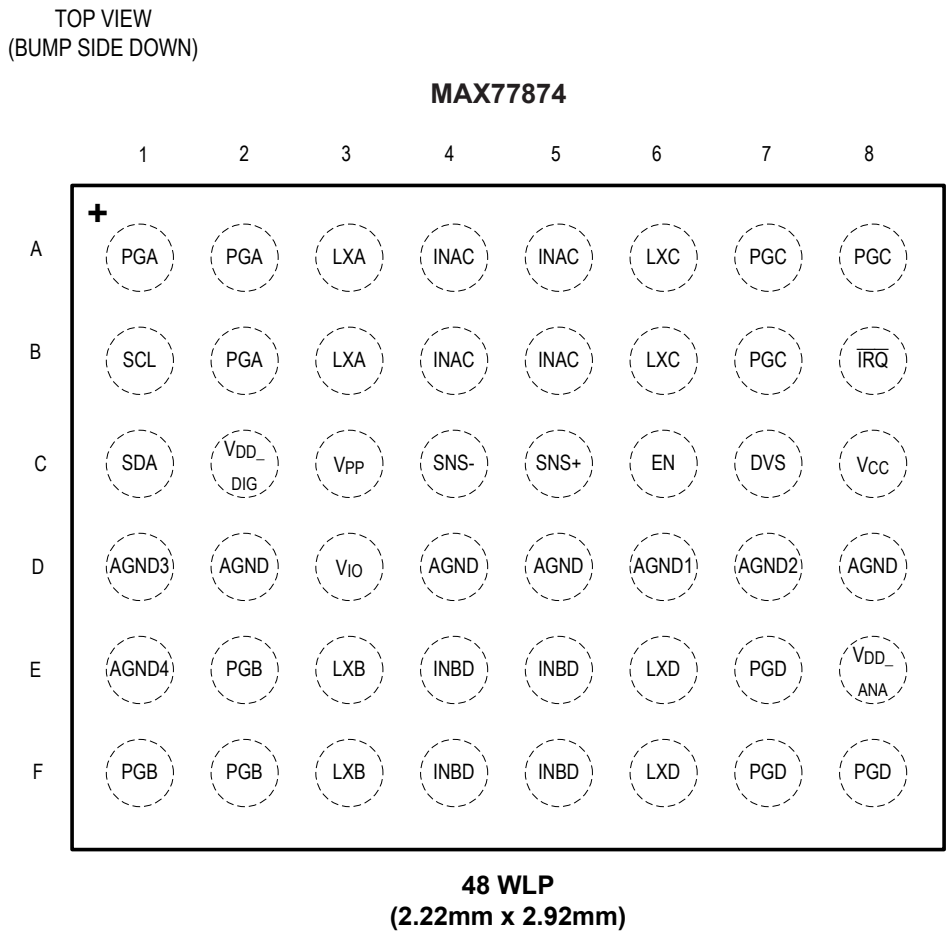
DVS TRANSITION, RISING



DVS TRANSITION, FALLING



Pin Configuration



48 WLP
(2.22mm x 2.92mm)

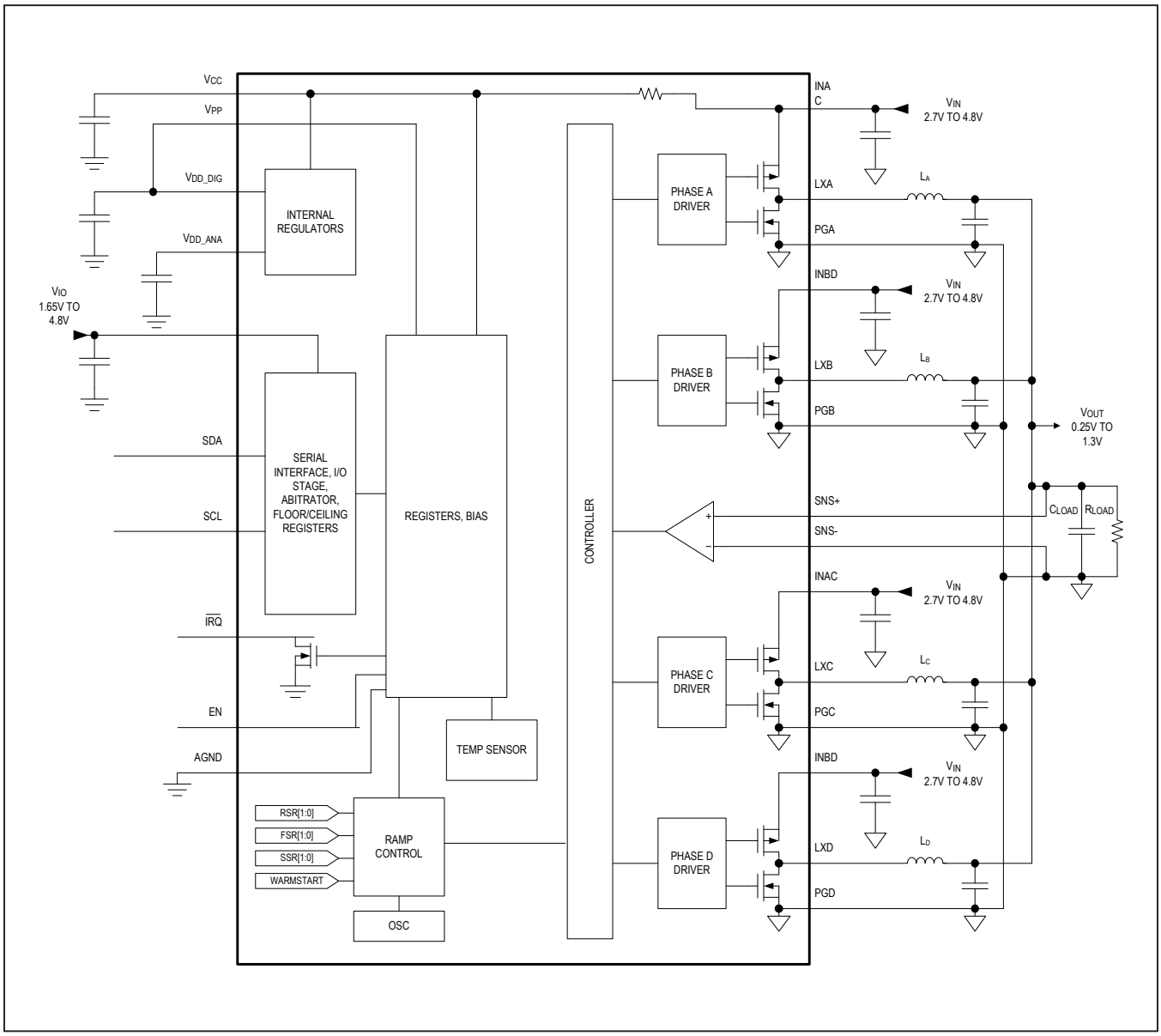
Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A1, A2, B2	PGA	Power GND	GND	GND
A3, B3	LXA	Inductor Connection. Pulled to PG with 100Ω when EN is low and BUCK0ADEN = 1.	IN	Power
A4, A5, B4, B5	INAC	Power Input to Power FETs and Gate Drivers		Power
A6, B6	LXC	Inductor Connection. Pulled to PG with 100Ω when EN is low and BUCK0ADEN = 1.	IN	Power
A7, A8, B7	PGC	Power GND	GND	GND

Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
B1	SCL	Serial Clock Input. SCL accepts a clock frequency of up to 3.4MHz.	V_{DD}	Logic Input
B8	$\overline{IRQ}$	Open-Drain Interrupt Output. High impedance when EN = 0.		Open-Drain Logic Output
C1	SDA	Serial Data Input/Output for I^2C 3.0 Interface	V_{DD}	Logic Input/ Output
C2	V_{DD_DIG}	Digital V_{DD}		Power
C3	V_{PP}	Power Pin for OTP Programming. Connect to V_{DD_DIG}.		Power
C4	SNS-	Negative Differential Voltage Sense Input. SNS- connects to GND at the point-of-load.	GND	Voltage Sense
C5	SNS+	Positive Differential Voltage Sense Input. Connect SNS+ to the output at the point-of-load.	V_{CC}	Voltage Sense
C6	EN	EN Logic Input. Drive high to enable the buck regulator output. Drive low to disable the buck regulator output.	V_{DD}	Logic Input
C7	DVS	DVS Logic Input. Drive high to set the target output voltage to the contents of the VOUT_DVS register. Drive low to set the target output voltage to the contents of the VOUT register.	V_{DD}	Logic Input
C8	V_{CC}	Powers the Battery Level Circuitry of the MAX77874	IN	Power
D1	AGND3	For Internal Use Only. Must be tied to AGND.		GND
D2, D4, D5, D8	AGND	Analog GND. Pin D2 is internally connected to AGND, and can be left unconnected or tied to AGND3/AGND4.	GND	GND
D3	V_{IO}	Power for SCL, SDA Pins. Bringing V_{IO} to GND resets the registers.		Power
D6	AGND1	For Internal Use Only. Must be tied to AGND.		GND
D7	AGND2	For Internal Use Only. Must be tied to AGND.		GND
E1	AGND4	For Internal Use Only. Must be tied to AGND.		GND
E2, F1, F2	PGB	Power GND	GND	GND
E3, F3	LXB	Inductor Connection. Pulled to PG with 100Ω when EN is low and BUCK0ADEN = 1.	IN	Power
E4, E5, F4, F5	INBD	Power Input to Power FETs and Gate Drivers		Power
E6, F6	LXD	Inductor Connection. Pulled to PG with 100Ω when EN is low and BUCK0ADEN = 1.	IN	Power
E7, F7, F8	PGD	Power GND	GND	GND
E8	V_{DD_ANA}	Analog V_{DD}		Power

Block Diagram and Simplified Schematic



Detailed Description—Quad Phase Core Buck Regulator

The MAX77874 is a highly efficient, small step-down converter that operates on an input voltage range of 2.7V to 4.8V and can output up to 16A of current. An integrated I²C interface allows for configuration of output voltage, dynamic voltage scaling (DVS), interrupts, and control mode.

Control Scheme

The quad phase core buck regulator uses Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme. This control scheme handles wide input/output voltage ratios (low duty-cycle applications) with ease and provides immediate response to load transients while maintaining a nearly constant switching frequency. Additionally, the scheme exhibits excellent stability with very high loop-bandwidth for minimal droop/soar and rapid recovery during load transients.

Skip, Turbo Skip, and Forced PWM

When enabled, the quad phase core buck operates in either skip, turbo skip, or forced PWM (FPWM) mode. Program the operating mode using the FPWMEN and TURBO_SKIP bits in the BUCK0CNFG0 register.

Skip mode provides the lowest supply current and highest efficiency at light loads, but has more V_{OUT} droop during load transients than the other modes. Turbo skip mode combines superior transient response (same as FPWM mode) with light load efficiency and supply current nearly as low as skip mode. For this reason, turbo skip mode is the default setting. Forced PWM mode provides near constant switching frequency for noise-sensitive applications, but has higher supply current and lower efficiency at light loads. FPWM has similar transient response to turbo skip mode. See the *Typical Operating Characteristics* section for efficiency, supply current, and load transient response for each operating mode.

The skip and turbo skip modes transition automatically between PWM operation at heavy load and rotational phase spreading at light loads to maintain high efficiency and low output ripple across all loads.

Rotational Phase Spreading

At light loads, proprietary rotational phase spreading switches all four phases in a rotational sequence with extended time at zero current between switching pulses. Compared to phase shedding techniques that disable some phases entirely, rotational phase spreading transitions across varying loads more smoothly with less output ripple and fewer glitches since phases do not get added or dropped. See the output ripple scope waveforms in the *Typical Operating Characteristics* section. To maintain efficiency, the phases are spread further and further apart as loads decrease, with each phase entering a low quiescent current mode when its current is zero and its synchronous rectifier is off.

Enhanced Transient Response

In skip and turbo skip modes, the converter is capable of activating all four phases simultaneously to respond to a load transient. However, in skip mode, the response is not as fast as in turbo skip mode in order to achieve a lower quiescent current. This enhanced transient response (ETR) circuit is not needed in FPWM mode due to the high-loop bandwidth of the controller.

Enable and Soft-Start

V_{IN} and V_{IO} must both be valid to enable the quad phase core buck regulator. See the *Electrical Characteristics* table for the valid voltage ranges. When both voltages are valid, enable the core buck regulator by using the dedicated EN logic input pin or by using the BUCK0EN bit in the BUCK0CNFG0 register. These two control mechanisms are a logic OR function, so setting either the pin or the logic bit to logic 1 enables the regulator.

Once enabled, there is a short delay (see the Startup Ramp Delay in *Electrical Characteristics* table) before the quad phase core buck regulator soft-starts with a linear voltage ramp at the output to control in-rush current and output voltage overshoot. There are a total of five soft-start ramp rates controlled through registers. The default setting is for cold startup, with a slow ramp of 1.25mV/µs. To enable warm startup ramp rates, set the WARMSTART bit in the BUCK0CNFG1 register to logic 1. Then select the desired warm startup ramp rate using the BUCK0SSR[1:0] bits in the BUCK0CNFG1 register. The default setting for warm startup ramp rate is 5mV/µs. The other settings are 10mV/µs, 20mV/µs, and 40mV/µs. Set the desired ramp rate prior to enabling the regulator.

Disable and Active Discharge

When both control mechanisms (BUCK0EN and the EN pin) are logic 0, the buck regulator is off and the output is high impedance.

The quad phase core buck regulator contains on-chip resistors for optional active discharge when disabled. To enable active discharge, set the BUCK0ADEN bit in the BUCK0CNFG0 register to logic 1. When active discharge is enabled and the regulator is disabled, four internal 100Ω resistors are internally connected from LX_ to PG_ (one resistor per phase for an effective discharge resistance of

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25Ω). When the buck is enabled, the discharge resistors are automatically disconnected regardless the state of the BUCK0ADEN bit. Therefore, if active discharge is always desired, the bit can be left enabled (logic 1) without causing additional loading when the buck is enabled.

Full Shutdown

By default, when the buck regulator is disabled, its bias circuits are also disabled to save supply current. When enabling the buck regulator, the bias is automatically enabled and disabled. If faster startup is desired, the bias circuits can be pre-enabled by setting the BIASEN bit in the BUCK0CNFG0 register to logic 1. This comes at the expense of higher supply current when the buck is disabled.

Even when the regulator and the bias are disabled, top-level circuits in the MAX77874 are still alive. The I²C is active and registers can still be read from and written to. Setting V_{IO} = 0V turns off the top-level circuits and results in the lowest possible shutdown current at V_{IN}. Additionally, when V_{IO} = 0V, all registers are reset to their default values.

See the *Typical Operating Characteristics* for a graph of supply current in each operating mode, as well as a scope photo of the faster startup.

Output Voltage Selection

The output voltage is I²C programmable from 0.25V to 1.3V in 5mV steps using the I2C_SD0_VOUT[7:0] bits in the I2C_SD0_VOUT configuration register. The default setting is trimmed to 0x82 = 0.900V. Consult the factory if a different default setting is required. This setting is programmable with the quad phase core buck enabled or disabled.

Dynamic Voltage Scaling (DVS)

The quad phase core buck includes DVS functionality. The DVS output voltage is I²C programmable from 0.25V to 1.3V in 5mV steps using the VBUCKDVS[7:0] bits in the VBUCKDVS configuration register. The default setting is trimmed to 0x82 = 0.900V. Consult the factory if a different default setting is required. The setting is programmable with the quad phase core buck enabled or disabled.

DVS Functionality

The purpose of the DVS function is to allow the buck output voltage to quickly change from one output voltage to another. An I²C write of a register can take several microseconds to a few milliseconds to complete depending upon the I²C speed. The I2C_SDOUT_VOUT[7:0] register controls the buck output voltage when the DVS pin is low. When the DVS pin is high, the buck output voltage is controlled by the VBUCKDVS[7:0] register. See Figure 1. When the I2C_SDOUT_VOUT register is set at a higher voltage than the VBUCKDVS register and the DVS pin transitions from low to high, then the buck output voltage falls to the voltage set by the VBUCKDVS register at a slew rate specified by the BUCK0FSR[1:0] bits in the BUCK0CNFG1 register. When the DVS pin transitions back from high to low, then the buck output voltage rises to the value specified by the I2C_SDOUT_VOUT register at a slew rate specified by the BUCK0RSR[1:0] bits in the BUCK0CNFG1 register.

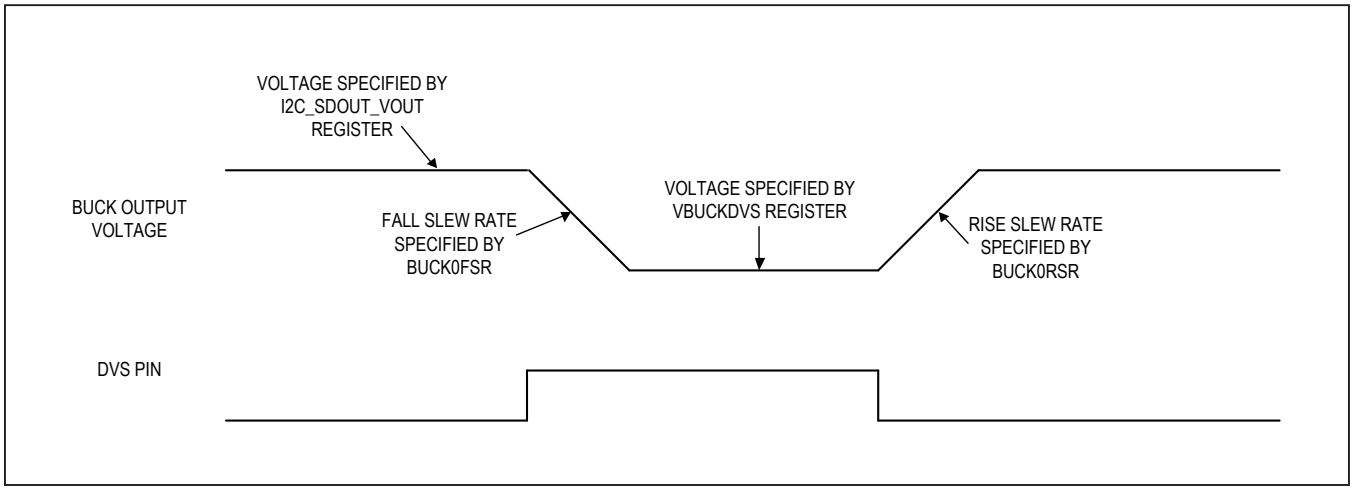


Figure 1. DVS Functionality

DVS and Current Limit

Any time the buck performs a DVS slew to change to a higher output voltage, extra current is required to charge the output capacitors. If the device is operating at maximum output current (16A), there may not be enough headroom to safely perform a DVS operation. Applications that expect a large load current coming and need to change the output voltage to respond to it should perform the DVS before the load step hits to prevent possible overcurrent damage to the inductors. Internal current limits in the buck protect the internal switches and synchronous rectifiers from damage.

Interrupt Events

The device has interrupt capability to monitor the status of the buck converter through the $\overline{IRQ}$ pin, which is an active-low, open-drain output that is typically routed to the processor to allow for quick notification of interrupt events. A pullup resistor is required for this pin.

Power OK

The buck regulator contains an internal, active-low $\overline{POK}$ signal that triggers an interrupt on the $\overline{IRQ}$ pin if the output voltage becomes invalid. This signal must be unmasked with $\overline{POK}$_INTM to assert $\overline{IRQ}$. Note that $\overline{POK}$ is not blanked during DVS slewing or startup.

Thermal Warnings

Two junction temperature thermal warnings, Thermal Alarm 1 and Thermal Alarm 2, trigger an interrupt if the junction temperature rises above their thresholds (T_{J120} and T_{J140}, respectively). These alarms must be unmasked with TJ120C_INTM and TJ140C_INTM to assert $\overline{IRQ}$. Monitor these interrupt events to protect the device from overheating under heavy load conditions.

Thermal Shutdown

If the junction temperature of the device exceeds +165°C, the device shuts down to reduce the temperature. Once the temperature falls approximately 15°C, the device tries to enable with soft-start. This try-retry process continues indefinitely.

Internal Compensation

Regulation loop compensation is on-chip and not user adjustable. The compensation is uniquely trimmed for inductance value and feedback type (remote or local). Although a given compensation can still function when used with the incorrect inductor or feedback type, the optimum transient response and loop stability are achieved when the trim option matches the inductor and feedback type.

Trim Options

The quad phase core buck regulator is factory trimmed using one-time programmable (OTP) registers. Optional versions can be trimmed for current limit, default output voltage settings, inductance value, switching frequency, and local versus remote feedback. See the *Ordering Information* at the end of this data sheet. Consult the factory for optional versions.

Detailed Description—I²C

General Description

The MAX77874 features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77874 acts as a slave-only device, and relies on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported.I²C is an open-drain bus, and therefore, SDA and SCL require pullups.Figure 3 shows the functional diagram for the I²C-based communications controller. For additional information on I²C, refer the I²C bus specification and user manual that is available from NXP (UM10204).

Features

- I²C Revision 3 Compatible Serial Communications Channel
- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)
- 0Hz to 3.4MHz (high-speed mode)
- Does Not Utilize I²C Clock Stretching

I²C System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The MAX77874 I²C-compatible interface operates as a slave on the I²C bus with transmit and receive capabilities.

I²C Interface Power

The MAX77874's I²C interface derives its power from V_{IO}. V_{IO} accepts voltages from 1.65V to 4.8V (V_{IO}). Cycling V_{IO} resets the I²C registers. See *External Components* and Figure 12 for bypass capacitor considerations.

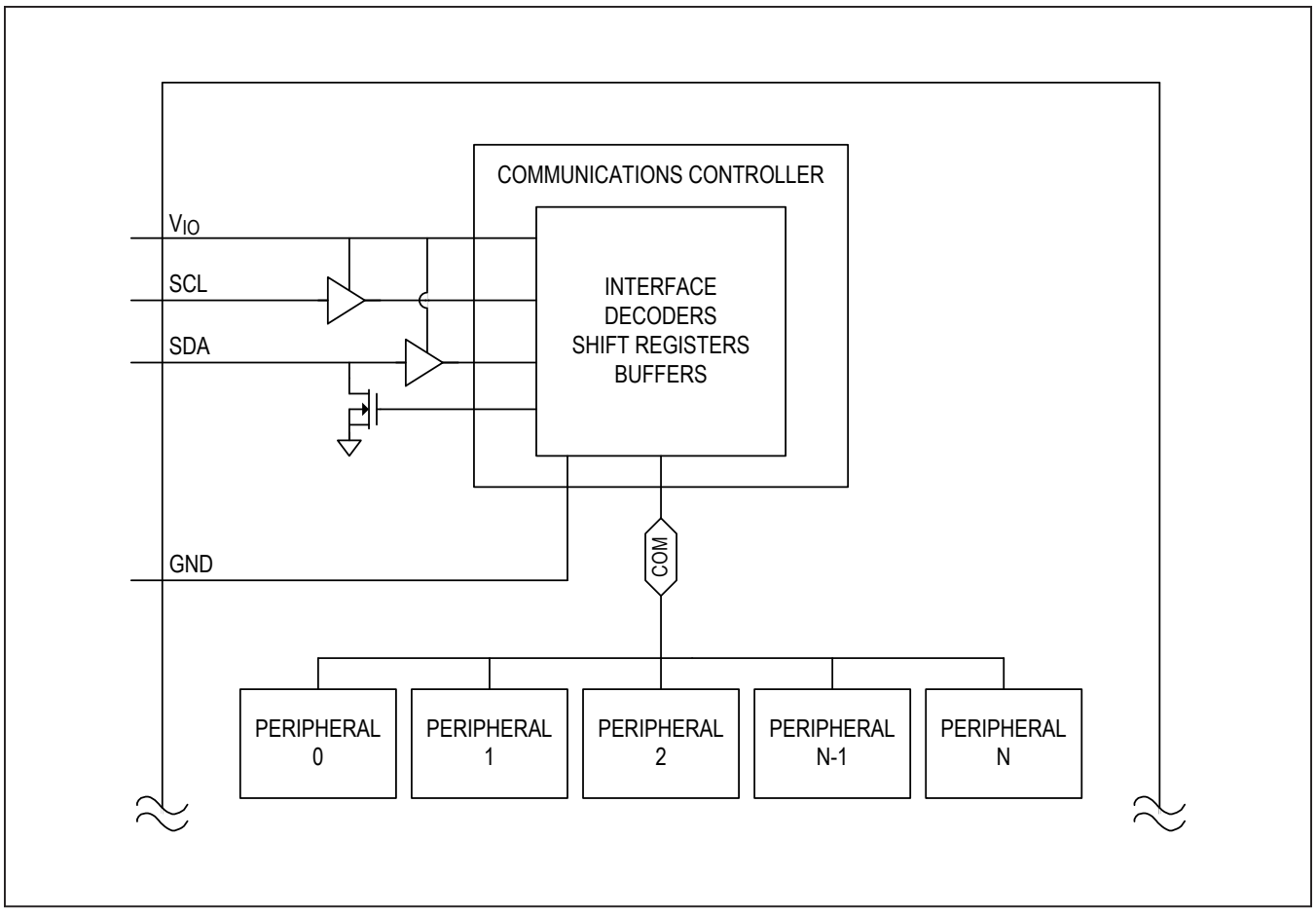


Figure 2. I²C Simplified Block Diagram

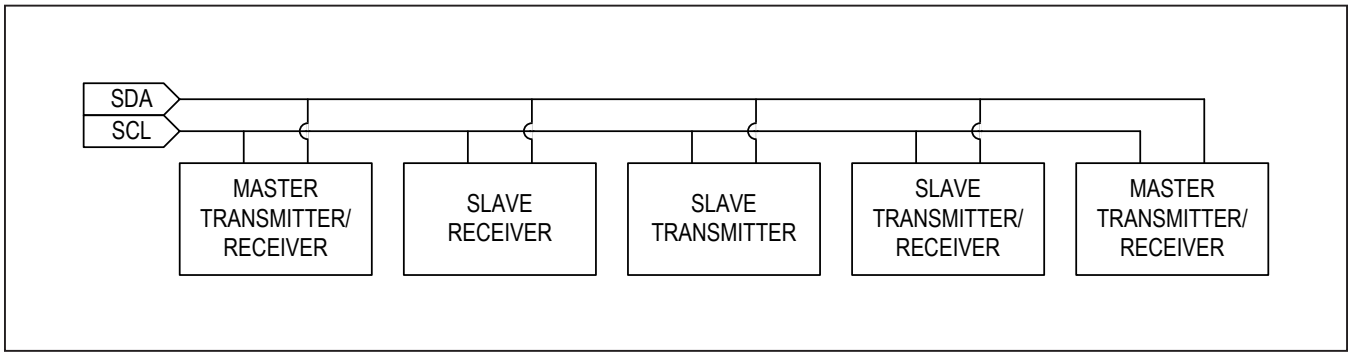


Figure 3. I²C System Configuration

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I²C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 4.

A START condition from the master signals the beginning of a transmission to the MAX77874. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *I²C Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the MAX77874 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

I²C Acknowledge Bit

Both the I²C bus master and the MAX77874 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 5. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

The MAX77874 issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

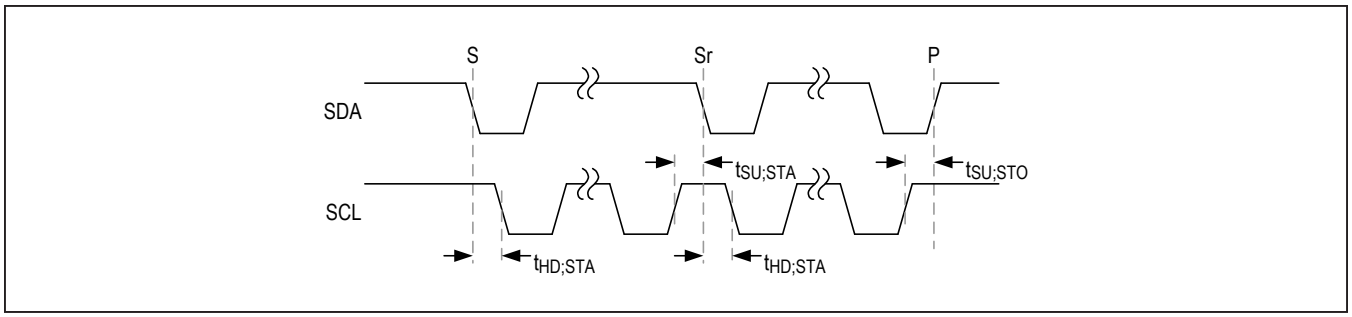


Figure 4. I²C Start and Stop Conditions

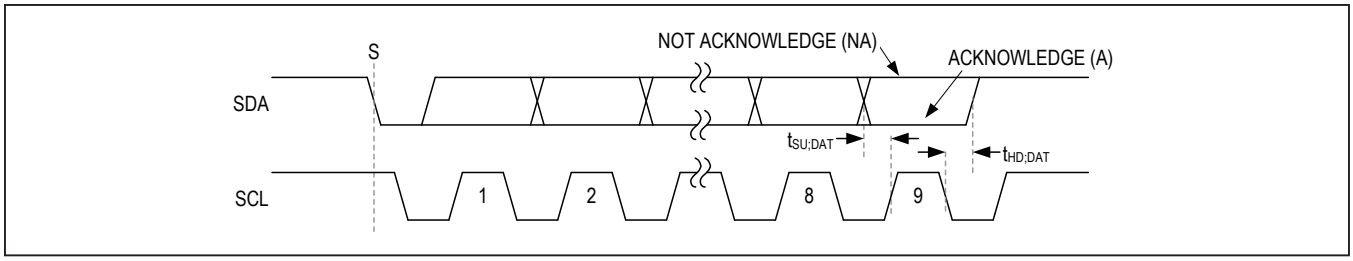


Figure 5. Acknowledge Bit

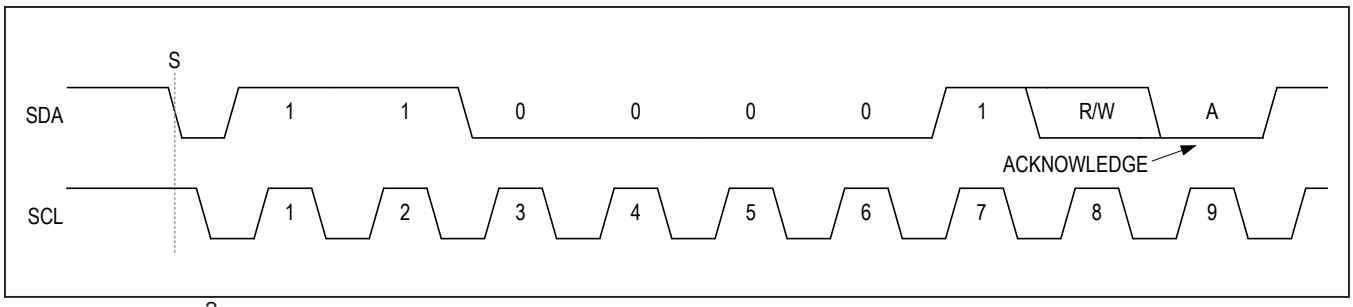


Figure 6. Example I²C Slave Address

Table 1. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address	0x61, 0b 110 0001	0xC2, 0b 1100 0010	0xC3, 0b 1100 0011
Other Addresses*	0x62, 0b 110 0010 0x63, 0b 110 0011 0x64, 0b 110 0100	0xC4, 0b 1100 0100 0xC6, 0b 1100 0110 0xC8, 0b 1100 1000	0xC5, 0b 1100 0101 0xC7, 0b 1100 0111 0xC9, 0b 1100 1001
Test Mode**	0x69, 0b 110 1001 0x6A, 0b 110 1010 0x6B, 0b 110 1011 0x6C, 0b 110 1100	0xD2, 0b 1101 0010 0xD4, 0b 1101 0100 0xD6, 0b 1101 0110 0xD8, 0b 1101 1000	0xD3, 0b 1101 0011 0xD5, 0b 1101 0101 0xD7, 0b 1101 0111 0xD9, 0b 1101 1001

**These addresses are acknowledged, but are for internal use only. Do not use any other I²C devices with these addresses on the same bus.*

***When test mode is unlocked, additional addresses are acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.*

I²C Slave Address

The I²C controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 6. The OTP address is factory programmable for one of two options. See Table 1. All slave addresses not mentioned in the Table 1 are not acknowledged.

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77874 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX77874 does not implement the I²C specifications general call address. If the MAX77874 sees the general call address (0b0000_0000), it does not issue an acknowledge.

I²C Device ID

The MAX77874 does not support the I²C device ID feature.

I²C Communication Speed

The MAX77874 is compatible with all 4 communication speed ranges as defined by the Revision 3 I²C specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I2C revision 3.0 specification (UM10204) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the *I2C Specification* section. The major considerations with respect to the MAX77874:

- The I2C bus master use current source pullups to shorten the signal rise.
- The I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the MAX77874 inputs filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I2C Communication Protocols* section.

I2C Communication Protocols

The MAX77874 supports both writing and reading from its registers.

Writing to a Single Register

Figure 7 shows the protocol for the I2C master device to write one byte of data to the MAX77874. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data
8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

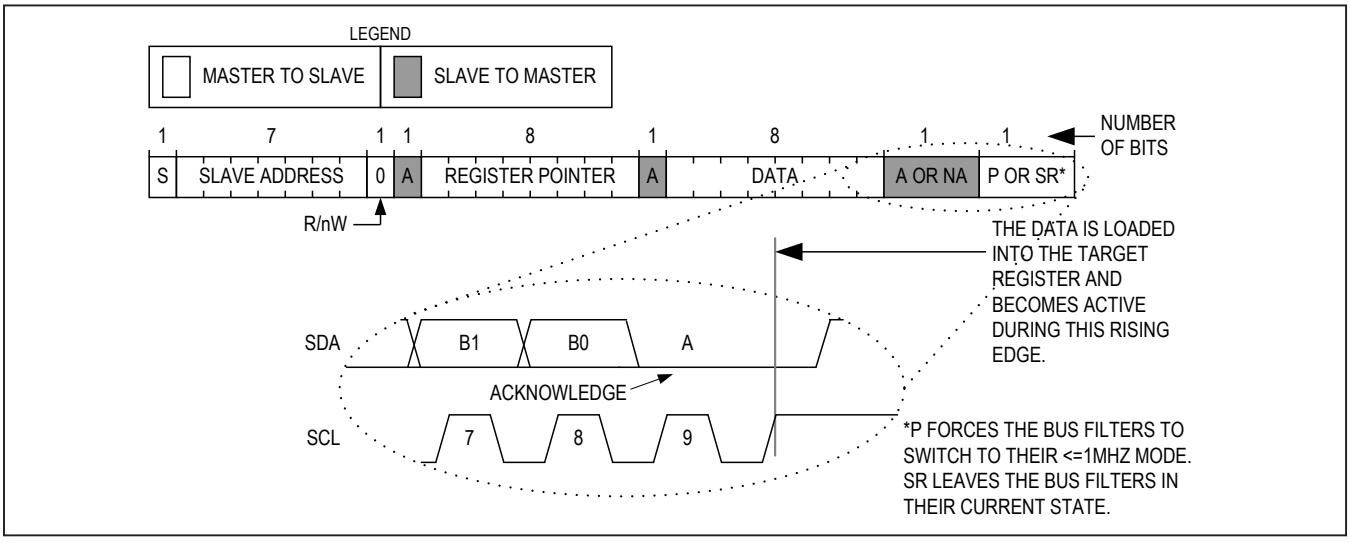


Figure 7. Writing to a Single Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 8 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a data byte.
- The slave acknowledges the data byte. The next rising edge on SDA load the data byte into its target register and the data becomes active.
- Steps 6 to 7 are repeated as many times as the master requires.
- During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

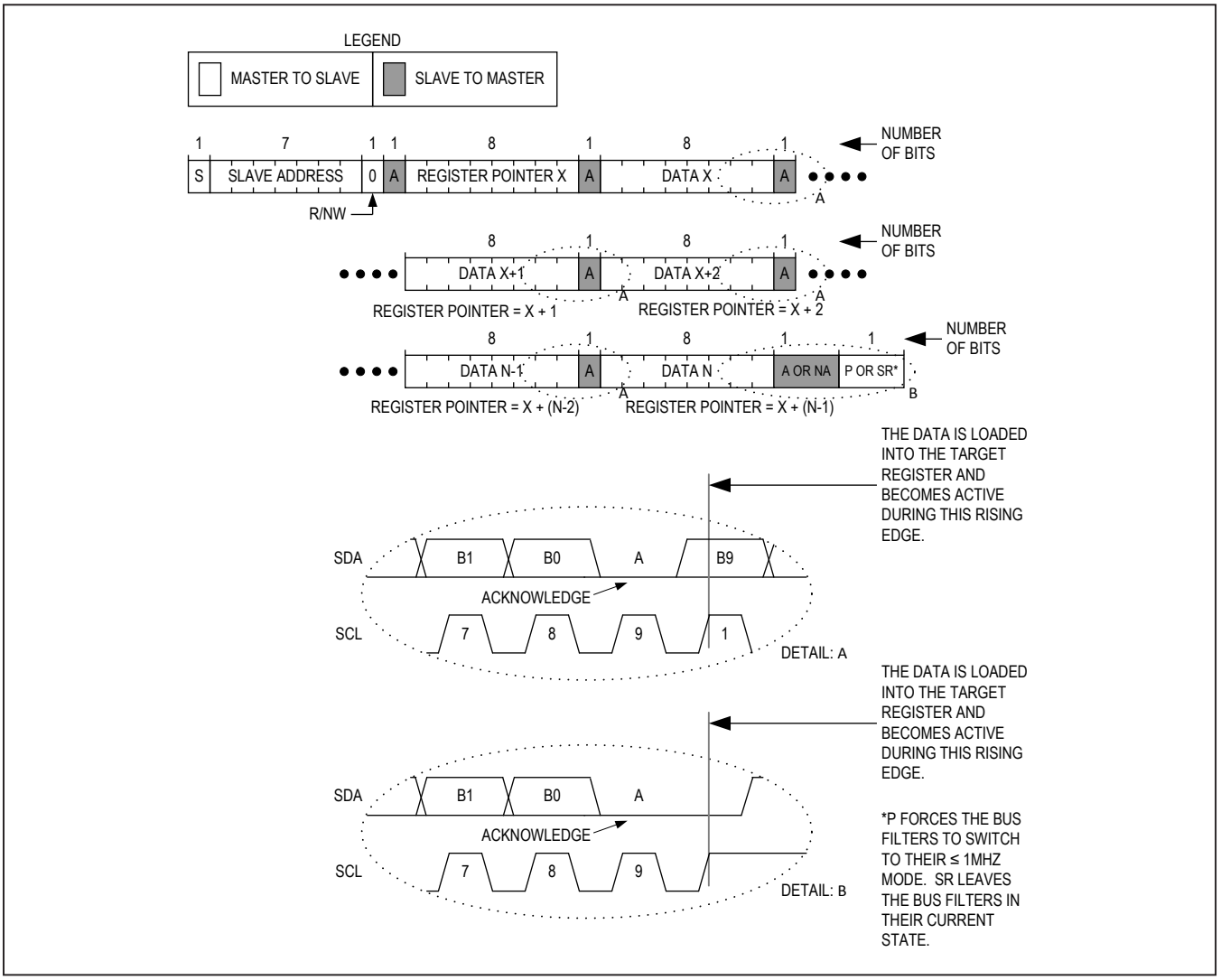


Figure 8. Writing to Sequential Registers X to N

Reading from a Single Register

Figure 9 shows the protocol for the I2C master device to read one byte of data to the MAX77874. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a repeated start command (Sr).
- The master sends the 7-bit slave address followed by a read bit (R/W = 1).
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- The master issues a not acknowledge (nA).
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the MAX77874 receives a stop it does not modify its register pointer.

Reading from Sequential Registers

Figure 10 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires, it issues a not acknowledge (nA) and a stop (P) to end the transmission.

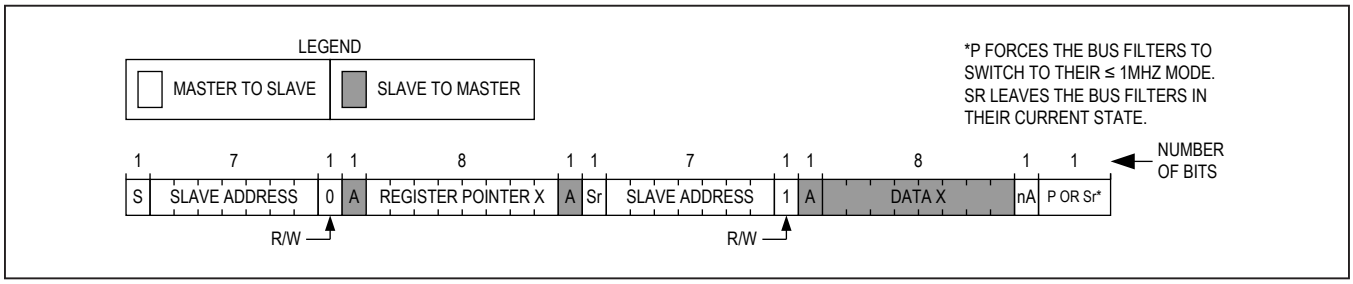


Figure 9. Reading from a Single Register with the Read Byte Protocol

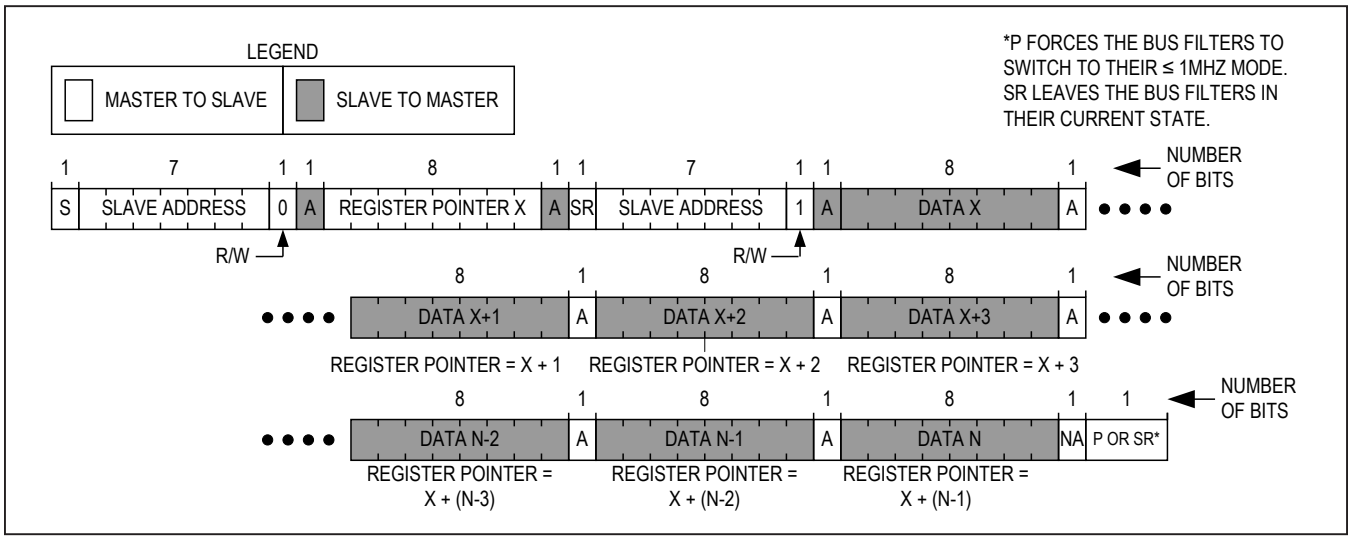


Figure 10. Reading Continuously from Sequential Registers X to N

The continuous read from sequential registers protocol is as follows:

- The master sends a start command (S).
- The master sends the 7-bit slave address followed by a write bit (R/W = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a repeated start command (Sr).
- The master sends the 7-bit slave address followed by a read bit (R/W = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
- The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
- Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the the MAX77874 receives a stop it does not modify its register pointer.

Engaging HS Mode for Operation Up to 3.4MHz

Figure 11 shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

- Begin the protocol while operating at a bus speed of 1MHz or lower
- The master sends a start command (S).
- The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
- The addressed slave issues a not acknowledge (nA).
- The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high speed mode, use repeated start (Sr).

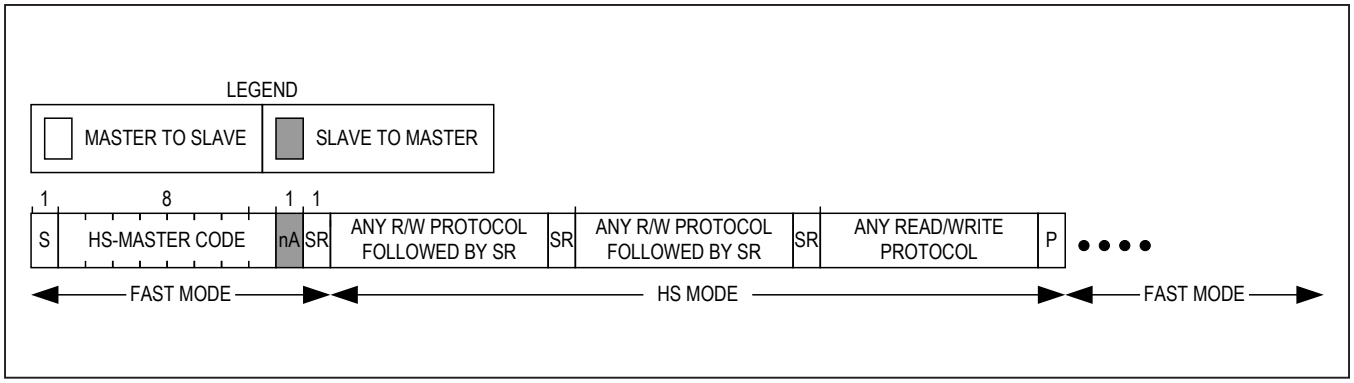


Figure 11. Engaging HS Mode

Registers

Top-Level Registers

I²C Slave Addresses

7-BIT ADDRESS	WRITE ADDRESS	READ ADDRESS
0x61	0xC2	0xC3

Other addresses available by request through trim.

Top-Level Register Map

ADDRESS	NAME	TYPE	ACCESS	RESET	B7	B6	B5	B4	B3	B2	B1	B0
0x00	CHIP_ID	Data	R	0x03	CHIP_ID[7:0]							
0x01	CHIP_REV	Status	R	0x00	CHIP_REV[7:0]							

CHIP_ID Data Register

REGISTER NAME	CHIP_ID
Slave Address	0xC3 R
Register Address	0x00
Access Type	Read only
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:0	CHIP_ID[7:0]	Chip Identification	0x03

CHIP_REV Status Register

REGISTER NAME	CHIP_REV
Slave Address	0xC3 R
Register Address	0x01
Access Type	Read only
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:0	CHIP_REV[7:0]	Chip Revision	0x00

Buck Regulator Registers

I²C Slave Addresses

7-BIT ADDRESS	WRITE ADDRESS	READ ADDRESS
0x61	0xC2	0xC3

Other addresses available by request through trim.

Buck I²C Register Map

ADDRESS	NAME	TYPE	ACCESS	RESET	B7	B6	B5	B4	B3	B2	B1	B0
0x10	BUCK0CNFG0	Config	R/W	0x02	FPWM EN	FSREN	BUCK0 ADEN	RSVD	BUCK0 EN	BIAS EN	TURBO_ SKIP	RSVD
0x11	BUCK0CNFG1	Config	R/W	0x00	BUCK0 SSR[1:0]		BUCK0 RSR[1:0]		BUCK0 FSR[1:0]		WARM START	RSVD
0x14	BUCK0INT	Intrrpt	R/C	0x00	RSVD	RSVD	RSVD	RSVD	RSVD	nPOK_ INT	TJ140C_ INT	TJ120C_ INT
0x15	BUCK0INTM	Mask	R/W	0xFF	RSVD	RSVD	RSVD	RSVD	RSVD	nPOK_ INTM	TJ140C_ INTM	TJ120C_ INTM
0x16	BUCK0INTS	Status	R	0x00	RSVD	RSVD	RSVD	RSVD	RSVD	nPOK_S	TJ140C_S	TJ120C_S
0x21	I2C_SD0_ VOUT	Config	R/W	0x82	I2C_SD0_VOUT[7:0]							
0x24	VBUCKDVS	Config	R/W	0x82	VBUCKDVS[7:0]							

BUCK0CNFG0 Configuration Register

REGISTER NAME	BUCK0CNFG0
Slave Address	0xC2 W/0xC3 R
Register Address	0x10
Access Type	Read/Write
Reset Condition	Global Shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7	FPWMEN	Forced-PWM Enable 0 = Normal (automatic skip at light loads, PWM at heavy loads) 1 = Forced-PWM at all loads	0
6	FSREN	Falling Slew Rate Enable 0 = Skip during slew down 1 = Forced PWM during slew down	0
5	BUCK0ADEN	Buck Active Discharge Enable 0 = Active discharge disabled 1 = Active discharge enabled	0
4	RSVD	Reserved	0
3	BUCK0EN	Buck Enable 0 = Disabled 1 = Enabled Buck0 can be enabled by this bit or by the EN pin.	0

BIT	BIT NAME	DESCRIPTION	DEFAULT
2	BIASEN	Bias Enable 0 = Disabled 1 = Enabled, preenable the bias even when Buck0 is disabled. Bias is automatically enabled whenever Buck0 is enabled.	0
1	TURBO_SKIP	Turbo-Skip Enable 0 = Disabled 1 = Enabled	1
0	RSVD	Reserved	0

BUCK0CNFG1 Configuration Register

REGISTER NAME	BUCK0CNFG1
Slave Address	0xC2 W/0xC3 R
Register Address	0x11
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:6	BUCK0SSR[1:0]	Buck startup slew rate when WARMSTART = 1. 00 = 5mV/µs 01 = 10mV/µs 10 = 20mV/µs 11 = 40mV/µs	00
5:4	BUCK0RSR[1:0]	Buck rising slew rate for DVS. 00 = 5mV/µs 01 = 10mV/µs 10 = 20mV/µs 11 = 40mV/µs	00
3:2	BUCK0FSR[1:0]	Buck falling slew rate for DVS. 00 = -5mV/µs 01 = -10mV/µs 10 = -20mV/µs 11 = -40mV/µs	00
1	WARMSTART	Warm vs. cold startup slew rate. 0 = 1.25mV/µs (cold startup) 1 = use BUCK0SSR[1:0] (warm startup)	0
0	RSVD	Reserved	0

BUCK0INT Interrupt Register

REGISTER NAME	BUCK0INT
Slave Address	0xC3 R
Register Address	0x14
Access Type	Read/clear
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:3	RSVD	Reserved	00000
2	nPOK_INT	$\overline{POK}$Interrupt 0 = Output voltage remained OK since cleared. 1 = Output voltage was not OK since cleared.	0
1	TJ140C_INT	TJ140C Interrupt 0 = Junction temperature remained less than +140ºC since cleared. 1 = Junction temperature was more than +140ºC since cleared.	0
0	TJ120C_INT	TJ120C Interrupt 0 = junction temperature remained less than +120ºC since cleared. 1 = junction temperature was more than +120ºC since cleared.	0

BUCK0INTM Mask Register

REGISTER NAME	BUCK0INTM
Slave Address	0xC2 W/0xC3 R
Register Address	0x15
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:3	RSVD	Reserved	11111
2	nPOK_INTM	$\overline{POK}$Interrupt Mask 0 = Interrupt not masked. 1 = Interrupt is masked.	1
1	TJ140C_INTM	TJ140C Interrupt Mask 0 = Interrupt not masked. 1 = Interrupt is masked.	1
0	TJ120C_INTM	TJ120C Interrupt Mask 0 = Interrupt not masked. 1 = Interrupt is masked.	1

BUCK0INTS Status Register

REGISTER NAME	BUCK0INTS
Slave Address	0xC3 R
Register Address	0x16
Access Type	Read only
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:3	RSVD	Reserved	00000
2	nPOK_S	$\overline{POK}$Status 0 = Output voltage is OK. 1 = Output voltage is not OK.	0

BIT	BIT NAME	DESCRIPTION	DEFAULT
1	TJ140C_S	TJ140C Status 0 = Junction temperature is less than +140ºC. 1 = Junction temperature is more than +140ºC.	0
0	TJ120C_S	TJ120C Status 0 = Junction temperature is less than +120ºC. 1 = Junction temperature is more than +120ºC.	0

I2C_SD0_VOUT Configuration Register

REGISTER NAME	I2C_SD0_VOUT
Slave Address	0xC2 W/0xC3 R
Register Address	0x21
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:0	I2C_SD0_ VOUT[7:0]	Buck output voltage control setting when DVS logic input is 0 (driven low). 0x00 = 0.250V 0x01 = 0.255V 0x02 = 0.260V …….. 0x82 = 0.900V …….. 0xD1 = 1.295V 0xD2 = 1.300V Codes beyond 0xD2 clamp the output voltage to 1.300V.	0x82

VBUCKDVS Configuration Register

REGISTER NAME	VBUCKDVS
Slave Address	0xC2 W/0xC3 R
Register Address	0x24
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:0	VBUCKDVS[7:0]	Buck output voltage control setting when DVS logic input is 1 (driven high). 0x00 = 0.250V 0x01 = 0.255V 0x02 = 0.260V …….. 0x82 = 0.900V …….. 0xD1 = 1.295V 0xD2 = 1.300V Codes beyond 0xD2 clamp the output voltage to 1.300V.	0x82

Register Reset

The MAX77874 does not have a manual reset input logic pin. However, when V_{IO} = 0V (through system reset or V_{IO} being switched off), the buck is disabled and all registers are reset to their default settings.

Applications Information—Quad Phase Core Buck Regulator

External Components

Input Capacitor Selection

Bypass each IN_ to GND with a 10µF (40µF total) capacitor with 0402 case size, X5R dielectric, and 6.3V rating. Ceramic capacitors with X5R are recommended due to their small size, low ESR, and small temperature coefficients.

Local Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and ensure regulation loop stability. The recommended minimum output capacitance per phase is 2x 22µF (44µF per phase) capacitors with 0402 case size, X5R dielectric, and 4V rating. Ceramic capacitors with X5R are recommended due to their small size, low ESR, and small temperature coefficients.

Remote Output Capacitor Selection

Decouple the remote sense lines with a minimum of 3x 22µF (66µF total) capacitors with 0402 case size, X5R dielectric, and 4V rating. Ceramic capacitors with X5R are recommended due to their small size, low ESR, and small temperature coefficients. Additional capacitance may be necessary to satisfy the microprocessor's own requirements.

Bias Capacitor Selection

Bypass each bias supply to ground with a 1µF, 0201 case size ceramic capacitor (V_{CC}, V_{IO}, V_{DD_DIG}, V_{DD_ANA}). Ceramic capacitors with X5R are recommended due to their small size, low ESR, and small temperature coefficients.

Inductor Selection

The MAX77874B is trimmed for inductors with nominal inductance of 220nH or 240nH. Choose an inductor with saturation current rating of at least the peak current limit of the regulator. Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load currents for the system. Consider the DC resistance (DCR), AC resistance (ACR), and case size of the inductor. Smaller inductors can have larger DCR and ACR. Inductors with lower DCR and lower ACR at 2MHz tend to provide better efficiency. Typically, metric 2012, 2016, and 2520 case size inductors are suitable.

PCB Layout Considerations

Due to fast switching and high currents, careful routing of traces is required. Minimize trace length between the ICs and the inductor, input capacitors, and output capacitors. Keep these critical traces short and wide. Ensure that the input and output capacitor ground connections are as close together as possible and connected to PG_, and route the AGND and PG_ traces directly to the ground plane. When routing the SNS+ and SNS- traces, keep the traces sufficiently short to minimize parasitic inductance, and connect SNS- to the ground terminal of the output capacitors, and SNS+ to the positive terminal of the output capacitors. Use intermediate grounding planes to shield the SNS+ and SNS- traces from noisy switching paths. The MAX77874 EV kit and Figure 12 serve as guidelines for layout. Keep all input and output capacitors as close as possible to the device, with the exception of the remote capacitors that should be closer to the load.

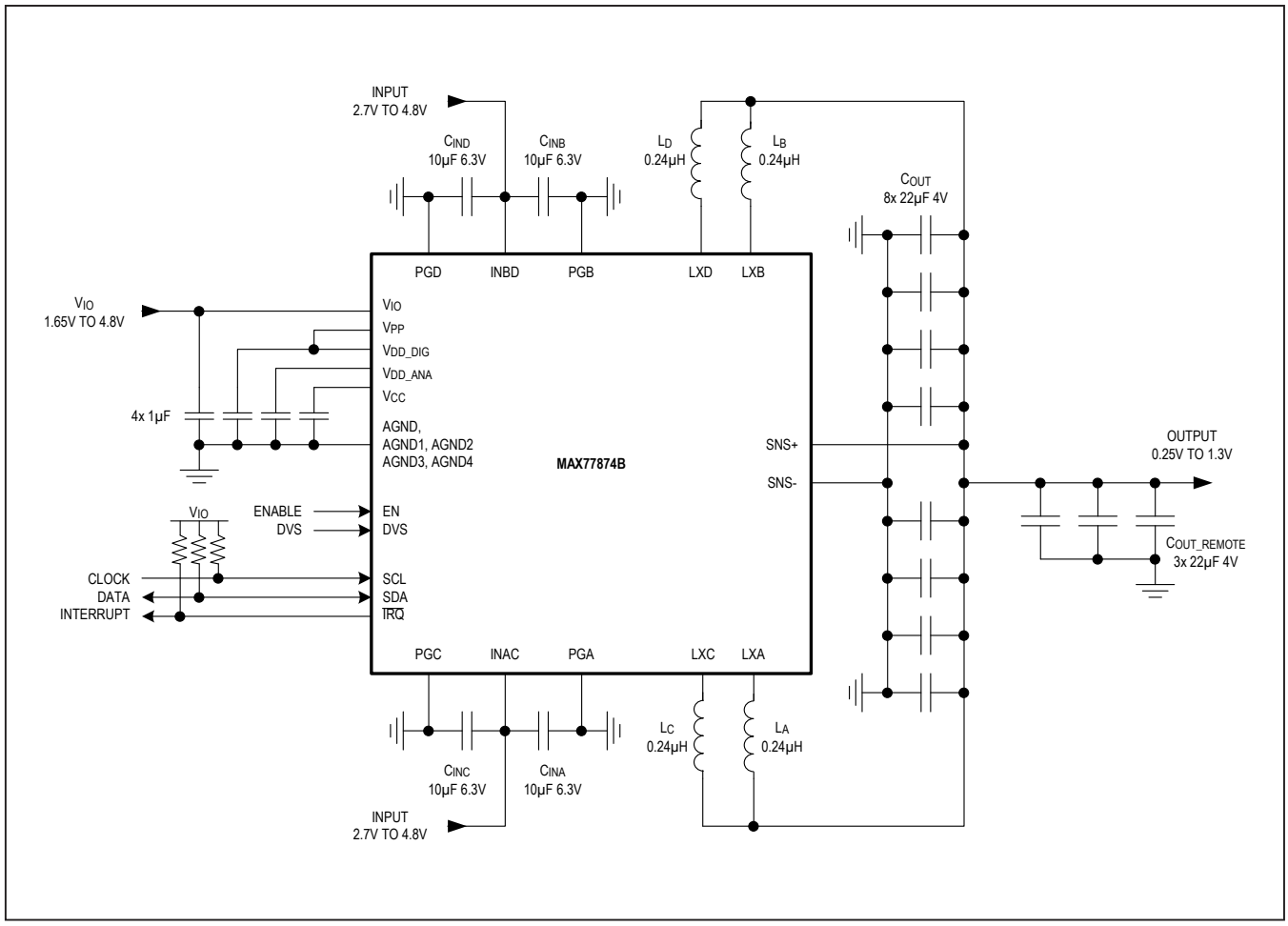


Figure 12. Typical Applications Circuit to Power a Multicore CPU/GPU Processor Up to 16A with MAX77874

Benefits and Features (continued)

- High Efficiency
  - 89% Peak Efficiency at $3.7V_{IN}$, $0.9V_{OUT}$, $3.5A_{OUT}$
  - Auto Rotational Phase Spreading at Light Loads
- Flexible Features
  - I^2C Interface and EN, DVS, $\overline{IRQ}$ Logic Pins
  - Programmable Soft-Start and DVS Ramp Rates
  - Two Thermal Alarms and POK Interrupts
- Small Solution Size
  - $37mm^2$ Total Area with 2012-Size Inductors
  - $41mm^2$ Total Area with 2016-Size Inductors
  - 2.22mm x 2.92mm WLP Package (0.35mm pitch)

Ordering Information

PART NUMBER*	I_{OUT} (A)	DEFAULT V_{OUT} (DVS)	INDUCTOR	f_{SW} (MHz)	FEEDBACK	TEMP RANGE	PIN-PACKAGE
MAX77874BEWM+T	16	0.9V (0.9V)	220nH/240nH	2	Local	-40°C to +85°C	48 WLP

**Contact factory for other versions.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/16	Initial release	—

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