MP3221

2.7A, 1.2MHz, High-Efficiency Step-Up Converter With Input Disconnect

DESCRIPTION

The MP3221 is a 1.2MHz frequency, 6-pin TSOT23 current mode step up converter intended for small, low power applications. The device can step up three-cell alkaline, NiCd, and NiMH batteries, or a single-cell Li-on battery up to 6V. It is capable of delivering 1A output current at 5V with a supply voltage of 3V.

The MP3221 provides the internal soft start and compensation to minimize the external component count and help producing a compact solution. It integrates a FAULT driver for external PMOS to disconnect the output from input when the part shuts down or in output short circuit condition. This disconnect feature allows the output to be completely discharged, thus allowing the part to draw less than 1μA off current in shutdown mode.

The MP3221 is available in a small 6-pin TSOT23 package.

FEATURES

- Integrated 88mΩ Power MOSFET
- 270μA Quiescent Current
- 2.5V to 6V Input Voltage
- 3V to 6V Output Voltage
- 1.2MHz Fixed Switching Frequency
- Internal 2.7A Switch Current Limit
- Integrated Input Disconnect Driver
- Internal Soft Start and Compensation
- True Output Disconnect from Input
- Under Voltage Lockout
- Short-Circuit Protection
- Over-Temperature Protection
- Available in a 6-Pin TSOT23-6 Package

APPLICATIONS

- Single-Cell Lion Battery or Three-Cell Alkaline, NiCd, or NiMH Battery Based Products
- Portable Media Players
- Wireless Peripherals
- Tablets and Smart Phones

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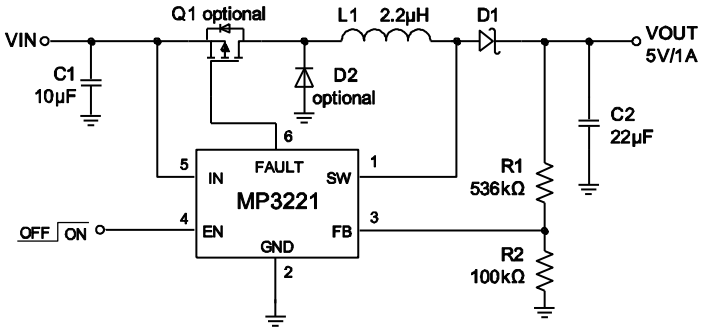
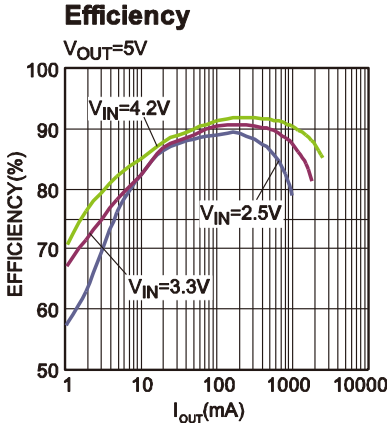
TYPICAL APPLICATION





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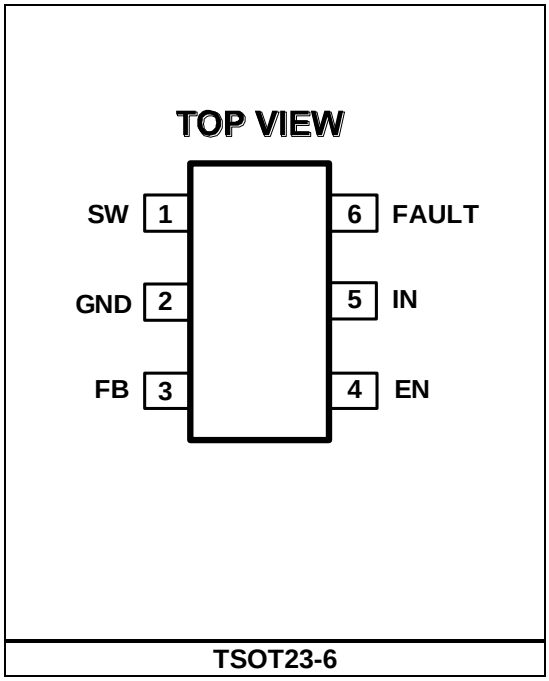
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3221GJ	TSOT23-6	AFB

* For Tape & Reel, add suffix –Z (e.g. MP3221GJ–Z);

PACKAGE REFERENCE



TSOT23-6

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW} ..... –0.3V(-2V for <10nS)to +8V(9V for <10nS)
All Other Pins..... –0.3V to +6.5 V
Continuous Power Dissipation(T_A = +25°C) (2) 0.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.5V to 6V
Output Voltage V_{OUT}..... 3V to 6V
Operating Junction Temp.(T_J) .. -40°C to +125°C

Thermal Resistance (4)

		θ_{JA}	θ_{JC}	
TSOT23-6	…….	220	110	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		2.5		6	V
IN Under Voltage Lockout	V_{UVLO}	V_{IN} Rising	2.0	2.2	2.4	V
IN Under Voltage Lockout Hysteresis				225		mV
Shutdown Current	I_{SD}	V_{EN} = 0V			0.15	µA
Quiescent Current		V_{FB} = 0.85V, No Switching		270		µA
Switching Frequency	f_{SW}		1	1.2	1.4	MHz
Minimum On time(5)	$T_{ON,MIN}$			80		ns
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.6V	90			%
EN Input High Voltage		$V_{EN\ H}$	1.3			V
EN Input Low Voltage		$V_{EN\ L}$			0.5	V
EN Input Bias Current		V_{EN} = 5V		4		µA
FB Voltage	V_{FB}	V_{EN} = 5V	0.780	0.796	0.812	V
FB Input Bias Current		V_{FB} = 0.82V	–50	–10		nA
FAULT Detection Threshold Voltage	$V_{FB-AULT}$	Step-up Converter Fails	110	150	185	mV
FAULT Pull Down Current	I_{FAULT}		85	115	145	µA
FAULT Pin Output Low Voltage		V_{FB}=0.6V, I=30µA			0.3	V
SW On Resistance	$R_{DS\ (ON)}$			88		mΩ
SW Current Limit		Duty Cycle = 40%	2.7	3.7	5.2	A
SW Leakage		V_{SW} = 5V			1	µA
Thermal Shutdown(5)	T_{SHDN_TH}			150		°C
Thermal Shutdown Hysteresis(5)	T_{SHDN_HYS}			20		°C

Notes:

5) Guaranteed by engineering sample characterization. not production tested.

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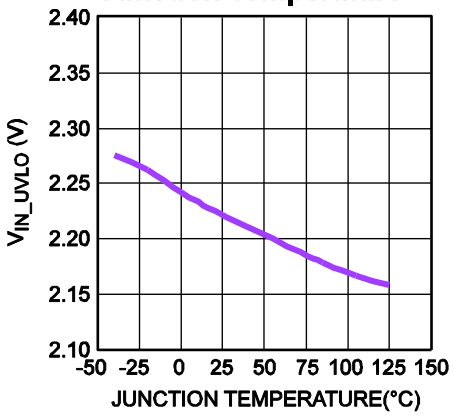
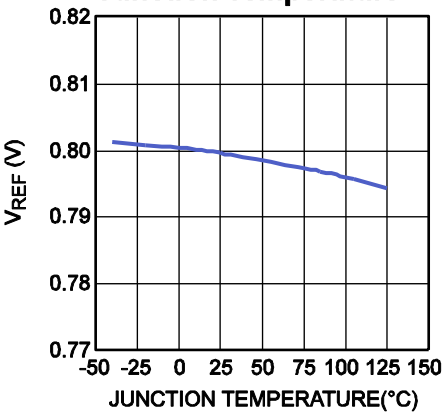
TYPICAL CHARACTERISTICS

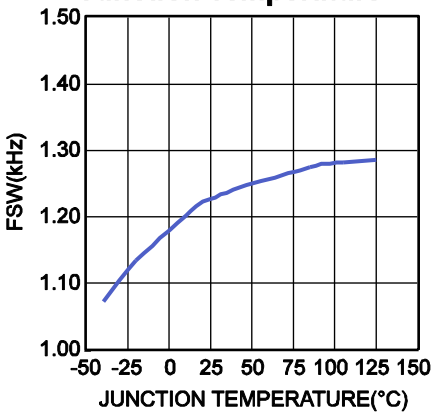
Vin UVLO vs. Junction Temperature



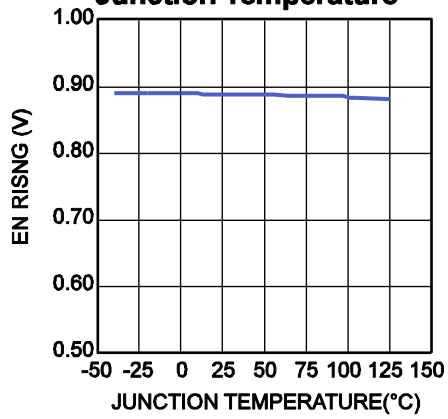
Vref vs. Junction Temperature



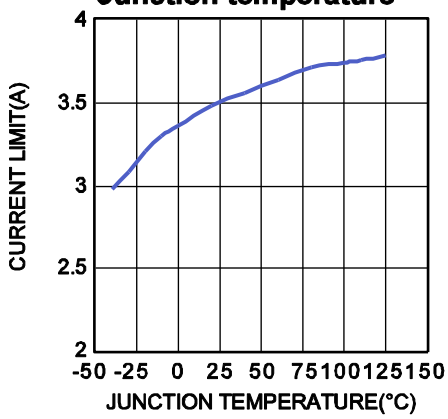
Fsw vs. Junction Temperature



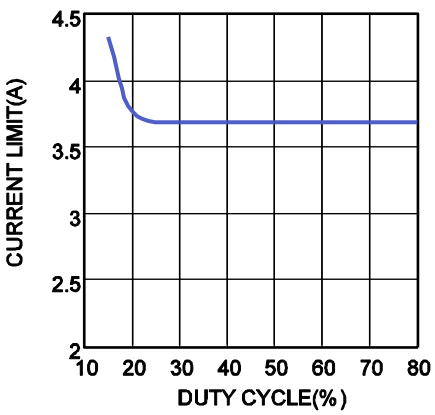
EN Rising vs. Junction Temperature



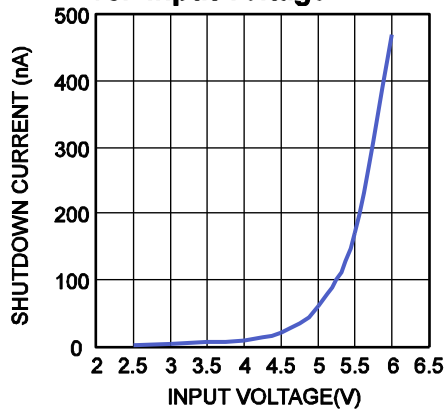
Current limit vs. Junction temperature



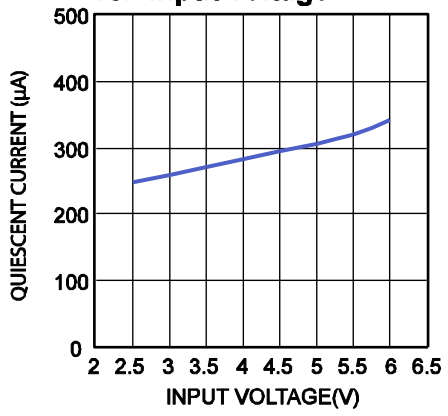
Current limit vs. Duty



Shutdown current vs. Input voltage



Quiescent current vs. Input voltage



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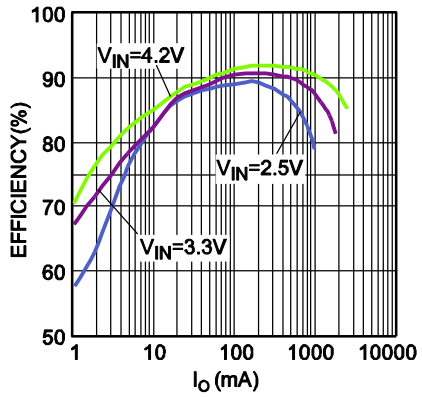
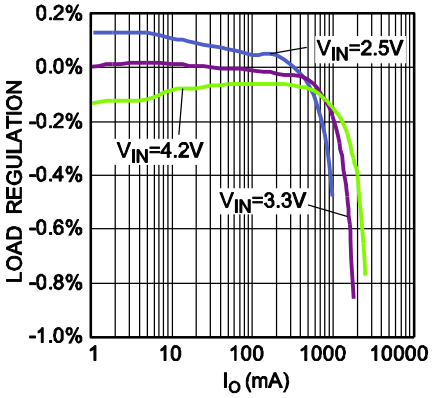
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

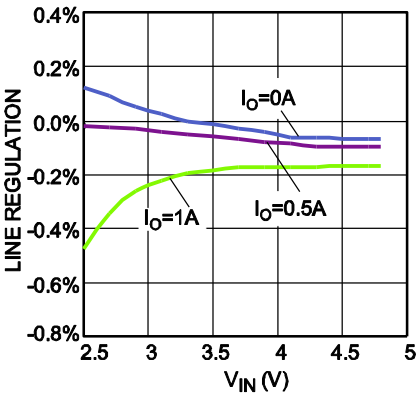
Efficiency



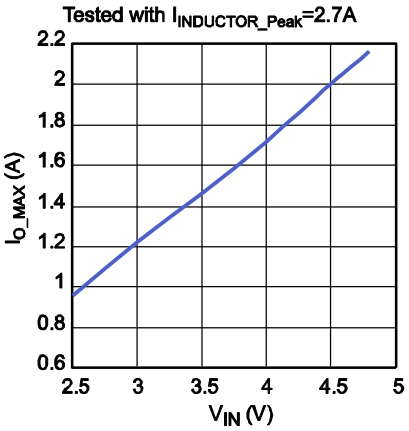
Load regulation



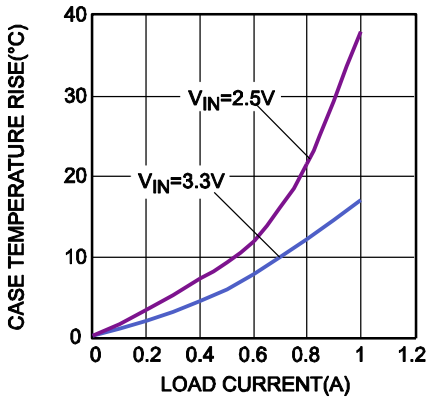
Line regulation



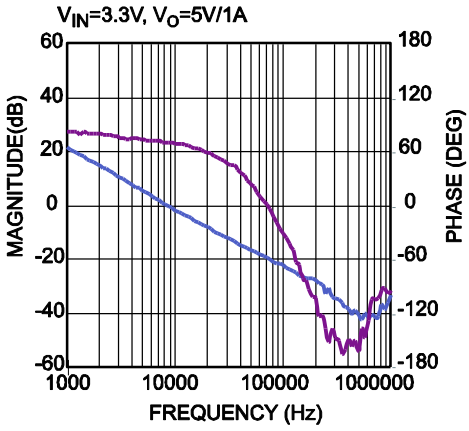
Max. Output Current Vs. Vin Voltage



Case temperaure Rise vs. Load current



Magnitude and phase vs. Frequency



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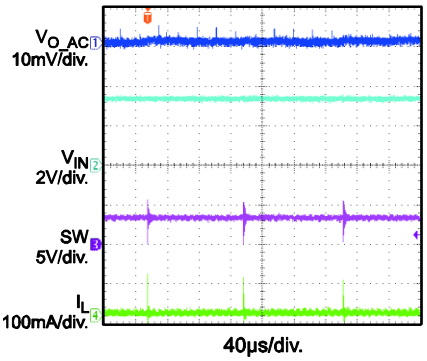
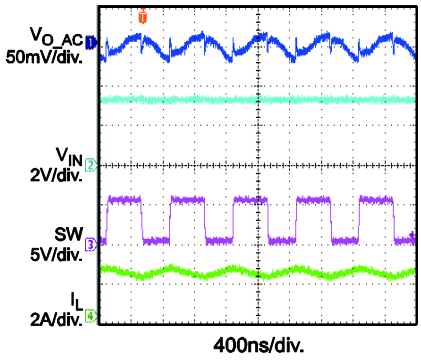
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

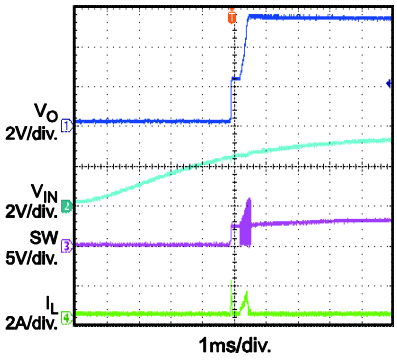
Steady state
V_{IN} = 3.3V, V_O = 5V/0A



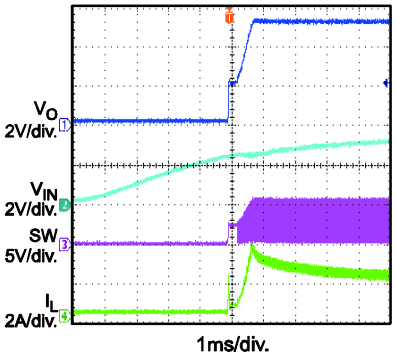
Steady state
V_{IN} = 3.3V, V_O = 5V/1A



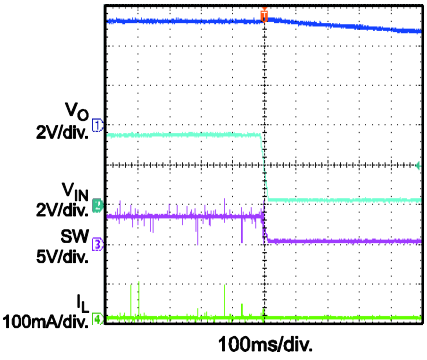
VIN startup
V_{IN} = 3.3V, V_O = 5V/0A



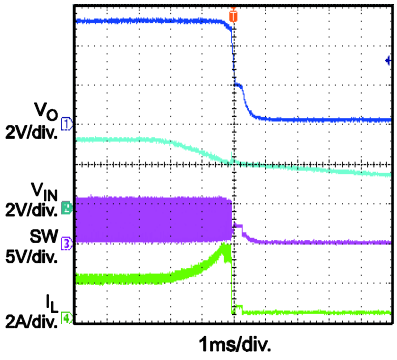
VIN startup
V_{IN} = 3.3V, V_O = 5V/1A



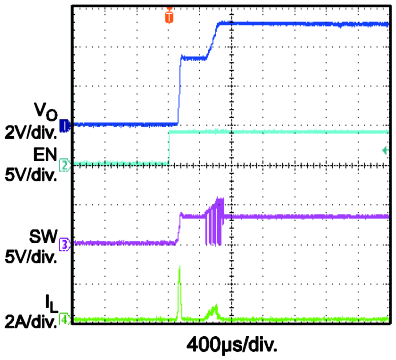
VIN shutdown
V_{IN} = 3.3V, V_O = 5V/0A



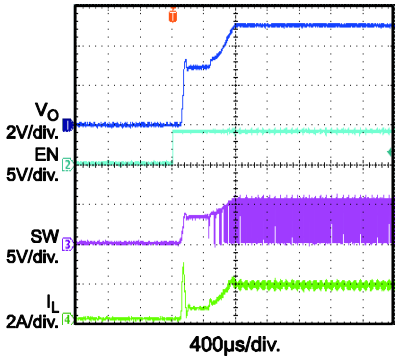
VIN shutdown
V_{IN} = 3.3V, V_O = 5V/1A



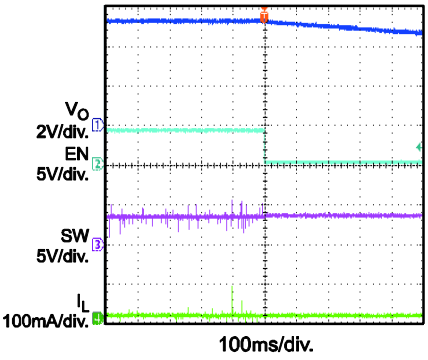
En startup
V_{IN} = 3.3V, V_O = 5V/0A



En startup
V_{IN} = 3.3V, V_O = 5V/1A



EN shutdown
V_{IN} = 3.3V, V_O = 5V/0A



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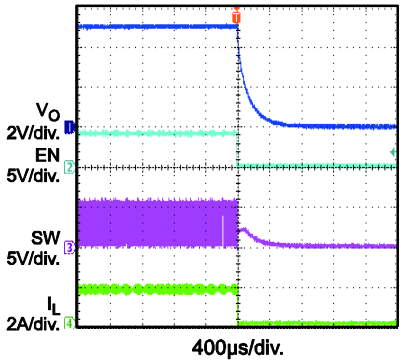
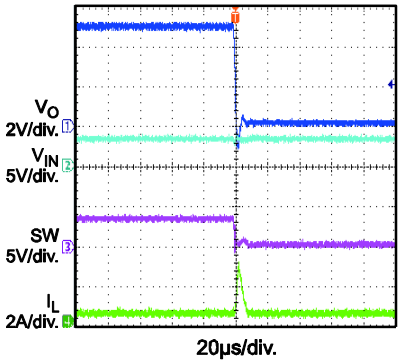
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

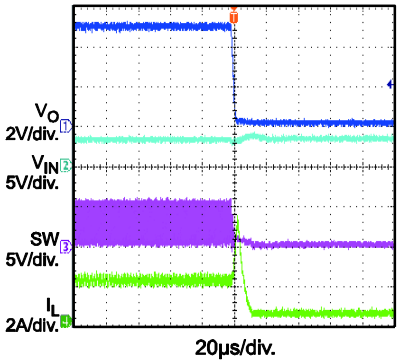
EN shutdown
V_{IN} = 3.3V, V_O = 5V/1A



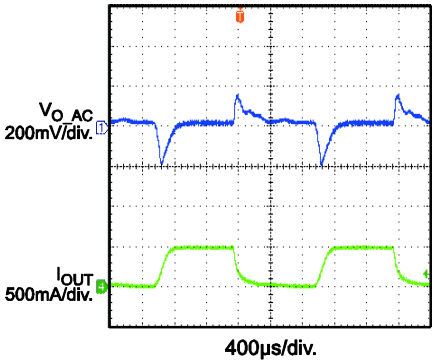
SCP entry
V_{IN} = 3.3V, V_O = 5V/0A to short



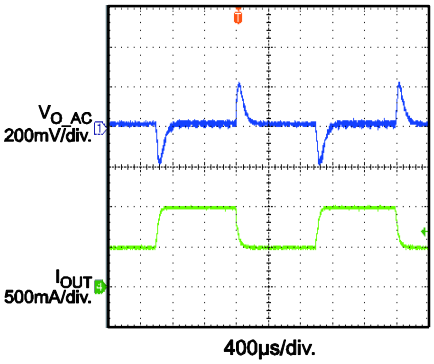
SCP entry
V_{IN} = 3.3V, V_O = 5V/1A to short



Load transient
V_{IN} = 3.3V, V_O = 5V,
I_O=0A->0.5A I ramp=10mA/µs



Load transient
V_{IN} = 3.3V, V_O = 5V,
I_O=0.5A->1A I ramp=10mA/µs



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PIN FUNCTIONS

Pin #	Name	Description
1	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW.
2	GND	Ground.
3	FB	Feedback Input. The FB voltage is 0.796V. Connect a resistor divider to FB.
4	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	IN	Input Supply Pin. Must be locally bypassed.
6	FAULT (6)	Fault Disconnection Switch Gate Output. When the system starts up normally, this pin smoothly turns on the external PMOS. When the MP3221 is disabled or in fault condition, the external PMOS is turned off to disconnect the input and output.

Notes:

6) Fault pin only can protect circuits in SCP condition after parts startup.

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FUNCTION DIAGRAM

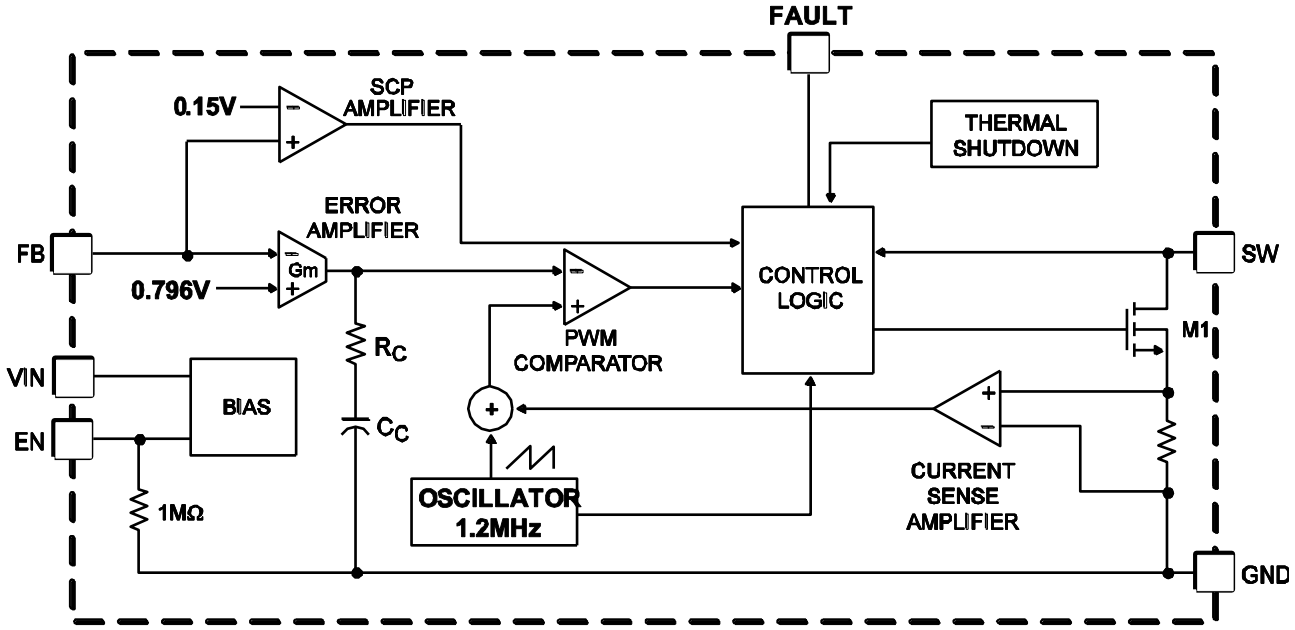

Figure 1: Functional Block Diagram

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OPERATION

The MP3221 uses a constant frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin.

The operation of the MP3221 can be understood by referring to the block diagram of Figure 1. At the start of each oscillating cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50%, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power MOSFET is turned off.

The voltage at the output of the error amplifier is an amplified version of the difference between the band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases, which results in more current flow through the power MOSFET, thus increasing the power delivered to the output.

Start-Up Sequence

When MP3221 is enabled, the FAULT pin drives the external Fault Disconnection PMOS to turn on slowly. After the FAULT pin voltage drops to VIN -1.8V, parts works and checks all fault condition, if they are all in function. MP3221 will boost the output voltage to the expect voltage controlled by the internal soft start.

Protection Operation

MP3221 has short-circuit protection function by turning off the external PMOS after parts startup. When FB voltage drops to 150mV due to the SCP occurs or any other factors, FAULT pin voltage will pull up quickly by MP3221`s internal logic. Then the PMOS will disconnect to isolate input and output. This function won't act before V_{FAULT} drop to V_{IN} -1.8V, MP3221 will also check other safety limits including UVLO and OTP.

V_{OUT} Disconnect from V_{IN}

To prevent the battery from discharging, the FAULT pin of MP3221 will drive and turn off the external PMOS to disconnect V_{OUT} from the battery when the part is in shut down mode. It also can disconnect output from input while the output is shorted to GND, thus help protect battery and circuit.

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APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are good choice for input decoupling and it should be located as close as possible to the IN and GND pin. Add a ceramic capacitor larger than 10μF close to the IC.

Selecting the Output Capacitor

The output capacitor requires a minimum capacitance value of 22μF at the programmed output voltage to ensure stability over the full operating range. A higher capacitance value may be required to lower the output ripple and also the transient response. Low ESR capacitors, such as X5R- or X7R-type ceramic capacitors, are recommended. Assuming that the ESR is zero, estimate the minimum output capacitance to support the ripple in the CCM mode as:

$$C_O \geq \frac{I_O \times (V_{OUT} + V_F - V_{IN(MIN)})}{f_S \times (V_{OUT} + V_F) \times \Delta V}$$

Where:

V_{OUT} = output voltage

$V_{IN(MIN)}$ = Minimum Input voltage

V_F= Diode Forward voltage

I_O= Output current

f_S = Switching frequency

ΔV= Acceptable output ripple

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-Channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

A 2.2μH inductor is recommended for most applications. However, a more exact inductance value can be calculated. A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN} \times (V_{OUT} + V_F - V_{IN})}{(V_{OUT} + V_F) \times f_{SW} \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, and η is efficiency.

Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. To reduce power loss due to diode forward voltage and recovery current, use a Schottky diode with the MP3221. The diode should be rated for a reverse voltage equal to or higher than the output voltage. The average current rating must be higher than the maximum load current, and the peak current rating must be higher than the peak inductor current.

Selecting the PMOS

The MP3221 is capable of driving P-Channel power MOSFETS to disconnect input and output. The critical parameter selection of a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Maximum current $I_{D(MAX)}$
3. On-resistance $R_{DS(ON)}$
4. Total gate charge, Q_G.

Ideally, the off-state voltage across the MOSFET is equal to the input voltage. $V_{DS(MAX)}$

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should be greater than 1.5 times of the input voltage.

The maximum current through the power MOSFET happens when the input voltage is minimum and the output power is maximum.

The maximum Average current is the input current. The ID(max) should be greater than 1.5 times the input current.

The on resistance of the MOSFET determines the conduction loss. It is smaller, it is better.

The Qg of PMOS should be well designed to avoid the triggering of SCP protection during start-up. Since V_{GATE} is pulled down with 115μA through the Fault pin, the SCP function is enabled after V_{GATE} drops to V_{IN}-1.8V. With higher Qg, the time to pull V_{GATE} from V_{IN} to V_{IN}-1.8V is longer, and output voltage can be charged to higher voltage. If Qg is low, V_{GATE} will be pulled down quickly, and feedback V_{FB} is still lower than 150mV when V_{GATE} drops to V_{IN}-1.8V, then SCP function may be triggered and the start-up will fail.

A 3.3nF cap between gate-to-source of PMOS is recommended if V_{OUT} can not rise up before V_{FAULT} drops to V_{IN} -1.8V due to large output cap.

PCB Layout Considerations

Layout is important, especially for switching power supplies with high switching frequencies; poor layout results in reduced performance, EMI problems, resistive loss, and even system instability. Following the rules below can help ensure a stable layout design:

1. All components must be placed as close to the IC as possible. Keep the path between L1, D1, C_{OUT}, and IC-GND extremely short for minimal noise and ringing.
2. C_{IN} must be placed close to the IN pin for best decoupling.
3. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace.
4. The ground return of C_{IN} and C_{OUT} should be tied close to the GND pin.

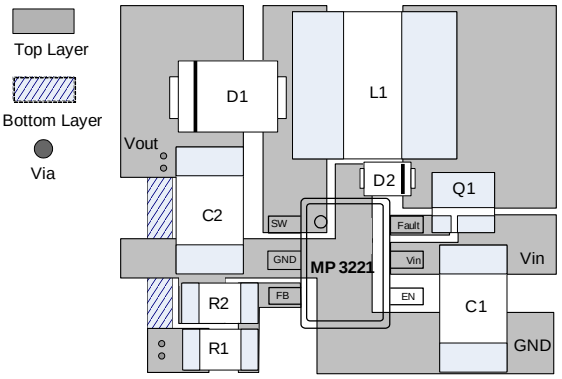

Figure 2: Layout

Notes:

Refer to SCH on page 1.

Design example

Below is a design example following the application guidelines for the following Specifications:

Table 1: Design Example

V_{IN}	2.5V-4.8V
V_{OUT}	5V
F_{SW}	1.2MHz

The typical application circuit for VOUT = 5V in Figure 3 shows the detailed application schematic, and is the basis for the typical performance and circuit waveforms. For more detailed device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

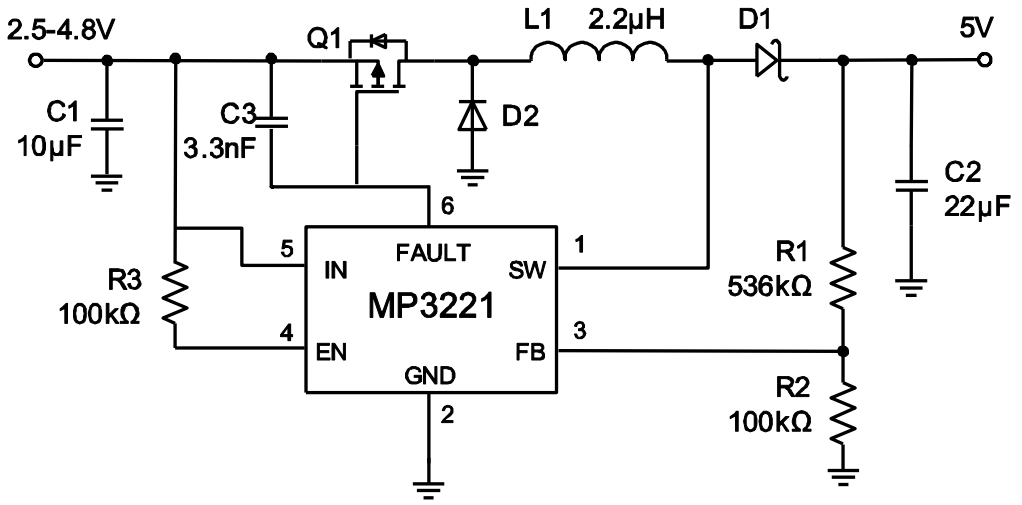

Figure 3: V_{IN}=2.5-4.8V, V_{OUT} =5V/1A, with Input/Output Disconnection

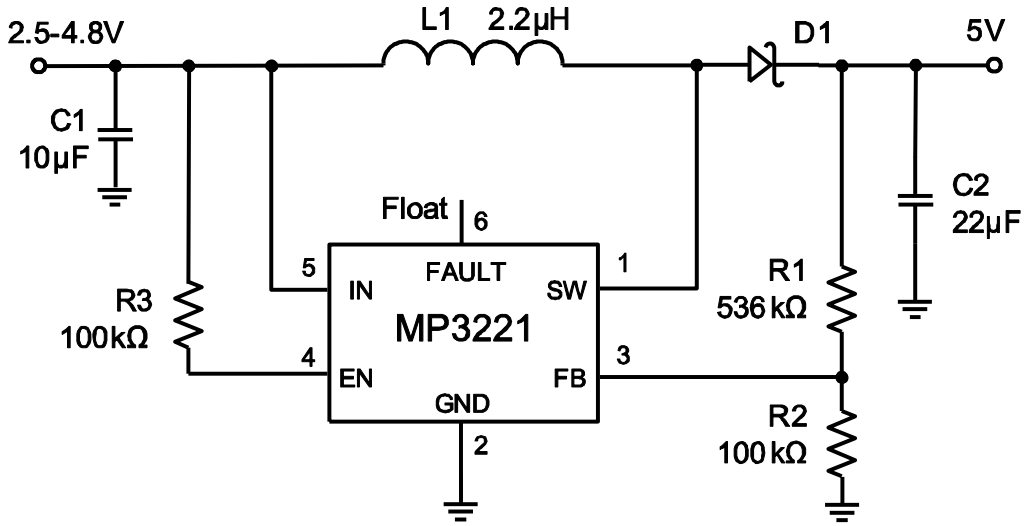

Figure 4: V_{IN} =2.5-4.8V, V_{OUT}=5V/1A, without Input/Output Disconnection

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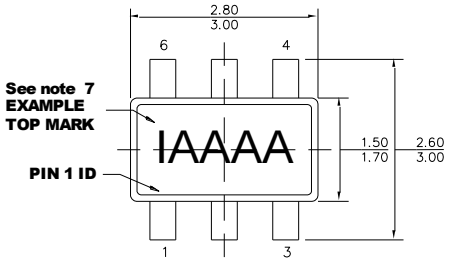
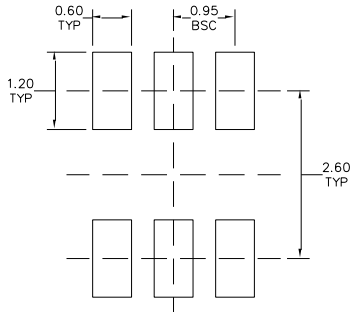
PACKAGE INFORMATION

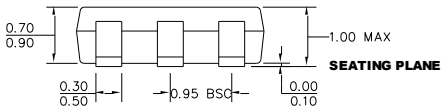
TSOT23-6



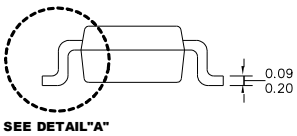
TOP VIEW



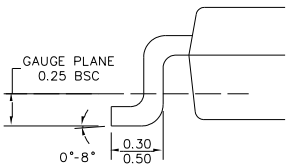
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK).

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