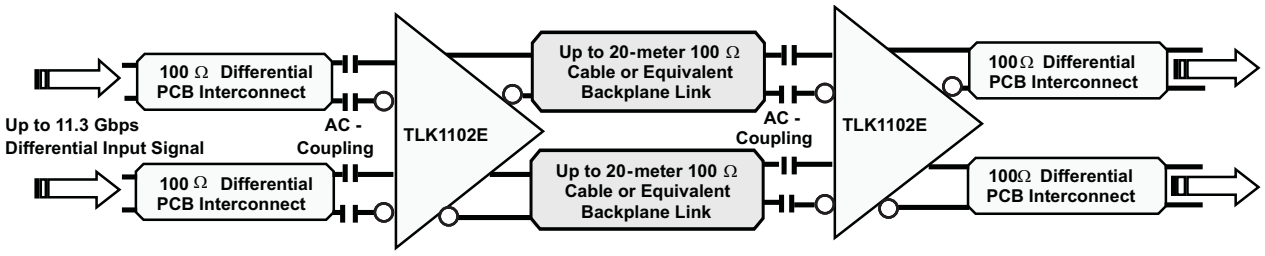
11.3-Gbps Dual-Channel Cable and PC Board Equalizer

FEATURES

- Dual-Channel Multi-Rate Operation up to 11.3Gbps
- Two-Wire Serial Interface (with 8 Selectable Device Addresses) or Device Pin Control
- Compensates for up to 30dB Loss on the Receive Side and up to 7dB Loss on the Transmit Side at 5.65GHz
- Adjustable Input Equalization Level
- Adjustable Output De-Emphasis: 0 - 7dB
- Adjustable Input Bandwidth: 4.5 - 11GHz
- Adjustable CML Output Swing: 225 - 1200mV$_{p-p}$
- Loss of Signal (LOS) Detection
- Output Disable with Selectable Auto-Squelch Function
- Output Polarity Switch
- Excellent High Frequency Input and Output Return Loss
- Surface Mount Small Footprint 4-mm × 4-mm 24-Pin QFN Package
- Single 3.3V Supply
- -40°C to 100°C Operation (Lead Temperature)

APPLICATIONS

- High-Speed Links In Communication and Data Systems
- Backplane, Daughtercard, and Cable Interconnects for 10GE, 8GFC, 10GFC, 10G SONET, SAS, SATA, and InfiniBand
- QSFP, SFP+, XFP, SAS, SATA, and InfiniBand Active Cable Assemblies



DESCRIPTION

The TLK1102E is a versatile and flexible high-speed dual-channel equalizer for applications in digital high-speed links with data rates up to 11.3Gbps.

The TLK1102E can be configured in many ways through its two-wire serial interface, available through the SDA and the SCL pins, to optimize its performance. The configurable parameters include the output de-emphasis settable from 0 to 7dB, the output differential voltage swing settable from 225 to 1200mV$_{p-p}$, the input equalization level settable for 0 to 20 meters of 24-AWG twinaxial cable, 0 to 40 inches of FR-4 PCB interconnect, or equivalent interconnect (see Table 1), the input filter bandwidth settable from 4.5 to 11GHz, and the LOS (loss of signal) assert voltage level.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Alternatively, the TLK1102E can be configured using its configuration pins in two modes selectable using the MODE pin. In Pin Control Mode 1 (see Figure 2b), a common setting can be set for the two channels for the output de-emphasis level and the interconnect length using the DE pin and LN0, LN1 pins respectively. In Pin Control Mode 2 (see Figure 2c), those parameters can be set individually for the two channels using DEA, DEB, LNA, and LNB pins. In both modes only a common setting is available for the output voltage swing using the SWG pin. For Pin Control Mode 2 the typical LOS assert and de-assert voltage levels are fixed at $90mV_{p-p}$ and $150mV_{p-p}$ respectively with 4.0dB hysteresis.

The outputs can be disabled using the DISA and DISB pins. The DISA/DISB pins and the LOSA/LOSB pins can be connected together to implement an external output squelch function. The TLK1102E implements an internal output squelch function that can be enabled using the two-wire serial interface. In addition, a special fast auto-squelch function can be selected through the two-wire serial interface when needed to support SAS and SATA out-of-band (OOB) signals.

The POLA and POLB pins can be used to reverse the polarity of the OUTA+/OUTA- and OUTB+/OUTB– pins respectively.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as $1600mV_{p-p}$ differential. The low-frequency cut-off is low enough to support low-frequency control signals such as SAS and SATA OOB signals. The loss-of-signal detection and output disable functions are carefully designed to meet SAS/SATA OOB signal timing constraints.

Table 1. Equalization Level Settings

CABLE LENGTH (meters) (1.8dB/m loss at 5 GHz)	PIN MODE 1		PIN MODE 2	TWO-WIRE SERIAL I/F MODE (registers 3 and 6)			
	LN1	LN0	LNA / LNB	EQ3	EQ2	EQ1	EQ0
0 – 2	GND	GND	GND	1	1	1	1
2 – 6	GND	VCC	GND	0	1	1	1
6 – 11	VCC	GND	1.8 MΩ to GND	0	1	0	1
11 – 15	VCC	VCC	VCC	0	0	0	0

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BLOCK DIAGRAM

A simplified block diagram of the TLK1102E is shown in Figure 1 for the two-wire serial interface control mode. This compact, low power, 11.3-Gbps dual-channel equalizer consists of a high-speed data path with an offset cancellation block combined with an analog input threshold selection circuitry, a loss of signal detection block, a two-wire interface with a control-logic block, a bandgap voltage reference, and a bias current generation block.

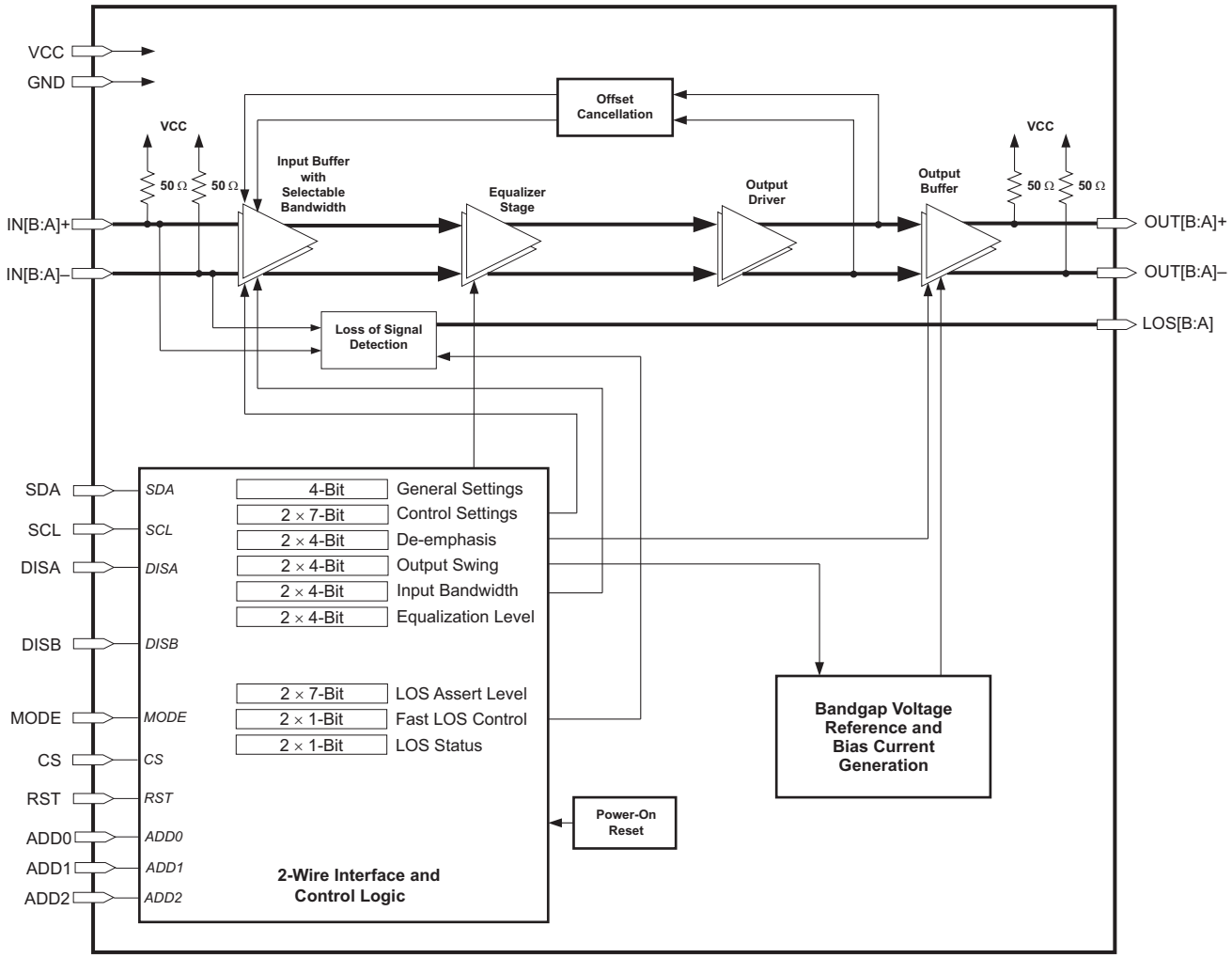


Figure 1. Simplified Block Diagram of the TLK1102E

PACKAGE

For the TLK1102E a small footprint 4-mm × 4-mm 24-pin QFN package is used, with a lead pitch of 0.5mm. Three pin-outs are available for this device as shown in Figure 2. The pin-out in Figure 2a is applicable for the case where the device is setup to be controlled through the two-wire serial interface. The pin-outs in Figure 2b and Figure 2c are applicable for the cases where the device is setup to be controlled through the device configuration pins. The MODE pin controls the pinout as described in the TERMINAL FUNCTIONS tables.

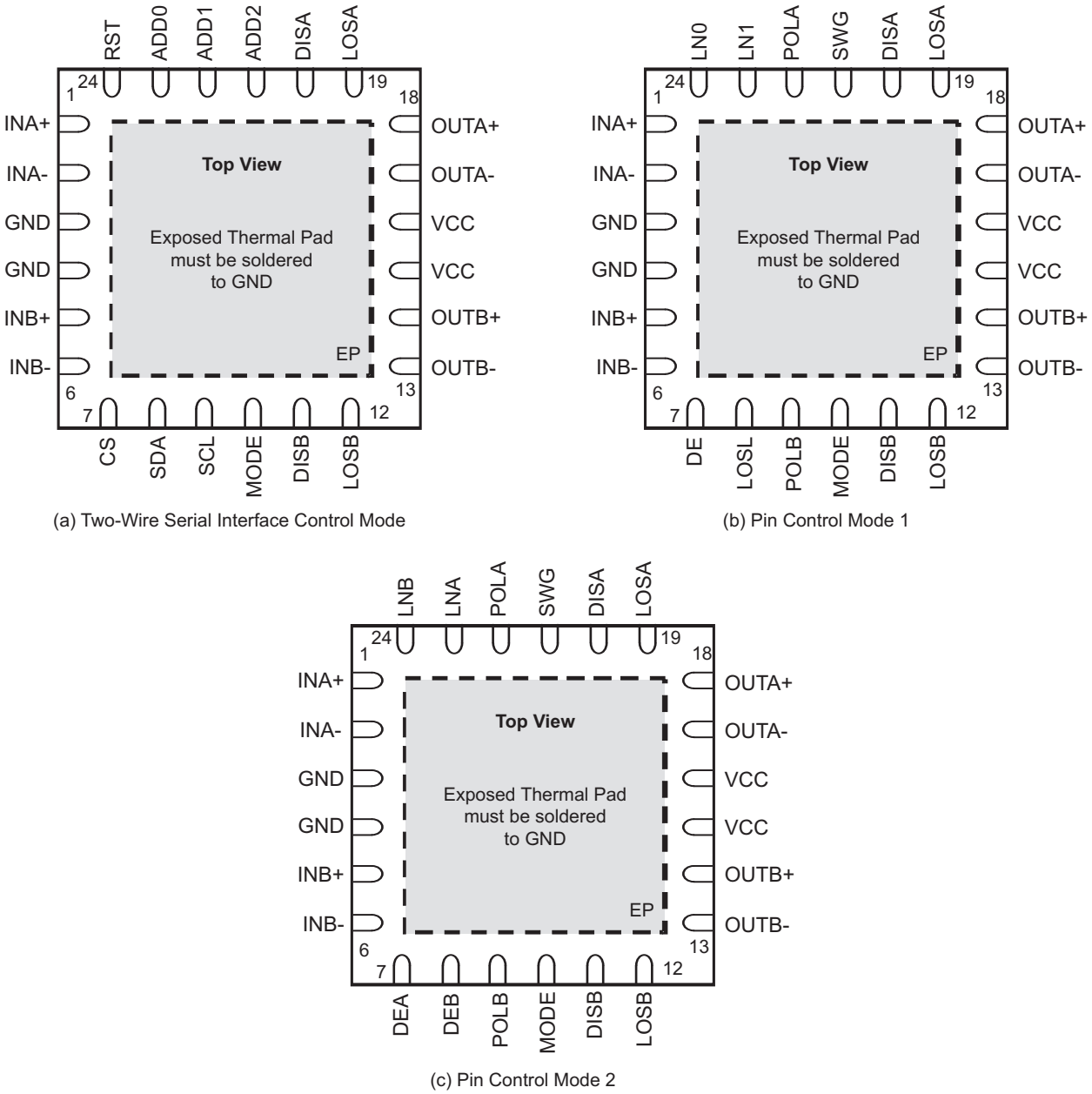


Figure 2. Pin-Out of the TLK1102E in a 4-mm × 4-mm 24-Pin QFN Package

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TERMINAL FUNCTIONS - TWO-WIRE SERIAL INTERFACE CONTROL MODE

Pin descriptions for the TLK1102E in a 4-mm x 4-mm 24-pin QFN package when the device is set to be controlled using the two-wire serial interface. This mode is selected through setting the MODE pin (pin 10) to high level.

PIN	SYMBOL	TYPE	DESCRIPTION
1, 2	INA+, INA-	analog-in	First pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
3, 4	GND	supply	Circuit ground.
5, 6	INB+, INB-	analog-in	Second pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
7	CS	digital-in	Chip Select pin. Disables the two-wire serial interface when set to low level. Internally pulled up.
8	SDA	digital-in/out	Bidirectional serial data pin for the two-wire serial interface. Open drain. Connect to a 10kΩ pull-up resistor if used. Leave open if unused.
9	SCL	digital-in	Serial clock pin for the two-wire serial interface. Connect to a 10kΩ pull-up resistor if used. Leave open if unused. Internally pulled up to VCC with a 500kΩ resistor.
10	MODE	three-state	Device control mode select. Pull up to VCC for the two-wire serial interface control mode.
11	DISB	digital-in	Disables CML output stage for OUTB+ and OUTB- when set to high level. Internally pulled down.
12	LOSB	digital-out	High level indicates that the input signal amplitude on INB+/INB- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
13, 14	OUTB-, OUTB+	analog-out	Second pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.
15, 16	VCC	supply	3.3V ± 10% supply voltage.
17, 18	OUTA-, OUTA+	analog-out	First pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.
19	LOSA	digital-out	High level indicates that the input signal amplitude on INA+/INA- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
20	DISA	digital-in	Disables CML output stage for OUTA+ and OUTA- when set to high level. Internally pulled down.
21, 22, 23	ADD2, ADD1, ADD0	digital-in	Configurable least significant bits (ADD[2:0]) of the two-wire serial interface device address. The fixed most significant bits (ADD[6:3]) of the 7-bit device address are 0101. The default address is 0101100. These pins are internally pulled up. Pull down externally to invert the associated bits.
24	RST	digital-in	Reset pin. Resets all the device digital circuits when set to high level. Internally pulled down.
EP	EP		Exposed die pad (EP) must be grounded.

TERMINAL FUNCTIONS - PIN CONTROL MODE 1

Pin descriptions for the TLK1102E in a 4-mm x 4-mm 24-pin QFN package when the device is set for Pin Control Mode 1. This mode is selected through setting the MODE pin (pin 10) to low level.

PIN	SYMBOL	TYPE	DESCRIPTION
1, 2	INA+, INA-	analog-in	First pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
3, 4	GND	supply	Circuit ground.
5, 6	INB+, INB-	analog-in	Second pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
7	DE	analog-in	Output signal de-emphasis control. A 0 to 1.2-V controlling voltage on this pin adjusts output de-emphasis on OUTA and OUTB pins from 0 to 7dB.
8	LOSL	analog-in	LOS threshold control. A 0 to 0.7-V controlling voltage on this pin adjusts the LOS assert and de-assert levels on INA and INB pins.
9	POLB	digital-in	Output data signal polarity select for OUTB+/OUTB- pins. Internally pulled up. Set to high level or leave open for normal polarity. Set to low level for inverted polarity.
10	MODE	three-state	Device control mode select. Tie to GND for pin control mode 1.
11	DISB	digital-in	Disables CML output stage for OUTB+ and OUTB- when set to high level. Internally pulled down.
12	LOSB	digital-out	High level indicates that the input signal amplitude on INB+/INB- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
13, 14	OUTB-, OUTB+	analog-out	Second pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.
15, 16	VCC	supply	3.3V ± 10% supply voltage.
17, 18	OUTA-, OUTA+	analog-out	First pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.

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PIN	SYMBOL	TYPE	DESCRIPTION
19	LOSA	digital-out	High level indicates that the input signal amplitude on INA+/INA- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
20	DISA	digital-in	Disables CML output stage for OUTA+ and OUTA- when set to high level. Internally pulled down.
21	SWG	three-state	OUTA, OUTB swing control. Tie to VCC for 1200mV$_{p-p}$ swing, tie to GND for 225mV$_{p-p}$ swing, or pull down with a 1.8MΩ resistor for 600mV$_{p-p}$ swing.
22	POLA	digital-in	Output data signal polarity select for OUTB+/OUTB- pins. Internally pulled up. Set to high level or leave open for normal polarity. Set to low level for inverted polarity.
23, 24	LN1, LN0	digital-in	Equalization level setting. Internally pulled up. Each pin supports two logic levels: high and low – four settings in the following low to high equalization order: LN1=LN0=0; LN1=0 LN0=1; LN1=1 LN0=0; LN1=LN0=1
EP	EP		Exposed die pad (EP) must be grounded.

TERMINAL FUNCTIONS - PIN CONTROL MODE 2

Pin descriptions for the TLK1102E in a 4-mm x 4-mm 24-pin QFN package when the device is set for Pin Control Mode 2. This mode is selected through pulling down the MODE pin (pin 10) with a 1.8-MΩ resistor.

PIN	SYMBOL	TYPE	DESCRIPTION
1, 2	INA+, INA-	analog-in	First pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
3, 4	GND	supply	Circuit ground.
5, 6	INB+, INB-	analog-in	Second pair of differential data inputs. Each pin is on-chip 50Ω terminated to VCC.
7	DEA	analog-in	Output signal de-emphasis control for OUTA. A 0 to 1.2-V controlling voltage on this pin adjusts output de-emphasis on OUTA+/OUTA- pins from 0 to 7dB.
8	DEB	analog-in	Output signal de-emphasis control for OUTB. A 0 to 1.2-V controlling voltage on this pin adjusts output de-emphasis on OUTB+/OUTB- pins from 0 to 7dB.
9	POLB	digital-in	Output data signal polarity select for OUTB+/OUTB- pins. Internally pulled up. Set to high level or leave open for normal polarity. Set to low level for inverted polarity.
10	MODE	three-state	Device control mode select. Pull down with a 1.8MΩ resistor for pin control mode 2.
11	DISB	digital-in	Disables CML output stage for OUTB+ and OUTB- when set to high level. Internally pulled down.
12	LOSB	digital-out	High level indicates that the input signal amplitude on INB+/INB- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
13, 14	OUTB-, OUTB+	analog-out	Second pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.
15, 16	VCC	supply	3.3V ± 10% supply voltage.
17, 18	OUTA-, OUTA+	analog-out	First pair of differential data outputs. Each pin is on-chip 50Ω terminated to VCC.
19	LOSA	digital-out	High level indicates that the input signal amplitude on INA+/INA- is below the programmed threshold level. Open drain. Requires an external 10kΩ pull-up resistor to VCC for proper operation.
20	DISA	digital-in	Disables CML output stage for OUTA+ and OUTA- when set to high level. Internally pulled down.
21	SWG	three-state	OUTA, OUTB swing control. Tie to VCC for 1200mV$_{p-p}$ swing, tie to GND for 225mV$_{p-p}$ swing, or pull down with a 1.8MΩ resistor for 600mV$_{p-p}$ swing.
22	POLA	digital-in	Output data signal polarity select for OUTB+/OUTB- pins. Internally pulled up. Set to high level or leave open for normal polarity. Set to low level for inverted polarity.
23	LNA	three-state	Equalization level setting. Supports three equalization settings. Tie to VCC for high setting, tie to GND for low setting, or pull down with 1.8MΩ resistor for medium setting. Internally tied to VCC/2.
24	LNB	three-state	Equalization level setting. Supports three equalization settings. Tie to VCC for high setting, tie to GND for low setting, or pull down with 1.8MΩ resistor for medium setting. Internally tied to VCC/2.
EP	EP		Exposed die pad (EP) must be grounded.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	-0.3 to 4.0	V
V_{IN+}, V_{IN-}	Voltage at INA+, INA-, INB+, INB-(2)	0.5 to 4.0	V
V_{IO}	Voltage at pin 7 to 11 and pin 20 to 24(2)	-0.3 to 4.0	V
$V_{IN,DIFF}$	Differential voltage between INA+ and INA-, and between INB+ and INB-	±2.5	V
I_{IN+}, I_{IN-}	Continuous current at data inputs	-25 to 25	mA
I_{OUT+}, I_{OUT-}	Continuous current at data outputs	-35 to 35	mA
I_{LOS}	Sink current at LOSA and LOSB outputs	25	mA
ESD	ESD rating at all pins	2.5	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.95	3.3	3.6	V
T_A	Operating lead temperature	-40		100	°C
V_{IH}	CMOS input high voltage	2.1			V
V_{IL}	CMOS input low voltage			0.7	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.95	3.3	3.6	V
I_{CC}	Supply current	600mV$_{p-p}$ SWG setting (CML output current included)		170	230	mA
		1200mV$_{p-p}$ SWG setting (CML output current included)		225	290	
	LOS high voltage	I_{SOURCE} = 50µA; 10kΩ Pull-up to V_{CC} on LOSA or LOSB pin	2.4			V
	LOS low voltage	I_{SINK} = 10mA; 10kΩ Pull-up to V_{CC} on LOSA or LOSB pin			0.4	V

AC ELECTRICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency -3dB bandwidth	With 0.1µF input AC-coupling capacitors		30	50	kHz
$V_{IN,MIN}$	Data input sensitivity	BER < 10^{-12} , K28.5 pattern at 11.3Gbps over a 10m 28AWG cable including two SMA connectors (27dB loss at 5.65GHz), SWG = 600mV$_{p-p}$ setting, no de-emphasis, maximum interconnect length setting. Voltage measured at the input of the cable.			250	mV$_{p-p}$
$V_{IN,MAX}$	Data input overload	BER < 10^{-12} , K28.5 pattern at 11.3Gbps, K28.5 pattern at 11.3Gbps over a 15m 24AWG cable including two SMA connectors (29dB loss at 5.65GHz), SWG = 600mV$_{p-p}$ setting, no de-emphasis, maximum interconnect length setting. Voltage measured at the input of the cable.	1600			mV$_{p-p}$

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AC ELECTRICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential data output voltage swing	DIS = Low, SWG = Low, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss.	150	225	350	mV_{p-p}
		DIS = Low, SWG = 600mV_{p-p} setting, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss.	400	600	800	
		DIS = Low, SWG = High, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss.	800	1200	1600	
$V_{CM,OUT}$	Data output common-mode voltage	DIS = Low, SWG = Low, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss, 50Ω to VCC output termination.	V_{CC}-0.12	V_{CC}-0.08	V_{CC}-0.04	V
		DIS = Low, SWG = 600mV_{p-p} setting, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss, 50Ω to VCC output termination.	V_{CC}-0.29	V_{CC}-0.205	V_{CC}-0.12	
		DIS = Low, SWG = High, V_{IN} = 400mV_{p-p}, no de-emphasis, no interconnect loss, 50Ω to VCC output termination.	V_{CC}-0.65	V_{CC}-0.45	V_{CC}-0.25	
$V_{CM,RIP}$	Common-mode output ripple	DIS = Low, SWG = 600mV_{p-p} setting, K28.5 pattern at 11.3Gbps, no interconnect loss, 600mV on DE pin, V_{IN} = 1600mV_{p-p}.		2	5	mV_{RMS}
$V_{OD,RIP}$	Differential output ripple	DIS = High, K28.5 pattern at 11.3Gbps, no interconnect loss, V_{IN} = 1600mV_{p-p}.		15	20	mV_{p-p}
DE	Output de-emphasis	K28.5 pattern at 11.3Gbps on both channels, no interconnect loss, V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, no de-emphasis.		0		dB
		K28.5 pattern at 11.3Gbps on both channels, no interconnect loss, V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, maximum de-emphasis level.		7		
DJ	Deterministic jitter	K28.5 pattern at 11.3Gbps on both channels, 10m 28AWG cable (27dB loss at 5.65GHz), V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, 600mV on DE pin, maximum interconnect length setting.		8		ps$_{p-p}$
		K28.5 pattern at 11.3Gbps on both channels, 15m 24AWG cable (29dB loss at 5.65GHz), V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, 600mV on DE pin, maximum interconnect length setting.		12		
RJ	Random jitter	K28.5 pattern at 11.3Gbps on both channels, 10m 28AWG cable (27dB loss at 5.65GHz), V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, 600mV on DE pin, maximum interconnect length setting.		1.2		ps$_{RMS}$
		K28.5 pattern at 11.3Gbps on both channels, 15m 24AWG cable (29dB loss at 5.65GHz), V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, 600mV on DE pin, maximum interconnect length setting.		1.4		
JPXT	Crosstalk jitter penalty	Channel A: K28.5 pattern at 11.3Gbps, 15m 24AWG cable (29dB loss at 5.65GHz), V_{IN} = 600mV_{p-p}, Register 2 = 10h (offset cancellation OFF), Register 3 = 01h (equalizer filter 1 OFF), Register 4 = 66h (680mVpp output swing, 3.3dB output de-emphasis); Channel B: Repeated 1010 pattern at 11.3Gbps, no interconnect line loss, V_{IN} = 600mV_{p-p}, Register 6 = 10h (offset cancellation OFF), Register 7 = 0Fh (all equalizer filters OFF), Register 8 = F6h (680mVpp output swing, 7dB output de-emphasis);			3	ps$_{p-p}$
t_R	Output rise time	20% to 80%, No interconnect line, V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, no de-emphasis		28		ps
t_F	Output fall time	20% to 80%, no interconnect loss, V_{IN} = 400mV_{p-p}, SWG = 600mV_{p-p} setting, no de-emphasis		28		

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AC ELECTRICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDD11	Differential input return loss	0.01GHz < f < 4.1GHz		See (1)		dB
		4.1GHz < f < 12.1GHz		See (2)		
SDD22	Differential output return loss	0.01GHz < f < 4.1GHz		See (1)		dB
		4.1GHz < f < 12.1GHz		See (2)		
SCC22	Common-mode output return loss	0.01GHz < f < 7.5GHz		See (3)		dB
		7.5GHz < f < 12.1GHz		See (4)		
V_{AS}	LOS assert threshold voltage	K28.5 Pattern at 11.3Gbps, no interconnect loss, LOSL = Open (also applies to Pin Control Mode 2)	45	90		mV_{p-p}
		K28.5 Pattern at 11.3Gbps, no interconnect loss, V(LOSL) = 0.7V	70	140		
V_{DAS}	LOS de-assert threshold voltage	K28.5 Pattern at 11.3Gbps, no interconnect loss, LOSL = Open (also applies to Pin Control Mode 2)		150	300	mV_{p-p}
		K28.5 Pattern at 11.3Gbps, no interconnect, V(LOSL) = 0.7V		235	500	
	LOS hysteresis	$20\log(V_{DAS} / V_{AS})$	2.5	4.0		dB
$T_{AS/DAS}$	LOS assert/De-assert time		1/10	2/20	4/30	µs
V_{FAS}	Fast LOS assert threshold voltage	K28.5 Pattern at 11.3Gbps, no interconnect loss, Reg 5/9 = 10111111b		150		mV_{p-p}
V_{FDAS}	Fast LOS de-assert threshold voltage	K28.5 Pattern at 11.3Gbps, no interconnect loss, Reg 5/9 = 10111111b		220		mV_{p-p}
	Fast LOS hysteresis	$20\log(V_{FDAS} / V_{FAS})$		3.3		dB
$T_{SQUELCH}$	Squelch time	Fast auto-squelch mode, no interconnect loss, $600mV_{p-p}$ input swing, K28.5 pattern, 1.5Gbps, SWG = $600mV_{p-p}$ setting. Time from input off to output voltage < $120mV_{p-p}$		5		ns
T_{DIS}	Disable response time			2		ns
T_{SKEW}	Channel-to-channel skew	OUTB+/ OUTB– relative to OUTA+/OUTA–		2		ps
	Latency	from IN[B:A]+/ IN[B:A]– to OUT[B:A]+/OUT[B:A]–		165		ps

(1) Differential return loss given by SDD11, SDD22 = $12.3 - 13 \log_{10}(f/5.5)$, f in GHz
(2) Differential return loss given by SDD11, SDD22 = $18 - 2\sqrt{f}$, f in GHz
(3) Common-mode output return loss given by SCC22 = 12 - 2.8f, f in GHz
(4) Common-mode output return loss given by SCC22 = 5.2 - 0.08f, f in GHz

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TWO-WIRE SERIAL INTERFACE AND CONTROL LOGIC

FUNCTIONAL DESCRIPTION

The TLK1102E uses a two-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven respectively by the serial data and serial clock from a microcontroller, for example. Both inputs require 10kΩ pull-up resistors to VCC when used. For driving these inputs, an open-drain output is recommended.

The two-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The TLK1102E is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the clock (SCL) signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address ($0101A_2\overline{A}_1\overline{A}_0$) followed by an eighth bit which is the data direction bit ($R/\overline{W}$). A zero indicates a WRITE and a 1 indicates a READ. The default slave address is 0101100. The A_2,$\overline{A}_1$, and $\overline{A}_0$ address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. Those pins are internally pulled up. Pulling down the ADD[2:0] pins changes the address to 0101011. Table 2 summarizes the slave address settings:
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Table 2. Slave Address Settings

ADD2	ADDR1	ADDR0	SLAVE ADDRESS
0	0	0	0101011
0	0	1	0101010
0	1	0	0101001
0	1	1	0101000
1	0	0	0101111
1	0	1	0101110
1	1	0	0101101
1	1	1	0101100

Regarding timing, the TLK1102E is I^2C-compatible. The typical timing is shown in Figure 3 and a complete data transfer is shown in Figure 4. Parameters for Figure 3 are defined in Table 3.

Bus Idle: Both SDA and SCL lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

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Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

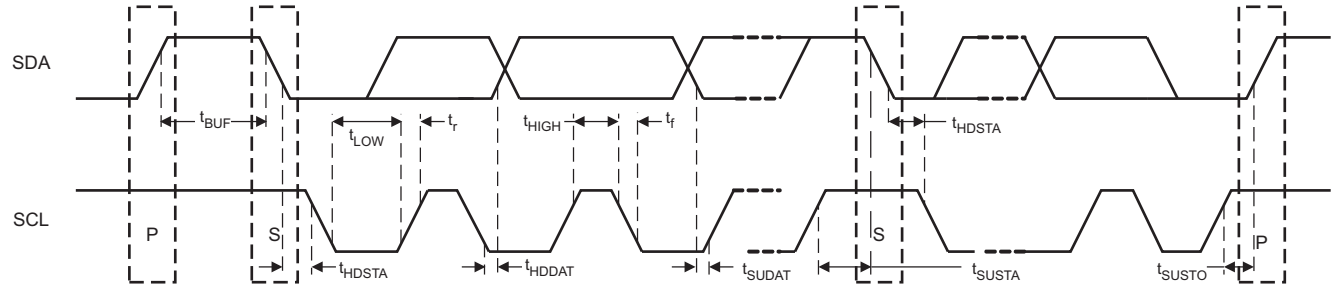


Figure 3. Two-Wire Serial Interface Timing Diagram.

Table 3. Two-Wire Serial Interface Timing Diagram Definitions

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCL}	SCL Clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HIGH}	High period of the SCL clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCL signals		300	ns
t_F	Fall time of both SDA and SCL signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

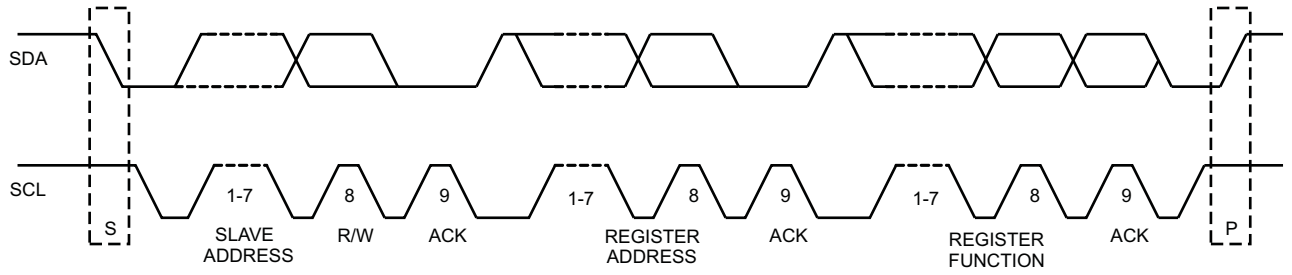


Figure 4. Two-Wire Serial Interface Data Transfer

REGISTER MAPPING

The register mapping for read/write register addresses 0 (0x00) through 15 (0x0F) are shown in Table 4 to Table 19. Table 20 describes the circuit functionality based on the register settings.

Table 4. Register 0x00 - General Device Settings

REGISTER ADDRESS 0x00							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
RESET	PWRDOWN	Reserved	Reserved	Reserved	Reserved	LOSRNG	CHA_TRACK

Table 5. Register 0x01 – Reserved

REGISTER ADDRESS 0x01							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 6. Register 0x02 – Control A Control Settings

REGISTER ADDRESS 0x02							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
INOFF	OUTOFF	LOSOFF	OCOFF	Reserved	SQUELCH	POL	DISABLE

Table 7. Register 0x03 – Control A Input Settings

REGISTER ADDRESS 0x03							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BW3	BW2	BW1	BW0	EQ3	EQ2	EQ1	EQ0

Table 8. Register 0x04 – Channel A Output Settings

REGISTER ADDRESS 0x04							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DEEM3	DEEM2	DEEM1	DEEM0	AMP3	AMP2	AMP1	AMP0

Table 9. Register 0x05 – Channel A LOS Settings

REGISTER ADDRESS 0x05							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
FAST	LOSLVL6	LOSLVL5	LOSLVL4	LOSLVL3	LOSLVL2	LOSLVL1	LOSLVL0

Table 10. Register 0x06 – Channel B Control Settings

REGISTER ADDRESS 0x06							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
INOFF	OUTOFF	LOSOFF	OCOFF	Reserved	SQUELCH	POL	DISABLE

Table 11. Register 0x07 – Channel B Input Settings

REGISTER ADDRESS 0x07							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
BW3	BW2	BW1	BW0	EQ3	EQ2	EQ1	EQ0

Table 12. Register 0x08 – Channel B Output Settings

REGISTER ADDRESS 0x08							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
DEEM3	DEEM2	DEEM1	DEEM0	AMP3	AMP2	AMP1	AMP0

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Table 13. Register 0x09 – Channel B LOS Settings

REGISTER ADDRESS 0x09							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
FAST	LOSLVL6	LOSLVL5	LOSLVL4	LOSLVL3	LOSLVL2	LOSLVL1	LOSLVL0

Table 14. Register 0x0A – Reserved

REGISTER ADDRESS 0x0A							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 15. Register 0x0B – Reserved

REGISTER ADDRESS 0x0B							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 16. Register 0x0C – Reserved

REGISTER ADDRESS 0x0C							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 17. Register 0x0D – Reserved

REGISTER ADDRESS 0x0D							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 18. Register 0x0E – Device Status

REGISTER ADDRESS 0x0E							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LOS_CHB	LOS_CHA

Table 19. Register 0x0F – Reserved

REGISTER ADDRESS 0x0F							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Table 20. Register Functionality

REGISTER	BIT(s)	NAME	DESCRIPTION	FUNCTION	DEFAULT
0	7	RESET	Software Reset	Resets all registers	00000000
	6	PWRDOWN	Powerdown	Set high to power down the device. In powerdown mode the the current consumption about 2.5mA	
	5 - 2	Reserved			
	1	LOSRNG	LOS Range Select	Set to high to increase LOS detection sensitivity	
	0	CHA_TRACK	Channel A Tracking Mode	All settings from channel A will be used for both channels, A and B	
1	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			
2	7	INOFF	Channel A Input Off	Set high to power down channel A input stages	00000000
	6	OUTOFF	Channel A Output Off	Set high to power down channel A output driver and buffer	
	5	LOSOFF	Channel A LOS Detector Off	Set high to power down channel A input signal detector	
	4	OCOFF	Channel A Offset Cancellation Off	Disables channel A offset cancellation circuit	
	3	Reserved			
	2	SQUELCH	Channel A Squelch Mode	High activates channel A internal output squelch function	
	1	POL	Channel A Polarity Switch	Set to high to change polarity of channel A output signal	
	0	DISABLE	Channel A Output Disable	Set to high to disable channel A output data and keep common mode level	
3	7	BW3	Channel A Bandwidth Select 3 (MSB)	0000 -> highest bandwidth 1111 -> lowest bandwidth	00000000
	6	BW2	Channel A Bandwidth Select 2		
	5	BW1	Channel A Bandwidth Select 1		
	4	BW0	Channel A Bandwidth Select 0 (LSB)		
	3	EQ3	Channel A EQ Filter Stage 3 Control (MSB)	Set to high to switch off channel A EQ filter 3	
	2	EQ2	Channel A EQ Filter Stage 2 Control	Set to high to switch off channel A EQ filter 2	
	1	EQ1	Channel A EQ Filter Stage 1 Control	Set to high to switch off channel A EQ filter 1	
	0	EQ0	Channel A EQ Filter Stage 0 Control (LSB)	Set to high to switch off channel A EQ filter 0	

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Table 20. Register Functionality (continued)

REGISTER	BIT(s)	NAME	DESCRIPTION	FUNCTION	DEFAULT
4	7	DEEM3	Channel A Output De-emphasis 3 (MSB)	0000 -> no peaking 1111 -> highest peaking	00000000
	6	DEEM2	Channel A Output De-emphasis 2		
	5	DEEM1	Channel A Output De-emphasis 1		
	4	DEEM0	Channel A Output De-emphasis 0 (LSB)		
	3	AMP3	Channel A Output Amplitude 3 (MSB)	0000 -> 225mV$_{p-p}$ 1111-> 1200mV$_{p-p}$ approximately 60mV$_{p-p}$ per step	
	2	AMP2	Channel A Output Amplitude		
	1	AMP1	Channel A Output Amplitude 1		
	0	AMP0	Channel A Output Amplitude 0 (LSB)		
5	7	FAST	Channel A Fast Signal Detection Mode	Set to high to select fast signal detection mode on channel A	00000000
	6	LOSLVL6	Channel A LOS Threshold Level 6 (MSB)	0000000 -> Minimum LOS assert level 1001100 -> Maximum LOS assert level Settings out of the above range are not supported	
	5	LOSLVL5	Channel A LOS Threshold Level 5		
	4	LOSLVL4	Channel A LOS Threshold Level 4		
	3	LOSLVL3	Channel A LOS Threshold Level 3		
	2	LOSLVL2	Channel A LOS Threshold Level 2		
	1	LOSLVL1	Channel A LOS Threshold Level 1		
	0	LOSLVL0	Channel A LOS Threshold Level 0 (LSB)		
6	7	INOFF	Channel B Input Off	Set high to power down channel B input stages	00000000
	6	OUTOFF	Channel B Output Off	Set high to power down channel B output driver and buffer	
	5	LOSOFF	Channel B LOS Detector Off	Set high to power down channel B input signal detector	
	4	OCOFF	Channel B Offset Cancellation Off	Disables channel B offset cancellation circuit	
	3	Reserved			
	2	SQUELCH	Channel B Squelch Mode	High activates channel B internal output squelch function	
	1	POL	Channel B Polarity Switch	Set to high to change polarity of channel B output signal	
	0	DISABLE	Channel B Output Disable	Set to high to disable channel B output data and keep common mode level	

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Table 20. Register Functionality (continued)

REGISTER	BIT(s)	NAME	DESCRIPTION	FUNCTION	DEFAULT
7	7	BW3	Channel B Bandwidth Select 3 (MSB)	0000 -> highest bandwidth 1111 -> lowest bandwidth	00000000
	6	BW2	Channel B Bandwidth Select 2		
	5	BW1	Channel B Bandwidth Select 1		
	4	BW0	Channel B Bandwidth Select 0 (LSB)		
	3	EQ3	Channel B EQ Filter Stage 3 Control (MSB)	Set to high to switch off channel B EQ filter 3	
	2	EQ2	Channel B EQ Filter Stage 2 Control	Set to high to switch off channel B EQ filter 2	
	1	EQ1	Channel B EQ Filter Stage 1 Control	Set to high to switch off channel B EQ filter 1	
	0	EQ0	Channel B EQ Filter Stage 0 Control (LSB)	Set to high to switch off channel B EQ filter 0	
8	7	DEEM3	Channel B Output De-emphasis 3 (MSB)	0000 -> no peaking 1111 -> highest peaking	00000000
	6	DEEM2	Channel B Output De-emphasis 2		
	5	DEEM1	Channel B Output De-emphasis 1		
	4	DEEM0	Channel B Output De-emphasis 0 (LSB)		
	3	AMP3	Channel B Output Amplitude 3 (MSB)	0000 -> 225mV$_{p-p}$ 1111-> 1200mV$_{p-p}$ approximately 60mV$_{p-p}$ per step	
	2	AMP2	Channel B Output Amplitude		
	1	AMP1	Channel B Output Amplitude 1		
	0	AMP0	Channel B Output Amplitude 0 (LSB)		
9	7	FAST	Channel B Fast Signal Detection Mode	Set to high to select fast signal detection mode on channel B	00000000
	6	LOSLVL6	Channel B LOS Threshold Level 6 (MSB)	0000000 = Minimum LOS assert level 1001100 = Maximum LOS assert level Settings outside the above range are not supported	
	5	LOSLVL5	Channel B LOS Threshold Level 5		
	4	LOSLVL4	Channel B LOS Threshold Level 4		
	3	LOSLVL3	Channel B LOS Threshold Level 3		
	2	LOSLVL2	Channel B LOS Threshold Level 2		
	1	LOSLVL1	Channel B LOS Threshold Level 1		
	0	LOSLVL0	Channel B LOS Threshold Level 0 (LSB)		

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Table 20. Register Functionality (continued)

REGISTER	BIT(s)	NAME	DESCRIPTION	FUNCTION	DEFAULT
10	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			
11	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			
12	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			
13	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			
14	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	LOS_CHB	LOS Channel B	Indicates LOS at input channel B	
	0	LOS_CHA	LOS Channel A	Indicates LOS at input channel A	

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Table 20. Register Functionality (continued)

REGISTER	BIT(s)	NAME	DESCRIPTION	FUNCTION	DEFAULT
15	7	Reserved			00000000
	6	Reserved			
	5	Reserved			
	4	Reserved			
	3	Reserved			
	2	Reserved			
	1	Reserved			
	0	Reserved			

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TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3V and T_A = 25°C, V_{IN} = 400mV_{p-p} (signal generator output), output swing = 600mV_{p-p} setting, no interconnect line at the output, and with default device settings (unless otherwise noted). Optimum input equalization level and output de-emphasis settings were used for the cable and backplane measurements. Differential S-parameter characteristics of Spectra-Strip® SKEWCLEAR® EXD twinaxial cables and a 40-inch N4000-13 SI™ backplane link with Amphenol XCede® backplane connectors used for the measurements captured in this document are as shown in Figure 5.

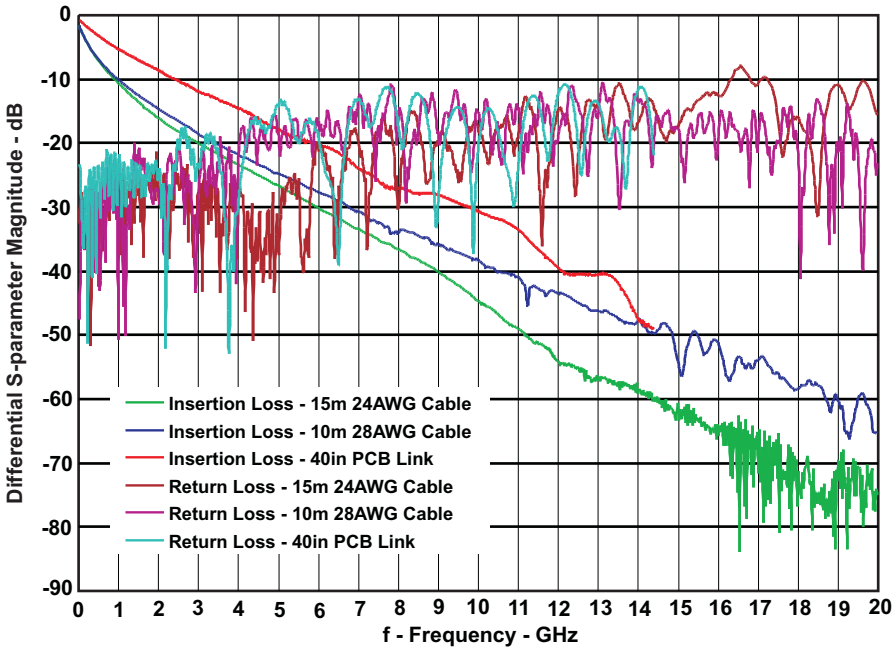


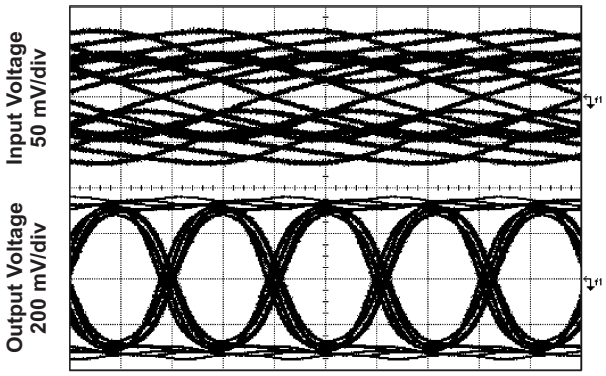
Figure 5. Typical Differential S-Parameter Characteristics of Twinaxial Cable and PCB Interconnect Lines

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TYPICAL CHARACTERISTICS (continued)

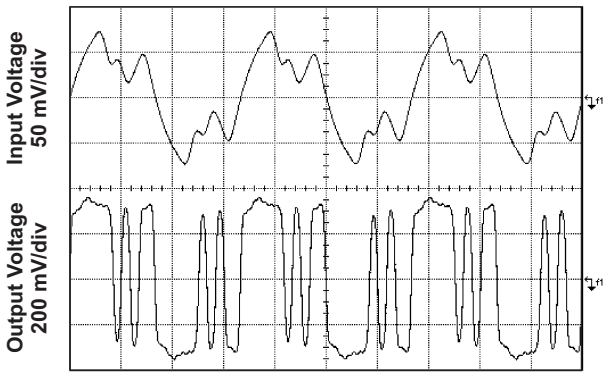
DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 12Gbps USING A K28.5 PATTERN

Input Interconnect: 15 meters 24AWG Twinaxial Cable



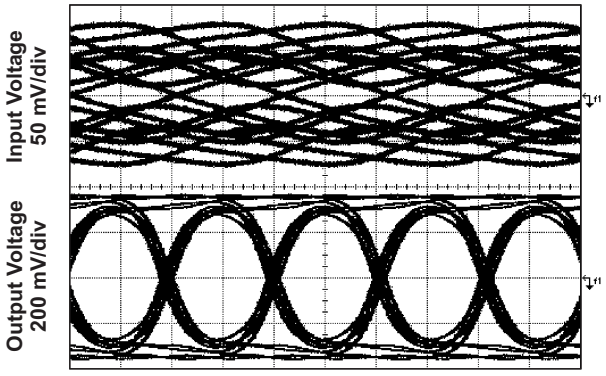
t – Time – 40 ps/div

Input Interconnect: 15 meters 24AWG Twinaxial Cable



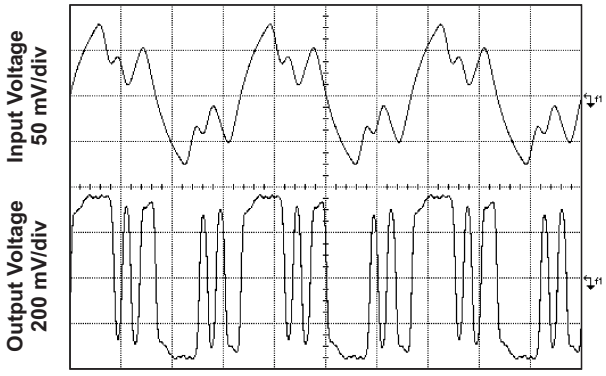
t – Time – 500 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



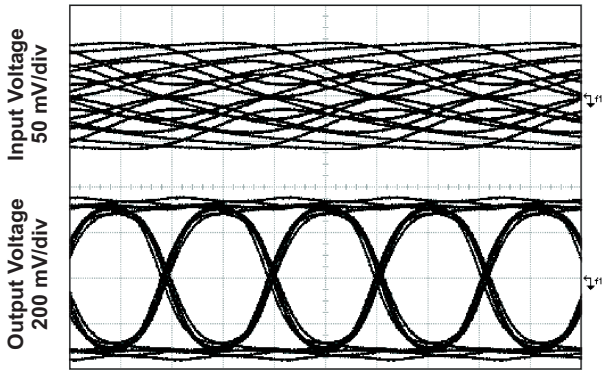
t – Time – 40 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



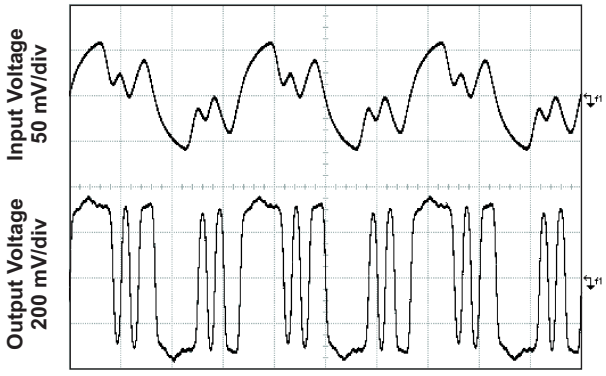
t – Time – 500 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 40 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 500 ps/div

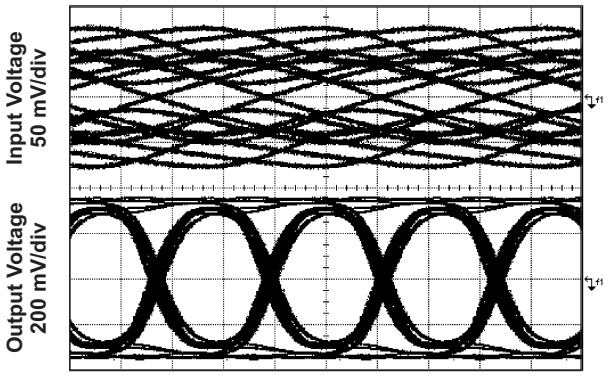
Figure 6. Equalizer Input and Output Signals with Different Interconnect Lines at 12Gbps

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TYPICAL CHARACTERISTICS (continued)

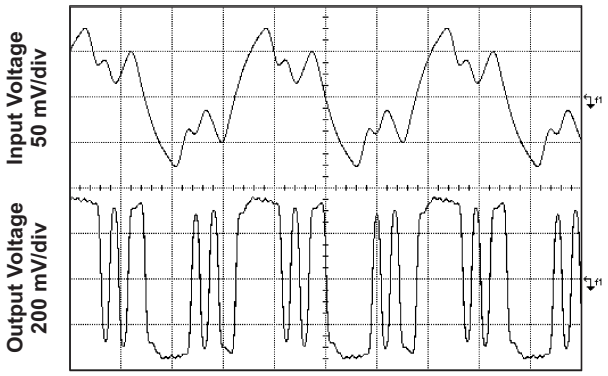
DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 11.3Gbps USING A K28.5 PATTERN

Input Interconnect: 15 meters 24AWG Twinaxial Cable



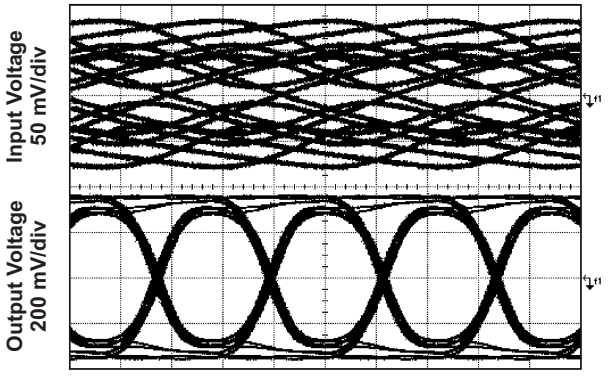
t – Time – 40 ps/div

Input Interconnect: 15 meters 24AWG Twinaxial Cable



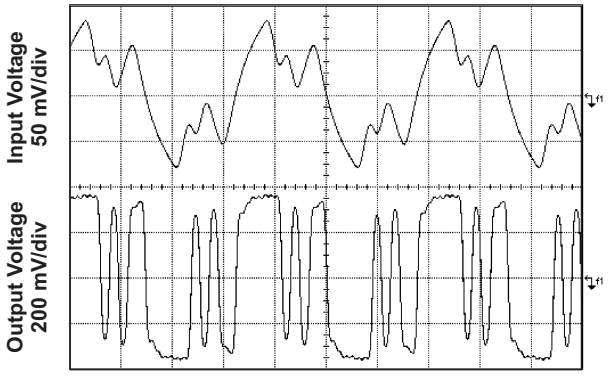
t – Time – 500 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



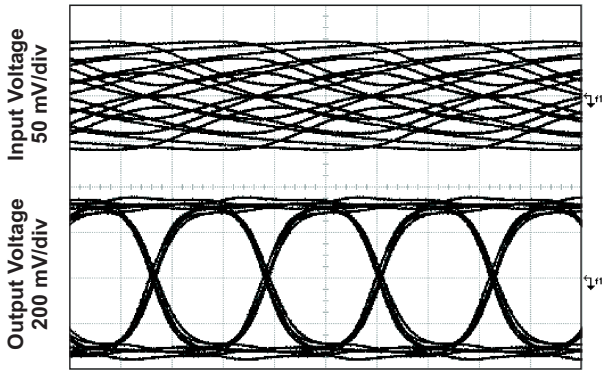
t – Time – 40 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



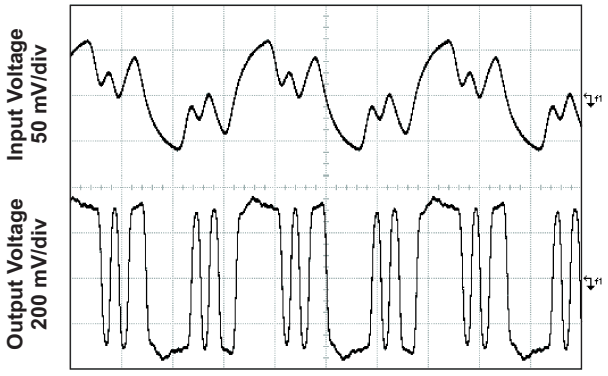
t – Time – 500 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 40 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 500 ps/div

Figure 7. Equalizer Input and Output Signals with Different Interconnect Lines at 11.3Gbps

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TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 10.3125Gbps USING A PRBS 2^{31}-1 PATTERN

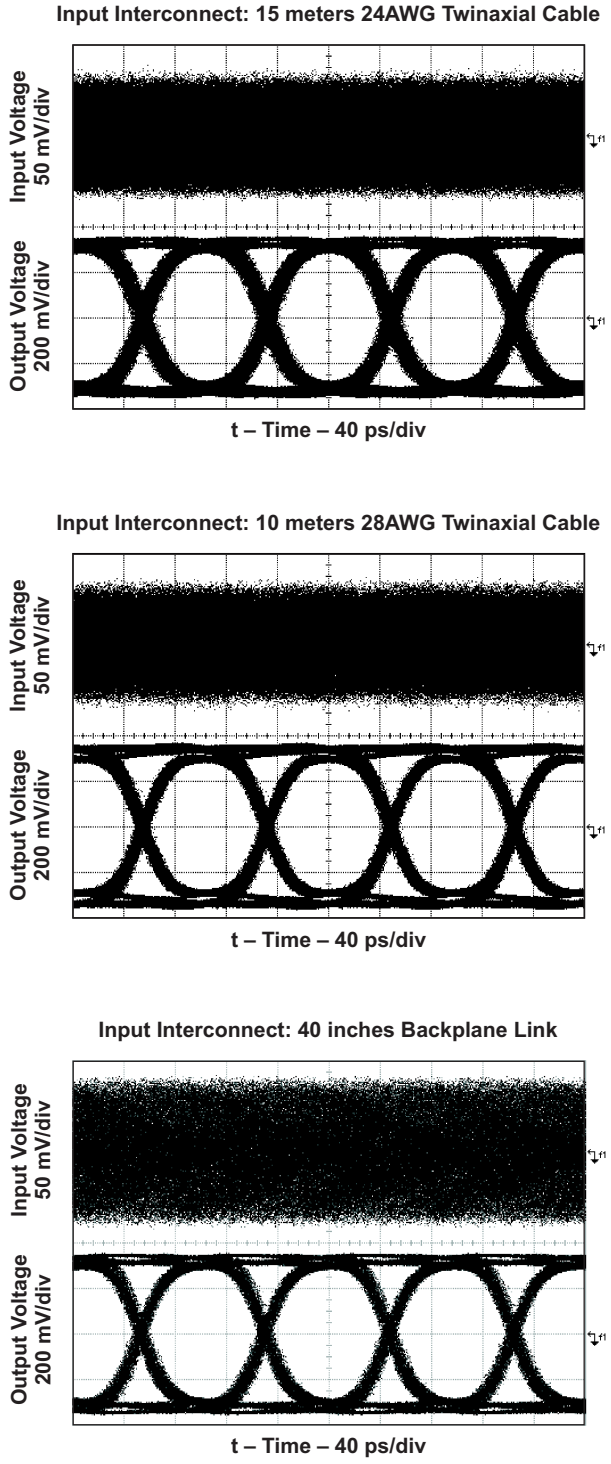


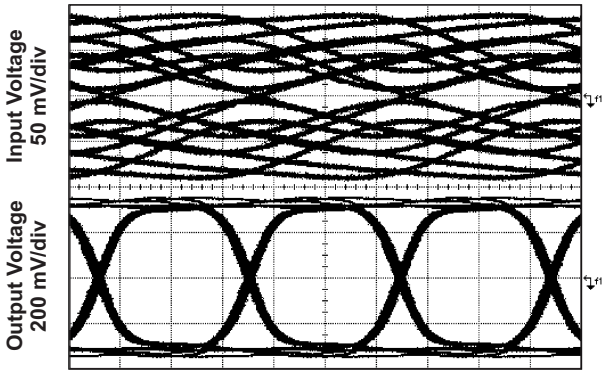
Figure 8. Equalizer Input and Output Signals with Different Interconnect Lines at 10.3125Gbps.

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TYPICAL CHARACTERISTICS (continued)

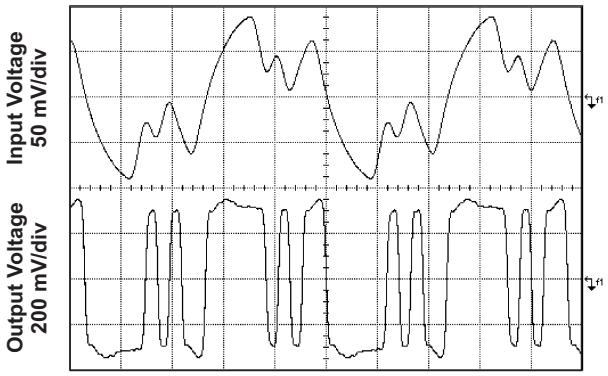
DIFFERENTIAL EQUALIZER INPUT SIGNAL (TOP) AND OUTPUT SIGNAL (BOTTOM) AT 8.5Gbps USING A K28.5 PATTERN

Input Interconnect: 15 meters 24AWG Twinaxial Cable



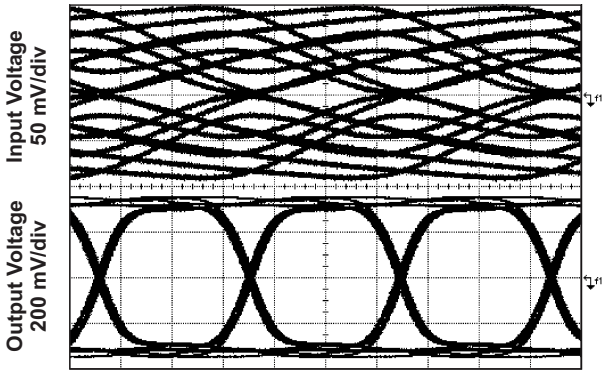
t – Time – 40 ps/div

Input Interconnect: 15 meters 24AWG Twinaxial Cable



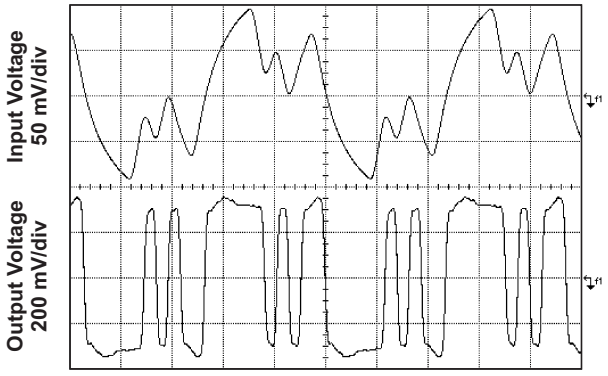
t – Time – 500 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



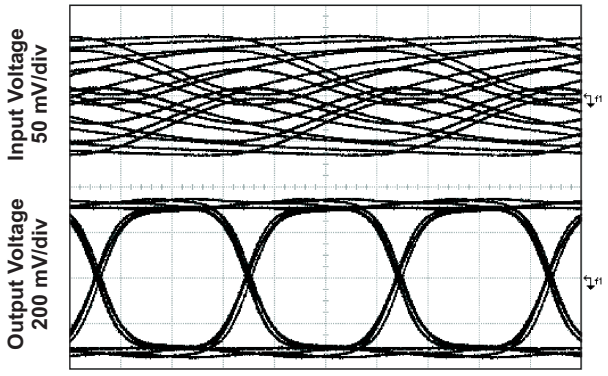
t – Time – 40 ps/div

Input Interconnect: 10 meters 28AWG Twinaxial Cable



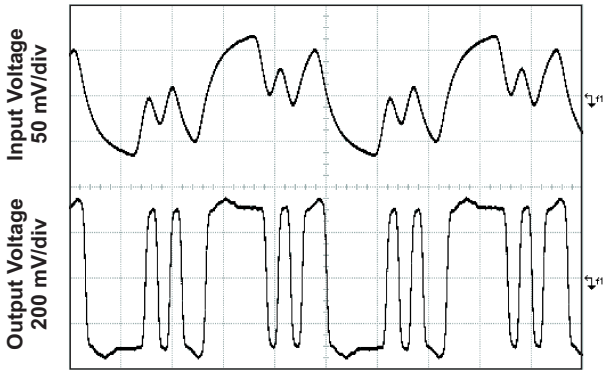
t – Time – 500 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 40 ps/div

Input Interconnect: 40 inches Backplane Link



t – Time – 500 ps/div

Figure 9. Equalizer Input and Output Signals with Different Interconnect Lines at 8.5Gbps.

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TYPICAL CHARACTERISTICS (continued)

RANDOM JITTER vs INPUT VOLTAGE (11.3Gbps, K28.5 Pattern, OC = OFF)

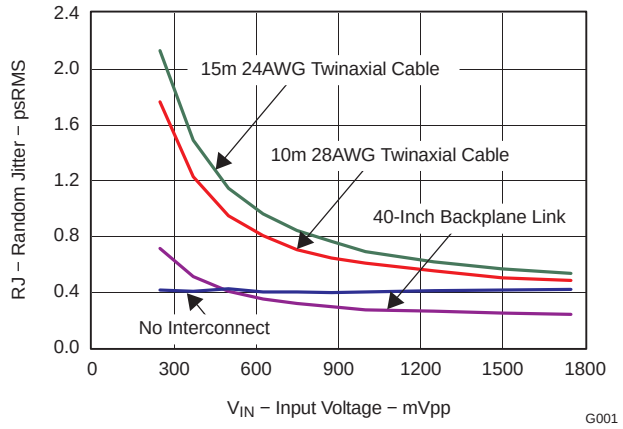


Figure 10.

RESIDUAL DETERMINISTIC JITTER vs INPUT VOLTAGE (11.3Gbps, K28.5 Pattern, OC = OFF)

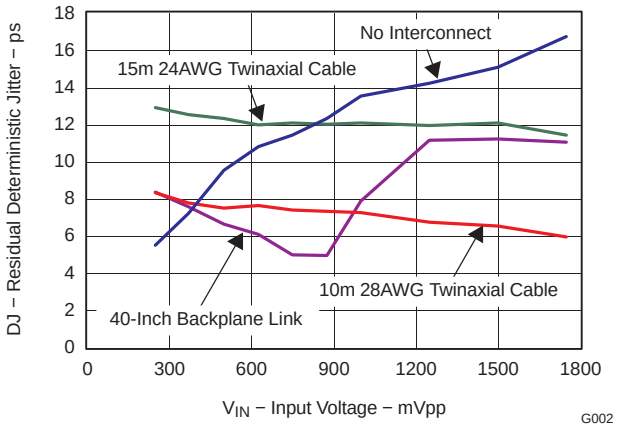


Figure 11.

DIFFERENTIAL INPUT RETURN LOSS vs FREQUENCY

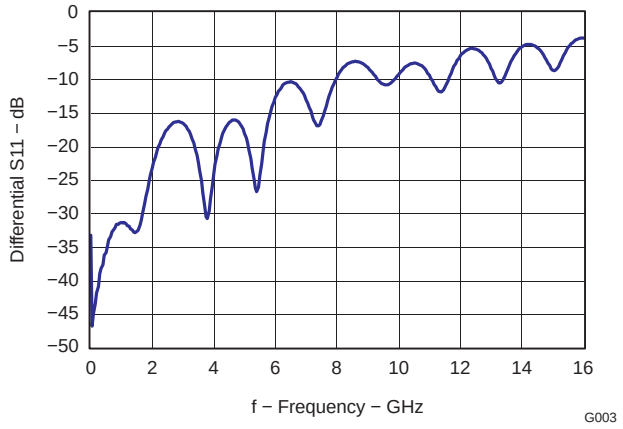


Figure 12.

DIFFERENTIAL OUTPUT RETURN LOSS vs FREQUENCY

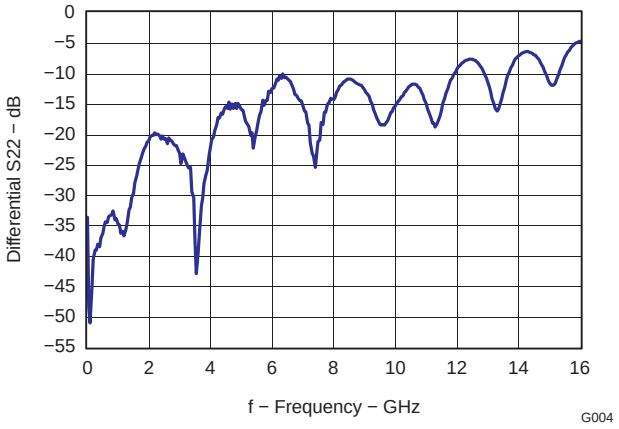


Figure 13.

REGISTER 5/9 SETTING/LOSL PIN VOLTAGE vs LOS THRESHOLD VOLTAGE

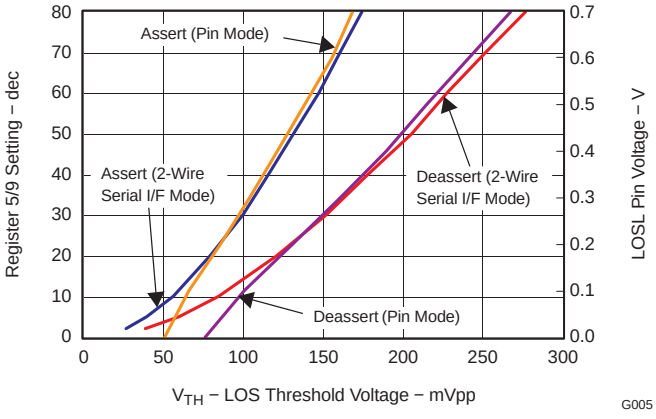


Figure 14.

REGISTER 5/9 SETTING/LOSL PIN VOLTAGE vs LOS HYSTERESIS

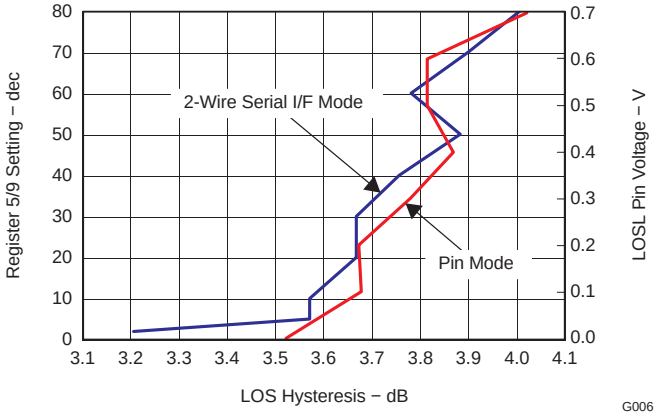


Figure 15.

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TYPICAL CHARACTERISTICS (continued)

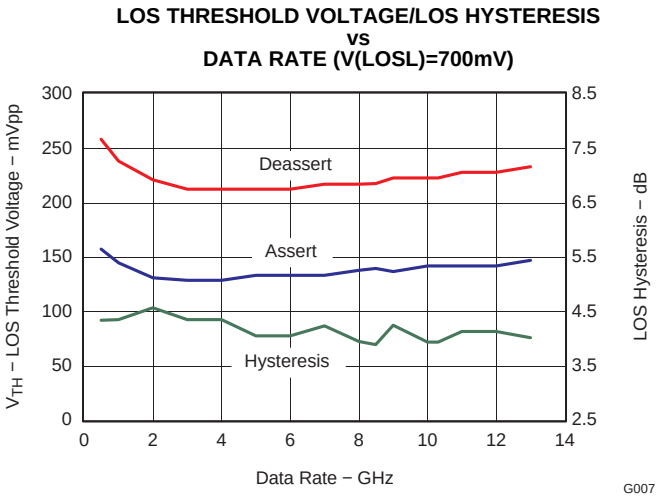


Figure 16.

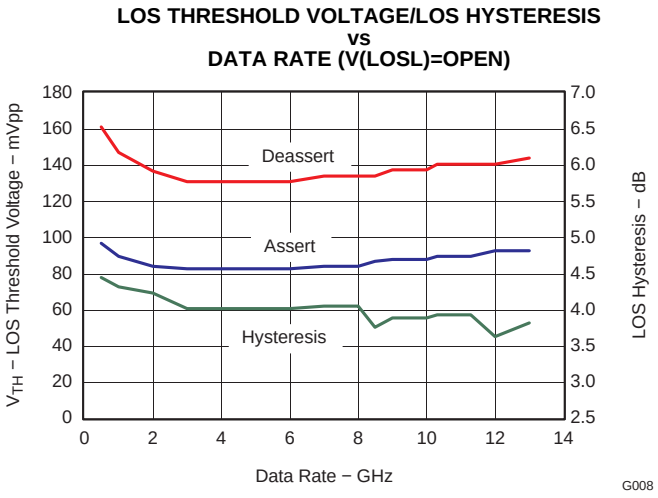


Figure 17.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK1102ERGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	TLK 1102E	Samples
TLK1102ERGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	TLK 1102E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

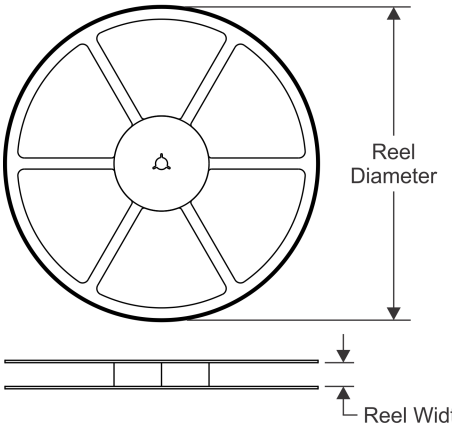
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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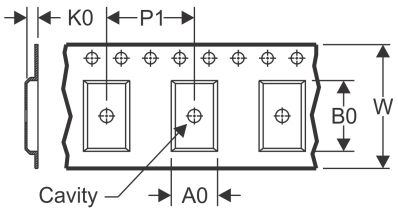
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

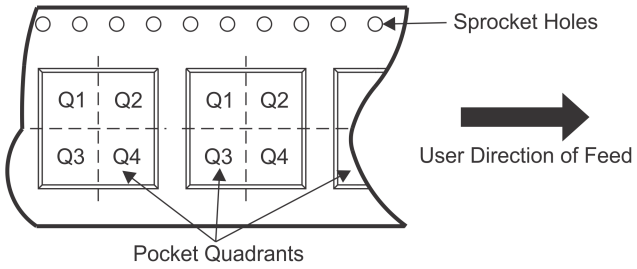


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

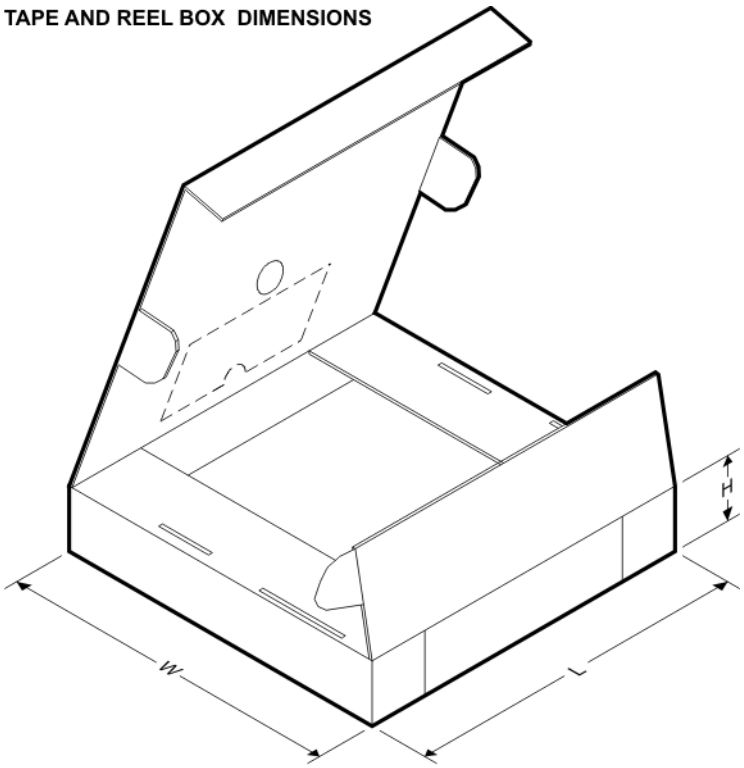
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK1102ERGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLK1102ERGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



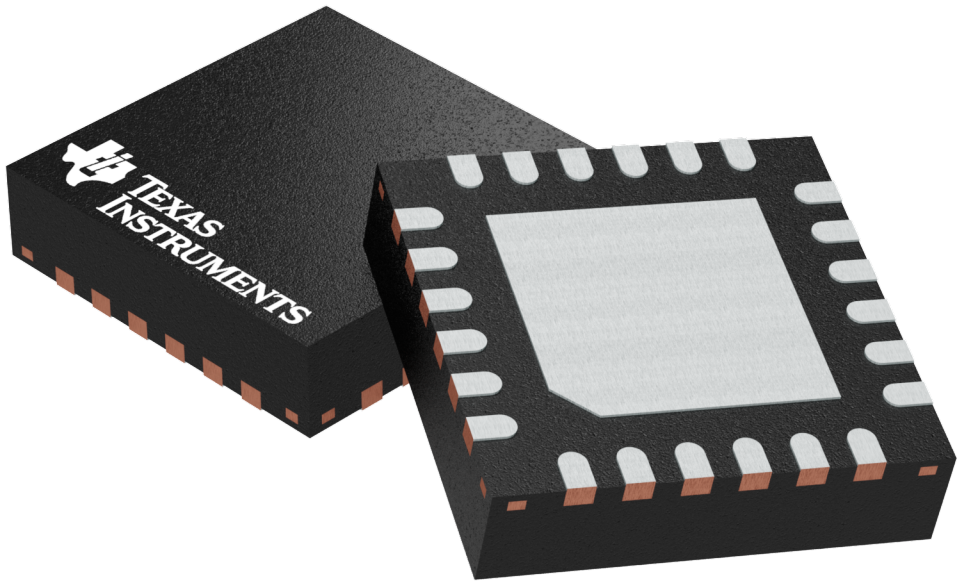
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK1102ERGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLK1102ERGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

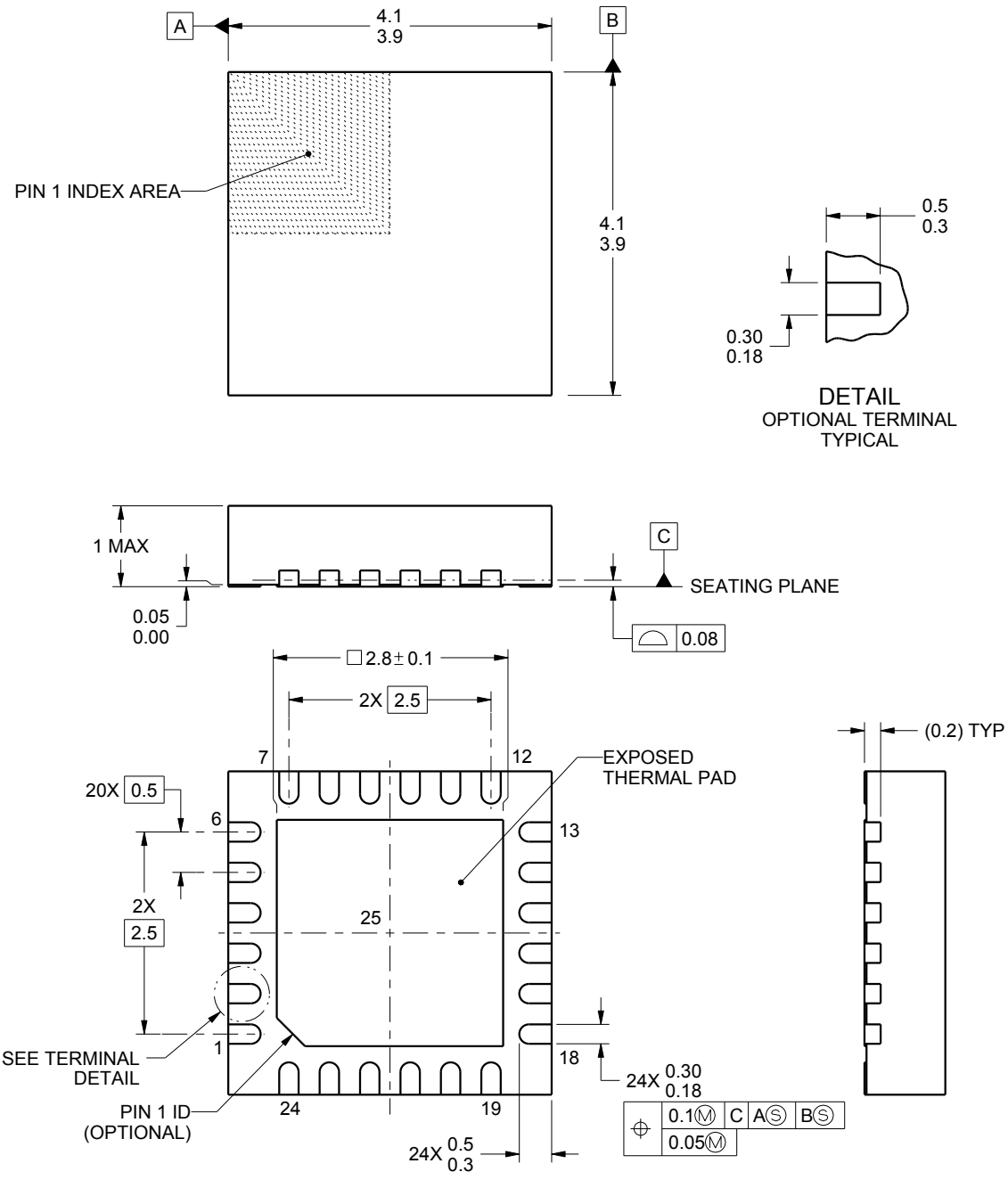
4204104/H

PACKAGE OUTLINE

RGE0024F

VQFN - 1 mm max height

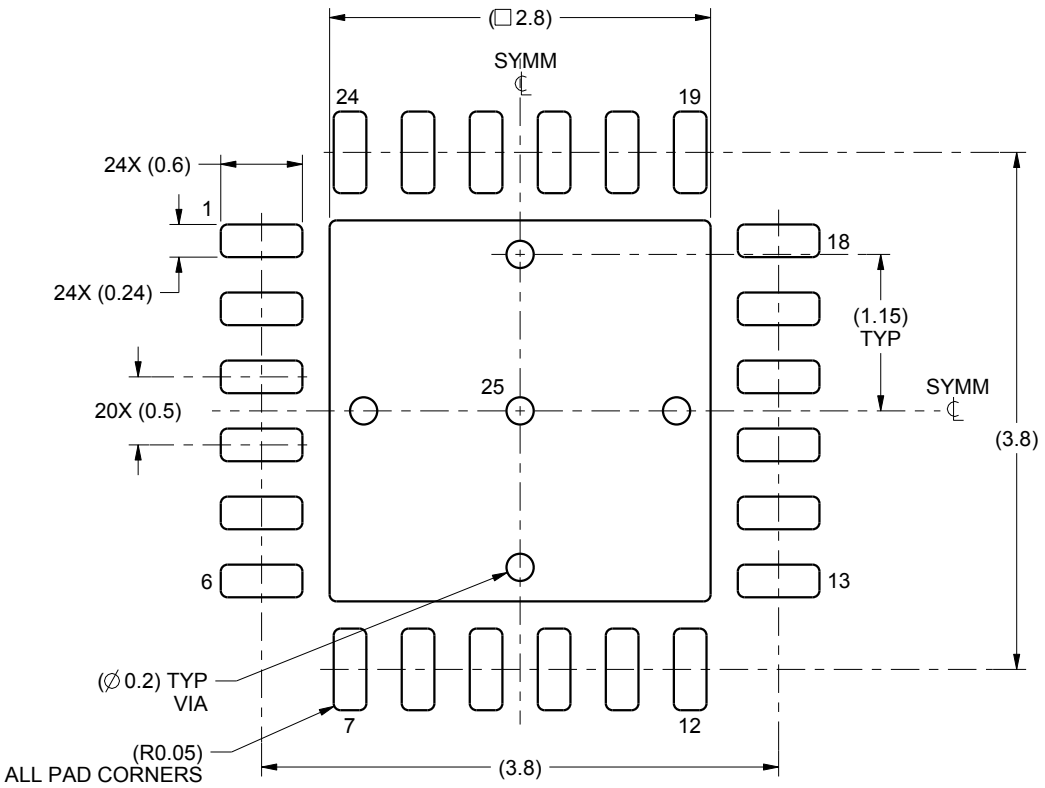
PLASTIC QUAD FLATPACK - NO LEAD



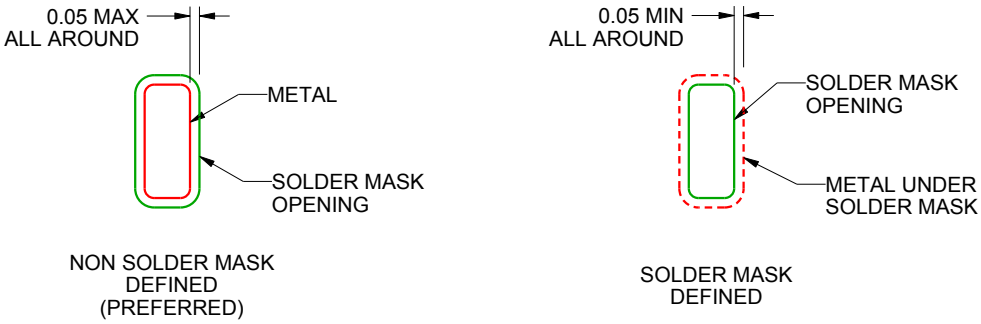
4222437/A 12/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
SCALE:18X

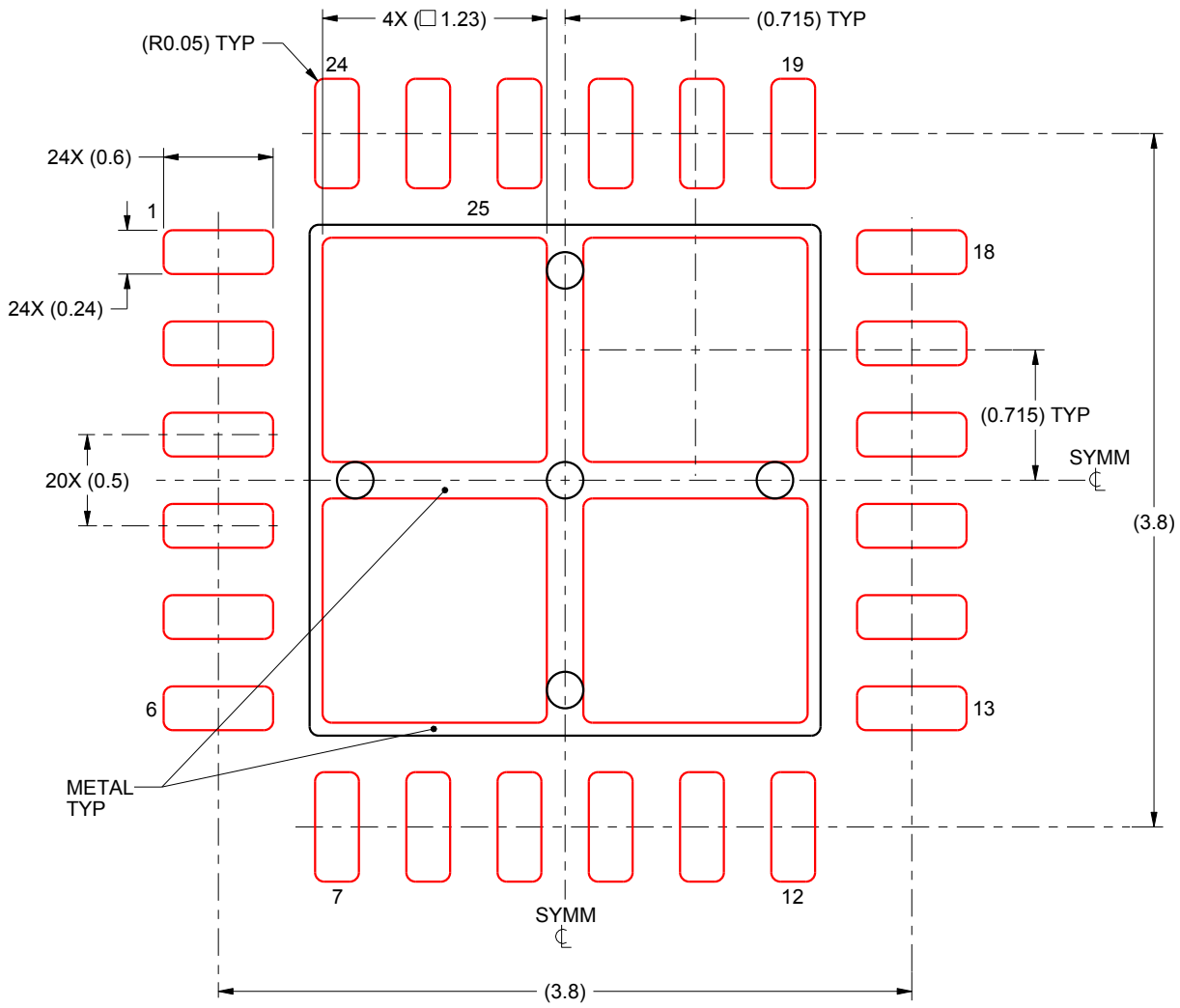


SOLDER MASK DETAILS

4222437/A 12/2015

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222437/A 12/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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