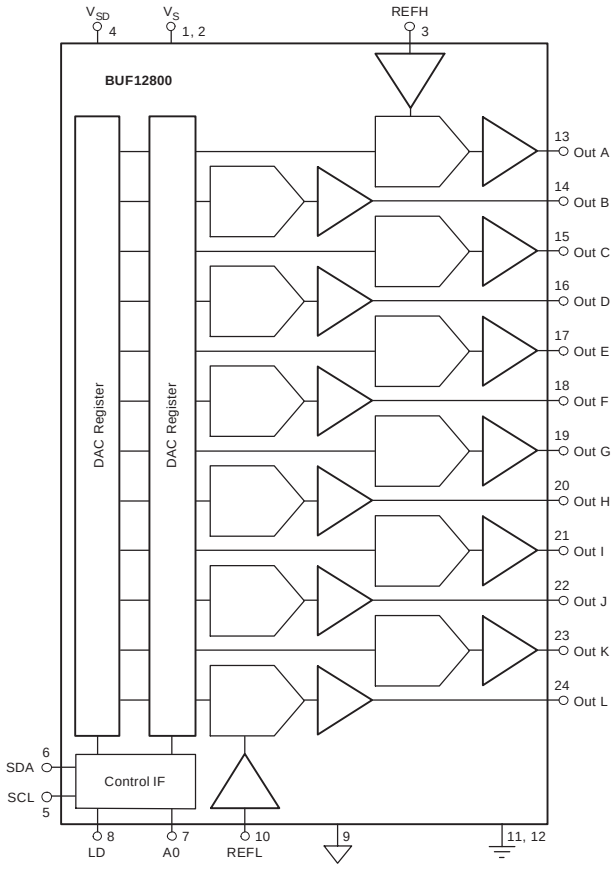
SBOS315D − DECEMBER 2004 − REVISED DECEMBER 2007

REFERENCE VOLTAGE GENERATOR for LCD GAMMA CORRECTION

FEATURES

- 12-CHANNEL GAMMA CORRECTION
- 10-BIT RESOLUTION
- DOUBLE-BUFFERED DAC REGISTERS
- INTEGRATED REFERENCE BUFFERS
- RAIL-TO-RAIL OUTPUT
- LOW SUPPLY CURRENT: 900µA/ch
- SUPPLY VOLTAGE: 7V to 18V
- DIGITAL SUPPLY: 2.3V to 5.5V
- INDUSTRY-STANDARD TWO-WIRE INTERFACE
  - High-Speed Mode: 3.4MHz
- HIGH ESD RATING:
  - 4kV HBM, 1kV CDM, 200V MM
- DEMO BOARD AND SOFTWARE AVAILABLE



APPLICATIONS

- TFT-LCD REFERENCE DRIVERS
- REFERENCE VOLTAGE GENERATORS
- INDUSTRIAL PROCESS CONTROL

DESCRIPTION

The BUF12800 is a programmable voltage reference generator designed for dynamic gamma correction in TFT-LCD panels. It provides 12 programmable outputs, each with 10-bit resolution.

TI's new, small geometry, state-of-the-art, analog CMOS process allows the use of one digital-to-analog converter (DAC) per channel while still maintaining a very small chip size. This topology has the advantage of significantly increased programming speed over existing programmable buffers.

Programming of each output occurs through an industry-standard, two-wire serial interface. Unlike existing programmable buffers, the BUF12800 offers a high-speed, two-wire interface mode that allows clock speeds up to 3.4MHz. The BUF12800 features a double-buffered DAC register structure that significantly simplifies implementation of dynamic gamma control. This further reduces programming time, especially when many channels have to be updated simultaneously.

Reference pins set the high and low voltages of the output range. They are internally buffered, which simplifies design. They may be connected to external resistors to divide the output range for finer resolution of outputs.

The BUF12800 is available in a TSSOP-24 PowerPAD™ package. It is specified from −40°C to +85°C.

BUF12800 RELATED PRODUCTS

FEATURES	PRODUCT
11-Channel Gamma Correction Buffer, Int V_{COM}	BUF11702
6-Channel Gamma Correction Buffer, Int V_{COM}	BUF07703
6-Channel Gamma Correction Buffer	BUF06703
4-Channel Gamma Correction Buffer, Int V_{COM}	BUF05703
High-Supply Voltage Gamma Buffers	BUFxx704
20-Channel Programmable Buffer, 10-Bit, V_{COM}	BUF20800

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_S	+20V
Supply Voltage, V_{SD}	+6V
Signal Input Terminals, SCL, SDA, AO, LD:	
Voltage	−0.5V to +6V
Current	±10mA
Output Short-Circuit(2)	Continuous
Operating Temperature	−40°C to +95°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+125°C
ESD Rating:	
Human Body Model (HBM)	4000V
Charged Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

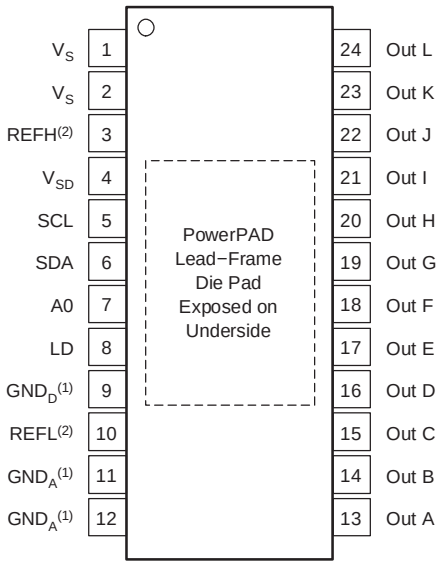
ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF12800	TSSOP-24	PWP	BUF12800

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATION

Top View **TSSOP**



(1) GND_D and GND_A are internally connected and must be at the same voltage potential.
(2) Connecting a capacitor to this node is not recommended.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = −40°C to +85°C.**

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, V_{REFH} = 17V, V_{REFL} = 1V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

PARAMETER		CONDITIONS	BUF12800 MIN	BUF12800 TYP	BUF12800 MAX	UNIT
ANALOG						
Buffer Output Swing—High		**Buffers A-F, Code = 1023, Sourcing 10mA, V_{REFH} = 17.8**	**17.7**	**17.8**		**V**
		Buffers G-L, Code = 1023, Sourcing 10mA, V_{REFH} = 17.8	**16.3**	**16.98**		**V**
Buffer Output Swing—Low		**Buffers A-F, Code = 0, Sinking 10mA, V_{REFL} = 0.2**		**1.0**	**1.1**	**V**
		Buffers G-L, Code = 0, Sinking 10mA, V_{REFL} = 0.2		**0.2**	**0.3**	**V**
Buffer Output Reset and Power-Up Value						
Buffer A		Code 3E0h (11 1110 0000)	16.452	16.502	16.552	V
Buffer B		Code 360h (11 0110 0000)	14.450	14.500	14.550	V
Buffer C		Code 320h (11 0010 0000)	13.450	13.500	13.550	V
Buffer D		Code 300h (11 0000 0000)	12.952	13.002	13.052	V
Buffer E		Code 2C0h (10 1100 0000)	11.952	12.002	12.052	V
Buffer F		Code 240h (10 0100 0000)	9.950	10.000	10.050	V
Buffer G		Code 1C0h (01 1100 0000)	7.955	8.005	8.055	V
Buffer H		Code 140h (01 0100 0000)	5.958	6.008	6.058	V
Buffer I		Code 100h (01 0000 0000)	4.957	5.007	5.057	V
Buffer J		Code 0E0h (00 1110 0000)	4.459	4.509	4.559	V
Buffer K		Code 0A0h (00 1010 0000)	3.457	3.507	3.557	V
Buffer L		Code 020h (00 0010 0000)	1.457	1.507	1.557	V
REFH Input Range			4		V_S − 0.2	V
REFL Input Range			0.2		V_S − 4	V
Integral Nonlinearity	INL			0.3		Bits
Differential Nonlinearity	DNL			0.3		Bits
Gain Error				0.12		%
Program to Out Delay	t_D			5		µs
Output Accuracy				±20	±50	mV
vs Temperature		V_{REFH} and V_{REFL} Held Constant		±25		µV/°C
Input Resistance at V_{REFH} and V_{REFL}	R_{INH}			100		MΩ
Load Regulation, 10mA, All Buffers	REG	V_{OUT} = V_S/2, I_{OUT} = +5mA to −5mA Step		0.5	1.5	mV/mA
50mA, Buffers A-F		V_{OUT} = V_S/2, $I_{SINKING}$ = 50mA, $I_{SOURCING}$ = 50mA		0.5	1.5	mV/mA
ANALOG POWER SUPPLY						
Operating Voltage Range	V_S		7		18	V
Total Analog Supply Current	I_S	Outputs at Reset Values, No Load		9	15	mA
over Temperature					**15**	**mA**
DIGITAL						
Logic 1 Input Voltage			0.7(V_{SD})			V
Logic 0 Input Voltage					0.3(V_{SD})	V
Logic 0 Output Voltage		I_{SINK} = 3mA		0.15	0.4	V
Input Leakage				±0.01	±10	µA
Clock Frequency	**f_{CLK}**	**Standard/Fast Mode**			**400**	**kHz**
		High-Speed Mode			**3.4**	**MHz**
DIGITAL POWER SUPPLY						
Operating Voltage Range	V_{SD}		2.3		5.5	V
Digital Supply Current(1)	I_{SD}	Outputs at Reset Values, No-Load, Two-Wire Bus Inactive		25	50	µA
over Temperature				**100**		**µA**
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range		Junction Temperature < +125°C	−40		+95	°C
Storage Range			−65		+150	°C
Thermal Resistance, TSSOP-24(2)						
Junction-to-Ambient	θ_{JA}			30.13		°C/W
Junction-to-Case	θ_{JC}			0.92		°C/W

(1) See the typical characteristic *Digital Supply Current vs Two-Wire Bus Activity.*
(2) PowerPAD attached to PCB, 0lfm airflow, and 76mm x 76mm copper area.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 18V, V_{SD} = 5V, V_{REFH} = 17V, V_{REFL} = 1V, R_L = 1.5kΩ connected to ground, and C_L = 200pF, unless otherwise noted.

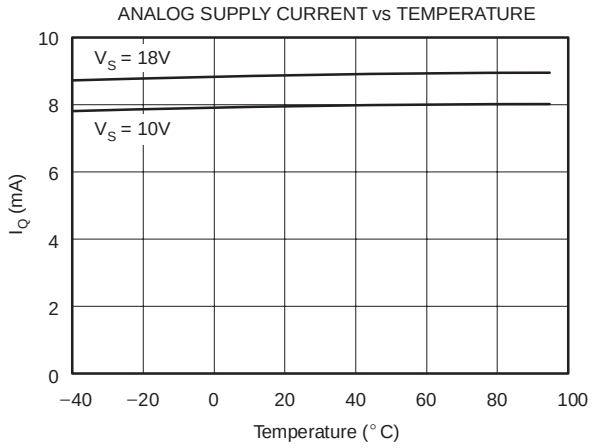


Figure 1

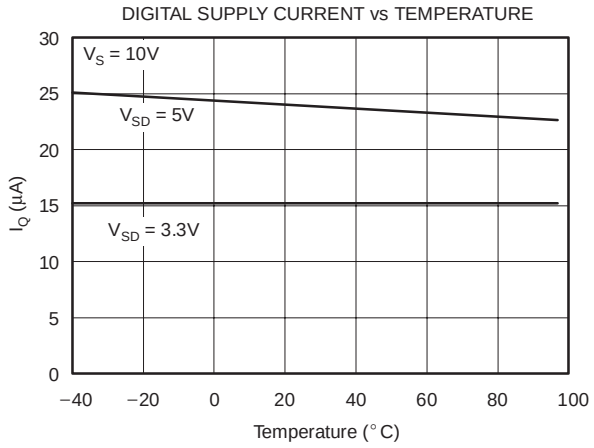


Figure 2

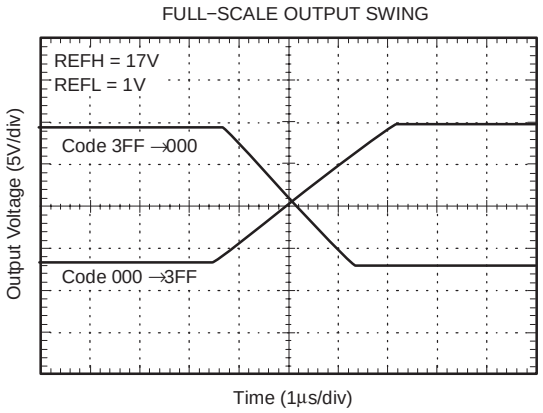


Figure 3

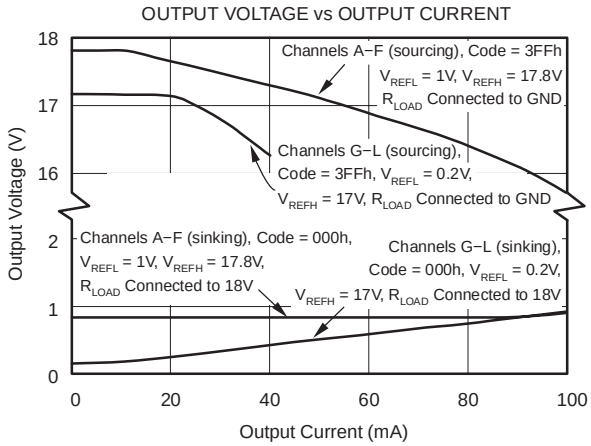


Figure 4

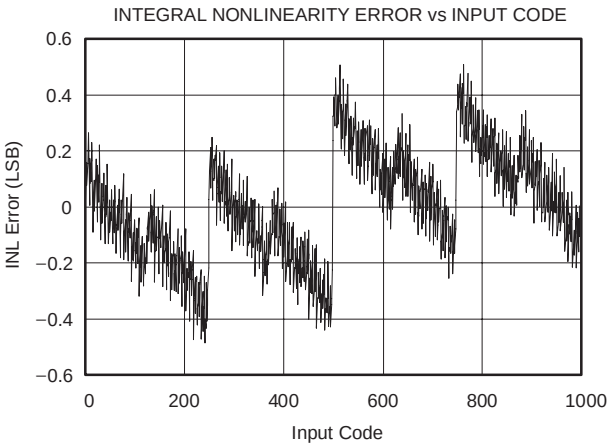


Figure 5

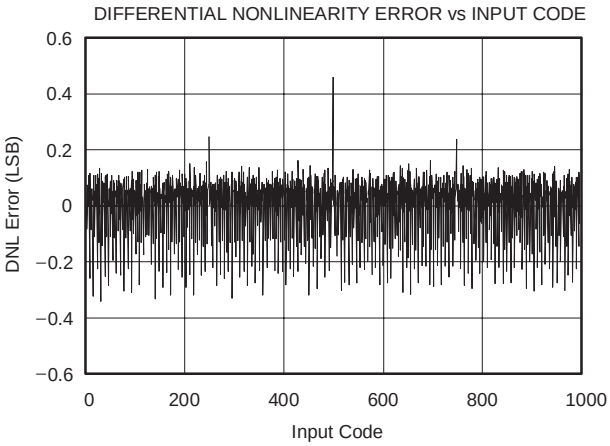


Figure 6

APPLICATIONS INFORMATION

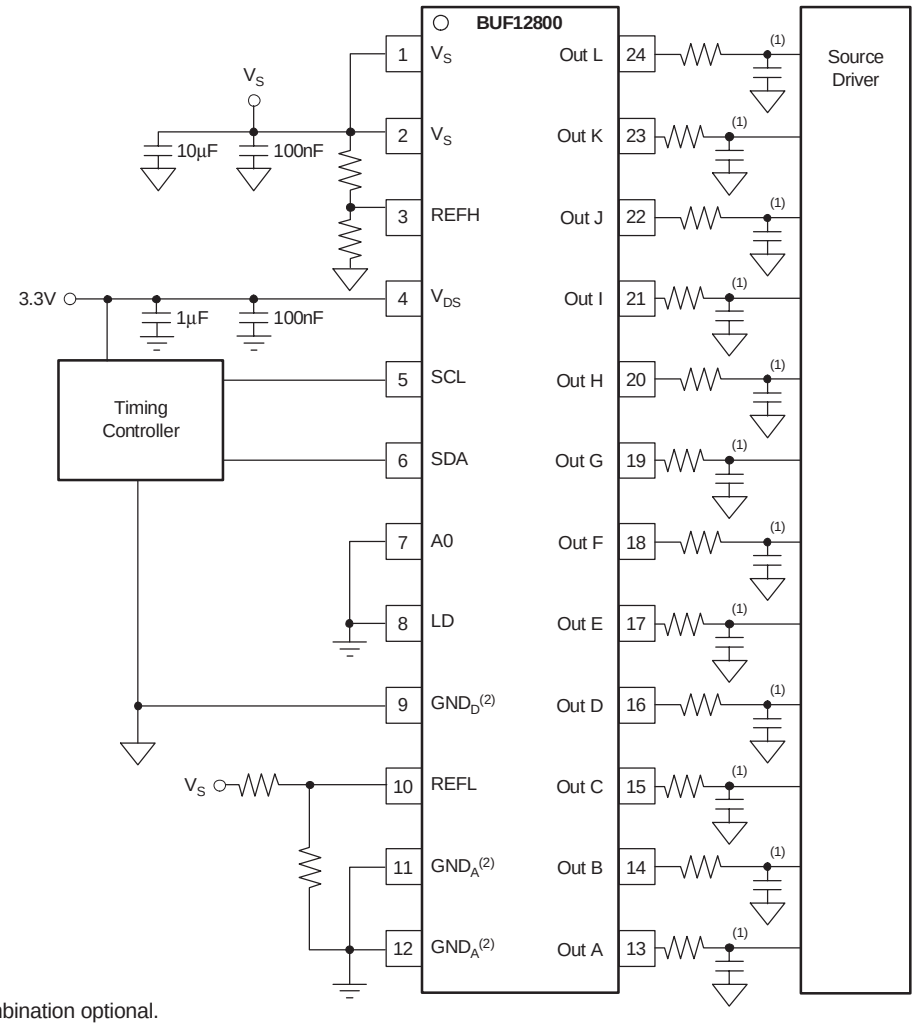
The BUF12800 programmable voltage reference allows fast and easy adjustment of 12 programmable reference outputs, each with 10-bit resolution. It allows very simple, time-efficient adjustment of the gamma reference voltages. The BUF12800 is programmed through a high-speed standard two-wire interface. The BUF12800 features a double-register structure for each DAC channel to simplify the implementation of dynamic gamma control (see the *Dynamic Control* section). This allows *pre-loading* of register data and rapid updating of all channels simultaneously.

Buffers A−F are able to swing to within 300mV of the positive supply rail, and to within 1.1V of the negative supply rail. Buffers G−L are able to swing to within 1.7V of the positive supply rail, and to within 300mV of the negative supply rail. (See the *Electrical Characteristics* table for further information).

Each buffer is capable of full-scale change in output voltage in less than 4µs; see Figure 4, typical characteristic *Full-Scale Output Swing*.

The BUF12800 uses an analog supply of 7V to 18V and a digital supply of 2.3V to 5.5V. The digital supply *must* be applied prior to or simultaneously with the analog supply to avoid excessive current and power consumption; damage to the device may occur if it is left connected only to the analog supply for an extended time.

Figure 7 shows the BUF12800 in a typical configuration. In this configuration, the BUF12800 device address is 74h. The output of each DAC is immediately updated as soon as data are received in the corresponding register (LD = 0). For maximum dynamic range, set $V_{REFH} = V_S - 0.2V$ and $V_{REFL} = V_S + 0.2V$.



(1) RC combination optional.
(2) GND_D and GND_A are internally connected and must be at the same voltage potential.

Figure 7. Typical Application Configuration

TWO-WIRE BUS OVERVIEW

The BUF12800 communicates through an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and 8 bits of data are sent followed by an Acknowledge Bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH will be interpreted as a START or STOP condition.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH while SCL is HIGH.

The BUF12800 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF12800.

ADDRESSING THE BUF12800

The address of the BUF12800 is 111010x, where *x* is the state of the A0 pin. When the A0 pin is LOW, the device will acknowledge on address 74h (1110100). If the A0 pin is HIGH, the device will acknowledge on address 75h (1110101).

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF12800 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001xxx, with SCL = 400kHz, following the START condition; *xxx* are bits unique to the Hs-capable master, which can be any value. The BUF12800 will respond to the High-speed mode command regardless of the value of these last three bits. This byte is called the Hs master code. (Note that this is different from normal address bytes—the low bit does not indicate read/write status.) The BUF12800 will not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. On receiving a master code, the BUF12800 will switch on its Hs mode filters, and communicate at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF12800 will switch out of Hs mode at the first occurrence of a STOP condition.

GENERAL CALL RESET AND POWER-UP

The BUF12800 responds to a General Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF12800 acknowledges both bytes. Upon receiving a General Call Reset, the BUF12800 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General Call address byte of 00h (0000 0000), but does not acknowledge any General Call data bytes other than 06h (0000 0110).

When the BUF12800 powers up, it automatically performs a reset. As part of the reset, the BUF12800 is configured based on the codes shown in Table 1.

Table 1. BUF12800 Reset Codes

	RESET CODES		
BUFFER	**(Hex)**	**(Decimal)**	**(Binary)**
BUFFER A	Code 3E0	992	11 1110 0000
BUFFER B	Code 360	864	11 0110 0000
BUFFER C	Code 320	800	11 0010 0000
BUFFER D	Code 300	768	11 0000 0000
BUFFER E	Code 2C0	704	10 1100 0000
BUFFER F	Code 240	576	10 0100 0000
BUFFER G	Code 1C0	448	01 1100 0000
BUFFER H	Code 140	320	01 0100 0000
BUFFER I	Code 100	256	01 0000 0000
BUFFER J	Code 0E0	224	00 1110 0000
BUFFER K	Code 0A0	160	00 1010 0000
BUFFER L	Code 020	32	00 0010 0000

Buffer values are calculated using Equation 1:

$$V_{OUT} = \left[\frac{V_{REFH} - V_{REFL}}{1024} \times \text{decimal value of code}\right] + V_{REFL} \quad (1)$$

Other reset values are available as a custom modification—contact your TI representative for details.

OUTPUT VOLTAGE

Buffer output values are determined by the reference voltages (V_{REFH} and V_{REFL}) and the decimal value of the binary input code used to program that buffer. The value is calculated using Equation 1; see the *Reset and Power-Up* section. The valid voltage ranges for the reference voltages are:

$$4V \le V_{REFH} \le V_S - 0.2V \text{ and } 0.2V \le V_{REFL} \le V_S - 4V$$

The BUF12800 outputs are capable of a full-scale voltage output change in less than 4µs—no intermediate steps are required.

READ/WRITE OPERATIONS

The BUF12800 is able to read from a single DAC or multiple DACs, or write to the register of a single DAC, or multiple DACs in a single communication transaction. DAC addresses begin with 0000, which corresponds to DAC_A, through 1011, which corresponds to DAC_L. Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH will perform a read transaction.

Writing

To write to a single DAC register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12800 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D4 are unused and should be set to 0. Bits D3−D0 are the DAC address. Only DAC addresses 0000 to 1011 are valid and will be acknowledged.
4. Send two bytes of data for the specified DAC. Begin by sending the most significant byte first (bits D15−D8, of which only bits D9 and D8 are used), followed by the least significant byte (bits D7−D0). The DAC register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF12800 will acknowledge each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register will not be updated. Updating the DAC register is not the same as updating the DAC output voltage. See the *Output Latch* section.

The process of updating multiple registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master will continue to send data for the next register. The BUF12800 will automatically and sequentially step through subsequent registers as additional data is sent. The process will continue until all desired registers have been updated or a STOP condition is sent.

To write to multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12800 will acknowledge this byte.
3. Send either the DAC_A address byte to start at the first DAC or send the address of whichever DAC will be the first to be updated. The BUF12800 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the bytes of data. The first two bytes are for the DAC addressed in step 3. Its register is automatically updated after receiving the second byte. The next two bytes are for the following DAC. The DAC register is updated after receiving the fourth byte. The last two bytes are for DAC_L. The DAC register is updated after receiving the 24th byte. For each DAC, begin by sending the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning), followed by the least significant byte (bits D7−D0).
5. Send a STOP condition on the bus.

The BUF12800 will acknowledge each byte. To terminate communication, send a STOP or START condition on the bus. Only DACs that have received both bytes will be updated.

Reading

To read the register of one DAC:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12800 will acknowledge this byte.
3. Send a DAC address byte. Bits D7−D4 have no meaning; Bits D3−D0 are the DAC address. Only DAC addresses 0000 to 1011 are valid and will be acknowledged.
4. Send a START or STOP/START condition on the bus.
5. Send correct device address and read/write bit = HIGH. The BUF12800 will acknowledge this byte.
6. Receive two bytes of data. They are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning); the next is the least significant byte (bits D7−D0).
7. Acknowledge after receiving each byte.
8. Send a STOP condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

To read multiple DAC registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF12800 will acknowledge this byte.
3. Send either the DAC_A address byte to start at the first DAC or send the address byte for whichever DAC will be the first in the sequence of DACs to be read. The BUF12800 will begin with this DAC and step through subsequent DACs in sequential order.
4. Send the device address and read/write bit = HIGH.
5. Receive bytes of data. The first two bytes are for the specified DAC. The first received byte is the most significant byte (bits D15−D8, of which only bits D9 and D8 have meaning). The next byte is the least significant byte (bits D7−D0).
6. Acknowledge after receiving each byte.
7. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge.

TIMING DIAGRAMS

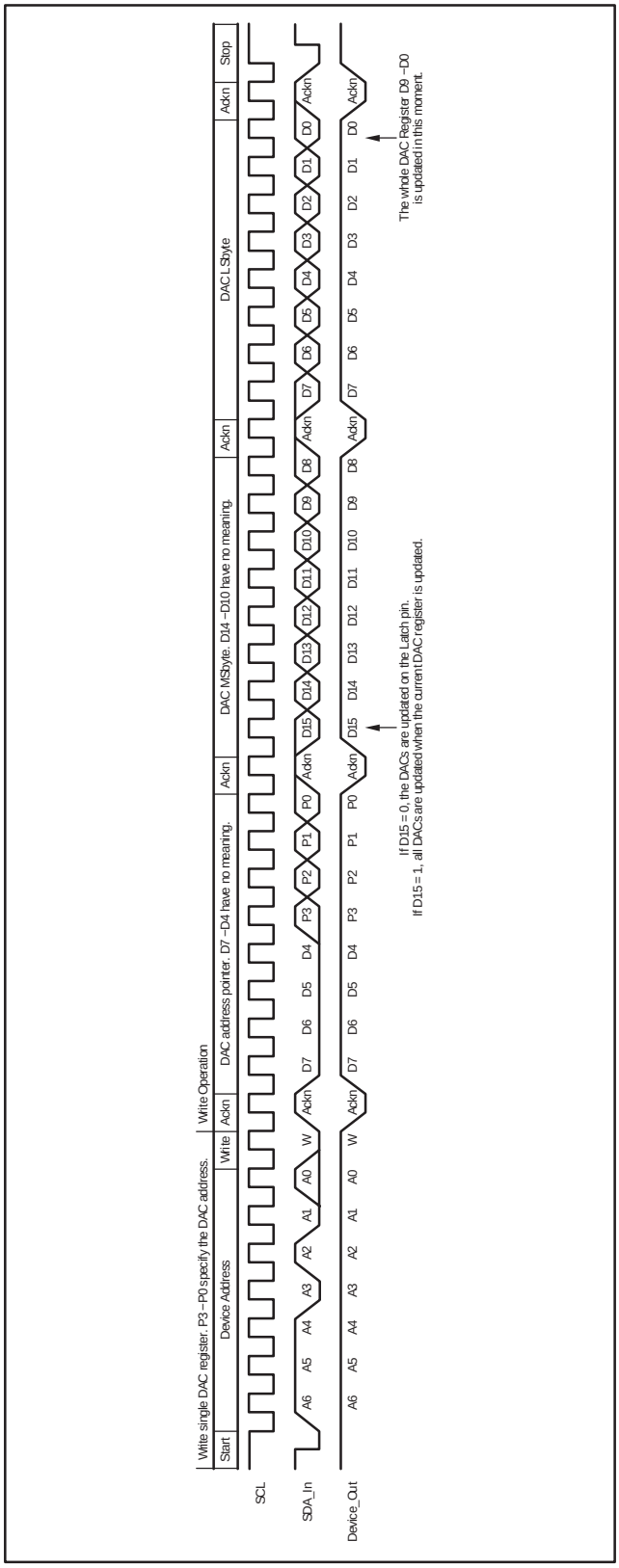


Figure 8. Write Single DAC Register

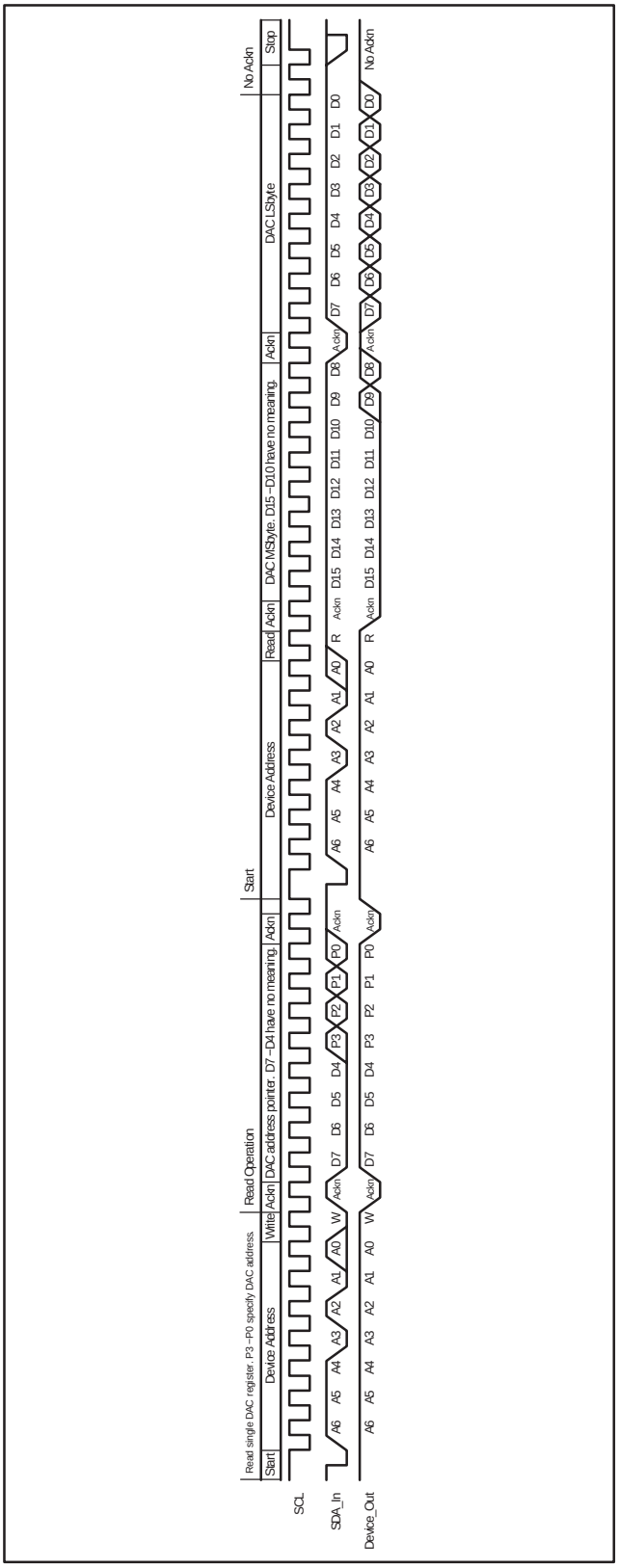


Figure 9. Read Single DAC Register

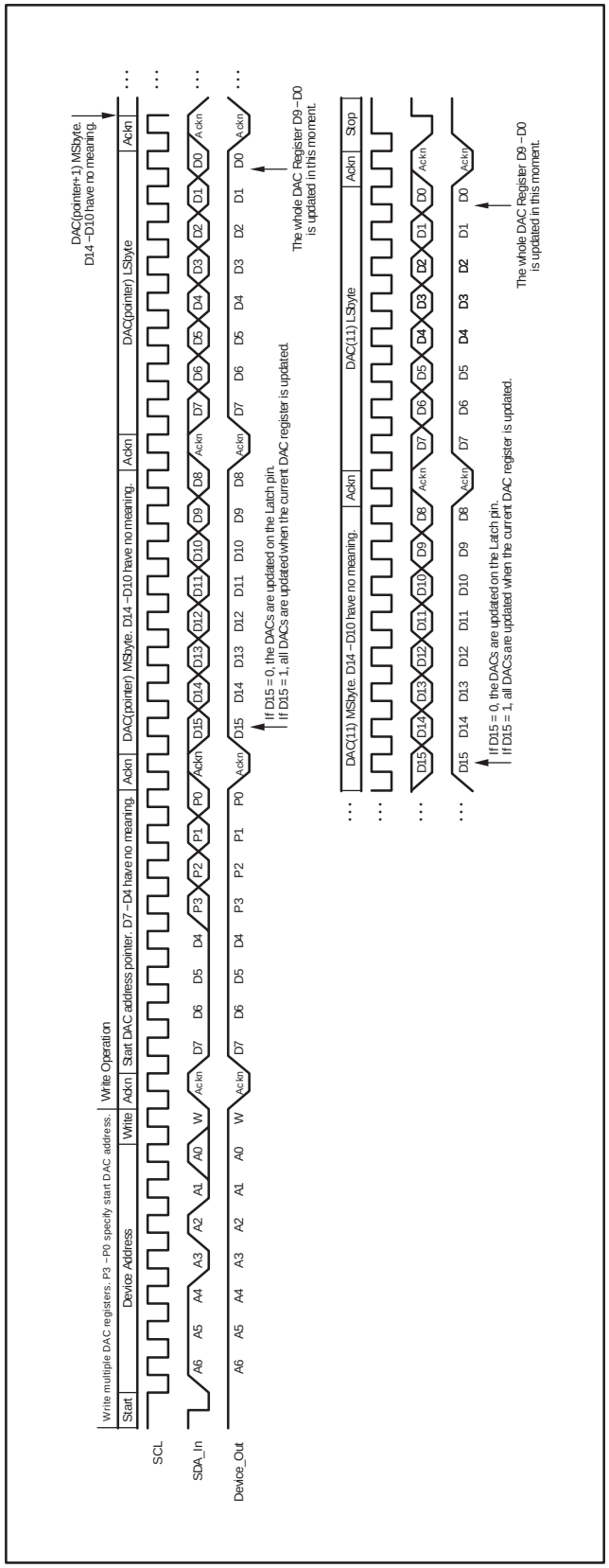


Figure 10. Write Multiple DAC Registers

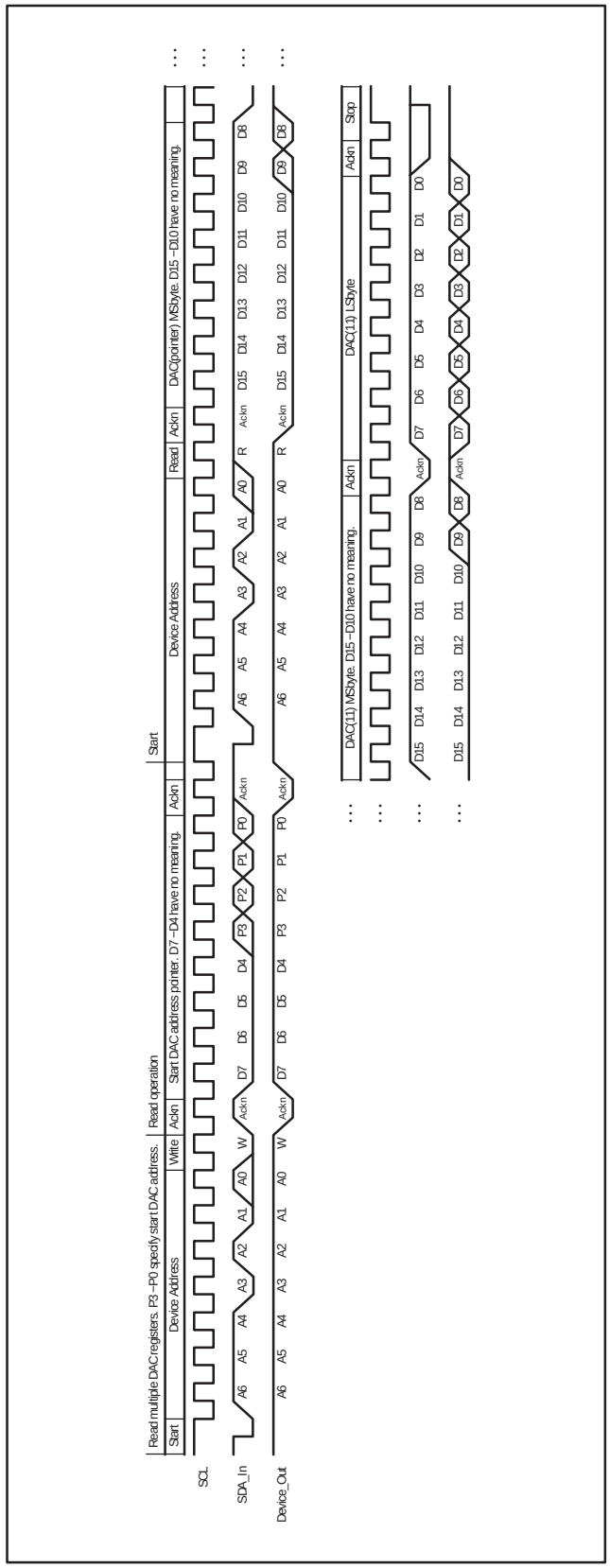


Figure 11. Read Multiple DAC Registers

OUTPUT LATCH

Because the BUF12800 features a double-buffered register structure, updating the DAC register is not the same as updating the DAC output voltage. There are three methods for latching transferred data from the storage registers into the DACs to update the DAC output voltage.

Method 1 requires externally setting the latch pin low, LD = LOW, which will update each DAC output voltage whenever its corresponding register is updated.

Method 2 externally sets LD = HIGH to allow all DAC output voltages to retain their values during data transfer and until LD = LOW, which will simultaneously update the output voltages of all 12 DACs to the new register values.

Method 3 uses software control. LD is maintained HIGH, and all 12 DACs are updated when the master writes a ‘1’ in bit 15 of any DAC register. The update will occur after receiving the 16-bit data for the currently-written register.

Use methods 2 and 3 to transfer a future data set into the first bank of registers in advance to prepare for a very fast update of DAC output voltages.

The General Call Reset and the power-up reset will update the DACs regardless of the state of the latch pin.

Table 2. BUF12800 Bus Address Options

BUF12800 ADDRESS	ADDRESS
A0 Pin is LOW (device will acknowledge on address 74h)	111 0100
A0 Pin is HIGH (device will acknowledge on address 75h)	111 0101

Table 3. Quick-Reference Table of DAC Addresses

DAC	ADDRESS
DAC A	0000 0000
DAC B	0000 0001
DAC C	0000 0010
DAC D	0000 0011
DAC E	0000 0100
DAC F	0000 0101
DAC G	0000 0110
DAC H	0000 0111
DAC I	0000 1000
DAC J	0000 1001
DAC K	0000 1010
DAC L	0000 1011

Table 4. Quick-Reference Table of Commands

COMMAND	CODE
General Call Reset	Address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110).
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code.

DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD TV applications. The brightness in each picture frame is analyzed and the gamma curves are adjusted on a frame-by-frame basis. The gamma curves are typically updated during the short vertical blanking period in the video signal. Figure 12 shows a block diagram using the BUF12800 for dynamic gamma control.

The BUF12800 is ideally suited for rapidly changing the gamma curves due to its unique topology:

- double register input structure to the DAC
- fast serial interface
- simultaneous updating of all DACs by software. See the *Read/Write Operations* to write to all registers and *Output Latch* sections.

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data is only stored into the first register bank, the DAC output values remain unchanged—the display is unaffected. During the vertical sync period, the DAC outputs (and therefore, the gamma voltages) can be quickly updated either by using an additional control line connected to the LD pin, or through software—writing a ‘1’ in bit 15 of any DAC register. For details on the operation of the double register input structure, see the *Output Latch* section.

Example: Update all 12 registers simultaneously via software.

Step 1: Check if LD pin is placed in HIGH state.

Step 2: Write DAC Registers 1−12 with bit 15 always 0.

Step 3: Write any DAC register a second time with identical data. Make sure that bit 15 is ‘1’. All DAC channels will be updated simultaneously after receiving the last bit of data.

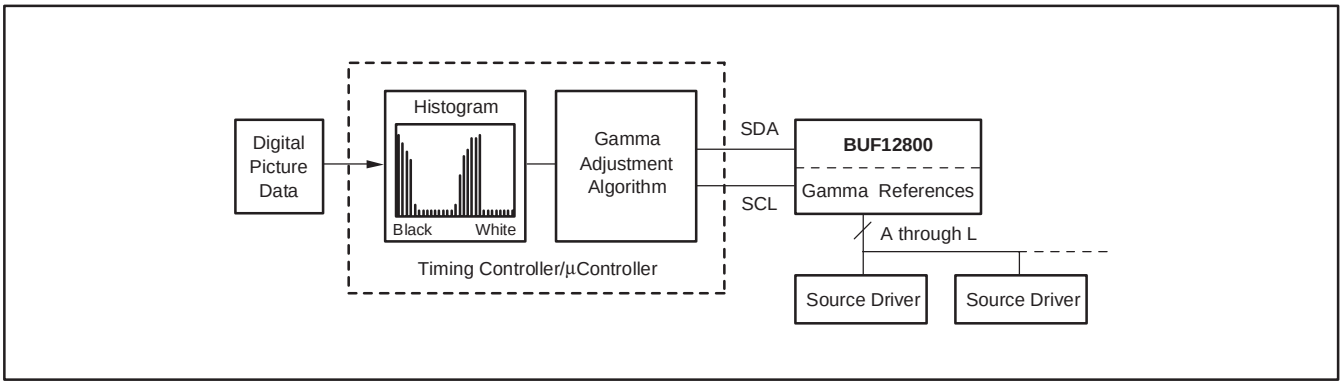


Figure 12. Dynamic Gamma Control

REPLACEMENT OF TRADITIONAL GAMMA BUFFER

Traditional gamma buffers rely on a resistor string (often using expensive 0.1% resistors) to set the gamma voltages. During development, the optimization of these gamma voltages can be time consuming. Programming these gamma voltages with the BUF12800 can significantly reduce the time required for gamma voltage optimization. The final gamma values can be written into an external EEPROM to replace a traditional gamma buffer solution. During power-up of the LCD panel, the timing controller can read the EEPROM and load the values into the BUF12800 to generate the desired gamma voltages. Figure 13a shows the traditional resistor string; Figure 13b shows the more efficient alternative method using the BUF12800.

BUF12800 uses the most advanced high-voltage CMOS process available today, which allows it to be competitive with traditional gamma buffers.

This technique offers significant advantages:

- It shortens development time significantly.
- It allows demonstration of various gamma curves to LCD monitor makers by simply *uploading* a different set of gamma values.
- It allows simple adjustment of gamma curves during production to accommodate changes in the panel manufacturing process.
- It decreases cost and space.

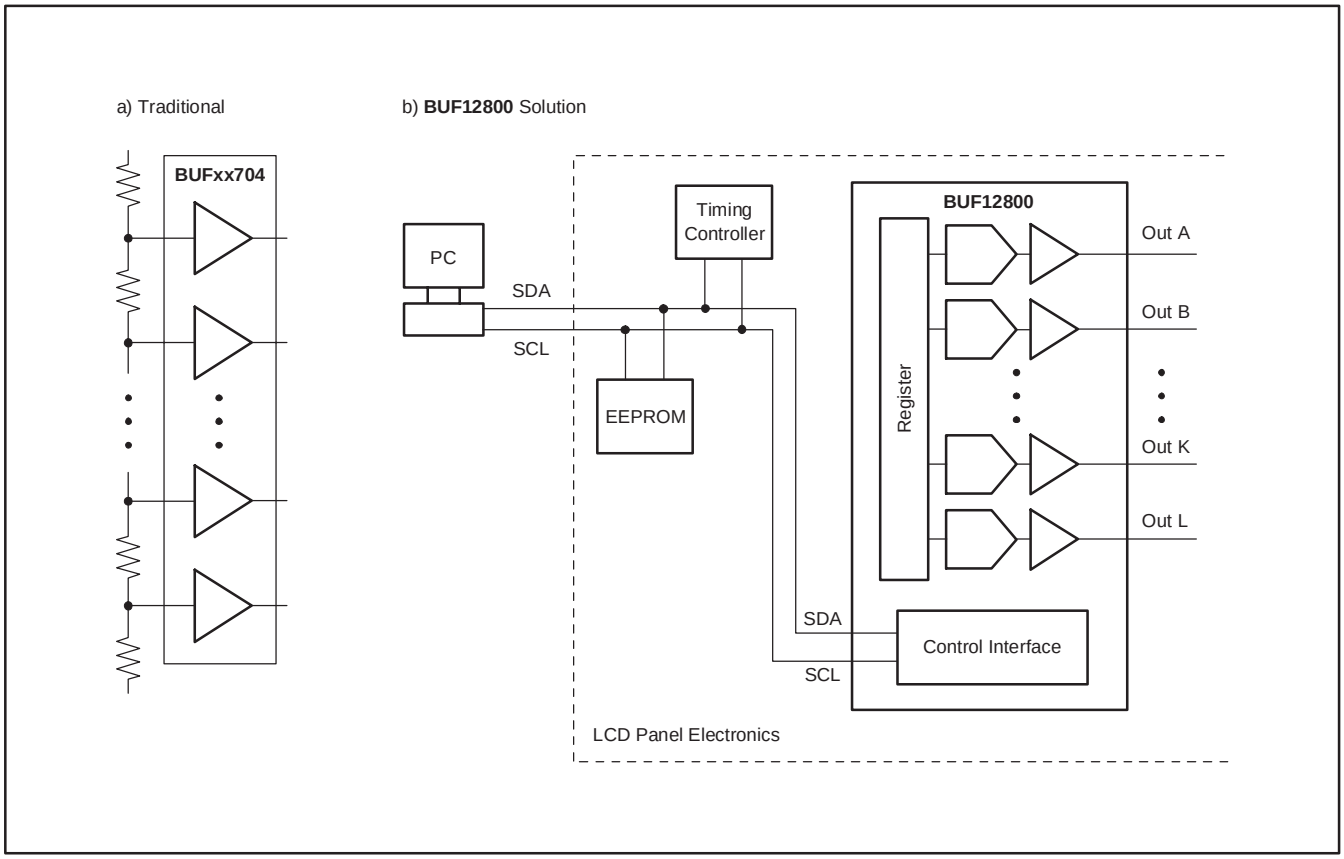


Figure 13. Replacement of Traditional Gamma Buffer

PROGRAMMABLE V_{COM}

Channels A−F of the BUF12800 can drive more than 100mA up to 2V to the supply rails (see Figure 4, typical characteristic *Output Voltage vs Output Current*). Therefore, any of these channels can be used to drive the V_{COM} node on the LCD panel. To store the gamma and the V_{COM} values, an external EEPROM is required. During power-up of the LCD panel, the timing controller can then read the EEPROM and load the values into the BUF12800 to generate the desired gamma voltages as well as V_{COM} voltages. Figure 14 shows channels A and B of the BUF12800 being used for V_{COM} voltages.

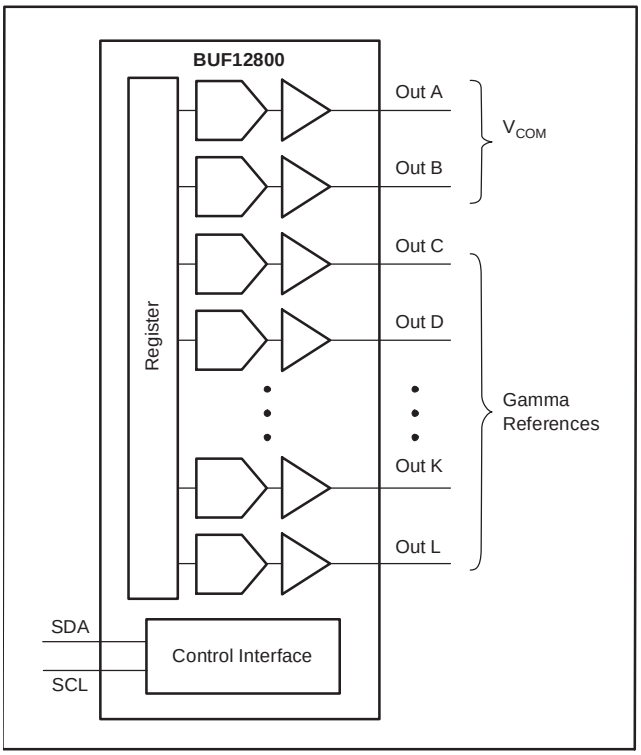


Figure 14. BUF12800 Used for Programmable V_{COM}

REFH AND REFL INPUT RANGE

Best performance and output swing range of the BUF12800 are achieved by applying REFH and REFL voltages that are slightly below the power-supply voltages. Most specifications have been tested at REFH = V_S − 200mV and REFL = GND + 200mV. The REFH internal buffer is designed to swing very closely to V_S and the REFL internal buffer to GND. However, there is a finite limit on how close they can swing before saturating. To avoid saturation of the internal REFH and REFL buffers, the REFH voltage should not be greater than V_S − 100mV and REFL voltage should not be lower than GND + 100mV. The other consideration when trying to maximize the output swing capability of the gamma buffers is the limitation in the swing range of output buffers (OUT A−L), which depends on the load current. A typical load in the LCD application is 5−10mA. For example, if OUT A is sourcing 10mA, the swing is typically limited to about V_S − 200mV. The same applies to OUT L, which typically limits at GND + 200mV when sinking 10mA. An increase in output swing can only be achieved for much lighter loads. For example, a 3mA load typically allows the swing to be increased to approximately V_S − 100mV and GND + 100mV.

Connecting REFH directly to V_S and REFL directly to GND does not damage the BUF12800. However, as discussed above, the output stages of the REFH and REFL buffers will saturate. This condition is not desirable and can result in a small error in the measured output voltages of OUT A−L. As described above, this method of connecting REFH and REFL does not help to maximize the output swing capability.

INDEPENDENTLY PROGRAMMABLE RGB GAMMA: BUF20800

Some very high resolution LCD screens require the adjustment of the gamma voltages for each color (Red—R, Green—G, Blue—B). The BUF20800 offers 20 programmable gamma channels. By using 6 channels for each color, 18 channels would be used in total for adjusting the gamma. In addition to those, 1 or 2 channels could be used to program V_{COM}.

TOTAL TI PANEL SOLUTION

In addition to the BUF12800 programmable voltage reference, TI offers a complete set of ICs for the LCD panel market, including gamma correction buffers, source and gate drivers, timing controllers, various power-supply solutions, and audio power solutions. Figure 15 shows the total IC solution from TI.

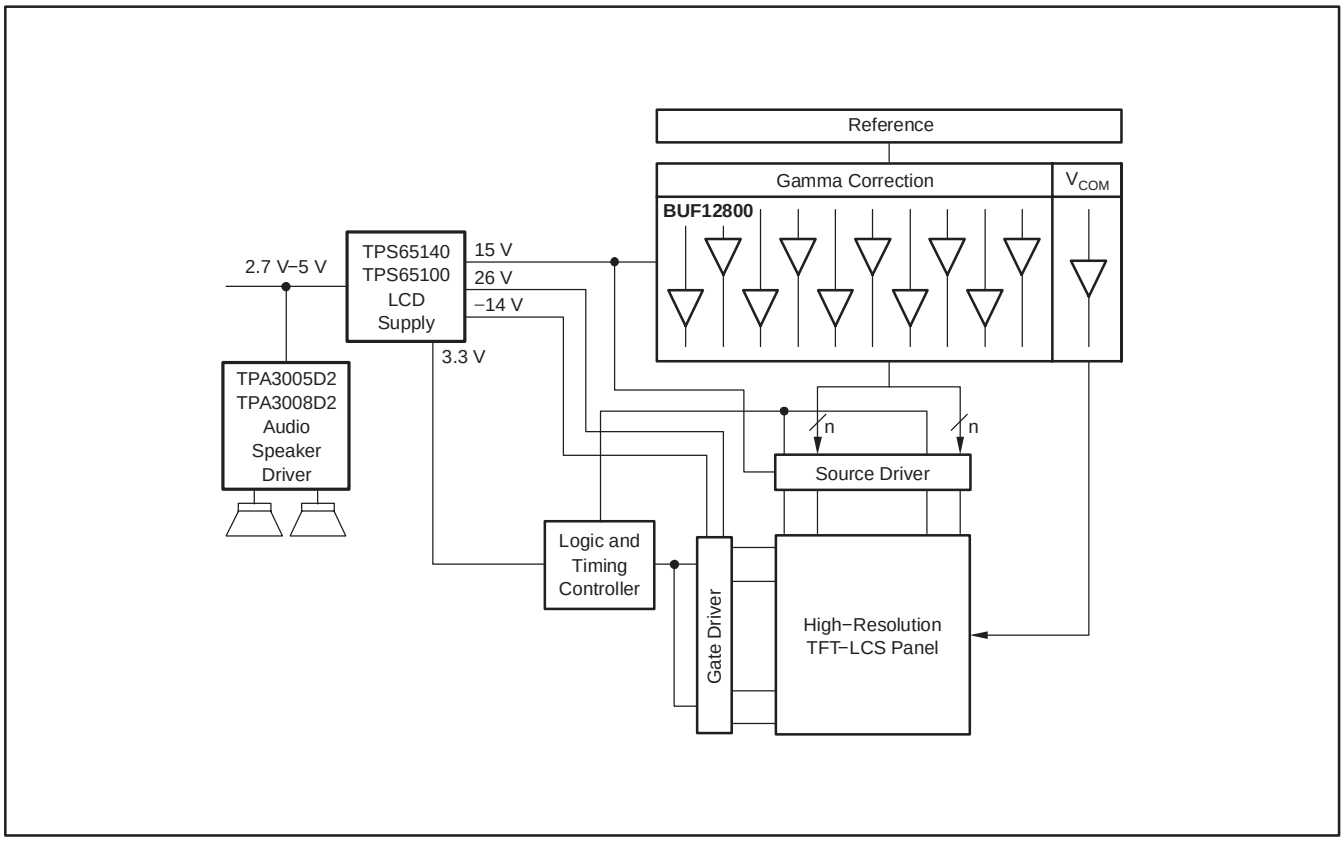


Figure 15. TI LCD Solution

BUF12800 IN INDUSTRIAL APPLICATIONS

The wide supply range, high output current and very low cost make the BUF12800 attractive for a range of medium accuracy industrial applications such as programmable power supplies, multi-channel data-acquisition systems, data loggers, sensor excitation and linearization, power-supply generation, and others. Each DAC channel features 1LSB DNL and INL.

Many systems require different levels of biasing and power supply for various components as well as sensor excitation, control-loop set-points, voltage outputs, current outputs, and other functions. The BUF12800, with its 12 programmable DAC channels, provides great flexibility to the whole system by allowing the designer to change all these parameters via software.

Figure 16 provides ideas on how the BUF12800 can be used in an application. A microcontroller with a two-wire serial interface controls the various DACs of the BUF12800. The BUF12800 can be used for:

- sensor excitation
- programmable bias/reference voltages
- variable power-supplies
- high-current voltage output
- 4-20mA output
- set-point generators for control loops.

NOTE: At power-up the output voltages of the BUF12800 DACs are pre-defined by the codes in Table 1. Therefore, each DAC voltage will be set to a different level at power-up or reset.

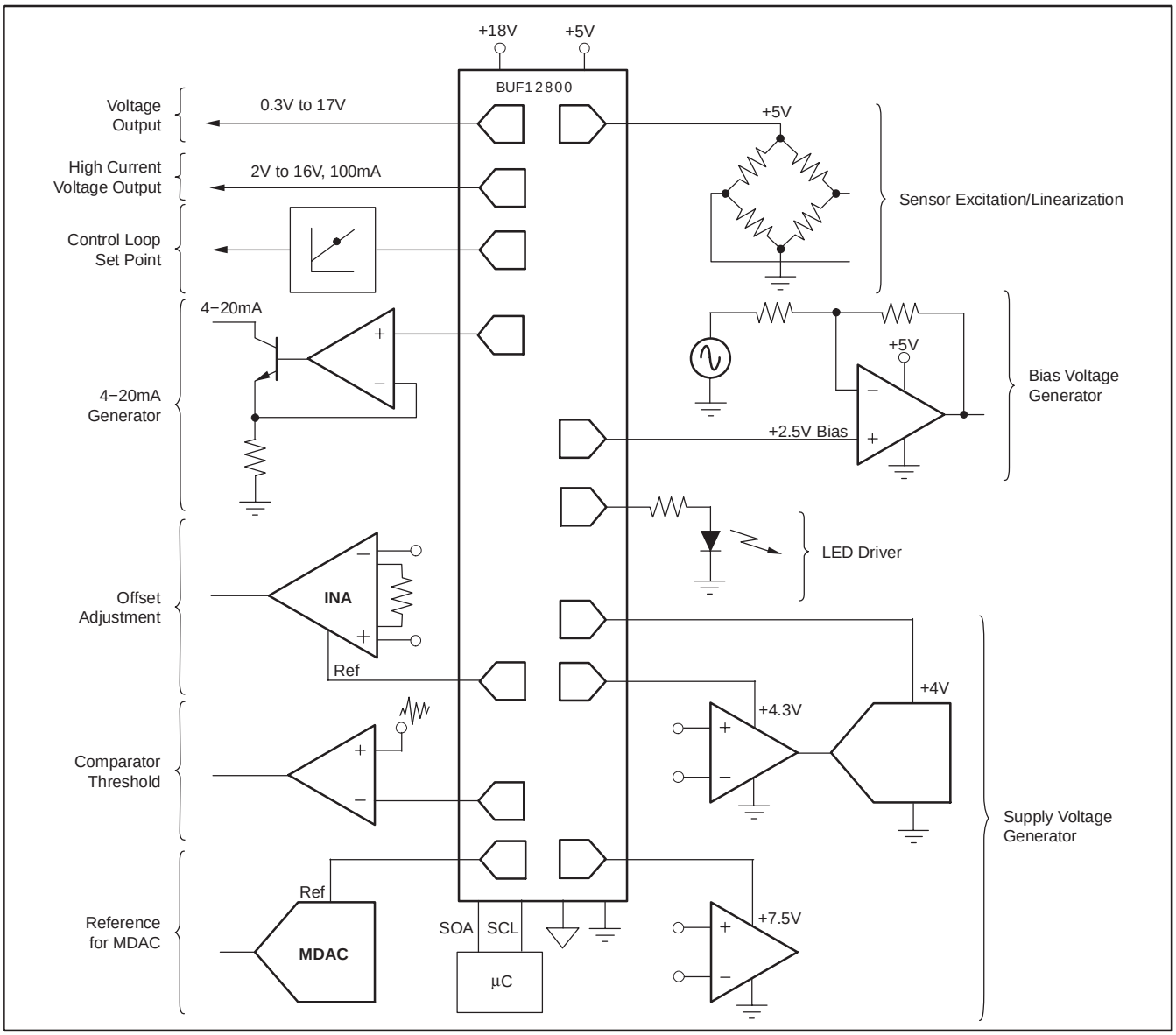


Figure 16. Industrial Application Ideas

GENERAL PowerPAD DESIGN CONSIDERATIONS

The BUF12800 is available in the thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted, as shown in Figure 17(a) and (b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see Figure 17(c). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. **Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.** This provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the device's most negative supply voltage, GND_A and GND_D.

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns (2x4) can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package* (SLMA002), available for download at www.ti.com. These holes should be 13 mils (0.330mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF12800 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF12800 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its eight holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF12800 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

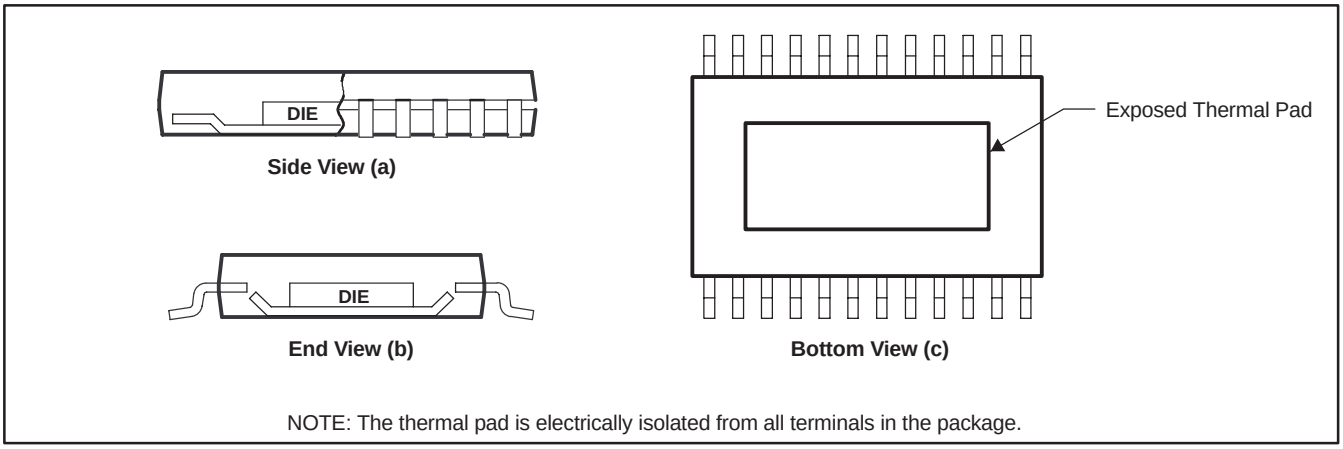


Figure 17. Views of Thermally-Enhanced DGN Package

For a given θ_{JA}, the maximum power dissipation is shown in Figure 18, and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = maximum power dissipation (W)

T_{MAX} = absolute maximum junction temperature (125°C)

T_A = free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = thermal coefficient from junction to case (°C/W)

θ_{CA} = thermal coefficient from case-to-ambient air (°C/W)

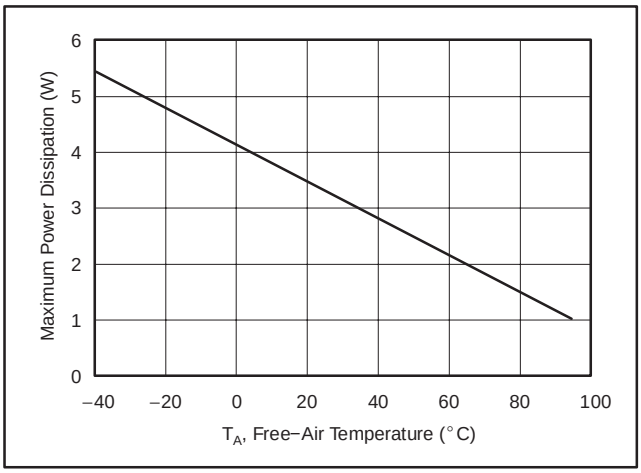


Figure 18. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF12800AIPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF12800	Samples
BUF12800AIPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF12800	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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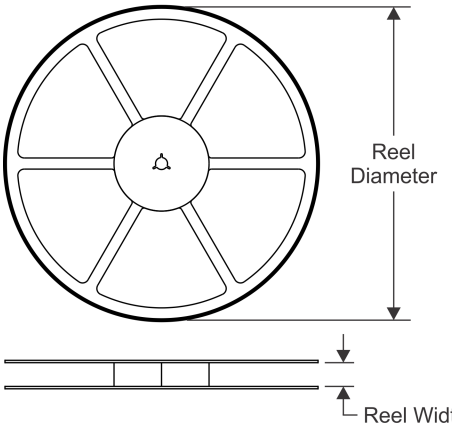
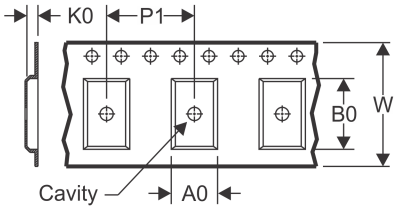
TAPE AND REEL INFORMATION

REEL DIMENSIONS

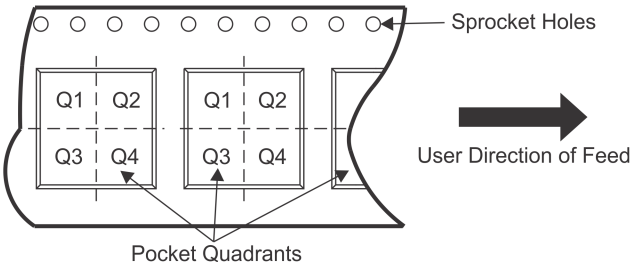


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

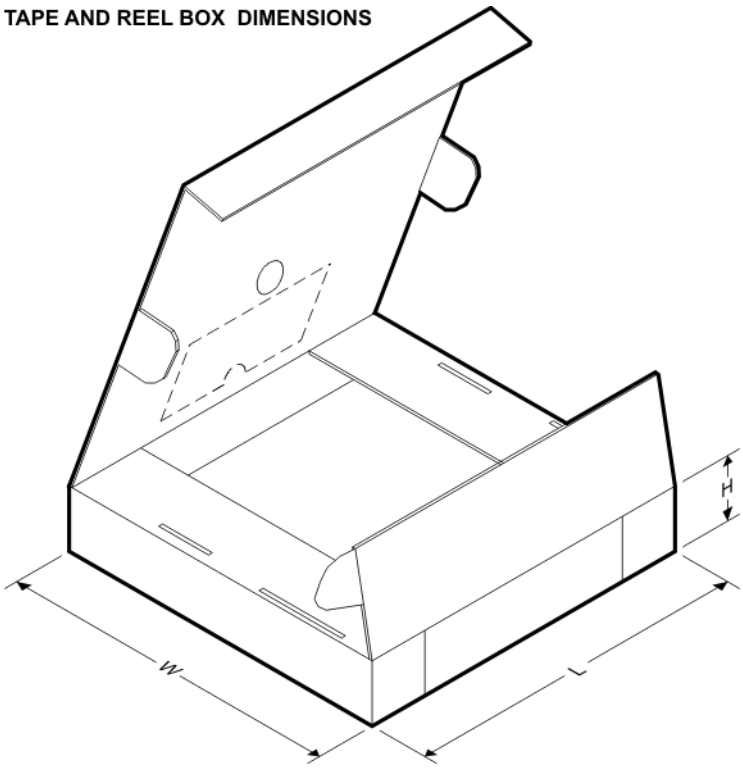
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF12800AIPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF12800AIPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

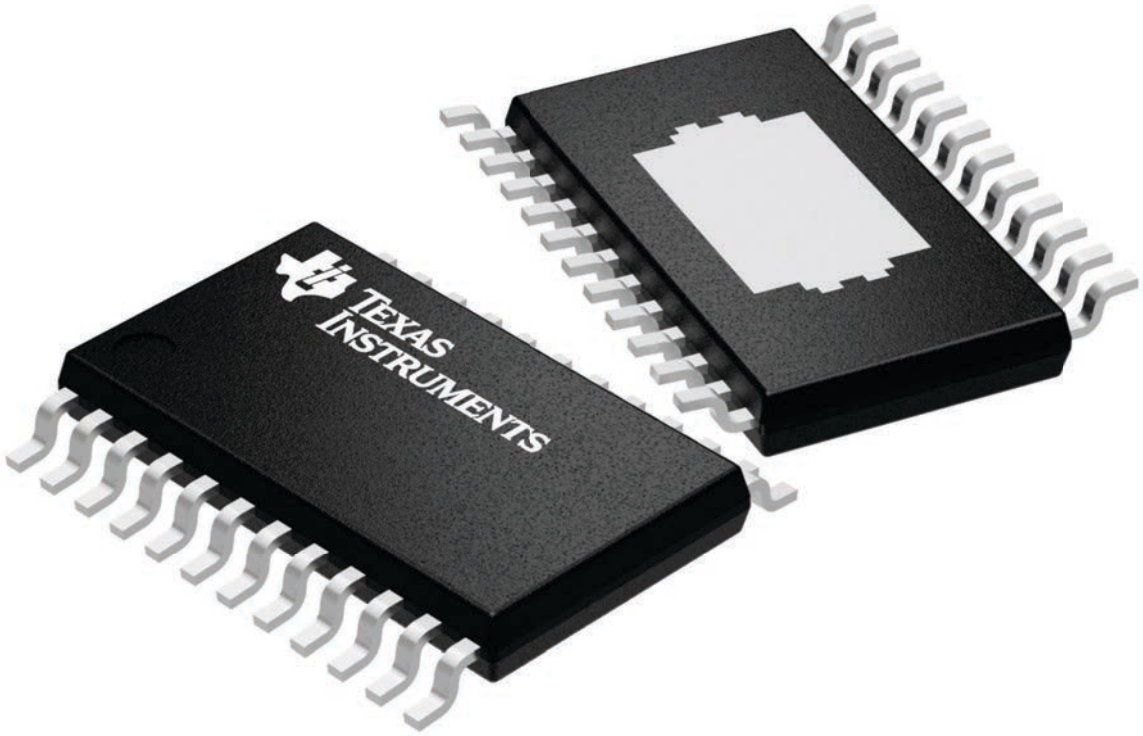
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

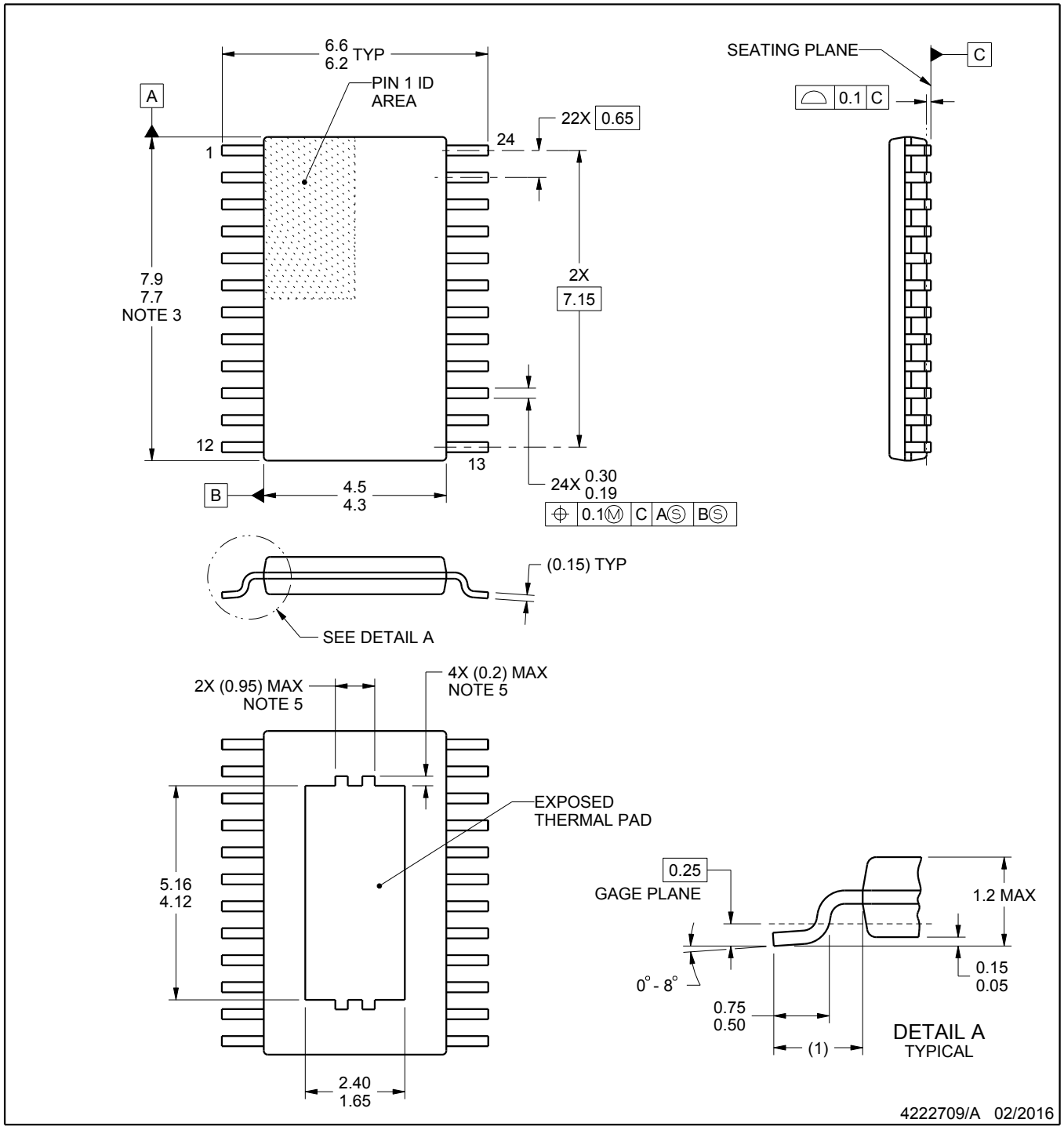
4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



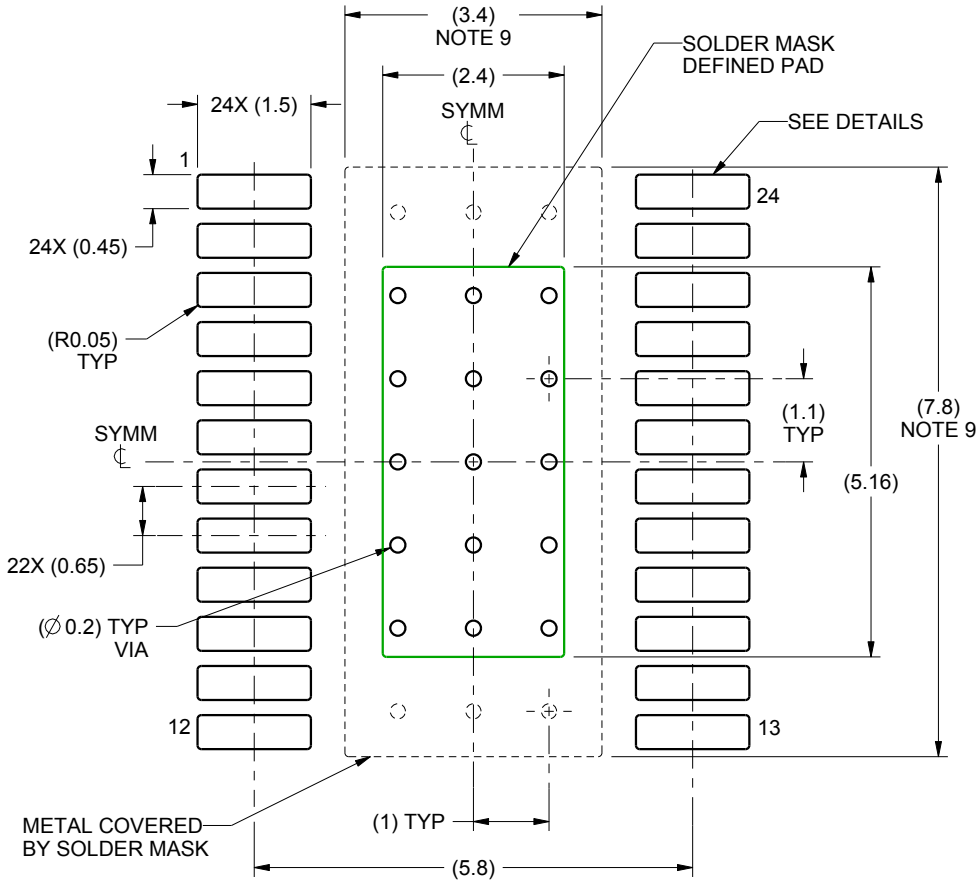
4224742/B



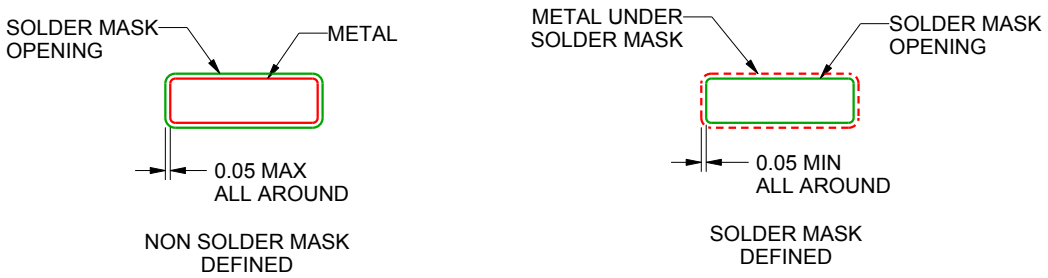
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X

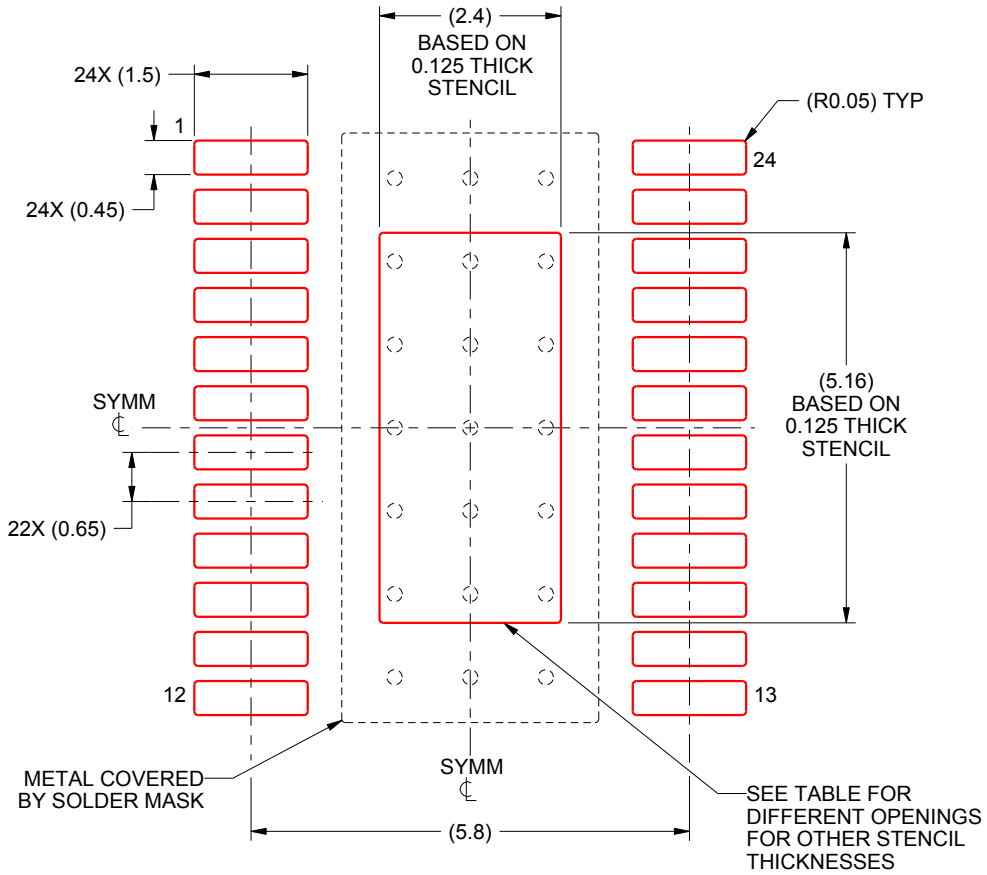


SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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