Low Power IEEE 802.15.4 Zero-IF 2.4 GHz Transceiver IC

ADF7241

FEATURES

- Frequency range (global ISM band)
  - 2400 MHz to 2483.5 MHz
- IEEE 802.15.4-2006-compatible (250 kbps)
- Low power consumption
  - 19 mA (typical) in receive mode
  - 21.5 mA (typical) in transmit mode (P_O = 3 dBm)
  - 1.7 µA, 32 kHz crystal oscillator wake-up mode
- High sensitivity
  - −95 dBm at 250 kbps
- Programmable output power
  - −20 dBm to +4.8 dBm in 2 dB steps
- Integrated voltage regulators
  - 1.8 V to 3.6 V input voltage range
- Excellent receiver selectivity and blocking resilience
  - Zero-IF architecture
  - Complies with EN300 440 Class 2, EN300 328, FCC CFR47 Part 15, ARIB STD-T66
- Digital RSSI measurement
- Fast automatic VCO calibration
- Automatic RF synthesizer bandwidth optimization
- On-chip low power processor performs
  - Radio control
  - Packet management
- Packet management support
  - Insertion/detection of preamble address/SFD/FCS
  - IEEEE 802.15.4-2006 frame filtering
  - IEEEE 802.15.4-2006 CSMA/CA unslotted modes
- Flexible 256-byte transmit/receive data buffer
- SPORT mode
- Flexible multiple RF port interface
  - External PA/LNA support hardware
  - Switched antenna diversity support
- Wake-up timer
- Very few external components
  - Integrated PLL loop filter, receive/transmit switch, battery monitor, temperature sensor, 32 kHz RC and crystal oscillators
- Flexible SPI control interface with block read/write access
- Small form factor 5 mm × 5 mm 32-lead LFCSP package

APPLICATIONS

- Wireless sensor networks
- Automatic meter reading/smart metering
- Industrial wireless control
- Healthcare
- Wireless audio/video
- Consumer electronics
- ZigBee

FUNCTIONAL BLOCK DIAGRAM

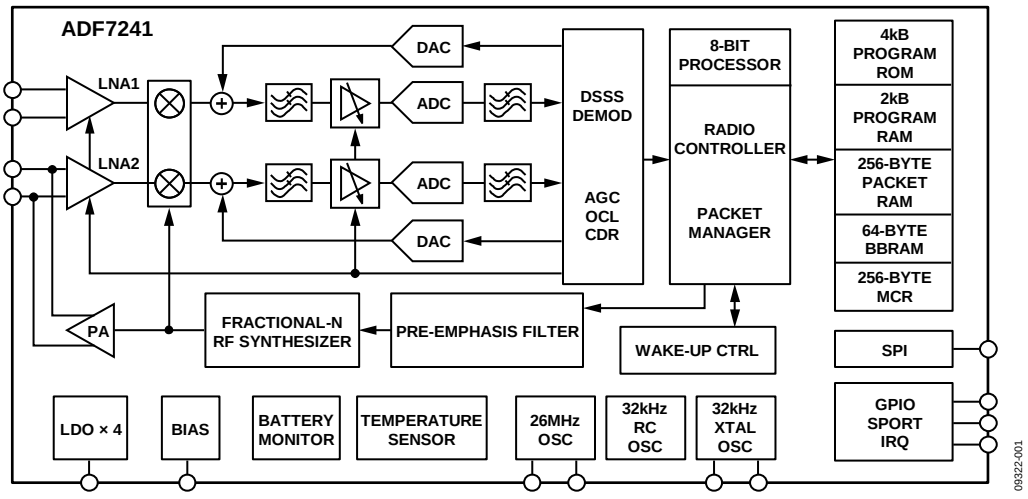


Figure 1.

Rev. 0

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REVISION HISTORY

1/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7241 is a highly integrated, low power, and high performance transceiver for operation in the global 2.4 GHz ISM band. It is designed with emphasis on flexibility, robustness, ease of use, and low current consumption. The IC supports the IEEE 802.15.4-2006 2.4 GHz PHY requirements in both packet and data streaming modes. With a minimum number of external components, it achieves compliance with the FCC CFR47 Part 15, ETSI EN 300 440 (Equipment Class 2), ETSI EN 300 328 (FHSS, DR > 250 kbps), and ARIB STD T-66 standards.

The ADF7241 complies with the IEEE 802.15.4-2006 2.4 GHz PHY requirements with a fixed data rate of 250 kbps and DSSS-OQPSK modulation. The transmitter path of the ADF7241 is based on a direct closed-loop VCO modulation scheme using a low noise fractional-N RF frequency synthesizer. The automatically calibrated VCO operates at twice the fundamental frequency to reduce spurious emissions and avoid PA pulling effects. The bandwidth of the RF frequency synthesizer is automatically optimized for transmit and receive operations to achieve best phase noise, modulation quality, and synthesizer settling time performance. The transmitter output power is programmable from −20 dBm to +4 dBm with automatic PA ramping to meet transient spurious specifications. An integrated biasing and control circuit is available in the IC to significantly simplify the interface to external PAs.

The receive path is based on a zero-IF architecture enabling very high blocking resilience and selectivity performance, which are critical performance metrics in interference dominated environments such as the 2.4 GHz band. In addition, the architecture does not suffer from any degradation of blocker rejection in the image channel, which is typically found in low IF receivers. The IC can operate with a supply voltage between 1.8 V and 3.6 V with very low power consumption in receive and transmit modes while maintaining its excellent RF performance, making it especially suitable for battery-powered systems.

The ADF7241 features a flexible dual-port RF interface that can be used with an external LNA and/or PA in addition to supporting switched antenna diversity.

The ADF7241 incorporates a very low power custom 8-bit processor that supports a number of transceiver management functions. These functions are handled by the two main modules of the processor: the radio controller and the packet manager.

The radio controller manages the state of the IC in various operating modes and configurations. The host MCU can use single byte commands to interface to the radio controller. In transmit mode, the packet manager can be configured to add preamble and SFD to the payload data stored in the on-chip packet RAM. In receive mode, the packet manager can detect and generate an interrupt to the MCU upon receiving a valid SFD, and store the received data payload in the packet RAM. A total of 256 bytes of transmit and receive packet RAM space is provided to decouple the over-the-air data rate from the host MCU processing speed. Thus, the ADF7241 packet manager eases the processing burden on the host MCU and saves the overall system power consumption.

In addition, for applications that require data streaming, a synchronous bidirectional serial port (SPORT) provides bit-level input/output data, and has been designed to directly interface to a wide range of DSPs, such as ADSP-21xx, SHARC®, TigerSHARC®, and Blackfin®. The SPORT interface can optionally be used.

The processor also permits the download and execution of a set of firmware modules, which include IEEE 802.15.4 automatic modes, such as node address filtering, as well as unslotted CSMA/CA. Execution code for these firmware modules is available from Analog Devices, Inc.

To further optimize the system power consumption, the ADF7241 features an integrated low power 32 kHz RC wake-up oscillator, which is calibrated from the 26 MHz crystal oscillator while the transceiver is active. Alternatively, an integrated 32 kHz crystal oscillator can be used as a wake-up timer for applications requiring very accurate wake-up timing. A battery backed-up RAM (BBRAM) is available on the IC where IEEE 802.15.4-2006 network node addresses can be retained when the IC is in the sleep state.

The ADF7241 also features a very flexible interrupt controller, which provides MAC-level and PHY-level interrupts to the host MCU. The IC is equipped with a SPI interface, which allows burst mode data transfer for high data throughput efficiency. The IC also integrates a temperature sensor with digital read-back and a battery monitor.

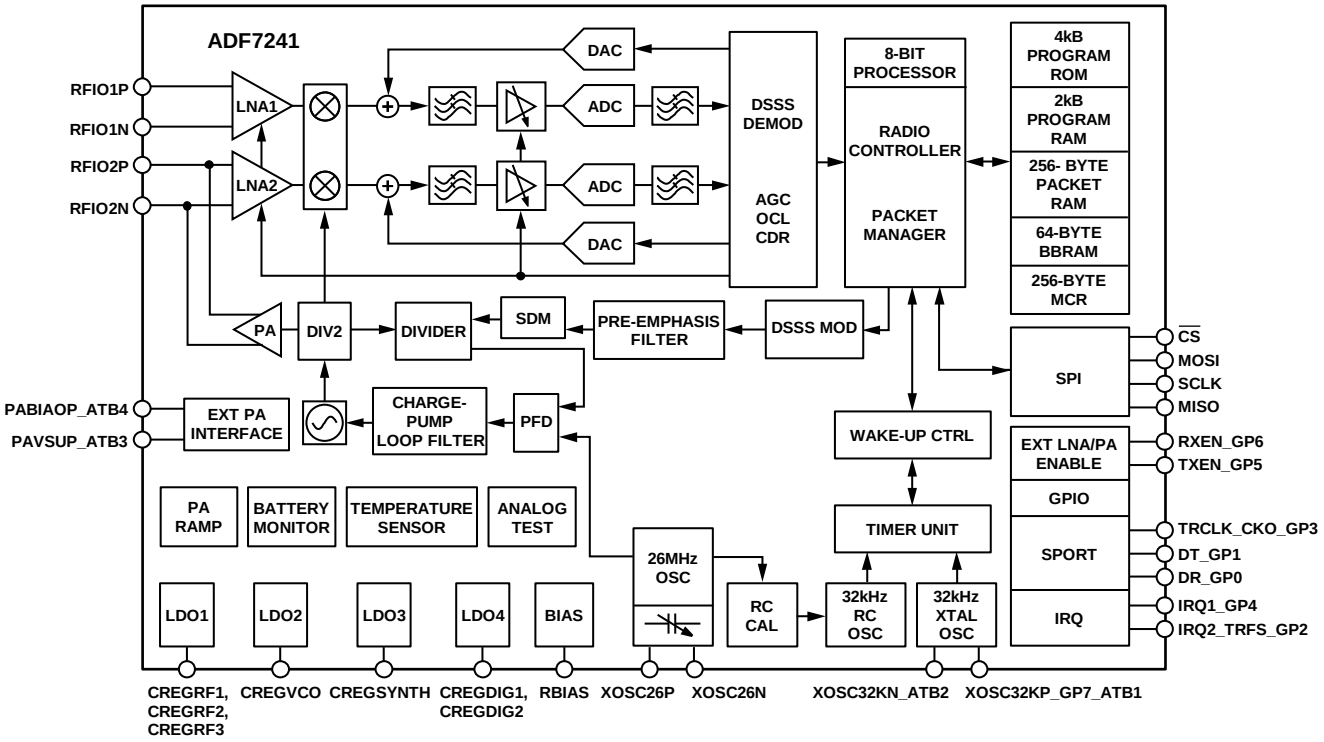


Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

VDD_BAT = 1.8 V to 3.6 V, GND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical specifications are at VDD_BAT = 3.6 V, T_A = 25°C, $f_{CHANNEL}$ = 2450 MHz. All measurements are performed using the ADF7241 reference design, RFIO2 port, unless otherwise noted.

GENERAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
GENERAL PARAMETERS					
Voltage Supply Range					
VDD_BAT Input	1.8		3.6	V	
Frequency Range	2400		2483.5	MHz	
Operating Temperature Range	−40		+85	°C	
Data Rate		250		kbps	

RF FREQUENCY SYNTHESIZER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions
CHANNEL FREQUENCY RESOLUTION		10		kHz	
PHASE ERROR		3		Degrees	Receive mode; integration bandwidth from 10 kHz to 400 kHz
		1.5		Degrees	Transmit mode; integration bandwidth from 10 kHz to 1800 kHz
VCO CALIBRATION TIME		52		µs	Applies to all modes
SYNTHESIZER SETTLING TIME					Frequency synthesizer settled to <±5 ppm of the target frequency within this time following a VCO calibration
		53		µs	Receive mode
		80		µs	Transmit mode
PHASE NOISE					Receive mode
		−135		dBc/Hz	10 MHz frequency offset
		−145		dBc/Hz	≥50 MHz frequency offset
REFERENCE AND CLOCK-RELATED SPURIOUS		70		dBc	Receive mode; $f_{CHANNEL}$ = 2405 MHz, 2450 MHz, and 2480 MHz
INTEGER BOUNDARY SPURS		60		dBc	Receive mode; measured at 400 kHz offset from $f_{CHANNEL}$ = 2405 MHz, 2418 MHz, 2431 MHz, 2444 MHz, 2457 MHz, 2470 MHz
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Maximum Parallel Load Capacitance		18		pF	
Minimum Parallel Load Capacitance		7		pF	
Maximum Crystal ESR		365.3		Ω	Guarantees maximum crystal frequency error of 0.2 ppm; 33 pF on XOSC26P and XOSC26N
Sleep-to-Idle Wake-Up Time		300		µs	15 pF load on XOSC26N and XOSC26P

TRANSMITTER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
TRANSMITTER SPECIFICATIONS					
Maximum Transmit Power		3		dBm	
Minimum Transmit Power		−25		dBm	
Maximum Transmit Power (High Power Mode)		4.8		dBm	Refer to Power Amplifier section for details on how to enable this mode
Minimum Transmit Power (High Power Mode)		−22		dBm	
Transmit Power Variation		2		dB	Transmit power = 3 dBm, $f_{CHANNEL}$ = 2400 MHz to 2483.5 MHz, T_A = −40°C to +85°C, VDD_BAT = 1.8 V to 3.6 V
Transmit Power Control Resolution		2		dB	Transmit power = 3 dBm
Optimum PA Matching Impedance		43.7 + 35.2j		Ω	For maximum transmit power = 3 dBm
Harmonics and Spurious Emissions					
Compliance with ETSI EN 300 440					
25 MHz to 30 MHz			−36	dBm	Unmodulated carrier, 10 kHz RBW[1]
30 MHz to 1 GHz			−36	dBm	Unmodulated carrier, 100 kHz RBW[1]
47 MHz to 74 MHz, 87.5 MHz to 118 MHz, 174 MHz to 230 MHz, 470 MHz to 862 MHz			−54	dBm	Unmodulated carrier, 100 kHz RBW[1]
Otherwise Above 1 GHz			−30	dBm	Unmodulated carrier, 1 MHz RBW[1]
Compliance with ETSI EN 300 328					
1800 MHz to 1900 MHz			−47	dBm	Unmodulated carrier
5150 MHz to 5300 MHz			−97	dBm/Hz	
Compliance with FCC CFR47, Part15					
4.5 GHz to 5.15 GHz			−41	dBm	1 MHz RBW[1]
7.25 GHz to 7.75 GHz			−41	dBm	1 MHz RBW[1]
Transmit EVM		2		%	Measured using Rohde & Schwarz FSU vector analyzer with Zigbee™ option
Transmit EVM Variation		1		%	$f_{CHANNEL}$ = 2405 MHz to 2480 MHz, T_A= −40°C to +85°C, VDD_BAT = 1.8 V to 3.6 V
Transmit PSD Mask		−56		dBm	RBW = 100 kHz; $\|f - f_{CHANNEL}\|$ > 3.5 MHz
Transmit 20 dB Bandwidth		2252		MHz	

[1] RBW = resolution bandwidth.

RECEIVER SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions
GENERAL RECEIVER SPECIFICATIONS					
RF Front-End LNA and Mixer IIP3		−13.6		dBm	At maximum gain, $f_{BLOCKER1}$ = 5 MHz, $f_{BLOCKER2}$ = 10.1 MHz, $P_{RF,IN}$ = −35 dBm
		−12.6		dBm	At maximum gain, $f_{BLOCKER1}$ = 20 MHz, $f_{BLOCKER2}$ = 40.1 MHz, $P_{RF,IN}$ = −35 dBm
		−10.5		dBm	At maximum gain, $f_{BLOCKER1}$ = 40 MHz, $f_{BLOCKER2}$ = 80.1 MHz, $P_{RF,IN}$ = −35 dBm

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Front-End LNA and Mixer IIP2		24.7		dBm	At maximum gain, $f_{BLOCKER1}$ = 5 MHz, $f_{BLOCKER2}$ = 5.5 MHz, $P_{RF,IN}$ = −50 dBm
RF Front-End LNA and Mixer 1 dB Compression Point		−20.5		dBm	At maximum gain
Receiver LO Level at RFIO2 Port		−100		dBm	IEEE 802.15.4 packet mode
LNA Input Impedance at RFIO1x Port		50.2 − 52.2j		Ω	Measured in RX state
LNA Input Impedance at RFIO2x Port		74.3 − 10.7j		Ω	Measured in RX state
Receive Spurious Emissions					
Compliant with EN 300 440					
30 MHz to 1000 MHz			−57	dBm	
1 GHz to 12.75 GHz			−47	dBm	
RECEIVE PATH IEEE 802.15.4-2006 MODE					
Sensitivity ($P_{rf,in,min}$, IEEE 802.15.4)		−95		dBm	1% PER with PSDU length of 20 bytes according to the IEEE 802.15.4-2006 standard
Saturation Level		−15		dBm	1% PER with PSDU length of 20 bytes
CW Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB
±5 MHz		55		dB	
±10 MHz		60		dB	
±20 MHz		63		dB	
±30 MHz		64		dB	
Modulated Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB
±5 MHz		48		dB	
±10 MHz		61		dB	
±15 MHz		62.5		dB	
±20 MHz		65		dB	
±30 MHz		65		dB	
Co-Channel Rejection		−6		dB	$P_{RF,IN} = P_{RF,IN,MIN}$ + 10 dB modulated blocker
Out-of Band Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB, measured at $f_{CHANNEL}$ = 2405 MHz
−5 MHz		−34.2		dBm	
−10 MHz		−30.7		dBm	
−20 MHz		−29.7		dBm	
−30 MHz		−25.7		dBm	
−60 MHz		−24.2		dBm	
					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB, measured at $f_{CHANNEL}$ = 2480 MHz
+5 MHz		−33.4		dBm	
+10 MHz		−29.9		dBm	
+20 MHz		−28.2		dBm	
+30 MHz		−23.7		dBm	
+60 MHz		−29.9		dBm	
Receiver Channel Bandwidth		2252		kHz	Two-sided bandwidth; cascaded analog and digital channel filtering
Frequency Error Tolerance	−80		+80	ppm	$P_{RF,IN} = P_{RF,IN,MIN}$ + 3 dB
RSSI					Measured using IEEE 802.15.4-2006 packet mode
Dynamic range		85		dB	
Accuracy		±3		dB	
Averaging Time		128		µs	
Minimum Sensitivity		−95		dBm	

AUXILIARY SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions
32 kHz RC OSCILLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1		ms	
32 kHz CRYSTAL OSCILLATOR					
Frequency		32.768		kHz	
Maximum ESR		319.8		kΩ	10 pF on XOSC32KP and XOSC32KN
Start-Up Time		2000		ms	12.5 pF load capacitors on XOSC32KP and XOSC32KN
WAKE-UP TIMER					
Prescaler Tick Period	0.0305		20,000	ms	
Wake-Up Period	61×10^{-6}		1.31×10^{5}	sec	
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Resolution		4.7		°C	
Accuracy		±6.4		°C	Average of 1000 ADC readbacks, after using linear fitting, with correction at known temperature
BATTERY MONITOR					
Trigger Voltage	1.7		3.6	V	
Trigger Voltage Step Size		62		mV	
Start-Up Time		5		µs	
Current Consumption		30		µA	
EXTERNAL PA INTERFACE					
R_{ON}, PAVSUP_ATB3 to VDD_BAT		5		Ω	extpa_bias_mode = 0, 1, 2, 5, 6
R_{OFF}, PAVSUP_ATB3 to GND		10		MΩ	extpa_bias_mode = 3, 4, power-down
R_{OFF}, PABIASOP_ATB4 to GND		10		MΩ	extpa_bias_mode = 0, power-down
PABIASOP_ATB4 Source Current, Maximum		80		µA	expta_bias_mode = 1, 3
PABIASOP_ATB4 Sink Current, Minimum		−80		µA	extpa_bias_mode = 2, 4
PABIASOP_ATB4 Current Control Resolution		6		Bits	extpa_bias_mode = 1, 2, 3, 4, 5
PABIASOP_ATB4 Compliance Voltage		150		mV	extpa_bias_mode = 2, 4
PABIASOP_ATB4 Compliance Voltage		3.45		V	extpa_bias_mode = 1, 3
Servo Loop Bias Current		22		mA	extpa_bias_mode = 5, 6
Servo Loop Bias Current Control Step		0.349		mA	extpa_bias_mode = 5, 6

CURRENT CONSUMPTION SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions
CURRENT CONSUMPTION					
TX Mode Current Consumption					
−20 dBm		16.5		mA	IEEE 802.15.4-2006 continuous packet transmission mode
−10 dBm		17.4		mA	IEEE 802.15.4-2006 continuous packet transmission mode
0 dBm		19.6		mA	IEEE 802.15.4-2006 continuous packet transmission mode
+3 dBm		21.5		mA	IEEE 802.15.4-2006 continuous packet transmission mode
+4 dBm		25		mA	IEEE 802.15.4-2006 continuous packet transmission mode
Idle Mode		1.8		mA	XTO26M + digital active
PHY_RDY Mode		10		mA	
RX Mode Current Consumption		19		mA	IEEE 802.15.4-2006 packet mode
MEAS State		3		mA	
SLEEP_BBRAM		0.3		µA	BBRAM contents retained
SLEEP_BBRAM_RCO		1		µA	32 kHz RC oscillator running, some BBRAM contents retained, wake-up time enabled
SLEEP_BBRAM_XTO		1.7		µA	32 kHz crystal oscillator running, some BBRAM contents retained, wake-up time enabled

TIMING AND DIGITAL SPECIFICATIONS

Table 7. Logic Levels

Parameter	Min	Typ	Max	Unit	Test Conditions
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × VDD_BAT			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}		±1		µA	
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	VDD_BAT − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Output Rise/Fall		5		ns	
Output Load		7		pF	

Table 8. GPIOs

Parameter	Min	Typ	Max	Unit	Test Conditions
GPIO OUTPUTS					
Output Drive Level		5		mA	All GPIOs in logic high state
Output Drive Level		5		mA	All GPIOs in logic low state

Table 9. SPI Interface Timing

Parameter	Min	Typ	Max	Unit	Description
t_1			15	ns	$\overline{CS}$ falling edge to MISO setup time (TRX active)
t_2	40			ns	$\overline{CS}$ to SCLK setup time
t_3	40			ns	SCLK high time
t_4	40			ns	SCLK low time
t_5	80			ns	SCLK period
t_6			10	ns	SCLK falling edge to MISO delay
t_7	5			ns	MOSI to SCLK rising edge setup time
t_8	5			ns	MOSI to SCLK rising edge hold time

Parameter	Min	Typ	Max	Unit	Description
t_9	40			ns	SCLK to $\overline{CS}$ hold time
t_{10}	10			ns	$\overline{CS}$ high to SCLK wait time
t_{11}	270			ns	$\overline{CS}$ high time
t_{12}		300	400	µs	$\overline{CS}$ low to MISO high wake-up time, 26 MHz crystal with 10 pF load capacitance, T_A = 25°C
t_{13}			20	ns	SCLK rise time
t_{14}			20	ns	SCLK fall time
t_{15}, t_{16}	2			ms	$\overline{CS}$ high time on wake-up after RC_RESET or RC_SLEEP command (see Figure 5 and Figure 31) 26 MHz crystal with 10 pF load

Table 10. IEEE 802.15.4 State Transition Timing

Parameter	Min	Typ	Max	Unit	Test Conditions
Idle to PHY_RDY State		142		µs	
PHY_RDY to Idle State		13.5		µs	
PHY_RDY or TX to RX State (Different Channel)		192		µs	VCO calibration performed
PHY_RDY or RX to TX State (Different Channel)		192		µs	VCO calibration performed
PHY_RDY or TX to RX State (Same Channel)		140		µs	VCO calibration skipped
RX or PHY_RDY to TX State (Same Channel)		140		µs	VCO calibration skipped
RX Channel Change		192		µs	VCO calibration performed
TX Channel Change		192		µs	VCO calibration performed
TX to PHY_RDY State		23		µs	
PHY_RDY to CCA State		192		µs	
CCA to PHY_RDY State		14.5		µs	
RX to Idle State		5.5		µs	
TX to Idle State		30.5		µs	
Idle to MEAS State		19		µs	
MEAS to Idle State		6		µs	
CCA to Idle State		14.5		µs	
RX to CCA State		18		µs	
CCA to RX State		205		µs	

Table 11. Timing IEEE 802.15.4-2006 SPORT Mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{21}	18			µs	SFD detect to TRCLK_CKO_GP3 (data bit clock) active delay
t_{22}		2		µs	TRCLK_CKO_GP3 bit period
t_{23}	0.51			µs	DR_GP0 to TRCLK_CKO_GP3 falling edge setup time
t_{24}		16		µs	TRCLK_CKO_GP3 symbol burst period
t_{35}	1.3		6.2	µs	PA nominal power to TRCLK_CKO_GP3 activity/entry into TX state
t_{36}		14		µs	RC_PHY_RDY to TRCLK_CKO_GP3 off
t_{37}		10		µs	RC_PHY_RDY to PA power shutdown

Table 12. MAC Timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{26}		38		µs	Time from frame received to rx_pkt_rcvd interrupt generation
t_{27}			150	µs	Time allowed, from issuing a RC_TX command, to update Register delaycfg2, Bit mac_delay_ext (0x10B[7:0])
t_{28}			150	µs	Time allowed, from issuing a RC_TX command, to cancel the RC_TX command
$t_{RX_MAC_DELAY}$		192		µs	IEEE 802.15.4 mode as defined by the standard

TIMING DIAGRAMS

SPI Interface Timing Diagram

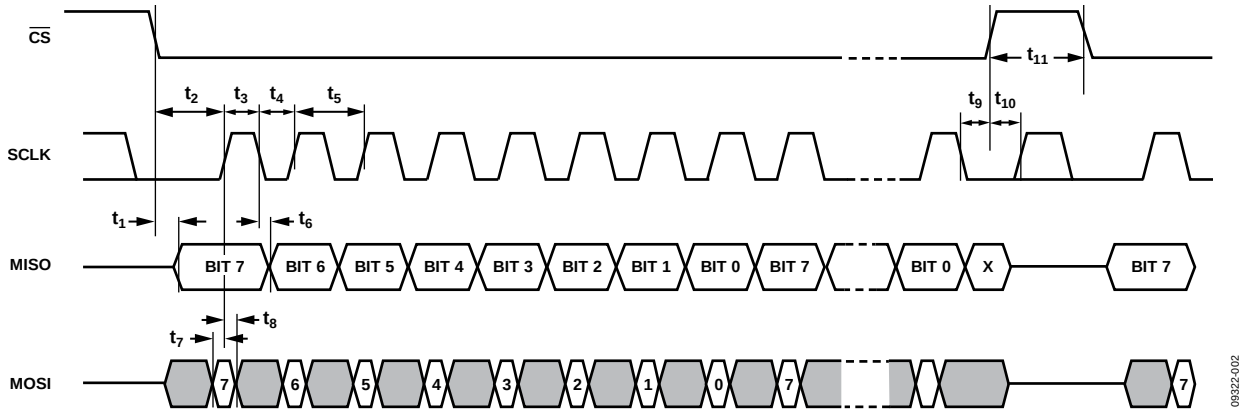


Figure 3. SPI Interface Timing

Additional description and timing diagrams are available in the Serial Peripheral interface section.

Sleep-to-Idle SPI Timing Diagrams

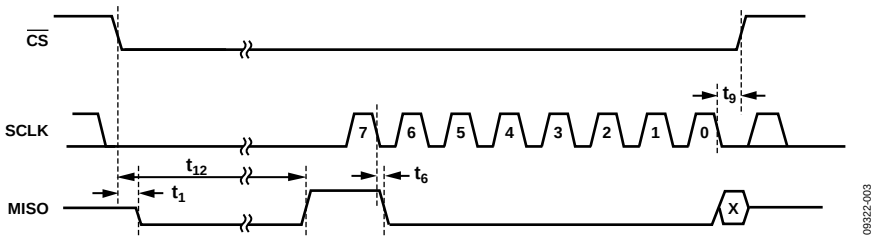


Figure 4. Sleep-to-Idle State Timing

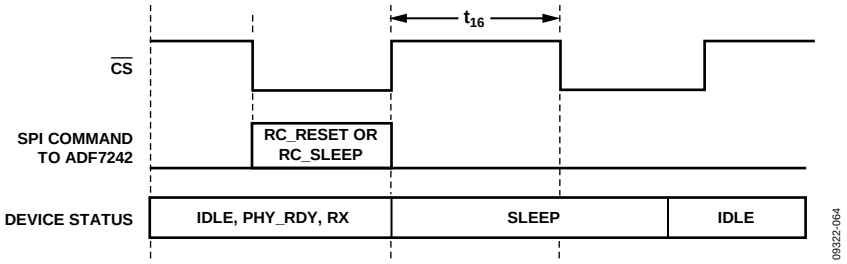


Figure 5. Wake-Up After an RC_RESET or RC_SLEEP Command

MAC Delay Timing Diagram

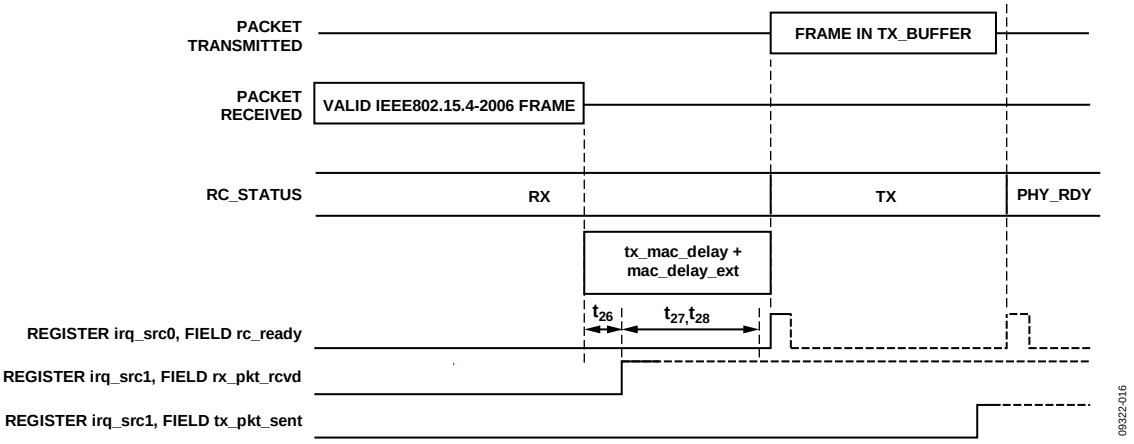


Figure 6. IEEE 802.15.4 MAC Timing

IEEE 802.15.4 RX SPORT Mode Timing Diagrams

Table 13. IEEE 802.15.4 RX SPORT Modes Configurations

Register rc_cfg, Field rc_mode (0x13E[7:0])	Register gp_cfg, Field gpio_config (0x32C[7:0])	Functionality
2	1	Bit clock and data available (see Figure 7)
0	7	Symbol clock and data available (see Figure 8)

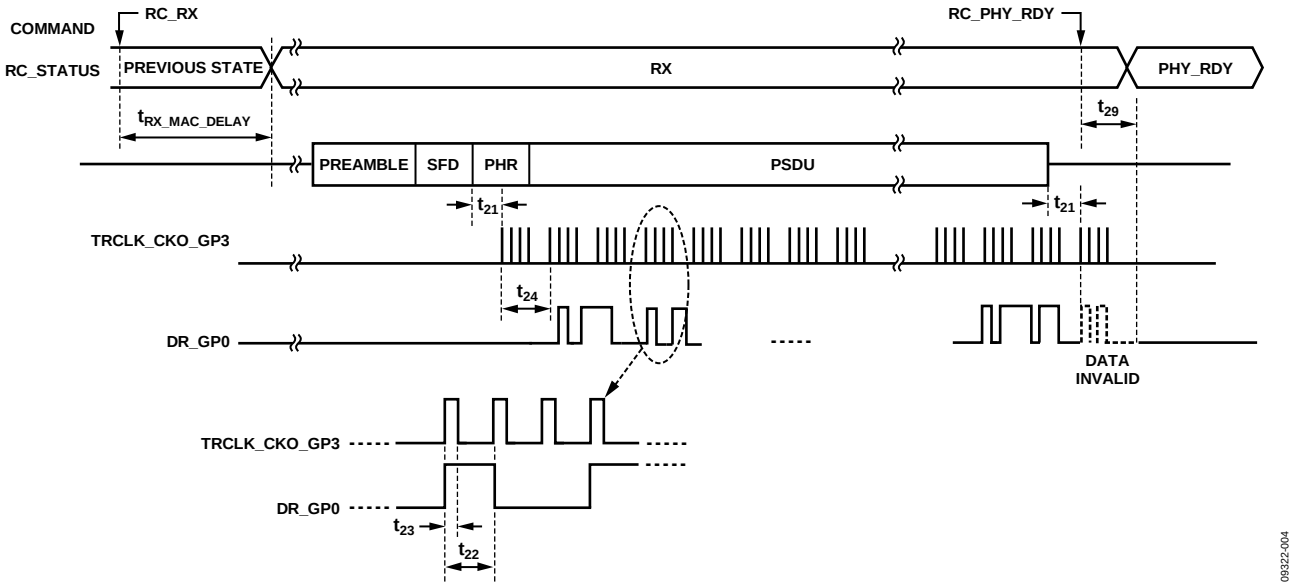


Figure 7. IEEE 802.15.4 RX SPORT Mode: Bit Clock and Data Available

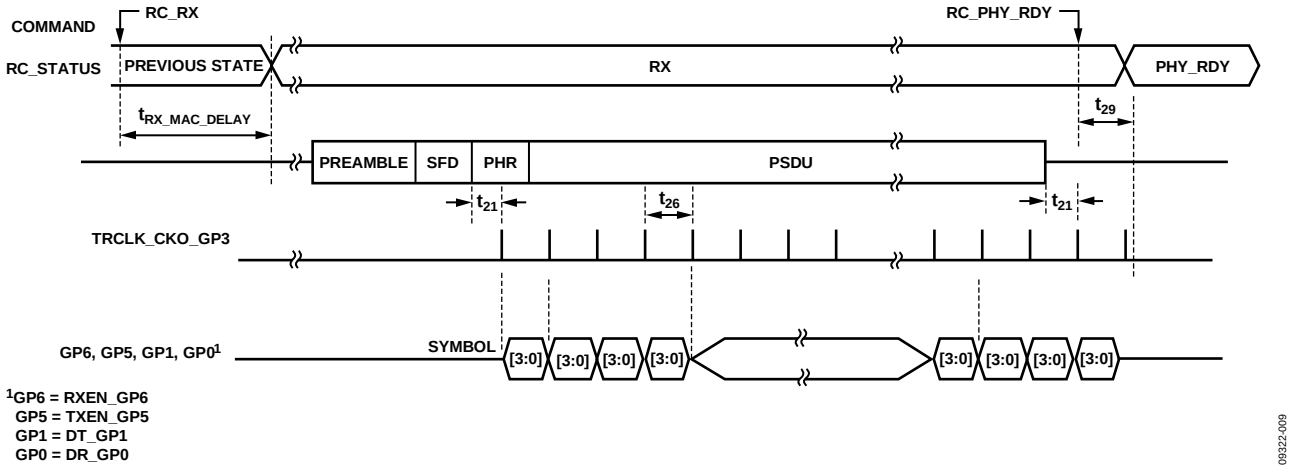


Figure 8. IEEE 802.15.4 RX SPORT Mode: Symbol Clock Output

IEEE 802.15.4 TX SPORT Mode Timing Diagram

Table 14. IEE 802.15.4 TX SPORT Mode Configurations

Register rc_cfg, Field rc_mode (0x13E[7:0])	Register gp_cfg, Field gpio_config (0x32C[7:0])	Functionality
3	1 or 4	Transmission starts after PA ramp up (see Figure 9) gpio_config = 1: data clocked in on rising edge of clock gpio_config = 4: data clocked in on falling edge of clock

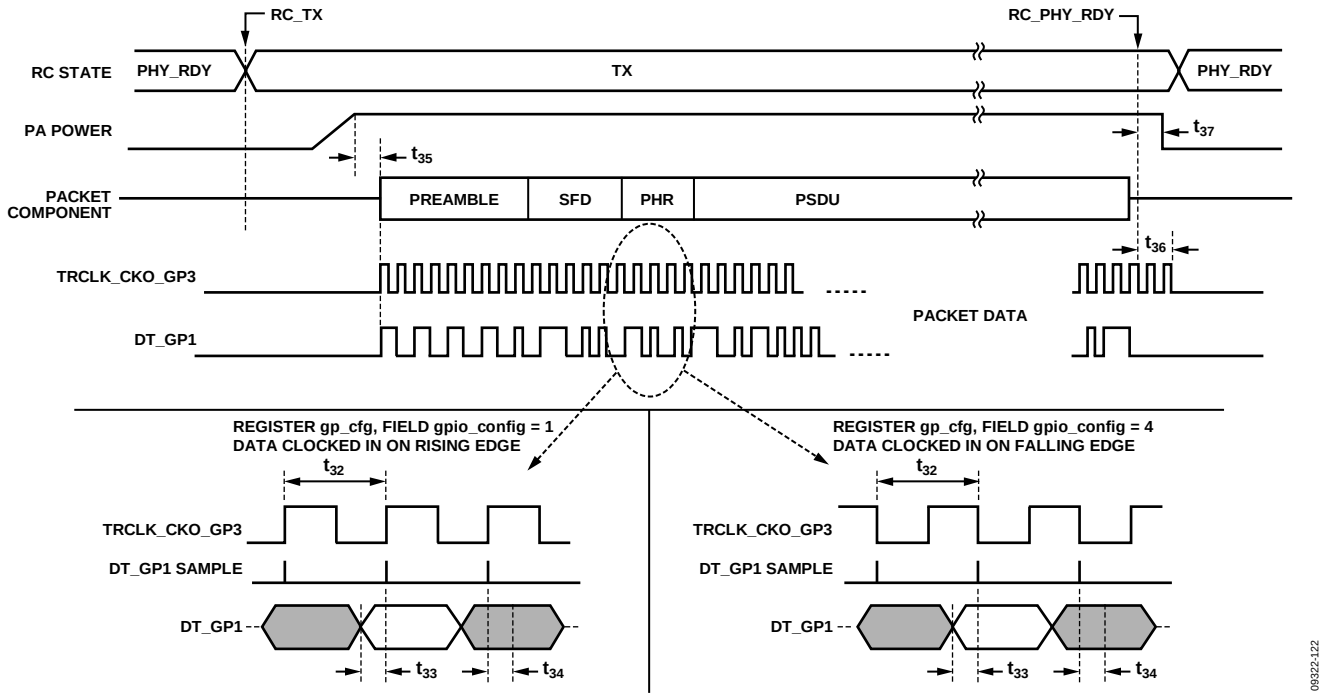


Figure 9. IEEE 802.15.4-2006 TX SPORT Mode

Refer to the SPORT Interface section for further details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 15.

Parameter	Rating
VDD_BAT to GND	−0.3 V to +3.9 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The exposed paddle of the LFCSP package should be connected to ground.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

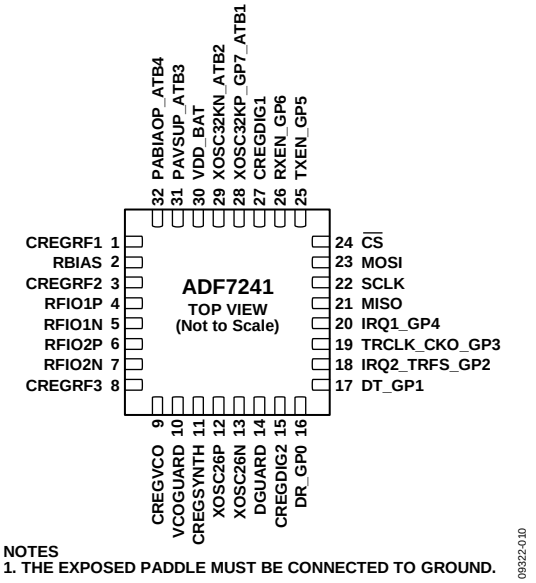


Figure 10. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CREGRF1	Regulated Supply Terminal for RF Section. Connect a 220 nF decoupling capacitor from this pin to GND.
2	RBIAS	Bias Resistor 27 kΩ to Ground.
3	CREGRF2	Regulated Supply for RF Section. Connect a 100 pF decoupling capacitor to ground.
4	RFIO1P	Differential RF Input Port 1 (Positive Terminal). A 10 nF coupling capacitor is required.
5	RFIO1N	Differential RF Input Port 1 (Negative Terminal). A 10 nF coupling capacitor is required.
6	RFIO2P	Differential RF Input/Output Port 2 (Positive Terminal). A 10 nF coupling capacitor required.
7	RFIO2N	Differential RF Input/Output Port 2 (Negative Terminal). A 10 nF coupling capacitor required.
8	CREGRF3	Regulated Supply for RF Section. Connect a 100 pF decoupling capacitor from this pin to GND.
9	CREGVCO	Regulated Supply for VCO Section. Connect a 220 nF decoupling capacitor from this pin to GND.
10	VCOGUARD	Guard Trench for VCO Section. Connect to Pin 9 (CREGVCO).
11	CREGSYNTH	Regulated Supply for PLL Section. Connect a 220 nF decoupling capacitor from this pin to GND.
12	XOSC26P	Terminal 1 of External Crystal and Loading Capacitor. This pin is no connect (NC) when an external oscillator is used.
13	XOSC26N	Terminal 2 of External Crystal and Loading Capacitor. Input for external oscillator.
14	DGUARD	Guard Trench for Digital Section. Connect to Pin 15 (CREGDIG2).
15	CREGDIG2	Regulated Supply for Digital Section. Connect a 220 nF decoupling capacitor to ground.
16	DR_GP0	SPORT Receive Data Output/General-Purpose IO Port.
17	DT_GP1	SPORT Transmit Data Input/General-Purpose IO Port.
18	IRQ2_TRFS_GP2	Interrupt Request Output 2/IEEE 802.15.4-2006 Symbol Clock/General-Purpose IO Port.
19	TRCLK_CKO_GP3	SPORT Clock Output/General-Purpose IO Port.
20	IRQ1_GP4	Interrupt Request Output 1/General-Purpose IO Port.
21	MISO	SPI Interface Serial Data Output.
22	SCLK	SPI Interface Data Clock Input.
23	MOSI	SPI Interface Serial Data Input.
24	$\overline{CS}$	SPI Interface Chip Select Input (and Wake-Up Signal).
25	TXEN_GP5	External PA Enable Signal/General-Purpose IO Port.
26	RXEN_GP6	External LNA Enable Signal/General-Purpose IO Port.
27	CREGDIG1	Regulated Supply for Digital Section. Connect a 1 nF decoupling capacitor from this pin to ground.
28	XOSC32KP_GP7_ATB1	Terminal 1 of 32 kHz Crystal Oscillator/General-Purpose IO Port/Analog Test Bus 1.
29	XOSC32KN_ATB2	Terminal 2 of 32 kHz Crystal Oscillator/Analog Test Bus 2.

Pin No.	Mnemonic	Description
30	VDD_BAT	Unregulated Supply Input from Battery.
31	PAVSUP_ATB3	External PA Supply Terminal/Analog Test Bus 3.
32	PABIAOP_ATB4	External PA Bias Voltage Output/Analog Test Bus 4.
33 (EPAD)	GND	Common Ground Terminal. The exposed paddle must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

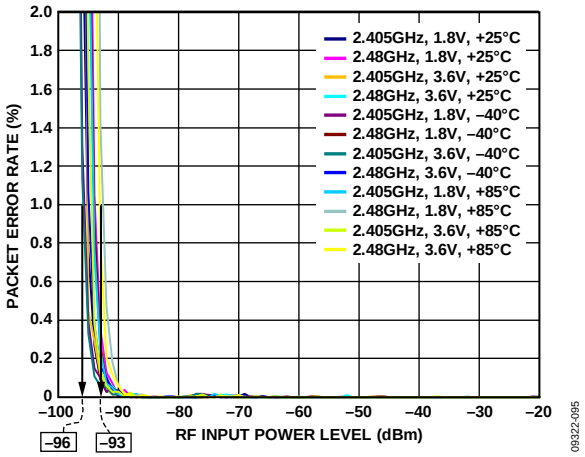


Figure 11. IEEE 802.15.4-2006 Packet Mode Sensitivity vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.405 GHz, 2.45 GHz, 2.48 GHz, RFIO2x

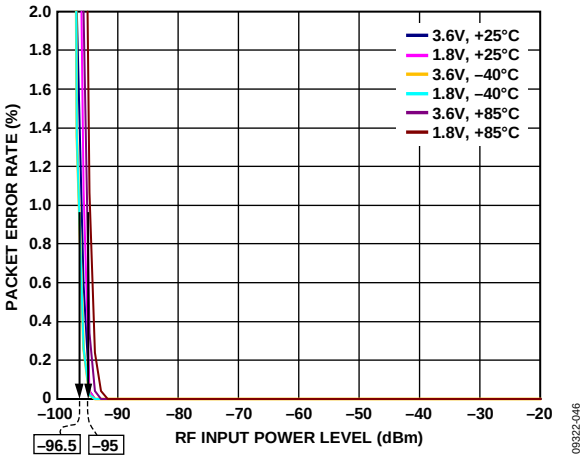


Figure 12. IEEE 802.15.4-2006 Packet Mode PER vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

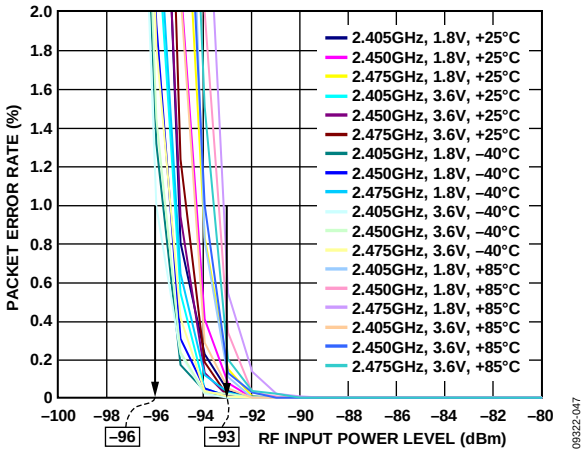


Figure 13. IEEE 802.15.4 Packet Mode Sensitivity vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.405 GHz, 2.45 GHz, 2.475 GHz, RFIO1x

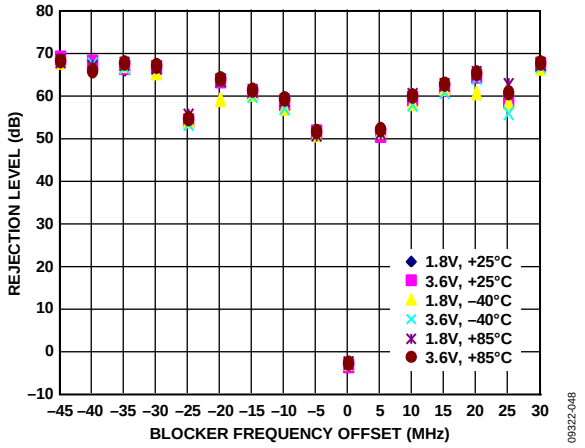


Figure 14. IEEE 802.15.4-2006 Packet Mode Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = –85 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

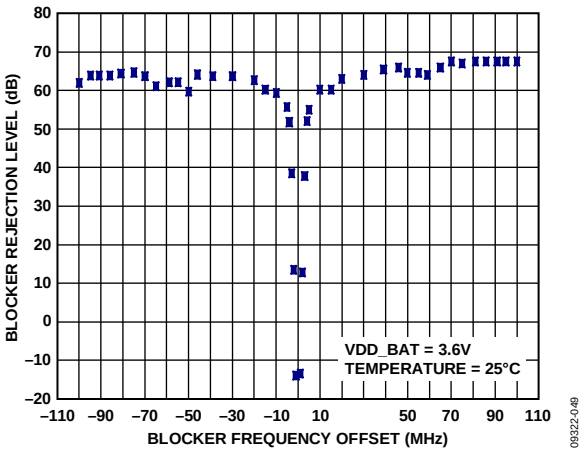


Figure 15. IEEE 802.15.4-2006 Packet Mode Wide-Band Blocker Rejection, CW Blocker, P_{WANTED} = –95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

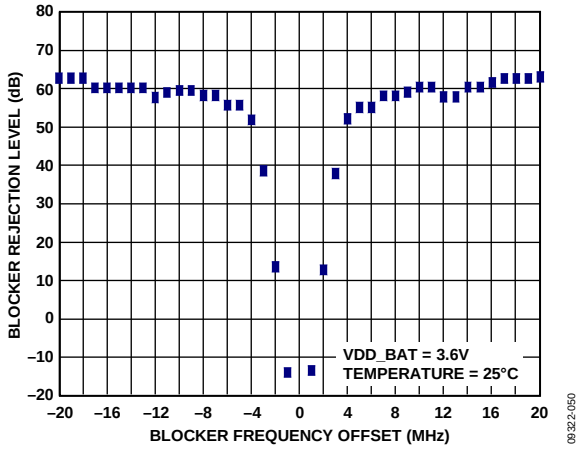


Figure 16. IEEE 802.15.4 Packet Mode Narrow-Band Blocker Rejection, CW Blocker, P_{WANTED} = –95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

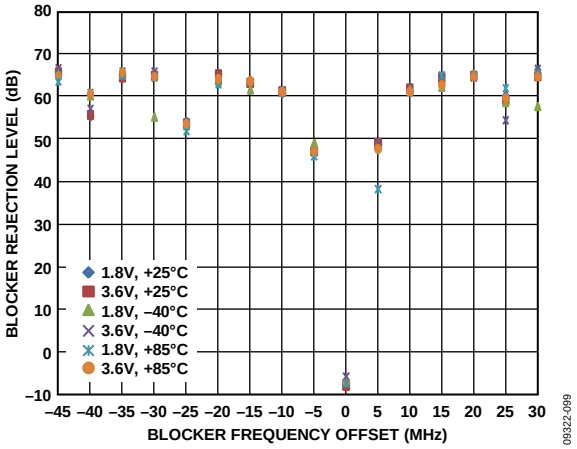


Figure 17. IEEE 802.15.4 Packet Mode Wide-Band Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

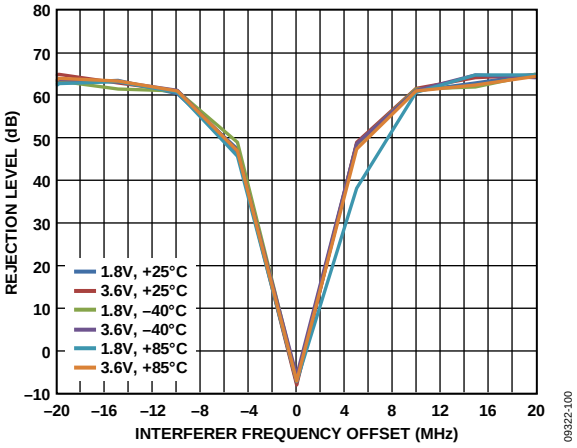


Figure 18. IEEE 802.15.4 Packet Mode Narrow-Band Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

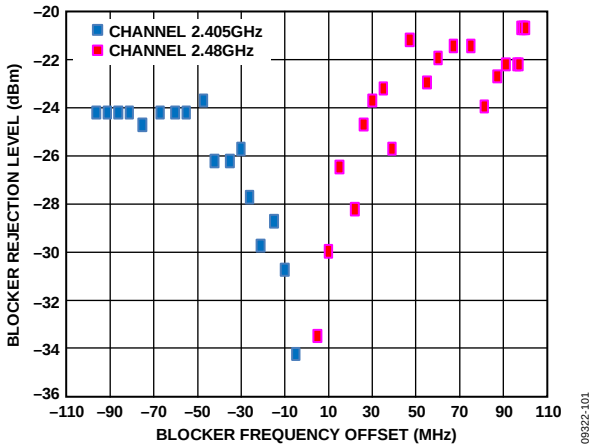


Figure 19. IEEE 802.15.4 Packet Mode Out-of-Band Blocker Rejection, CW Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.405 GHz and 2.48 GHz, RFIO2x, VDD_BAT = 3.6 V, Temperature = 25°C

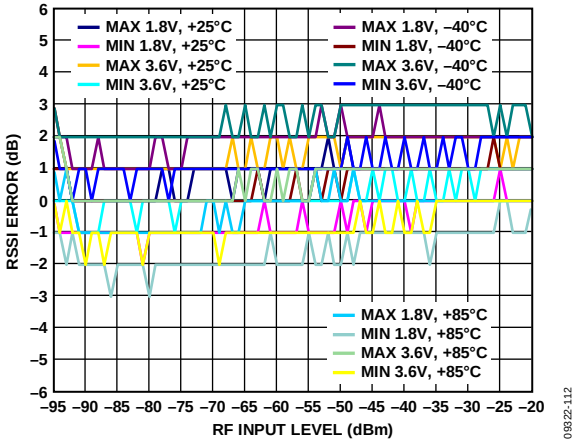


Figure 20. IEEE 802.15.4 Packet Mode RSSI Error vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

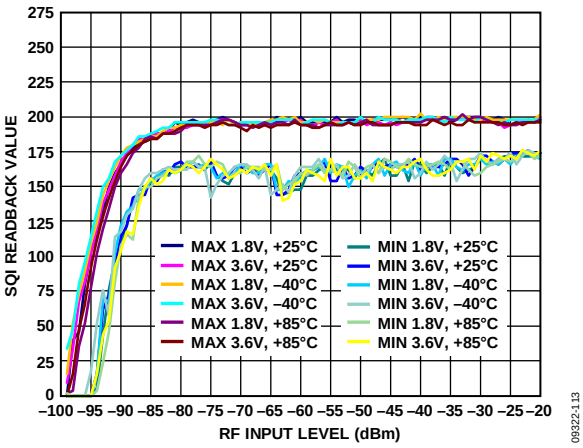


Figure 21. IEEE 802.15.4 Packet Mode SQI vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

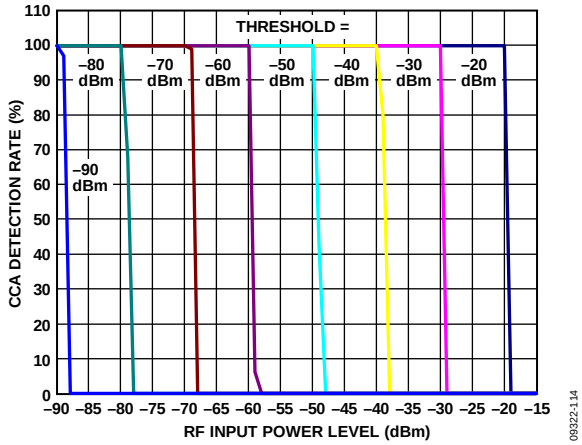


Figure 22. IEEE 802.15.4-2006 CCA Operation vs. RSSI Threshold, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C, RFIO2x

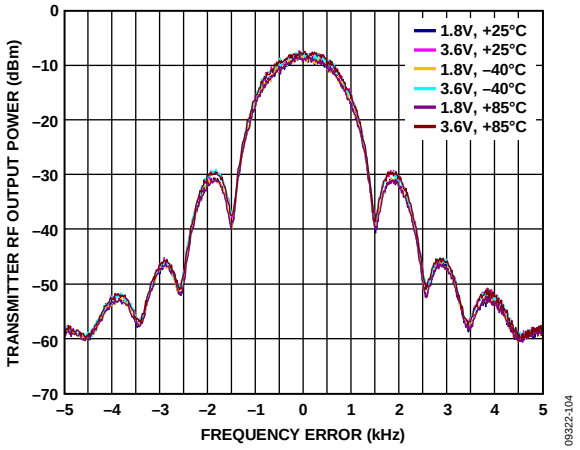


Figure 23. IEEE 802.15.4-2006 Transmitter Spectrum vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, Output Power = 3 dBm

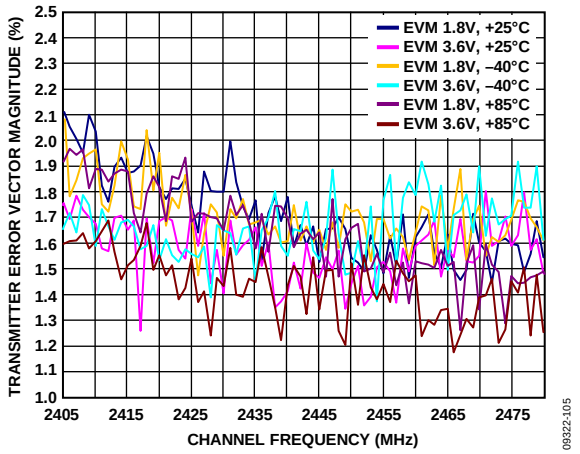


Figure 24. IEEE 802.15.4-2006 Transmitter EVM vs. Temperature and VDD_BAT at All Channels, Output Power = 3 dBm

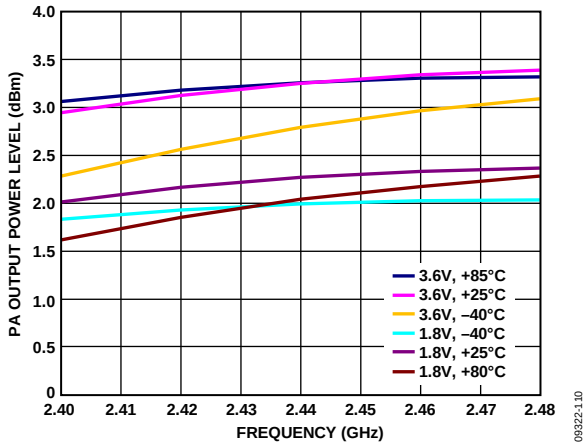


Figure 25. PA Output Power vs. RF Carrier Frequency, Temperature, and VDD_BAT (A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

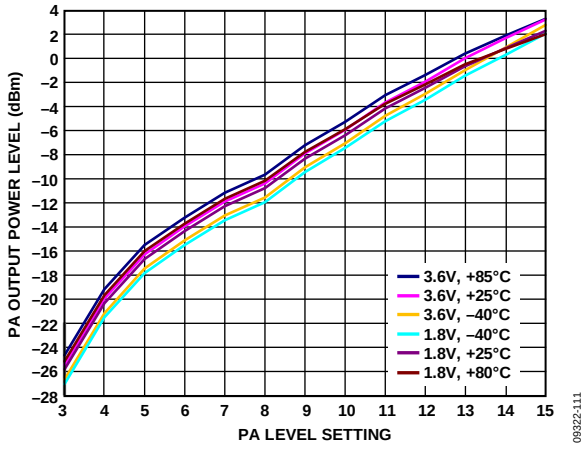


Figure 26. PA Output Power vs. Control Word, Temperature, and VDD_BAT, $f_{CHANNEL}$ = 2.44 GHz (A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

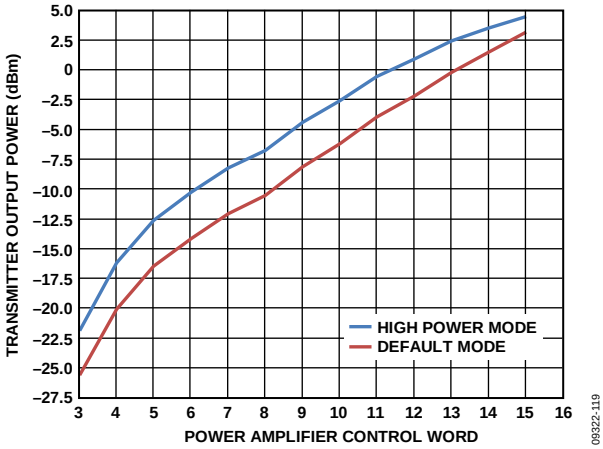


Figure 27. Transmitter Output Power vs. Control Word for Default and High Power Modes, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C, RF Carrier Frequency, Temperature, and VDD_BAT
(A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

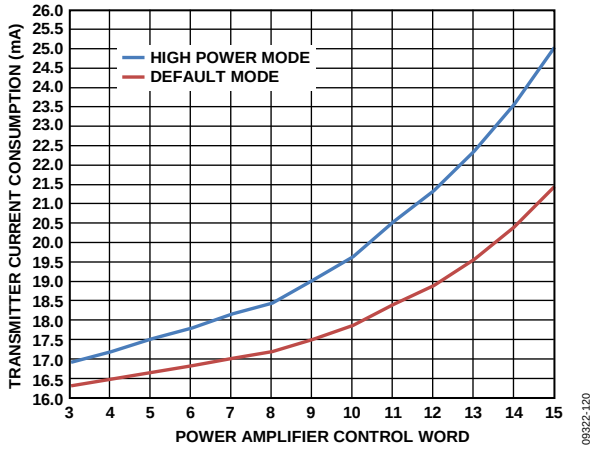


Figure 28. Transmitter Current Consumption vs. Control Word, for Default and High Power Modes, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C

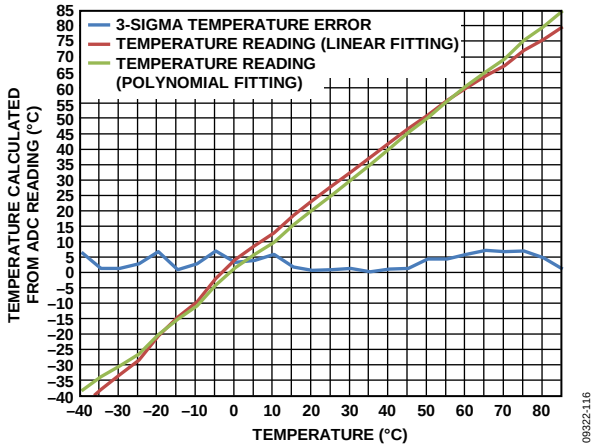


Figure 29. Temperature Sensor Performance (Average of 1000 ADC Readbacks) and 3-∑ Error vs. Temperature, VDD_BAT = 3.6 V

TERMINOLOGY

ACK
IEEE 802.15.4-2006 acknowledgment frame

ADC
Analog-to-digital converter

AGC
Automatic gain control

Battmon
Battery monitor

CCA
Clear channel assessment

BBRAM
Backup battery random access memory

CSMA/CA
Carrier-sense-multiple-access with collision avoidance

DR
Data rate

DSSS
Direct sequence spread spectrum

FCS
Frame check sequence

FHSS
Frequency hopping spread spectrum

FCF
Frame control field

LQI
Link quality indicator

MCR
Modem configuration register

MCU
Microcontroller unit

NC
Not connected

OCL
Offset correction loop

OQPSK
Offset-quadrature phase shift keying

PA
Power amplifier

PHR
PHY header

PHY
Physical layer

POR
Power-on reset

PSDU
PHY service data unit

RC
Radio controller

RCO32K
32 kHz RC oscillator

RSSI
Receive signal strength indicator

RTC
Real-time clock

SFD
Start-of-frame delimiter

SQI
Signal quality indicator

VCO
Voltage-controlled oscillator

WUC
Wake-up controller

XTO26M
26 MHz crystal oscillator

XTO32K
32 kHz crystal oscillator

RADIO CONTROLLER

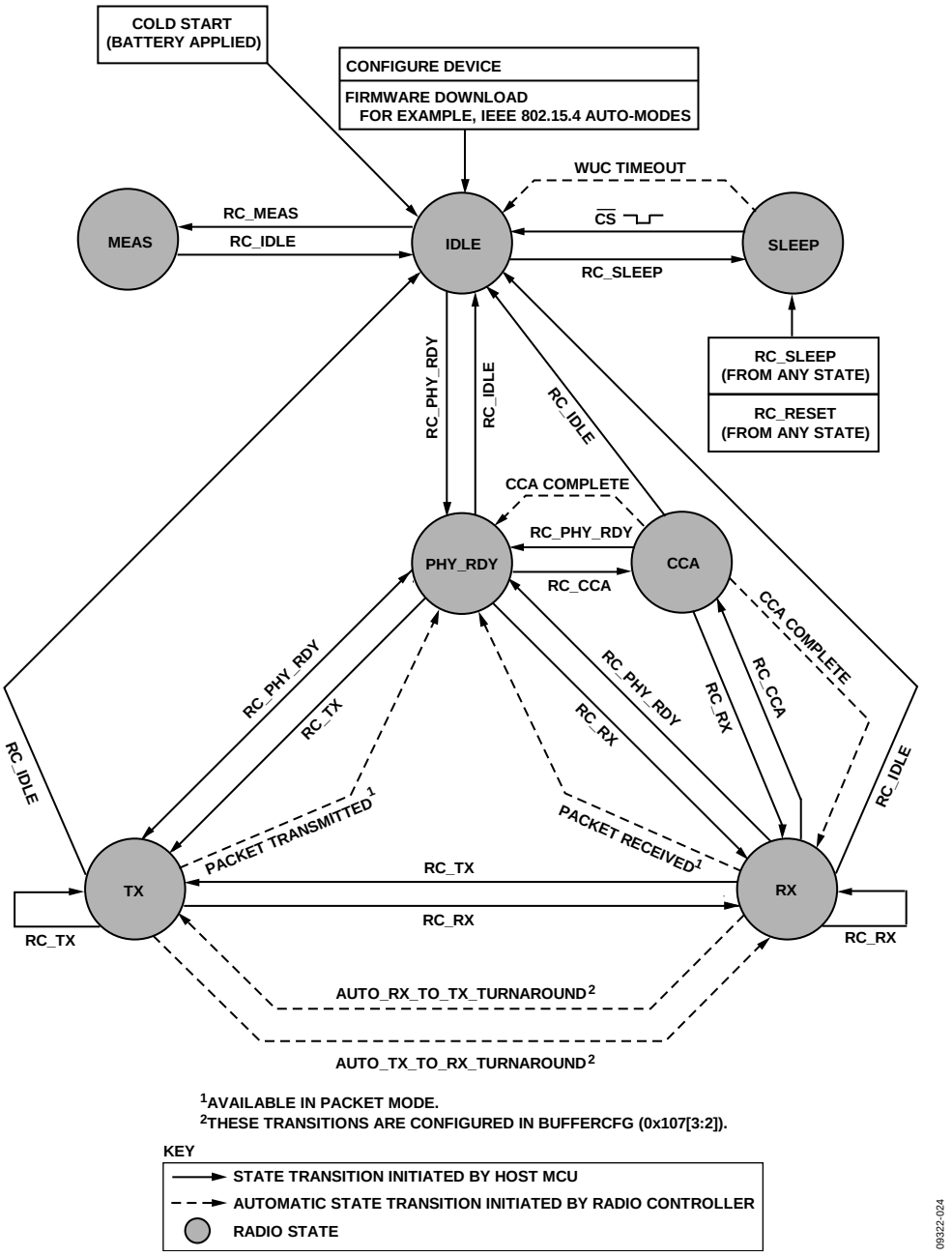


Figure 30. State Diagram

The ADF7241 incorporates a radio controller that manages the state of the IC in various operating modes and configurations. The host MCU can use single-byte commands to interface to the radio controller. The function of the radio controller includes the control of the sequence of powering up and powering down various blocks as well as system calibrations in different states of the device. Figure 30 shows the state diagram of the ADF7241 with possible transitions that are initiated by the host MCU and automatically by the radio controller.

Device Initialization

When the battery voltage is first applied to the ADF7241, a cold start-up sequence should be followed, as shown in Figure 31. The start-up sequence is as follows:

- Apply the battery voltage, VDD_BAT, to the device with the desired voltage ramp rate. After a time, t_{RAMP}, VDD_BAT reaches its final voltage value.
- After t_{RAMP}, execute the SPI command, RC_RESET. This command resets and shuts down the device.
- After the specified time, t_{15}, the host MCU can set the $\overline{CS}$ port of the SPI low.
- Wait until the MISO output of the SPI (SPI_READY flag) goes high, at which time the device is in the idle state and ready to accept commands.

A power-on reset takes place when the host MCU sets the $\overline{CS}$ port of the SPI low. All device LDOs are enabled together with the 26 MHz crystal oscillator and the digital core. After the radio controller initializes the configuration registers to their default values, the device enters the idle state.

The cold start-up sequence is needed only when the battery voltage is first applied to the device. Afterwards, a warm start-up sequence can be used where the host MCU can wake up the device from a sleep state by setting the $\overline{CS}$ port of the SPI low.

Idle State

In this state, the receive and transmit blocks are powered down. The digital section is enabled and all configuration registers, as well as the packet RAM, are accessible. The host MCU must set any configuration parameters, such as modulation scheme, channel frequency, and WUC configuration, in this state.

Bringing the $\overline{CS}$ input low in the sleep state causes a transition into the idle state. The transition from the sleep state to the idle state timing is shown in Figure 4. The idle state can also be entered by issuing an RC_IDLE command in any state other than the sleep state.

PHY_RDY State

Upon entering the PHY_RDY state from the idle state, the RF frequency synthesizer is enabled and a system calibration is carried out. The receive and transmit blocks are not enabled in this state. The system calibration is omitted when the PHY_RDY state is entered from the RX, TX, or CCA state.

The PHY_RDY state can be entered from the idle, RX, TX, or CCA state by issuing an RC_PHY_RDY command.

RX State

The RF frequency synthesizer is automatically calibrated to the programmed channel frequency upon entering the RX state from the PHY_RDY or TX state. The frequency synthesizer calibration can be omitted for single-channel communication systems if short turnaround times are required. Following a programmable MAC delay period, the ADF7241 starts searching for a preamble and a synchronization word if enabled by the user.

The RX state can be entered from the PHY_RDY, CCA, and TX states by issuing an RC_RX command. Depending on whether the device is configured to operate in packet or SPORT mode by setting Register buffercfg, Field rx_buffer_mode, the device can revert automatically to the PHY_RDY state when a packet is received, or remain in the RX state until a command to enter a different state is issued. Refer to the Receiver section for further details.

CCA State

Upon entering the CCA state, a clear channel assessment is performed. The CCA state can be entered from the PHY_RDY or RX state by issuing an RC_CCA command. By default, upon completion of the clear channel assessment, the ADF7241 automatically reverts to the state from which the RC_CCA command originated.

TX State

Upon entering the TX state, the RF frequency synthesizer is automatically calibrated to the programmed channel frequency. The frequency synthesizer calibration can be omitted for communication systems operating on a single channel if short turnaround times are required. Following a programmable delay period, the PA is ramped up and transmission is initiated.

The TX state can be entered from the PHY_RDY or RX state by issuing the RC_TX command. Depending on whether the device is configured to operate in packet or SPORT mode by setting Register buffercfg, Field rx_buffer_mode, the device can revert automatically to the PHY_RDY state when a packet is transmitted, or remain in the TX state until a command to enter a different state is issued. Refer to the Transmitter section for further details.

MEAS State

The MEAS state is used to measure the chip temperature. The transmitter and receiver blocks are not enabled in this state. The chip temperature is measured using the ADC, which can be read from Register adc_rbk, Field adc_out, and is continuously updated with the chip temperature reading.

This state is enabled by issuing the RC_MEAS command from the idle state and can be exited using the RC_IDLE command.

Sleep States

The sleep state is entered with the RC_SLEEP command. The sleep state can be configured to operate in three different modes, which are listed in Table 17.

Table 17. ADF7241 Sleep Modes

Sleep Mode	Active Circuits	Functionality
SLEEP_BBRAM	BBRAM	Packet RAM and modem configuration register (MCR) contents are not maintained. BBRAM retains the IEEE 802.15.4-2006 node addresses[1].
SLEEP_BBRAM_XTO	BBRAM and 32 kHz crystal oscillator	32 kHz crystal oscillator is enabled, with data retention in the BBRAM.
SLEEP_BBRAM_RCO	BBRAM and 32 kHz RC Oscillator	32 kHz RC oscillator is enabled, with data retention in the BBRAM.

[1] Refer to the Receiver Configuration in Packet Mode section for further details.

SLEEP MODES

The sleep modes are configurable with the wake-up configuration registers, tmr_cfg0 and tmr_cfg1. The contents of Register tmr_cfg0 and Register tmr_cfg1 are reset in the sleep state.

SLEEP_BBRAM

This mode is suitable for applications where the MCU is equipped with its own wake-up timer. SLEEP_BBRAM mode is enabled by setting Register tmr_cfg1, Field sleep_config = 1.

SLEEP_BBRAM_XTO

This mode enables the 32 kHz crystal oscillator and retains certain configuration registers in the BBRAM during the sleep state. To enable SLEEP_BBRAM_XTO mode, set Register tmr_cfg1, Field sleep_config = 5. A wake-up interrupt can be set using, for example, Register irq1_en0, Field wakeup = 1. Refer to the Wake-Up Controller (WUC) section for details on how to configure the ADF7241 WUC.

SLEEP_BBRAM_RCO

This mode enables the 32 kHz RC oscillator and retains certain configuration registers in the BBRAM during the sleep state. This mode can be used when lower timer accuracy is acceptable by the communication system. It is enabled by setting Register tmr_cfg1, Field sleep_config = 11. A wake-up interrupt can be set using, for example, Register irq1_en0, Field wakeup = 1. Refer to the Wake-Up Controller (WUC) section for details on how to configure the ADF7241 WUC.

Wake-Up from the Sleep State

The host MCU can bring $\overline{CS}$ low at any time to wake the ADF7241 from the sleep state. After bringing $\overline{CS}$ low, it must wait until the MISO output (SPI_READY flag) goes high prior to accessing the SPI port. This delay reflects the start-up time of the ADF7241. When the MISO output is high, the voltage regulator of the digital section and the crystal oscillator have stabilized. Unless the chip is in the sleep state, the MISO pin always goes high immediately after bringing $\overline{CS}$ low. The sleep state can also be exited by a timeout event with the WUC configured. Refer to the Wake-Up Controller (WUC) section for details on how to configure the ADF7241 WUC.

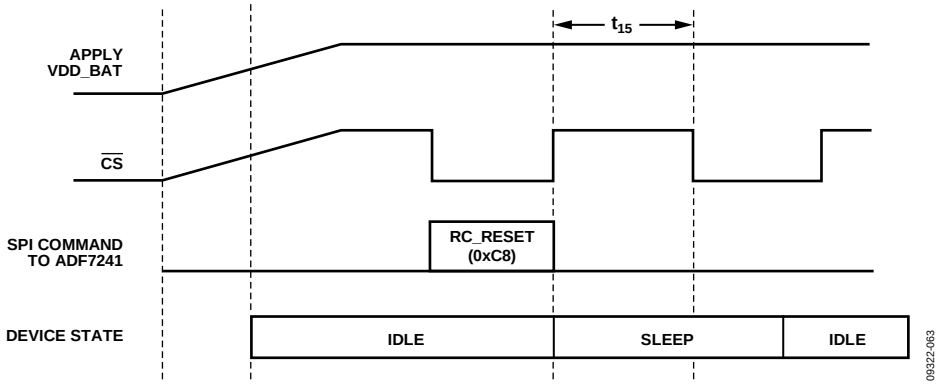


Figure 31. Cold Start Sequence from Application of the Battery

RF FREQUENCY SYNTHESIZER

A fully integrated RF frequency synthesizer is used to generate both the transmit signal and the receive LO signal. The architecture of the frequency synthesizer is shown in Figure 32. The receiver uses the frequency synthesizer circuit to generate the local oscillator (LO) for downconverting an RF signal to the baseband. The transmitter is based on a direct closed-loop VCO modulation scheme using a low noise fractional-N RF frequency synthesizer, where a high resolution Σ-Δ modulator is used to generate the required frequency deviations at the RF in response to the data being transmitted.

The VCO and the frequency synthesizer loop filter of the ADF7241 are fully integrated. To reduce the effect of VCO pulling by the power-up of the power amplifier, as well as to minimize spurious emissions, the VCO operates at twice the RF frequency. The VCO signal is then divided by 2 giving the required frequency for the transmitter and the required LO frequency for the receiver. The frequency synthesizer also features automatic VCO calibration and bandwidth selection.

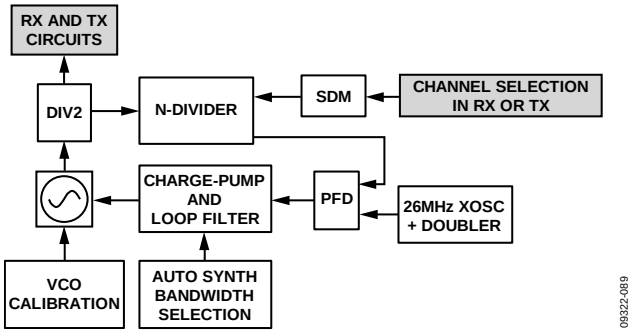


Figure 32. Synthesizer Architecture

RF FREQUENCY SYNTHESIZER CALIBRATION

The ADF7241 requires a system calibration prior to being used in the RX, CCA, or TX state. Because the calibration information is reset when the ADF7241 enters a sleep state, a full system calibration is automatically performed on the transition between the idle and PHY_RDY states. The system calibration is omitted when the PHY_RDY state is entered from the TX, RX, or CCA state.

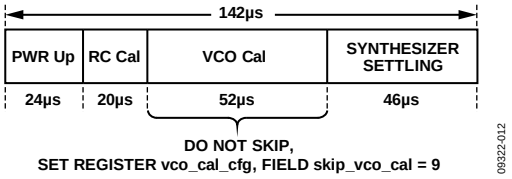


Figure 33. System Calibration Following RC_PHY_RDY

Figure 33 shows a breakdown of the total system calibration time. It comprises a power-up delay, calibration of the receiver baseband filter (RC Cal), and a VCO calibration (VCO Cal). Once the VCO is calibrated, the frequency synthesizer is allowed to settle to within ±5 ppm of the target frequency. A fully automatic fast VCO frequency and amplitude calibration scheme is used to mitigate the effect of temperature, supply voltage, and process variations on the VCO performance.

The VCO calibration phase must not be skipped during the system calibration in the PHY_RDY state. Therefore, it is important to ensure that Register vco_cal_cfg, Field skip_vco_cal = 9 prior to entering the PHY_RDY state from the idle state. This is the default setting and, therefore, only requires programming if skipping of the calibration was previously selected.

The VCO calibration can be skipped on the transition from the PHY_RDY state to the RX, TX, and CCA states on the condition that the calibration has been performed in the PHY_RDY state on the same channel frequency to be used in the RX, TX, and CCA states. The following sequence should be used if skipping the VCO calibration is required in any state following the PHY_RDY state:

1. After the system calibration is performed in the PHY_RDY state, the VCO frequency band in Register vco_band_rb, Field vco_band_val_rb and the VCO bias DAC code in Register vco_idac_rb, Field vco_idac_val_rb should be read back.
2. Before transitioning to any other state and assuming operation on the same channel frequency, the VCO frequency band and amplitude DAC should be overwritten as follows:
   a) Set Register vco_cal_cfg, Field skip_vco_cal = 15 to skip the VCO calibration.
   b) Enable the VCO frequency over-write mode by setting Register vco_ovrw_cfg, Field vco_band_ovrw_en = 1.
   c) Write the VCO frequency band read back after the system calibration in the PHY_RDY state to Register vco_band_ovrw, Field vco_band_ovrw_val.
   d) Enable the VCO bias DAC over-write mode by setting Register vco_ovrw_cfg, Field vco_idac_ovrw_en = 1
   e) Write the VCO bias DAC read back after the system calibration in the PHY_RDY state to Register vco_idac_ovrw, Field vco_idac_ovrw_val .

Following the preceding procedure, the device can transition to other states, which use the same channel frequency without performing a VCO calibration. If it is required to change the channel frequency before entering the RX, TX, or CCA state at any point after the preceding procedure has been used, Register vco_cal_cfg, Field skip_vco_cal must be set to 9 before transitioning to the respective state. Then the VCO calibration is automatically performed.

RF FREQUENCY SYNTHESIZER BANDWIDTH

The ADF7241 radio controller optimizes the RF frequency synthesizer bandwidth based on whether the device is in the RX or the TX state. If the device is in the RX state, the frequency synthesizer bandwidth is set by the radio controller to ensure optimum blocker rejection. If the device is in the TX state, the radio controller sets the frequency synthesizer bandwidth based on the required data rate to ensure optimum modulation quality.

RF CHANNEL FREQUENCY PROGRAMMING

The frequency of the synthesizer is programmed with the frequency control word, ch_freq[23:0], which extends over Register ch_freq0, Register ch_freq1, and Register ch_freq2. The frequency control word, ch_freq[23:0], contains a binary representation of the absolute frequency of the desired channel divided by 10 kHz.

Writing a new channel frequency value to the frequency control word, ch_freq[23:0], takes effect after the next frequency synthesizer calibration phase. The frequency synthesizer is calibrated by default during the transition into the PHY_RDY from the idle state as well as in the TX, RX and CCA states. Refer to the RF Frequency Synthesizer Calibration, Transmitter, and Receiver sections for further details. To facilitate fast channel frequency changes, a new frequency control word can be written in the RX state before a packet has been received. The next RC_RX or RC_TX command initiates the required frequency synthesizer calibration and settling cycle. Similarly, a new frequency control word can be written after a packet has been transmitted while in the TX state and the next RC_RX or RC_TX command initiates the frequency synthesizer calibration and settling cycle.

REFERENCE CRYSTAL OSCILLATOR

The on-chip crystal oscillator generates the reference frequency for the frequency synthesizer and system timing. The oscillator operates at a frequency of 26 MHz. The crystal oscillator is amplitude controlled to ensure a fast start-up time and stable operation under different operating conditions. The crystal and associated external components should be chosen with care because the accuracy of the crystal oscillator can have a significant impact on the performance of the communication system. Apart from the accuracy and drift specification, it is important to consider the nominal loading capacitance of the crystal. Crystals with a high loading capacitance are less sensitive to frequency pulling due to tolerances of external capacitors and the printed circuit board parasitic capacitances. When selecting a crystal, these advantages should be balanced against the higher current consumption, longer start-up time, and lower trimming range resulting from a larger loading capacitance.

The total loading capacitance must be equal to the specified load capacitance of the crystal and comprises the external parallel loading capacitors, the parasitic capacitances of the XOSC26P and XOSC26N pins, as well as the parasitic capacitance of tracks on the printed circuit board.

The ADF7241 has an integrated crystal oscillator tuning capacitor that facilitates the compensation of systematic production tolerance and temperature drift. The tuning capacitor is controlled with Register xto26_trim _cal, Field xto26_trim (0x371). The tuning range provided by the tuning capacitor depends on the loading capacitance of a specific crystal. The total tuning range is typically 25 ppm.

TRANSMITTER

TRANSMIT OPERATING MODES

The two primary transmitter operating modes are:

- IEEE 802.15.4-2006 packet mode
- IEEE 802.15.4-2006 SPORT mode

The desired mode of operation is selected via Register rc_cfg, Field rc_mode.

The modulator preemphasis filter must be enabled with Register tx_m, Field preemp_filt = 1. This is enabled by default if using packet mode only, but must be programmed if using SPORT mode.

IEEE 802.15.4-2006-compatible mode with packet manager support is selected with Register rc_cfg, Field rc_mode = 0 (0x13E). In this mode, the ADF7241 packet manager automatically generates the IEEE 802.15.4-2006-compatible preamble and SFD. There is also an option to use a nonstandard SFD by programming Register sfd_15_4 with the desired alternative SFD. Refer to the Programmable SFD subsection of the Receiver section for further details. There are 256 bytes of dedicated RAM (packet RAM), which constitute TX_BUFFER and RX_BUFFER, available to store transmit and receive packets. The packet header must be the first byte written to TX_BUFFER. The address of the first byte of TX_BUFFER is stored in Register txpb, Field tx_pkt_base.

If the automatic FCS field generation has been disabled (Register pkt_cfg, Field auto_fcs_off = 1), the full frame including FCS must be written to TX_BUFFER. In this case, the number of bytes written to TX_BUFFER must be equal to the length specified in the PHR field.

If automatic FCS field generation has been enabled (Register pkt_cfg, Field auto_fcs_off = 0), the FCS is automatically appended to the frame in TX_BUFFER. In this case, the number of bytes written to TX_BUFFER must be equal to the length specified in the PHR field minus two.

The format of the frame in TX_BUFFER, both with automatic FCS field generation enabled and with it disabled, is shown in Figure 34.

Details of how to configure IEEE 802.15.4-2006 TX SPORT mode are given in the SPORT Interface section.

IEEE 802.15.4-2006 Transmitter Timing and Control

This section applies when IEEE 802.15.4-2006 packet mode is enabled. Accurate control over the transmission slot timing is maintained by two delay timers (Register delaycfg1, Field tx_mac_delay and Register delaycfg2, Field mac_delay_ext), which introduce a controlled delay between the rising edge of the $\overline{CS}$ signal following the RC_TX command and the start of the transmit operation. Figure 35 illustrates the timing of the transmit operation assuming that the ADF7241 was operating in PHY_RDY, RX, or TX state prior to the execution of an RC_TX command.

If enabled, the external PA interface, as described in the Power Amplifier section, is powered up prior to the synthesizer calibration to allow sufficient time for the bias servo loop to settle. Ramp-up of the PA is completed shortly before the overall MAC delay has elapsed. If enabled, an rc_ready interrupt (see the Interrupt Controller section) is generated at the transition into the TX state. Following the completion of the PA ramp-up phase, the transceiver enters the TX state. The minimum and maximum times for the PA ramp-up to complete prior to the transceiver entering the TX state are given by Parameter t_{35} in Table 11.

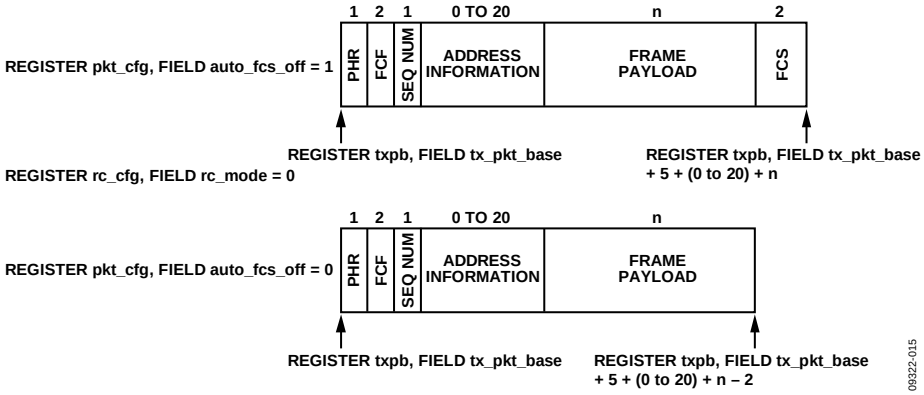


Figure 34. Field Format of TX_BUFFER

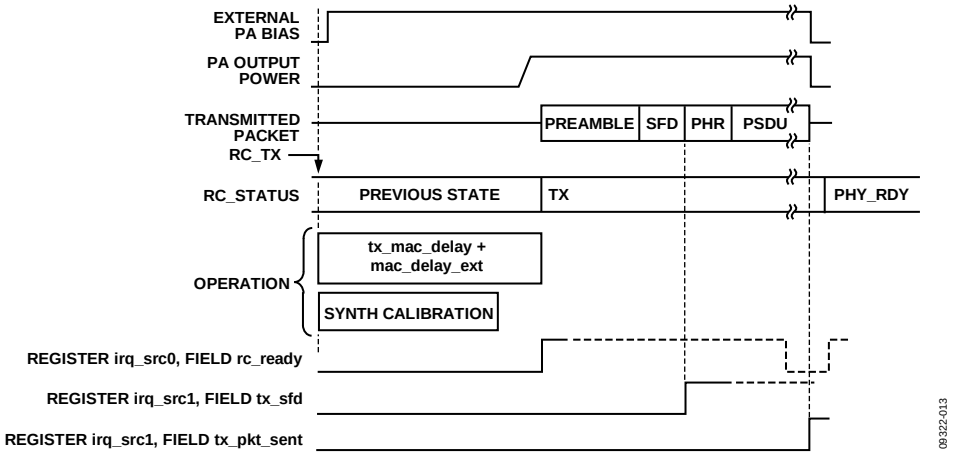


Figure 35. Transmit Timing and Control

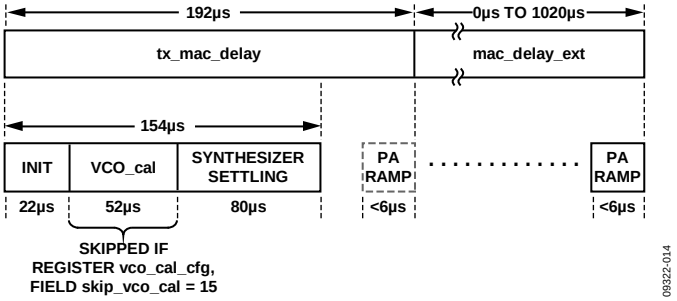


Figure 36. Synthesizer Calibration Following RC_TX

The radio controller first transmits the automatically generated preamble and SFD. If it has been enabled, an SFD interrupt is asserted after the SFD is transmitted. The packet manager then reads TX_BUFFER, starting with the PHR byte and transmits its contents. Following the transmission of the entire frame, the radio controller turns the PA off and asserts a tx_pkt_sent interrupt. The ADF7241 then automatically returns to the PHY_RDY state unless automatic operating modes have been configured.

By default, the synthesizer is recalibrated each time an RC_TX command is issued. Figure 36 shows the synthesizer calibration sequence that is performed each time the transceiver enters the TX state. The total TX MAC delay is defined by the combined delay configured with Register delaycfg1, Field tx_mac_delay and Register delaycfg2, Field mac_delay_ext. Register delaycfg1, Field tx_mac_delay is programmable in steps of 1 µs, whereas Register delaycfg2, Field mac_delay_ext is programmable in steps of 4 µs. The default value of Register delaycfg1, Field tx_mac_delay is the length of 12 IEEE 802.15.4-2006-2.4 GHz symbols or 192 µs.

The default value of Register delaycfg2, Field mac_delay_ext is 0 µs. Following the issue of the RC_TX command, while the delay defined by Register delaycfg1, Field tx_mac_delay is elapsing, Register delaycfg2, Field mac_delay_ext can be updated up until the time, t_{27}, specified in Table 12. This allows a dynamic adjustment of the transmission timing for acknowledge (ACK) frames for networks using slotted CSMA/CA. To ensure correct settling of the synthesizer prior to PA ramp-up, the total TX MAC delay should not be programmed to a value shorter than specified by the PHY_RDY or RX to TX timing specified in Table 10. The RC_TX command can be aborted up to the time specified by Parameter t_{28} in Table 12 by means of issuing an RC_PHY_RDY, RC_RX, or RC_IDLE command.

The VCO calibration (VCO_cal) can be skipped if shorter turnaround times are required. Skipping the VCO calibration is possible if the channel frequency control word ch_freq[23:0] has remained unchanged since the last RC_PHY_RDY, RC_RX, RC_CCA, or RC_TX command was issued with VCO_cal enabled. The initialization, synthesizer settling, and PA ramping phases are mandatory however because the synthesizer bandwidth is changed between receive and transmit operation. Skipping the VCO calibration is an option for single-channel communication systems, or systems where an ACK frame is transmitted on the same channel upon reception of a packet.

VCO_cal is skipped by setting Register vco_cal_cfg, Field skip_vco_cal = 15. In this case, tx_mac_delay can be reduced to 140 µs. The VCO calibration is executed if Register vco_cal_cfg, Field skip_vco_cal = 9.

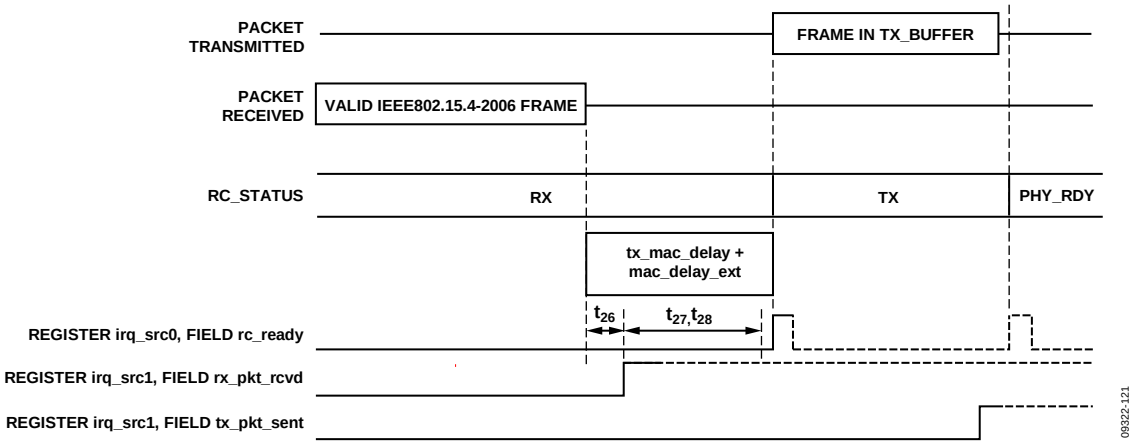


Figure 37. IEEE 802.15.4 Auto RX-to-TX Turnaround Mode

IEEE 802.15.4 AUTOMATIC RX-TO-TX TURNAROUND MODE

The ADF7241 features an automatic RX-to-TX turnaround mode when it is operating in IEEE 802.15.4-2006 packet mode (Register rc_cfg, Field rc_mode = 0). The automatic RX-to-TX turnaround mode facilitates the timely transmission of acknowledgment frames.

Figure 37 illustrates the timing of the automatic RX-to-TX turnaround mode. When enabled by setting Register buffercfg, Field auto_rx_to_tx_turnaround, the ADF7241 automatically enters the TX state following the reception of a valid IEEE 802.15.4-2006 frame. After the combined transmit MAC delay (tx_mac_delay + mac_delay_ext), the ADF7241 enters the TX state and transmits the frame stored in TX_BUFFER. After the transmission is complete, the ADF7241 enters the PHY_RDY state. There is a 38 µs delay between the reception of the last symbol and the generation of the rx_pkt_rcvd interrupt. The transmit MAC delay timeout period begins immediately after the reception of the last symbol. Therefore, the host MCU has up to t_{28} µs (see Table 12) after a frame has been received to cancel the transmit operation by means of issuing an RC_IDLE, RC_PHY_RDY, or RC_RX command.

POWER AMPLIFIER

The integrated power amplifier (PA) is connected to the RFIO2P and RFIO2N RF ports. It is equipped with a built-in harmonic filter to simplify the design of the external harmonic filter. The output power of the PA is set with Register extpa_msc, Field pa_pwr with an average step size of 2 dB. The step size increases at the lower end of the control range. Refer to Figure 26 for the typical variation of output power step size with the control word value. The PA also features a high power mode, which can be enabled by setting Register pa_bias, Field pa_bias_ctrl = 63 and Register pa_cfg, Field pa_bridge_dbias = 21.

PA Ramping Controller

The PA ramping controller of the ADF7241 minimizes spectral splatter generated by the transmitter. Upon entering the TX state, the ramping controller automatically ramps the output power of the PA from the minimum output power to the specified nominal value. In packet mode, transmission of the packet commences after the ramping phase. When the transmission of the packet is complete or the TX state is exited, the PA is turned off immediately. It is also possible to allow the PA to ramp down its output power using the same ramp rate for the ramp-up phase, by setting Register ext_ctrl, Field pa_shutdown_mode to 1.

Figure 38 illustrates the shape of the PA ramping profile and its timing. It follows a linear-in-dB shape. The ramp time depends on the output power setting in Register extpa_msc, Field pa_pwr and is specified with Register pa_rr, Field pa_ramp_rate according to the following equation:

$$t_ramp = 2^{pa_rr.pa_ramp_rate} \times 2.4\ \text{ns} \times extpa_msc.pa_pwr$$

External PA Interface

The ADF7241 has an integrated biasing block for external PA circuits as shown in Figure *39*. It is suitable for external PA circuits based on a single GaAs MOSFET and a wide range of integrated PA modules. The key components are shown in Figure 40. A switch between Pin VDD_BAT and Pin PAVSUP_ATB3 controls the supply current to the external FET. PABIOP_ATB4 can be used to set a bias point for the external FET. The bias point is controlled by a 5-bit DAC and/or a bias servo loop.

To have the external PA interface under direct control of the host MCU, set Register ext_ctrl, Field extpa_auto_en = 0. The host MCU can then use Register pd_aux, Field extpa_bias_en to enable or disable the external PA. If Register ext_ctrl, Field extpa_auto_en = 1, the external PA automatically turns on when entering, and turns off when exiting the TX state. If this setting is used, the host MCU should not alter the configuration of Register pd_aux, Field extpa_bias_en.

The function of the two pins, PAVSUP_ATB3 and PABIAOP_ATB4, depends on the mode selected with Register extpa_msc, Field extpa_bias_mode, as shown in Table 18.

The reference current source for the DAC is controlled with Register extpa_msc, Field extpa_bias_src (0x3AA[3]). If Register extpa_msc, Field extpa_bias_src = 0, the current is derived from the external bias resistor. If Register extpa_msc, Field extpa_bias_src = 1, the current is derived from the internal reference generator. The first option is more accurate and is recommended whenever possible.

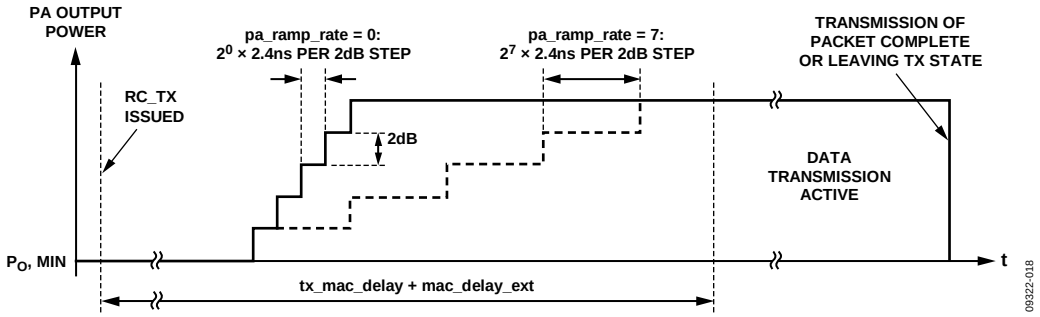


Figure 38. PA Ramping Profile

External PA Interface Modes

- Mode 0 allows supply to an external circuit to be switched on or off. This is useful for circuits that have no dedicated power-down pin and/or have a high power-down current.
- Mode 1 allows the supply to an external circuit to be switched on or off. In addition, the PABIOP_ATB4 pin acts as a programmable current source. A programmable voltage can be generated if a suitable resistor is connected between PABIAOP_ATB4 and GND.
- Mode 2 allows the supply to an external PA circuit to be switched on or off. In addition, the PABIOP_ATB4 pin acts as a programmable current sink. A programmable voltage can be generated if a suitable resistor is connected between PABIAOP_ATB4 and VDD_BAT.
- Mode 3 is the same as Mode 1, except that the switch between PAVSUP_ATB3 and VDD_BAT is open.
- Mode 4 is the same as Mode 2, except that the switch between PAVSUP_ATB3 and VDD_BAT is open.
- Mode 5 is intended for a PA circuit based on a single external FET. The supply voltage to this FET is controlled through the PAVSUP_ATB3 pin to ensure a low leakage current in the power-down state. The bias servo loop controls the gate bias voltage of the external FET such that the current through the supply switch is equal to a reference current. The reference current for the bias servo loop is generated by the 5-bit reference DAC. In this mode, the bias servo loop expects the current in the FET to increase with increasing voltage at the PABIAOP_ATB4 output.
- Mode 6 is the same as Mode 5, except that the bias servo loop expects the current in the FET to increase with decreasing voltage at the PABIAOP_ATB4 output.

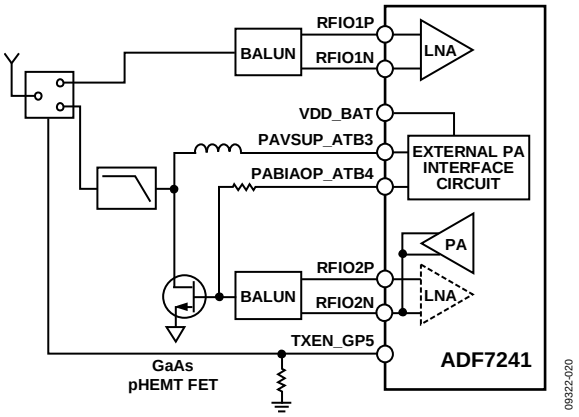


Figure 39. Typical External PA Applications Circuit

Table 18. PA Interface

Register extpa_msc, Field extpa_bias_mode	Register pd_aux, Field extpa_bias_en[1]	VDD_BAT to PAVSUP_ATB3 Switch	Function of Pin PABIAOP_ATB4
X[2]	0	Open	Not used
0	1	Closed	Not used
1	1	Closed	Current source
2	1	Closed	Current sink
3	1	Open	Current source
4	1	Open	Current sink
5	1	Closed	Bias current servo output, positive polarity
6	1	Closed	Bias current servo output, negative polarity
7	1	Reserved	Reserved

[1] Autoenabled when Register ext_ctrl, Field extpa_auto_en = 1.
[2] X = don't care.

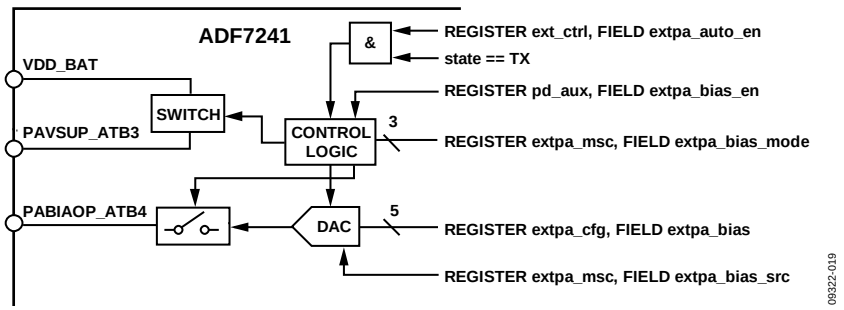


Figure 40. Details of External PA Interface circuit

RECEIVER

RECEIVE OPERATION

The two primary receiver operating modes are

- IEEE 802.15.4-2006 packet manager mode
- IEEE 802.15.4-2006 SPORT mode

The desired operating mode is selected with Register rc_cfg, Field rc_mode. The SPORT modes are explained in more detail in the SPORT Interface section.

The output of the post demodulator filter is fed into a bank of correlators, which compare the incoming data sequences to the expected IEEE 802.15.4-2006 sequences. The receiver block operates in three primary states.

- Preamble qualification
- Symbol timing recovery
- Data symbol reception

During preamble qualification, the correlators check for the presence of preamble. When preamble is qualified, the device enters symbol timing recovery mode. The device symbol timing is achieved once a valid SFD is detected. The ADF7241 supports programmable SFDs. Refer to the Programmable SFD section for further details.

The received symbols are then passed to the packet manager in packet mode or the SPORT interface in SPORT mode. In SPORT mode, four serial clocks are output on Pin TRCLK_CKO_GP3, and four data bits are shifted out on Pin DR_GP0 for each received symbol. Refer to the SPORT Interface section for further details.

If in packet mode, when the packet manager determines the end of a packet, the ADF7241 automatically transitions to PHY_RDY or TX or remains in RX, depending on the setting in Register buffercfg, Field rx_buffer_mode (see Receiver Configuration in Packet Mode section). If in SPORT mode, the part remains in RX until the user issues a command to change to another state.

Programmable SFD

An alternative to the standard IEEE 802.15.4-2006 SFD byte can optionally be selected by the user. The default setting of Register sfd_15_4, Field sfd_symbol_1 and Field sfd_symbol_2 (0x3F4[7:0]) is the standard IEEE 802.15.4-2006 SFD. If the user programs this register with an alternative value, this is used as the SFD in receive and transmit. The requirements are as follows:

- The value must not be a repeated symbol (for example, not 0x11 or 0x22).
- The value must not be similar to the preamble symbol (that is, not Symbol 0x0 or Symbol 0x8).

Receiver Configuration in Packet Mode

Packet management support is selected when Register rc_cfg, Field rc_mode = 0 (0x13E[7:0]). RX_BUFFER is overwritten when the ADF7241 enters the RX state following an RC_RX command and an SFD is detected. The SFD is stripped off the incoming frame, and all data following and including the frame length (PHR) is written to RX_BUFFER.

If Register pkt_cfg, Field auto_fcs_off = 1, the FCS of the incoming frame is stored in RX_BUFFER. When the entire frame has been received, an rx_pkt_rcvd interrupt is asserted irrespective of the correctness of the FCS. If auto_fcs_off = 0, the radio controller calculates the FCS of the incoming frame according to the FCS polynomial defined in the IEEE 802.15.4-2006 standard (see Equation 1), and compares the result against the FCS of the incoming frame. An rx_pkt_rcvd interrupt is asserted only if both FCS fields match. The FCS is not written to RX_BUFFER but is replaced with the measured RSSI and signal quality indicator (SQI) values of the received frame (see Figure 41).

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

The behavior of the radio controller following the reception of a frame can be configured with Register buffercfg, Field rx_buffer_mode (0x107[1:0]). With the default setting rx_buffer_mode = 0, the part reverts automatically to PHY_RDY when an rx_pkt_rcvd interrupt condition occurs. This mode prevents RX_BUFFER from being overwritten by the next frame before the host MCU can read it from the ADF7241. This is because a new frame is always written to RX_BUFFER starting from the address stored in Register rxpb, Field rx_pkt_base (0x315[7:0]). Note that reception of the next frame is inhibited until the MAC delay following an RC_RX command has elapsed.

If Register buffercfg, Field rx_buffer_mode = 1 (0x107[1:0]), the part remains in the RX state, and the reception of the next packet is enabled one MAC delay period after the frame has been written to RX_BUFFER. Depending on the network setup, this mode can cause an unnoticed violation of RX_BUFFER integrity if a frame arrives prior to the MCU having read the frame from RX_BUFFER.

If Register buffercfg, Field rx_buffer_mode = 2 (0x107[1:0]), the reception of frames is disabled. This mode is useful for RSSI measurements and CCA, if the contents of RX_BUFFER are to be preserved.

RECEIVER CALIBRATION

The receive path is calibrated each time an RC_RX command is issued. Figure 42 outlines the synthesizer and receive path calibration sequence and timing. The calibration step VCO_cal is omitted by setting Register vco_cal_cfg, Field skip_vco_cal = 15 (0x36F[3:0]), which is an option if the value of ch_freq[23:0] remains unchanged during transitions between the PHY_RDY, RX, and TX states. The synthesizer settling phase is always required because the PLL bandwidth is optimized differently for RX and TX operation. The static offset correction phase (OCL_stat) and dynamic offset correction phase (OCL_dyn) are also mandatory.

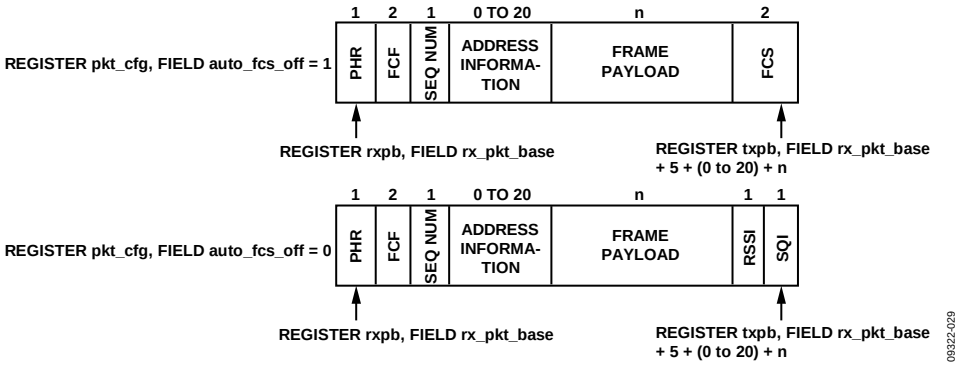


Figure 41. IEEE 802.15.4-2006 Packet Fields Stored by the Packet Manager in RX_BUFFER

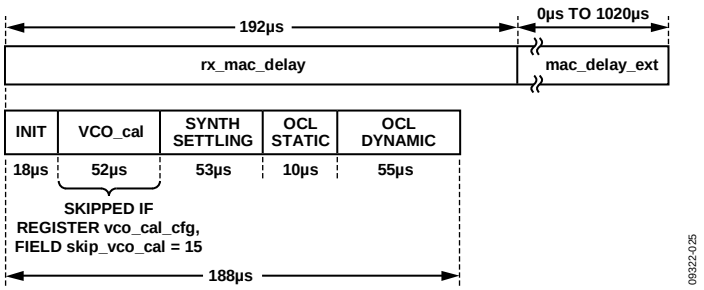


Figure 42. RX Path Calibration

RECEIVE TIMING AND CONTROL

Register rc_cfg, Field rc_mode = 0 (0x13E[7:0]) for packet mode, and Register rc_cfg, Field rc_mode = 2 for RX SPORT mode. See the SPORT Interface section for details on the operation of the SPORT interface. By default, ADF7241 performs a synthesizer and a receiver path calibration immediately after it receives an RC_RX command. The transition into the RX state occurs after the receiver MAC delay has elapsed. The total receiver MAC delay is determined by the sum of the delay times configured in Register delaycfg0, Field rx_mac_delay (0x109[7:0]) and Register delaycfg2, Field mac_delay_ext (0x10B[7:0]). Register delaycfg0, Field rx_mac_delay (0x109[7:0]) is programmable in steps of 1 µs, whereas Register delaycfg2, Field mac_delay_ext (0x10B[7:0]) is programmable in steps of 4 µs. Register delaycfg2, Field mac_delay_ext is typically set to 0. It can, however, be dynamically used to accurately align the RX slot timing.

Figure 43 shows the timing sequence for packet mode. If SPORT mode is enabled, the timing sequence is the same except that no rx_pkt_rcvd interrupt is generated and no automatic transition into the PHY_RDY state occurs.

When entering the RX state, if Register cca2, Field rx_auto_cca = 1 (0x106[1]), a CCA measurement is started. The radio controller asserts a cca_complete interrupt when the CCA result is available in the status word. Upon detection of the SFD, the radio controller asserts an rx_sfd interrupt, which can be used by the host MCU for synchronization purposes. By default, the ADF7241 transitions into the PHY_RDY state when a valid frame has been received into RX_BUFFER and, if enabled, an rx_pkt_rcvd interrupt is asserted. This mechanism protects the integrity of RX_BUFFER. The RX state can be exited at any time by means of an appropriate radio controller command.

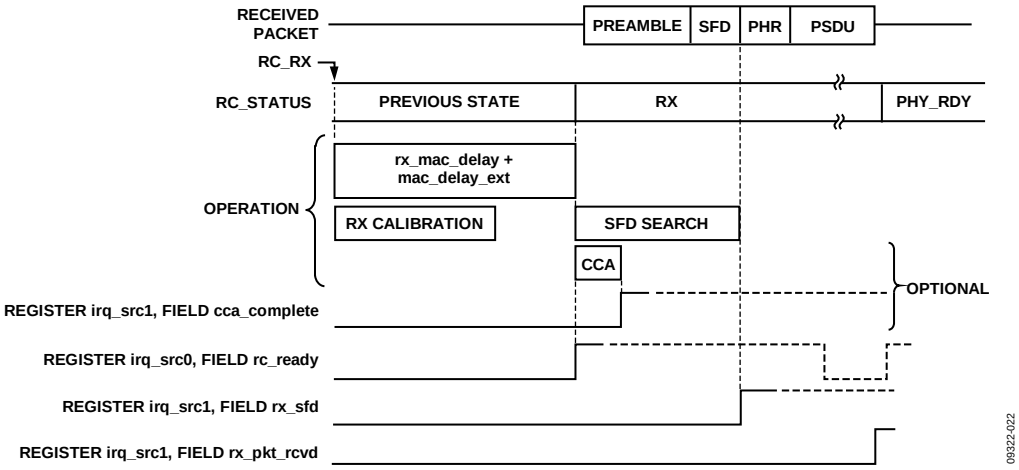


Figure 43. RX Timing and Control

CLEAR CHANNEL ASSESSMENT (CCA)

The CCA function of the ADF7241 complies with CCA Mode 1 as per IEEE 802.15.4-2006. A CCA can be specifically requested by means of an RC_CCA command or automatically obtained when the transceiver enters the RX state. In both cases, the start of the CCA averaging window is defined by when the RC_CCA or RC_RX command is issued and when the delay is configured in Register delaycfg0, Field rx_mac_delay (0x109[7:0]) and Register delaycfg2, Field mac_delay_ext (0x10B[7:0]). The CCA result is determined by comparing Register cca1, Field cca_thres (0x105[7:0]) against the average RSSI value measured throughout the CCA averaging window. If the measured RSSI value is less than the threshold value configured in Register cca1, Field cca_thres (0x105[7:0]), CCA_RESULT in the status word is set; otherwise, it is reset. The cca_complete interrupt is asserted when CCA_RESULT in the status word is valid.

Figure 44 shows the timing sequence after issuing the RC_CCA command when Register cca2, Field continuous_cca = 0 (0x106[2]). Following the RC_CCA command, the transceiver starts the CCA observation window after the delay specified by the sum of Register delaycfg0, Field rx_mac_delay (0x109[7:0]) and Register delaycfg2, field mac_delay_ext (0x10b[7:0]) has elapsed. A cca_complete interrupt is asserted at the end of the CCA averaging window, and the transceiver enters the PHY_RDY state.

When Register cca2, Field continuous_cca = 1 (0x106[2]), the transceiver remains in CCA state and continues to calculate CCA results repeatedly until a RC_PHY_RDY command is issued. This case is illustrated in Figure 45. The first cca_complete interrupt occurs when the first CCA averaging window after the RX MAC delay has elapsed. The transceiver then repeatedly restarts the CCA averaging window each time a cca_complete interrupt is asserted.

This configuration is useful for longer channel scans. CCA_RESULT in the status word can be used to identify if the configured CCA RSSI threshold value has been exceeded during a CCA averaging period. Alternatively, the RSSI value in Register rrb, Field rssi_readback can be read by the host MCU after each cca_complete interrupt. As indicated in Figure 45, the RSSI readback value holds the results of the previous RSSI measurement cycle throughout the CCA averaging window and is updated only shortly before the cca_complete interrupt is asserted.

LINK QUALITY INDICATION (LQI)

The link quality indication (LQI) is defined in the IEEE 802.15.4-2006 standard as a measure of the signal strength and signal quality of a received IEEE 802.15.4-2006 frame. The ADF7241 makes several measurements available from which an IEEE 802.15.4-2006-compliant LQI value can be calculated in the MCU. The first parameter is the RSSI value (see the Automatic Gain Control (AGC) and Receive Signal Strength Indicator (RSSI) subsection of the Receiver Radio Blocks section).

The second parameter required for the LQI calculation can be read from Register lrb, Field sqi_readback (0x30D[7:0]), which contains an 8-bit value representing the quality of a received IEEE 802.15.4-2006 frame. It increases monotonically with the signal quality and must be scaled to comply with the IEEE 802.15.4-2006 standard.

If the ADF7241 is operating in packet mode (Register rc_cfg, Field rc_mode = 0 (0x13E[7:0])), and Register pkt_cfg, Bit auto_fcs_off = 0 (0x108[0]), the SQI of a received frame is measured and stored together with the frame in RX_BUFFER. The SQI is measured over the entire packet and stored in place of the second byte of the FCS of the received frame in RX_BUFFER.

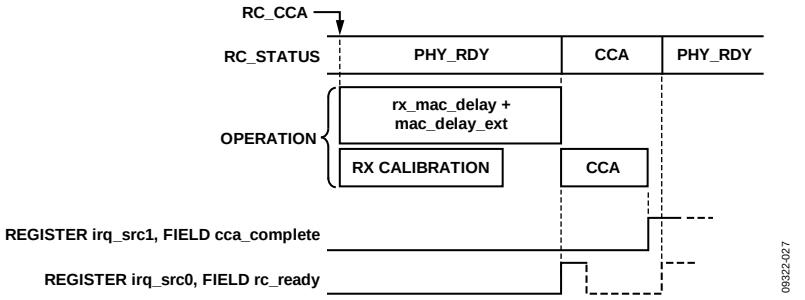


Figure 44. CCA Timing Sequence, Register cca2, Field continuous_cca = 0 (0x106[2])

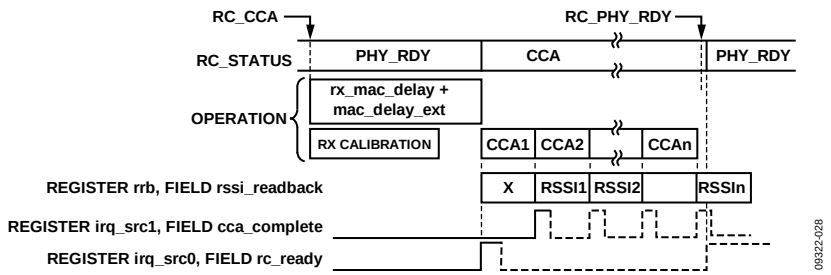


Figure 45. CCA Timing Sequence, Register cca2, Field continuous_cca = 1 (0x106[2])

AUTOMATIC TX-TO-RX TURNAROUND MODE

The ADF7241 features an automatic TX-to-RX turnaround mode when operating in IEEE 802.15.4-2006 packet mode. The automatic TX-to-RX turnaround mode facilitates the timely reception of acknowledgment frames.

Figure 46 illustrates the timing of the automatic TX-to-RX turnaround mode. When enabled by setting Register buffercfg, Field auto_tx_to_rx_turnaround (0x107[3]), the ADF7241 automatically enters the RX state following the transmission of an IEEE 802.15.4-2006 frame. After the combined receiver MAC delay (Register delaycfg0, Field rx_mac_delay + Register delaycfg2, Field mac_delay_ext), the ADF7241 enters the RX state and is ready to receive a frame into RX_BUFFER. Subsequently, when a valid IEEE 802.15.4-2006 frame is received, the ADF7241 enters the PHY_RDY state.

IEEE 802.15.4 FRAME FILTERING, AUTOMATIC ACKNOWLEDGE, AND AUTOMATIC CSMA/CA

The following IEEE 802.15.4-2006 functions are enabled by the firmware module, RCCM_IEEEX:

- Automatic IEEE 802.15.4 frame filtering
- Automatic acknowledgment of received valid IEEE 802.15.4 frames
- Automatic frame transmission using unslotted CSMA/CA with automatic retries

See the Downloadable Firmware Modules and Writing to the ADF7241 sections for details on how to download a firmware module to the ADF7241.

Frame Filtering

Frame filtering is available when the ADF7241 operates in IEEE 802.15.4 packet mode. The frame filtering function rejects received frames not intended for the wireless node. The filtering procedure is a superset of the procedure described in Section 7.5.6.2 (third filtering level) of the IEEE 802.15.4-2006 standard. Field addon_en in Register pkt_cfg controls whether frame filtering is enabled

Automatic Acknowledgment

The ADF7241 has a feature that enables the automatic transmission of acknowledgment frames after successfully receiving a frame. The automatic acknowledgment feature of the receiver can only be used in conjunction with the IEEE 802.15.4 frame filtering feature. When enabled, an acknowledgment frame is automatically transmitted when the following conditions are met:

- The received frame is accepted by the frame filtering procedure.
- The received frame is not a beacon or acknowledgment frame.
- The acknowledgment request bit is set in the FCF of the received frame.

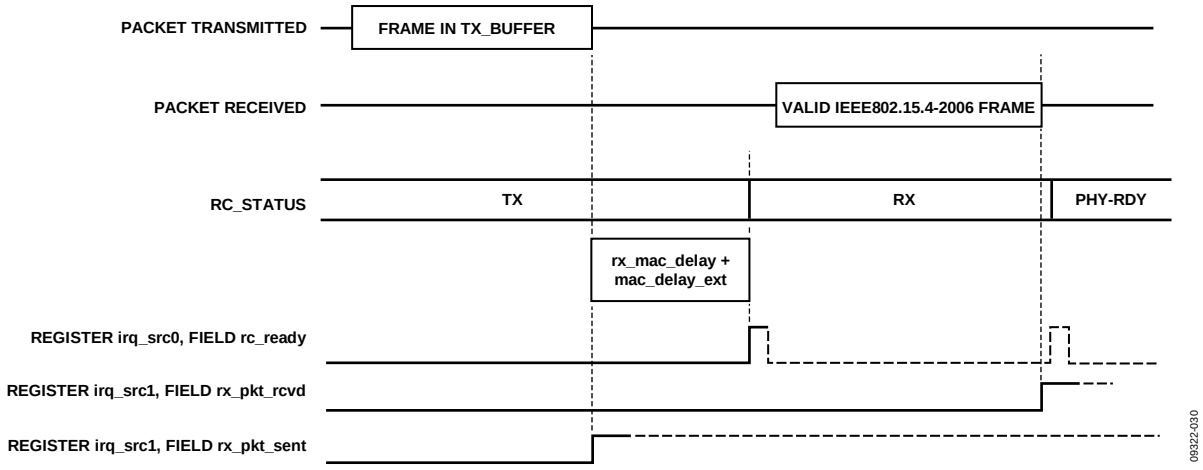


Figure 46. IEEE 802.15.4-2006 Auto TX-to-RX Turnaround Mode

Figure 47 shows the format of the acknowledgment frame assembled by the ADF7241. The sequence number (Seq. Num.) is copied from the frame stored in RX_BUFFER. The automatic acknowledgment feature of the receiver uses TX_BUFFER to store the constructed acknowledgment frame prior to its transmission. Any data present in TX_BUFFER is overwritten by the acknowledgment frame prior to its transmission.

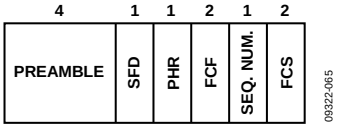


Figure 47. ACK Frame Format

The transmission of the ACK frame starts after the combined delay given by the sum of the delays specified in Register delaycfg1, Field tx_mac_delay and Register delay_cfg2, Field mac_delay_ext has elapsed. The default settings of Register delaycfg1, Field tx_mac_delay = 192 and Register delay_cfg2, Field mac_delay_ext = 0 result in a delay of 192 µs, which suits networks using unslotted CSMA/CA. Optionally, Register delay_cfg2, Field mac_delay_ext can be updated dynamically while the delay specified in Register delaycfg1, Field tx_mac_delay elapses. This option enables accurate alignment of the acknowledgment frame with the back-off slot boundaries in networks using slotted CSMA/CA.

When the receiver automatic acknowledgment mode is enabled, the ADF7241 remains in the RX state until a valid frame has been received. When enabled, an rx_pkt_rcvd interrupt is generated. The ADF7241 then automatically enters the TX state until the transmission of the acknowledgment frame is complete. When enabled, a tx_pkt_sent interrupt is generated to signal the end of the transmission phase. Subsequently, the ADF7241 returns to the PHY_RDY state.

Automatic Unslotted CSMA/CA Transmit Operation

The automatic CSMA/CA transmit operation automatically performs all necessary steps to transmit frames in accordance with the IEEE 802.15.4-2006 standard for unslotted CSMA/CA network operation. It includes automatic CCA retries with random backoff, frame transmission, reception of the acknowledgment frame, and automatic retries in the case of transmission failure. Partial support is provided for slotted CSMA/CA operation.

The number of CSMA/CA CCA retries can be specified between 0 and 5 in accordance with the IEEE 802.15.4 standard. The CSMA/CA can also be disabled, causing the transmission of the frame to commence immediately after the MAC delay has expired. This configuration facilitates the implementation of the transmit procedure in networks using slotted CSMA/CA. In this case, the timing of the CCA operation must be controlled by the host MCU, and the number of retries must be set to 1.

Prior to the transmission of the frame stored in TX_BUFFER, the radio controller checks if the acknowledge request bit in the FCF of that frame is set. If it is set, then an acknowledgment frame is expected following the transmission. Otherwise, the transaction is complete after the frame has been transmitted. The acknowledgment request bit is Bit 5 of the byte located at the address contained in Register txpb, Field tx_packet_base + 1.

Figure 48 depicts the automatic CSMA/CA operation. The firmware module download enables an additional command, RC_CSMACA, to initiate this CSMA/CA operation. It also enables an additional interrupt, csma_ca_complete, to be set to indicate when the CSMA/CA procedure is completed. As per the IEEE 802.15.4-2006 standard for unslotted CSMA/CA, the first CCA is delayed by a random number of backoff periods, where a unit backoff period is 320 µs. The CCA is carried out for a period of 128 µs as specified in the IEEE 802.15.4-2006 standard.

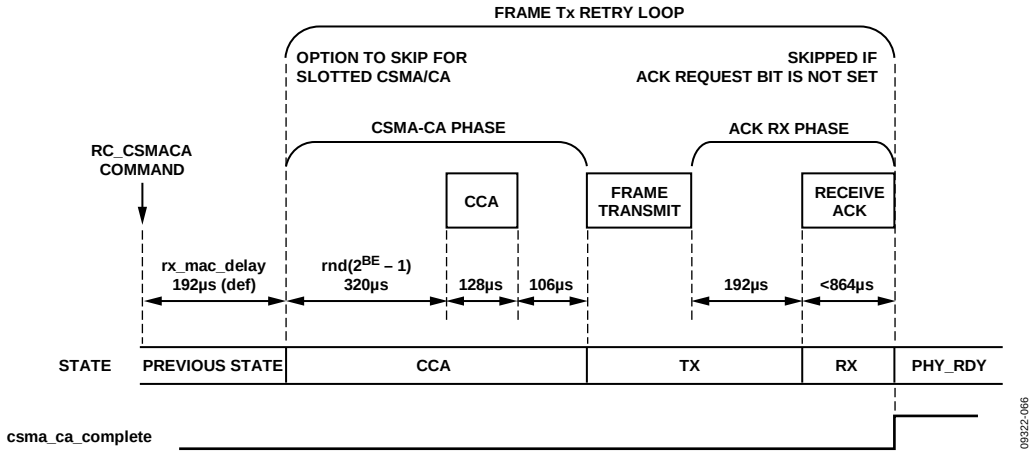


Figure 48. Automatic CSMA/CA Transmit Operation (with CCA)

If a busy channel is detected during the CCA phase, the radio controller performs the next delay/CCA cycle until the maximum number of CCA retries specified has been reached. If the maximum number of allowed CCA retries has been reached, the operation is aborted, and the device transitions to the PHY_RDY state.

If the CCA is successful, the radio controller changes the device state from the CCA state to the TX state and transmits the frame stored in TX_BUFFER. The minimum turnaround time from RX to TX is 106 µs. If neither the acknowledge request bit in the transmitted frame nor the csma_ca_turnaround bit are set, the device returns to the PHY_RDY state immediately upon completion of the frame transmission. Otherwise, it enters the RX state and waits for up to 864 µs for an acknowledgment. If an acknowledgment is not received within this time and the maximum number of frame retries has not been reached, the ADF7241 remains inside the frame transmit retry loop and starts the next CSMA/CA cycle. Otherwise, it exits to the PHY_RDY state. The procedure exits with a csma_ca_complete interrupt.

RECEIVER RADIO BLOCKS

Baseband Filter

Baseband filtering on the ADF7241 is accomplished by a cascade of analog and digital filters. These are configured for optimum performance assuming a crystal frequency tolerance of ±40 ppm.

Offset Correction Loop (OCL)

The ADF7241 is equipped with a fast and autonomous offset correction loop (OCL), which cancels both static and dynamic time-varying offset voltages present in the zero-IF receiver path. The OCL operates continuously and is not constrained by the formatting, timing, or synchronization of the data being received. The scheme is suitable for frequency hopping spread-spectrum (FHSS) communication systems.

Automatic Gain Control (AGC) and Receive Signal Strength Indicator (RSSI)

The ADF7241 AGC circuit features fast overload recovery using dynamic bandwidth adjustments for fast preamble acquisition and optimum utilization of the dynamic range of the receiver path. The radio controller automatically enables the AGC after an offset correction phase, which is carried out when the transceiver enters the RX state.

The RSSI readback value is continuously updated while the ADF7241 is in the RX state. The result is provided in Register rrb, Field rssi_readback (0x30C[7:0]) in decibels relative to 1 mW (dBm) using signed twos complement notation. The RSSI averaging window is synchronized with the start of the active RX phase at the end of the MAC delay following an RC_RX command.

The RSSI averaging period is 128 µs, or eight symbol periods, in compliance with the IEEE 802.15.4-2006 standard. If the ADF7241 is operating in the IEEE 802.15.4-2006 packet mode, the RSSI of received frames is measured and stored together with the frame in RX_BUFFER. The RSSI is measured in a window with a length of eight symbols immediately following the detected SFD. The result is then stored in place of the first byte of the FCS of the received frame in RX_BUFFER. It is also possible to compensate for systematic errors of the measured RSSI value and/or production tolerances by adjusting the RSSI readback value by an offset value that can be programmed in Register agc_cfg5, Field rssi_offs (0x3B9[4:2]). The adjustment resolution is in 1 dB steps.

SPORT INTERFACE

The SPORT interface is a high speed synchronous serial interface suitable for interfacing to a wide variety of MCUs and DSPs, without the use of glue logic. These include, among others, the ADSP-21xx, SHARC, TigerSHARC and Blackfin DSPs. Figure 66 and Figure 67 show typical application diagrams using one of the available SPORT modes. The interface uses four signals, a clock output (TRCLK_CKO_GP3), a receive data output (DR_GP0), a transmit data input (DT_GP1), and a framing signal output (IRQ2_TRFS_GP2). The IRQ2 output functionality is not available while the SPORT interface is enabled. The SPORT interface supports receive and transmit operations. Table 19 lists the SPORT interface options. Refer to Device Configuration section for further details on register programming requirements. To use the SPORT interface for transmitting IEEE 802.15.4 the symbol chipping operation must be performed externally.

SPORT MODE

SPORT Mode Receive Operation

The ADF7241 provides an operating mode in which the SPORT interface is active and the packet manager is bypassed. It allows the reception of packets of arbitrary length. The mode is enabled by setting Register rc_cfg, Field rc_mode = 2 (0x13E[7:0]) and Register gp_cfg, Field gpio_config = 1 (0x32C[7:0]). When the SFD is detected, data and clock signals appear on the SPORT outputs, DR_GP0 and TRCLK_CKO_GP3, respectively. The SPORT interface remains active until an RC_RX command is reissued or the RX state is exited by another command. The rx_pkt_rvcd interrupt is not available in this mode. Figure 7 illustrates the timing for this configuration. Refer to Table 19 for details of pins relevant to the SPORT interface mode.

Receive Symbol Clock in SPORT Mode

The ADF7241 offers a symbol clock output option during IEEE 802.15.4 packet reception. This option is useful when a tight timing synchronization between incoming packets and the network is required, and the SFD interrupt (rx_sfd) cannot be used to achieve this. When in IEEE 802.15.4-2006 packet mode (Register rc_cfg, Field rc_mode = 0), set Register gp_cfg, Field gpio_config = 7 (0x32C[7:0]) to enable the symbol clock output.

SPORT Mode Transmit Operation

TX SPORT mode is enabled by setting Register rc_cfg, Field rc_mode = 3. It is necessary for the host MCU to perform the IEEE 802.15.4 chipping sequence in this mode. The data, sent through the SPORT interface on Pin DT_GP1, should be synchronized with the clock signal that appears on Pin TRCLK_CKO_GP3. Figure 9 shows the timing for this configuration. The polarity of this clock signal can be set by Register gp_cfg, Field gpio_config. The tx_pkt_sent interrupt is not available in this mode. See Table 19 for details of pins relevant to this SPORT mode.

Table 19. SPORT Interface Configuration

Register gp_cfg, Field gpio_config	Register rc_cfg, Field rc_mode	IRQ2_TRFS_GP2	DR_GP0	DT_GP1	RXEN_GP5	RXEN_GP6	TRCLK_CKO_GP3
1	2	RX: ignore	RX: data output, changes at rising edge of data clock	RX: ignore	RX: ignore	RX: ignore	RX: data clock
7	2	RX: ignore	RX: Symbol 0	RX: Symbol 1	RX: Symbol 2	RX: Symbol 3	RX: symbol clock
1	3	TX: ignore	TX: ignore	TX: data input, sampled at rising edge of data clock	TX: ignore	TX: ignore	TX: data clock
4	3	TX: ignore	TX: ignore	TX: data input, sampled at falling edge of data clock	TX: ignore	TX: ignore	TX: data clock

DEVICE CONFIGURATION

After a cold start, or wake-up from sleep, it is necessary to configure the ADF7241. The device can be configured in two ways: an IEEE 802.15.4-2006 packet mode and an IEEE 802.15.4-2006 SPORT mode. Registers applicable to the setup each of the two primary modes are detailed in Table 22.

Table 20 and Table 21 detail the values that should be written to the register locations given in Table 22 to configure the ADF7241 in the desired mode of operation.

CONFIGURATION VALUES

If it is desired to use RF Port 1 rather than RF Port 2 (see the RF Port Configurations/Antenna Diversity section), the value specific to the desired operating mode given in Table 20 should be written to the relevant register field.

Table 20. Settings Required to Select Between LNA Port 1 and LNA Port 2

Address	Register Field	Value
0x39B[4]	rxfe_cfg, lna_sel	0x0: LNA1 0x1: LNA2

Configuration Values for IEEE 802.15.4-2006 Packet and SPORT Modes

No register writes are required to configure IEEE 802.15.4 packet mode unless it is desired to select RF Port 1 rather than RF Port 2. For SPORT mode, the values detailed in Table 21 should be written to the ADF7241.

Table 21. IEEE 802.15.4 Configuration Settings

Address	Register Name	Packet Mode	SPORT Mode
0x13E	rc_cfg	N/A	See Table 19
0x306	tx_m	N/A	0x01
0x32C	gp_cfg	N/A	See Table 19

Note that, if it is desired to use a nonstandard SFD, an additional register write is required. Refer to the Programmable SFD section for details.

Table 22. Register Writes Required to Configure the ADF7241

Register Group Description	Register	IEEE 802.15.4 Packet Mode	IEEE 802.15.4 SPORT Mode
RFIO Port	0x39B	Yes	Yes
Packet/SPORT Mode Selection	0x13E	No	Yes
SPORT Mode Configuration	0x32C	No	Yes
Sync Word	0x3F4[1]	Yes[1]	Yes[1]
Transmit Filters	0x306	No	Yes

[1] This applies only when the user wishes to program a nonstandard SFD.

RF PORT CONFIGURATIONS/ANTENNA DIVERSITY

ADF7241 is equipped with two fully differential RF ports. Port 1 is capable of receiving, whereas Port 2 is capable of receiving or transmitting. RF Port 1 comprises Pin RFIO1P and Pin RFIO1N, and RF Port 2 comprises Pin RFIO2P and Pin RFIO2N. Only one of the two RF ports can be active at any one time.

The availability of two RF ports facilitates the use of switched antenna diversity and results in a simplified application circuit if the ADF7241 is connected to an external LNA and/or PA. Port selection for receive operation is configured through Register rxfe_cfg, Field lna_sel (0x39B[4]).

Configuration A

Configuration A of Figure 49 is the default connection where a single antenna is connected to RF Port 2. This selection is made by setting Register rxfe_cfg, Field lna_sel = 1 (default setting).

Configuration B

Configuration B shows a dual-antenna configuration that is suitable for switched antenna diversity. In this case, the link margin can be maximized by comparing the RSSI level of the signal received on each antenna and thus selecting the optimum antenna. In addition, the SQI value in Register lrb, Field sqi_readback can be used in the antenna selection decision.

Suitable algorithms for the selection of the optimum antenna depend on the particulars of the underlying communication system. Switching between two antennas is likely to cause a short interruption of the received data stream. Therefore, it is advisable to synchronize the antenna selection phase with the preamble component of the packet. In a static communication system, it is often sufficient to select the optimum antenna once.

Configuration C

Configuration C shows that connecting an external PA and/or LNA is possible with a single external receive/transmit switch. The PA transmits on RF Port 2. RF Port 1 is configured as the receive input (Register rxfe_cfg, Field lna_sel = 0).

ADF7241 provides two signals, RXEN_GP6 and TXEN_GP5, to automatically enable an external LNA and/or a PA. If Register ext_ctrl, Field txen_en = 1, the ADF7241 outputs a logic high level at the TXEN_GP5 pin while in TX state, and a logic low level while in any other state. If Register ext_ctrl, Field rxen_en = 1, the ADF7241 outputs a logic high level at the RXEN_GP6 pin while in RX state and a logic low level while in any other state.

The RXEN_GP6 and TXEN_GP5 outputs have high impedance in the sleep state. Therefore, appropriate pull-down resistors must be provided to define the correct state of these signals during power-down. See the PA Ramping Controller section for further details on the use of an external PA, including details of the integrated biasing block, which simplifies connection to PA circuits based upon a single FET.

Configuration D

Configuration D is similar to Configuration A, except that a dipole antenna is used. In this case, a balun is not required.

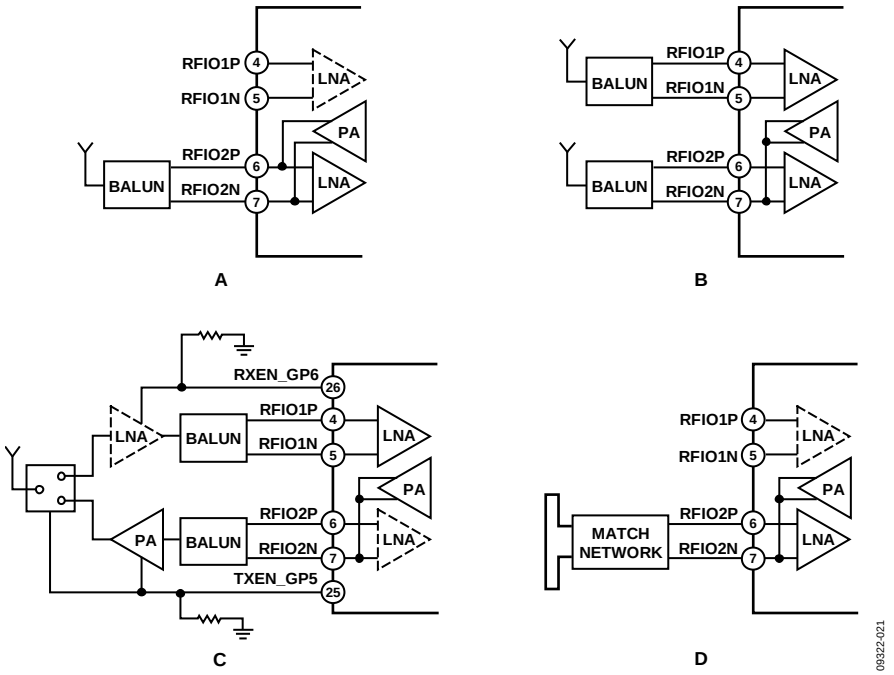


Figure 49. RF Interface Configuration Options (A: Single Antenna; B: Antenna Diversity; C: External LNA/PA; D: Dipole Antenna)

AUXILLARY FUNCTIONS

TEMPERTURE SENSOR

To perform a temperature measurement, the MEAS state is invoked using the RC_MEAS command. The result can be read back from Register adc_rbk, Field adc_out (0x3AE[5:0]). Averaging multiple readings improves the accuracy of the result. The temperature sensor has an operating range from −40°C to +85°C.

The die (ambient) temperature is calculated as follows:

$$t_{die} = (4.72°C \times Register\ adc_rbk, Field\ adc_out) + 65.58°C + correction\ value.$$

where *correction value* can be determined by performing a readback at a single known temperature. Note also that averaging a number of ADC readbacks can improve the accuracy of the temperature measurement.

BATTERY MONITOR

The battery monitor features very low power consumption and can be used in any state other than the sleep state. The battery monitor generates a batt_alert interrupt for the host MCU when the battery voltage drops below the programmed threshold voltage. The default threshold voltage is 1.7 V, and can be increased in 62 mV steps to 3.6 V with Register bm_cfg, Field battmon_voltage (0x3E6[4:0]).

WAKE-UP CONTROLLER (WUC)

Circuit Description

The ADF7241 features a 16-bit wake-up timer with a programmable prescaler. The 32.768 kHz RC oscillator or the 32.768 kHz external crystal provides the clock source for the timer. This tick rate clocks a 3-bit programmable prescaler whose output clocks a preloadable 16-bit down counter. An overview of the timer circuit is shown in Figure 50 lists the possible division rates for the prescaler. This combination of programmable prescaler and 16-bit down counter gives a total WUC range of 30.52 µs to 36.4 hours.

Table 23. Prescaler Division Factors

timer_prescal (0x316[2:0])	32.768 kHz Divider	Tick Period
000	1	30.52 µs
001	4	122.1 µs
010	8	244.1 µs
011	16	488.3 µs
100	128	3.91 ms
101	1024	31.25 ms
110	8,192	250 ms
111	65,536	2000 ms

An interrupt generated when the wake-up timer has timed out can be enabled in Register irq1_en0 or Register irq2_en0.

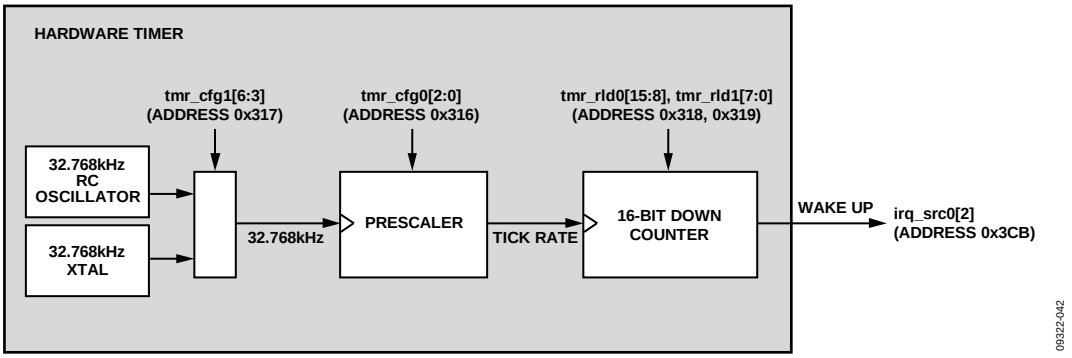


Figure 50. Hardware Wake-Up Timer Diagram

WUC Configuration and Operation

The wake-up timer can be configured as follows:

- The clock signal for the timer is taken from the external 32.768 kHz crystal or the internal RC oscillator. This is selectable via Register tmr_cfg1, Field sleep_config (0x317[6:3]).
- A 3-bit prescaler, which is programmable via Register tmr_cfg0, Field timer_prescal (0x316[2:0]) determines the tick period.

This is followed by a preloadable 16-bit down counter. After the clock is selected, the reload value for the down counter (tmr_rld0 and tmr_rld1) and the prescaler values (Register tmr_cfg0, Field timer_prescal) can be programmed. When the clock has been enabled, the counter starts to count down at the tick rate starting from the reload value. If wake-up interrupts are enabled, the timer unit generates an interrupt when the timer value reaches 0x0000. When armed, the wake-up interrupt triggers a wake-up from sleep.

The reliable generation of wake-up interrupts requires the WUC timeout flag to be reset immediately after the reload value has been programmed. To do this, first write 1 and then write 0 to Register tmr_ctrl, Field wake_timer_flag_reset. To enable automatic wake-up from the sleep state, arm the timer unit for wake-up operation by writing 1 to Register tmr_cfg1, Field wake_on_timeout. After writing this sequence to the ADF7241, a sleep command can be issued.

Calibrating the RC oscillator

The RC oscillator is not automatically calibrated. If it is desired to use the RC oscillator as the clock source for the WUC, the host MCU should initiate a calibration. This can be performed at any time in advance of entering the sleep state. To perform a calibration, the host MCU should

- Set Register tmr_ctrl, Field wuc_rc_osc_cal = 0
- Set Register tmr_ctrl, Field wuc_rc_osc_cal = 1

The calibration time is typically 1 ms. When the calibration is complete Register wuc_32khzosc_status, Field rc_osc_cal_ready is high. Following calibration, the host MCU can transition to the SLEEP_BBRAM_RCO sleep state, by following the full procedure given in the WUC Configuration and Operation section.

TRANSMIT TEST MODES

The ADF7241 has various transmit test modes that can be used in SPORT mode. These test modes can be enabled by writing to Register tx_test (Location 0x3F0), as described in Table 24. A continuous packet transmission mode is also available in packet mode. This mode can be enabled using the following procedure:

1. An IEEE 80.215.4-2006 packet with random payload should be written to TX_BUFFER as described in the Transmitter section. It is recommended to use a packet with the maximum length of 127 bytes.
2. Set Register buffercfg, Field trx_mac_delay = 1.
3. Set Register buffercfg, Field tx_buffer_mode = 3.
4. Set Register pkt_cfg, Field skip_synth_settle = 1.
5. Issue Command RC_TX. The transmitter continuously transmits the packet stored in TX_BUFFER.
6. If Command RC_PHY_RDY is issued at any point after this step, all the preceding configuration registers must be rewritten to the device before reissuing Command RC_TX.

Note that the transmitter momentarily transmits an RF carrier between packets due to a finite delay from when the packet handler finishes transmitting a packet in TX_BUFFER and going back to transmit the start of TX_BUFFER again.

Table 24. 0x3F0: tx_test

Bit	Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	2	Reserved, set to default.
1	carrier_only	R/W	0	Transmits unmodulated tone at the programmed frequency f_{CH}.
0	Reserved	R/W	0	Reserved, set to default.

SERIAL PERIPHERAL INTERFACE (SPI)

GENERAL CHARACTERISTICS

The ADF7241 is equipped with a 4-wire SPI interface, using the SCLK, MISO, MOSI, and $\overline{CS}$ pins. The ADF7241 always acts as a slave to the host MCU. Figure 51 shows an example connection diagram between the host MCU and the ADF7241. The diagram also shows the direction of the signal flow for each pin. The SPI interface is active and the MISO output enabled only while the $\overline{CS}$ input is low. The interface uses a word length of eight bits, which is compatible with the SPI hardware of most microprocessors. The data transfer through the SPI interface occurs with the most significant bit of address and data first. Refer to Figure *3* for the SPI interface timing diagram. The MOSI input is sampled at the rising edge of SCLK. As commands or data are shifted in from the MOSI input at the SCLK rising edge, the status word or data is shifted out at the MISO pin synchronous with the SCLK clock falling edge. If $\overline{CS}$ is brought low, the most significant bit of the status word appears on the MISO output without the need for a rising clock edge on the SCLK input.

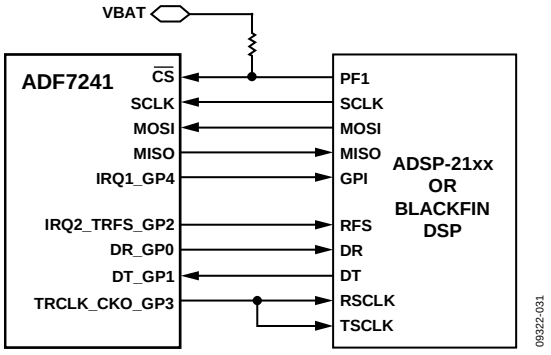


Figure 51. SPI Interface Connection

COMMAND ACCESS

The ADF7241 is controlled through commands. Command words are single-byte instructions that control the state transitions of the radio controller and access to the registers and packet RAM. The complete list of valid commands is given in Table 25. Commands with the RC prefix are handled by the radio controller, whereas memory access commands, which have the SPI prefix are handled by an independent controller. Thus, SPI commands can be issued independent of the state of the radio controller.

A command is initiated by bringing $\overline{CS}$ low and shifting in the command word over the SPI as shown in Figure 52.

All commands are executed after $\overline{CS}$ goes high again or at the next positive edge of the SCLK input. The latter condition occurs in the case of a memory access command. In this case, the command is executed on the positive SCLK clock edge corresponding to the most significant bit of the first parameter word. The $\overline{CS}$ input must be brought high again after a command has been shifted into the ADF7241 to enable the recognition of successive command words. This is because a single command can be issued only during a $\overline{CS}$ low period (with the exception of a double NOP command).

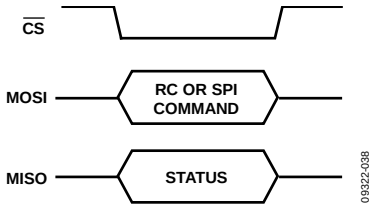


Figure 52. Command Write

The execution of certain commands by the radio controller may take several instruction cycles, during which the radio controller unit is busy. Prior to issuing a radio controller command, it is, therefore, necessary to read the status word to determine if the ADF7241 is ready to accept a new radio controller command. This is best accomplished by shifting in SPI_NOP commands, which cause status words to be shifted out. The RC_READY variable is used to indicate when the radio controller is ready to accept a new RC command, whereas the SPI_READY variable indicates when the memory can be accessed. To take the burden of repeatedly polling the status word off the host MCU for complex commands such as RC_RX, RX_TX, and RC_PHY_RDY, the IRQ handler can be configured to generate an RC_READY interrupt. See the Interrupt Controller section for details. Otherwise, the user can program timeout periods according to the command execution times provided under the state transition timing given in Table 10.

STATUS WORD

The status word of the ADF7241 is automatically returned over the MISO each time a byte is transferred over the MOSI. The meaning of the various status word bit fields is illustrated in Table 26. The RC_STATUS field reflects the current state of the radio controller. By definition, RC_STATUS reflects the state of a completed state transition. During the state transition, RC_STATUS maintains the value of the state from which the state transition was invoked.

Table 25. Command List

Command	Code	Description
SPI_NOP	0xFF	No operation. Use for dummy writes.
SPI_PKT_WR	0x10	Write data to the packet RAM starting from the transmit packet base address pointer, Register txpb, Field tx_pkt_base (0x314[7:0]).
SPI_PKT_RD	0x30	Read data from the packet RAM starting from the receive packet base address pointer, Register rxpb, Field rx_pkt_base (0x315[7:0]).
SPI_MEM_WR	0x18 + memory address[10:8]	Write data to MCR or packet RAM sequentially.
SPI_MEM_RD	0x38 + memory address[10:8]	Read data from MCR or packet RAM sequentially.
SPI_MEMR_WR	0x08 + memory address[10:8]	Write data to MCR or packet RAM as a random block.
SPI_MEMR_RD	0x28 + memory address[10:8]	Read data from MCR or packet RAM as a random block.
SPI_PRAM_WR	0x1E	Write data to the program RAM.
RC_SLEEP	0xB1	Invoke transition of the radio controller into the sleep state
RC_IDLE	0xB2	Invoke transition of the radio controller into the idle state
RC_PHY_RDY	0xB3	Invoke transition of the radio controller into the PHY_RDY state
RC_RX	0xB4	Invoke transition of the radio controller into the RX state
RC_TX	0xB5	Invoke transition of the radio controller into the TX state
RC_MEAS	0xB6	Invoke transition of the radio controller into the MEAS state
RC_CCA	0xB7	Invoke clear channel assessment
RC_PC_RESET	0xC7	Program counter reset. This should only be used after a firmware download to the program RAM
RC_RESET	0xC8	Resets the ADF7241 and puts it in the sleep state

Table 26. SPI Status Word

Bit	Name	Description
7	SPI_READY	0: SPI is not ready for access. 1: SPI is ready for access.
6	IRQ_STATUS	0: no pending interrupt condition. 1: pending interrupt condition. (IRQ_STATUS = 1 when either the IRQ1_GP4 or IRQ2_TRFS_GP2 pin is high)
5	RC_READY	0: radio controller is not ready to accept RC_xx command strobe. 1: radio controller is ready to accept new RC_xx command strobe.
4	CCA_RESULT	0: channel busy. 1: channel idle. Valid when Register irq_src1, Bit cca_complete (0x3CC[0]) is asserted.
[3:0]	RC_STATUS	Radio controller status: 0: reserved. 1: idle. 2: MEAS. 3: PHY_RDY. 4: RX. 5: TX. 6 to 15: reserved.

MEMORY MAP

The various memory locations used by the ADF7241 are shown in Figure 53. The radio control and packet management of the part are realized through the use of an 8-bit, custom processor, and an embedded ROM. The processor executes instructions stored in the embedded program ROM. There is also a local RAM, subdivided into three sections, that is used as a data packet buffer, both for transmitted and received data (packet RAM), and for storing the radio and packet management configuration (BBRAM and MCR). The RAM addresses of these variables are 11 bits in length.

BBRAM

The 64-byte battery back-up, or BBRAM, is used to maintain settings needed at wake-up from sleep state by the wake-up controller.

MODEM CONFIGURATION RAM (MCR)

The 256-byte modem configuration RAM, or MCR, contains the various registers used for direct control or observation of the physical layer radio blocks of the ADF7241. Contents of the MCR are not retained in the sleep state.

PROGRAM ROM

The program ROM consists of 4 kB of nonvolatile memory. It contains the firmware code for radio control, packet management, and smart wake mode.

PROGRAM RAM

The program RAM consists of 2 kB of volatile memory. This memory space is used for various software modules, such as address filtering and CSMA/CA, which are available from Analog Devices. The software modules are downloaded to the program RAM memory space over the SPI by the host microprocessor. See the Program RAM Write subsection of the Memory Access section for details on how to write to the program RAM.

PACKET RAM

The packet RAM consists of 256 bytes of memory space from Address 0x000 to Address 0x0FF, as shown in Figure 53. This memory is allocated for storage of data from valid received packets and packet data to be transmitted. The packet manager stores received payload data at the memory location indicated by the value of Register rxpb, Field rx_pkt_base, the receive address pointer. The value of Register txpb, Field tx_pkt_base, the transmit address pointer, determines the start address of data to be transmitted by the packet manager. This memory can be arbitrarily assigned to store single or multiple transmit or receive packets, both with and without overlap as shown in Figure 54. The rx_pkt_base value should be chosen to ensure that there is enough allocated packet RAM space for the maximum receiver payload length.

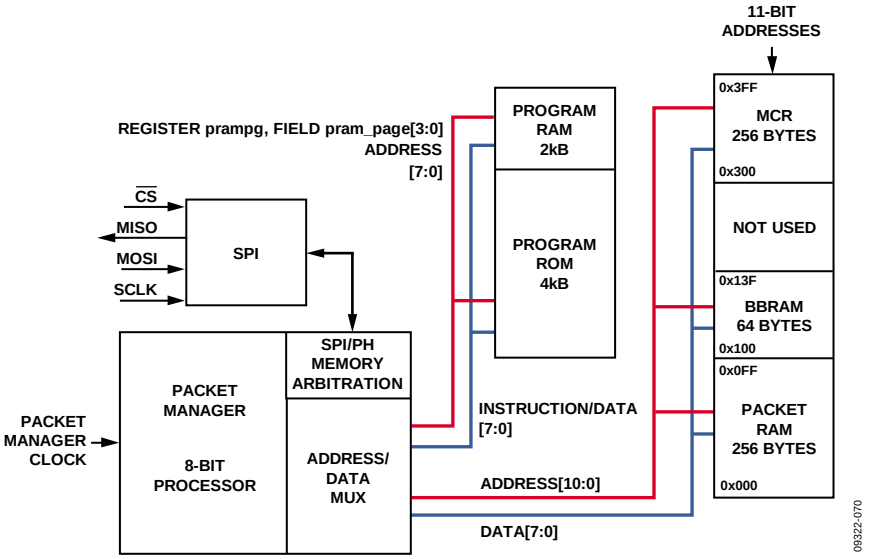


Figure 53. ADF7241 Memory Map

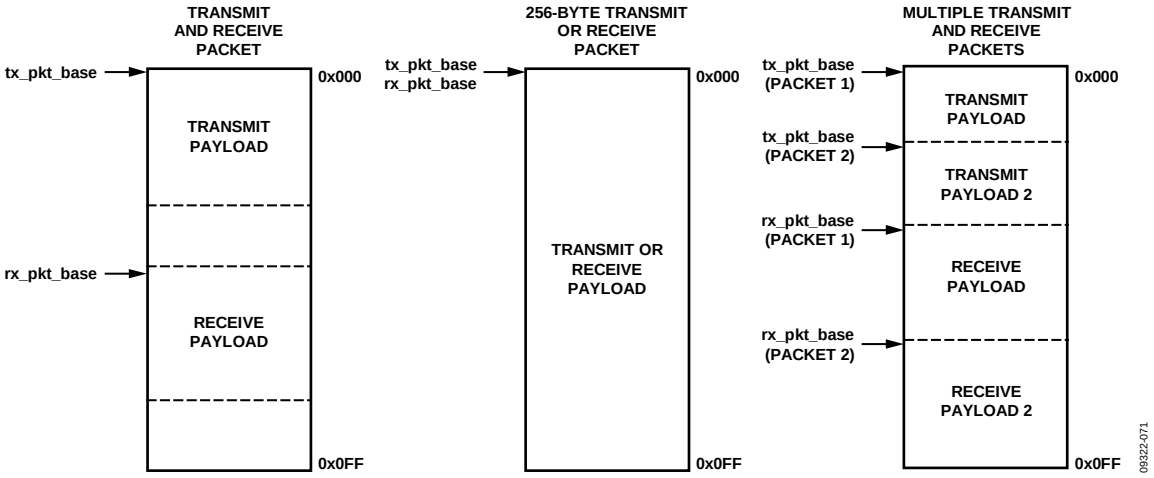


Figure 54. Example Packet RAM Configurations Using the Transmit Packet and Receive Packet Address Pointers

MEMORY ACCESS

Memory locations are accessed by invoking the relevant SPI command. An 11-bit address is used to identify registers or locations in the memory space. The most significant three bits of the address are incorporated into the command by appending them as the LSBs of the command word. Figure 55 illustrates the command, address, and data partitioning. The various SPI memory access commands are different depending on the memory location being accessed. This is described in Table 27.

An SPI command should be issued only if the SPI_READY bit of the status word is high.

In addition, an SPI command should not be issued while the radio controller is initializing. SPI commands can be issued in any radio controller state including during state transition.

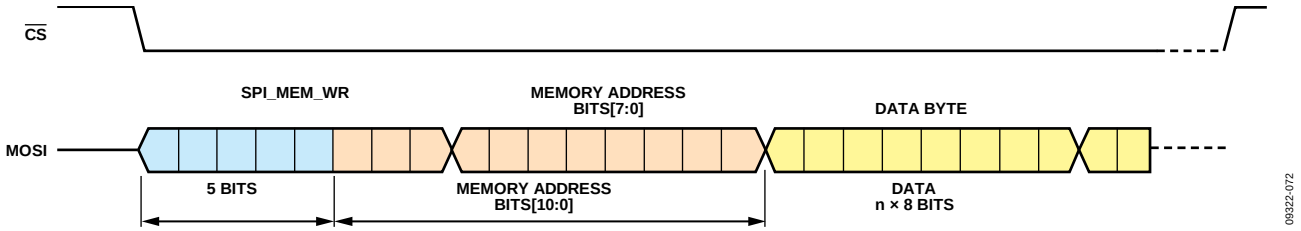


Figure 55. SPI Memory Access Command/Address Format

Table 27. Summary of SPI Memory Access Commands

SPI Command	Command Value	Description
SPI_PKT_WR	= 0x10	Write telegram to the packet RAM starting from the transmit packet base address pointer, Register txpb, Field tx_pkt_base (0x314[7:0]).
SPI_PKT_RD	= 0x30	Read telegram from the packet RAM starting from receive packet base address pointer, Register rxpb, Field rx_pkt_base (0x315[7:0]).
SPI_MEM_WR	= 0x18 (packet RAM) = 0x19 (BBRAM) = 0x1B (MCR)	Write data to BBRAM, MCR, or packet RAM sequentially. An 11-bit address is used to identify memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address.
SPI_MEM_RD	= 0x38 (packet RAM) = 0x39 (BBRAM) = 0x3B (MCR)	Read data from BBRAM, MCR, or packet RAM sequentially. An 11-bit address is used to identify memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address, which is subsequently followed by the appropriate number of SPI_NOP commands.
SPI_MEMR_WR	= 0x08 (packet RAM) = 0x09 (BBRAM) = 0x0B (MCR)	Write data to BBRAM/MCR or packet RAM at random.
SPI_MEMR_RD	= 0x28 (packet RAM) = 0x29 (BBRAM) = 0x2B (MCR)	Read data from BBRAM/MCR or packet RAM at random.
SPI_PRAM_WR	=0x1E (program RAM)	Write data to program RAM.
SPI_PRAM_RD	= 0x3E (program RAM)	Read data from program RAM
SPI_NOP	= 0xFF	No operation. Use for dummy writes when polling the status word and used as dummy data on the MOSI line when performing a memory read.

WRITING TO THE ADF7241

Block Write

Packet RAM memory locations can be written to in block format using the SPI_PKT_WR. The SPI_PKT_WR command is 0x10. This command provides pointer-based write access to the packet RAM. The address of the location written to is calculated from the base address in Register txpb, Field tx_pkt_base (0x314[7:0]), plus an index. The index is zero for the first data word following the command word and is auto-incremented for each consecutive data word written. The first data word following an SPI_PKT_WR command is, thus, stored in the location with Address txpb, Field tx_pkt_base (0x314[7:0]), the second in packet RAM location with Address txpb, Field tx_pkt_base + 1, and so on. This feature makes this command efficient for bulk writes of data that recurrently begin at the same address. Figure 56 shows the access sequence for Command SPI_PKT_WR.

The MCR, BBRAM, and packet RAM memory locations can be written to in block format using the SPI_MEM_WR command. The SPI_MEM_WR command code is 00011xxxb, where xxxb represent Bits[10:8] of the first 11-bit address. If more than one data byte is written, the write address is automatically incremented for every byte sent until $\overline{CS}$ is set high, which terminates the memory access command. See Figure 57 for more details. The maximum block write for the MCR, packet RAM, and BBRAM memories are 256 bytes, 256 bytes, and 64 bytes, respectively. These maximum block-write lengths should not be exceeded.

Example

Write 0x00 to the rc_cfg register (Location 0x13E).

- The first five bits of the SPI_MEM_WR command are 00011.
- The 11-bit address of rc_cfg is 00100111110.
- The first byte sent is 00011001 or 0x19.
- The second byte sent is 00111110 or 0x3E.
- The third byte sent is 0x00.

Thus, 0x193F00 is written to the part.

Random Address Write

MCR, BBRAM, and packet RAM memory locations can be written to in random address format using the SPI_MEMR_WR command. The SPI_MEMR_WR command code is 00001xxxb, where xxxb represent Bits[10:8] of the 11-bit address. The lower eight bits of the address should follow this command and then the data byte to be written to the address. The lower eight bits of the next address are entered followed by the data for that address until all required addresses within that block are written, as shown in Figure 58. Note that the SPI_MEMR_WR command facilitates the modification of individual elements of a packet in RX_BUFFER and TX_BUFFER without the need to download and upload an entire packet.

The address location of a particular byte in RX_BUFFER and TX_BUFFER in the packet RAM is determined by adding the relative location of a byte to Address Pointer rx_pkt_base (Register rxpb; 0x315[7:0]) or Address Pointer tx_pkt_base (Register txpb; 0x314[7:0]), respectively.

Program RAM Write

The program RAM can only be written to using the memory block write, as illustrated in Figure 59. The SPI_PRAM_WR command is 0x1E. The program RAM is organized in eight pages with a length of 256 bytes each. The code module must be stored in the program RAM starting from Address 0x0000, or Address 0x00 in Page 0. The current program RAM page is selected with Register prampg, Field pram_page (0x313[3:0]). Prior to uploading the program RAM, the radio controller code module must be divided into blocks of 256 bytes commensurate with the size of the program RAM pages. Each 256-byte block is uploaded into the currently selected program RAM page using the SPI_PRAM_WR command. Figure 59 illustrates the sequence required for uploading a code block of 256 bytes to a PRAM page. The SPI_PRAM_WR command code is followed by Address Byte 0x00 to align the code block with the base address of the program RAM page. Figure 60 shows the overall upload sequence. With the exception of the last page written to the program RAM, all pages must be filled with 256 bytes of module code.

READING FROM THE ADF7241

Block Read

Command SPI_PKT_RD provides pointer-based read access from the packet RAM. The SPI_PKT_RD command is 0x30. The address of the location to be read is calculated from the base address in Register rxpb, Field rx_pkt_base, plus an index. The index is zero for the first readback word. It is auto-incremented for each consecutive SPI_NOP command. The first data byte following a SPI_PKT_RD command is invalid and should be ignored. Figure 61 shows the access sequence for Command SPI_PKT_RD.

The SPI_MEM_RD command can be used to perform a block read of MCR, BBRAM, and packet RAM memory locations. The SPI_MEM_RD command code is 00111xxxb, where xxxb represent Bits[10:8] of the first 11-bit address. This command is followed by the remaining eight bits of the address to be read and then two SPI_NOP commands (dummy byte). The first byte available after writing the address should be ignored, with the second byte constituting valid data. If more than one data byte is to be read, the read address is automatically incremented for subsequent SPI_NOP commands sent. See Figure 62 for more details.

Random Address Read

MCR, BBRAM, and Packet RAM memory locations can be read from in a nonsequential manner using the SPI_MEMR_RD command. The SPI_MEMR_RD command code is 00101xxxb, where xxxb represent Bits[10:8] of the 11-bit address. This command is followed by the remaining eight bits of the address to be written and then two SPI_NOP commands (dummy byte).

The data byte from memory is available on the second SPI_NOP command. For each subsequent read, an 8-bit address should be followed by two SPI_NOP commands as shown in Figure *63*.

Example

Read the value stored in the rc_cfg register.

- The first five bits of the SPI_MEM_RD command are 00111.
- The 11-bit address of rc_cfg register is 00100111111.
- The first byte sent is 00111001, or 0x39.
- The second byte sent is 00111110, or 0x3E.
- The third byte sent is 0xFF (SPI_NOP).
- The fourth byte sent is 0xFF.

Thus, 0x393EFFFF is written to the part.

The value shifted out on the MISO line while the fourth byte is sent is the value stored in the rc_cfg register.

This allows individual elements of a packet in RX_BUFFER and TX_BUFFER to be read without the need to download the entire packet.

Program RAM Read

The SPI_PRAM_RD command is used to read from the program RAM. This may be performed to verify that a firmware module has been correctly written to the program RAM. Like the SPI_PRAM_WR command, the host MCU must select the program RAM page to read via Register prampg, Field pram_page. Following this, the host MCU may use the SPI_PRAM_RD command to block read the selected program RAM page. The structure of this command is identical to the SPI_MEM_RD command.

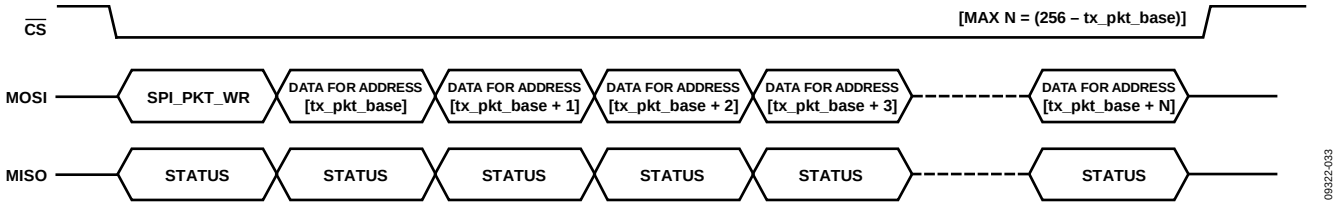


Figure 56. Packet RAM Write
(tx_pkt_base is the address base pointer value for TX, which is programmed in Register txbp, Bit tx_pkt_base.)

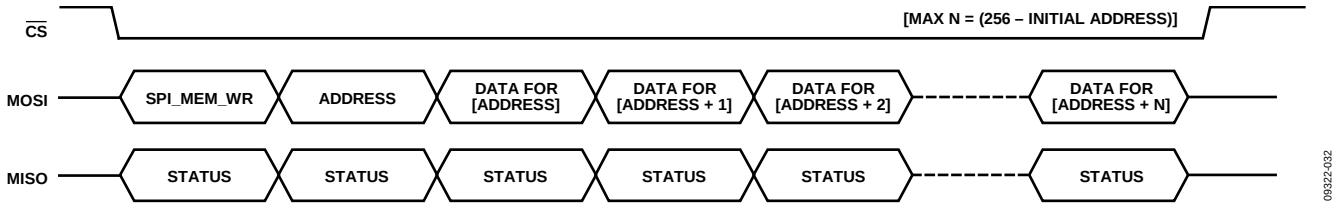


Figure 57. Memory (Register or Packet RAM) Block Write

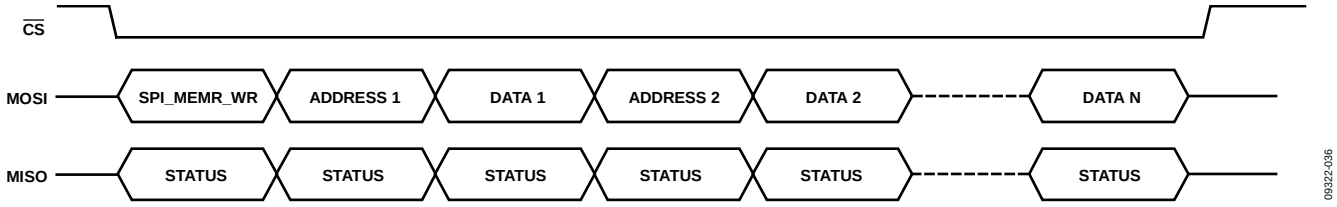


Figure 58. Memory (Register or Packet RAM) Random Address Write

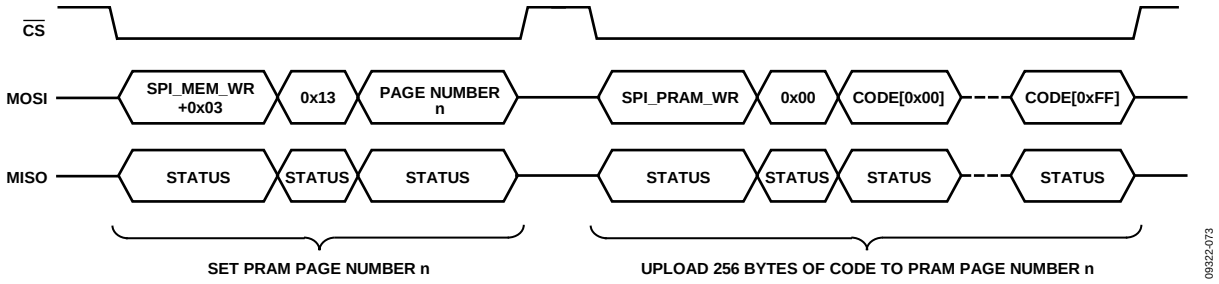


Figure 59. Upload Sequence for a Program RAM Page



Figure 60. Download Sequence for Code Module

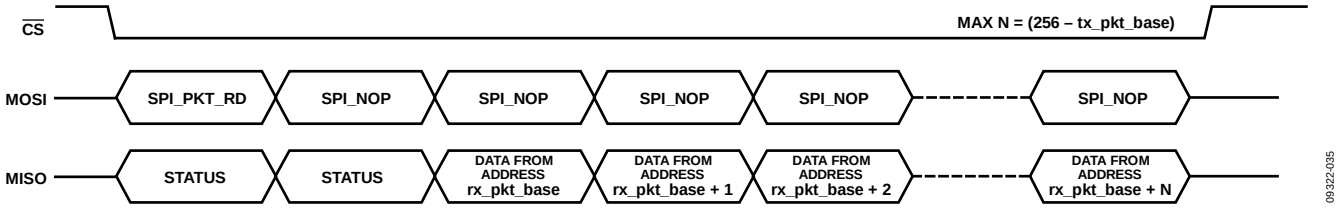


Figure 61. Packet RAM Read
(rx_pkt_base is the address base pointer value for RX, which is programmed in Register rxbp, Bit rx_pkt_base.)

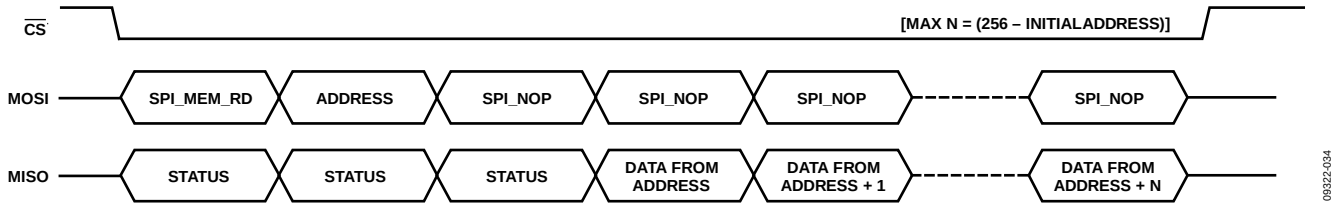


Figure 62. Memory (Register or Packet RAM) Block Read

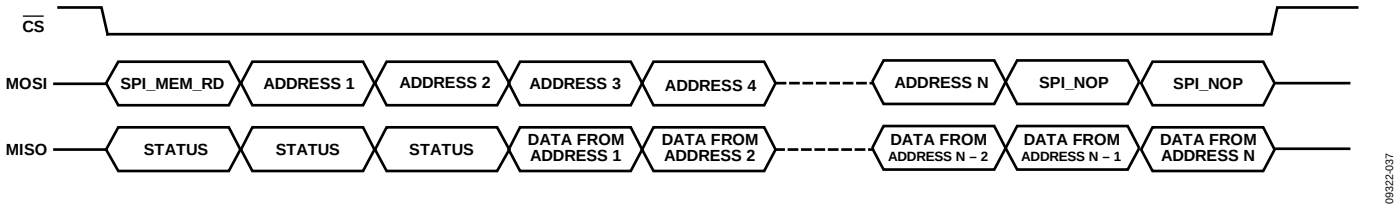


Figure 63. Memory (Register or Packet RAM) Random Address Read

DOWNLOADABLE FIRMWARE MODULES

The program RAM of the ADF7241 can be used to store firmware modules for the on-chip processor that provide extra functionality. The executable code for these firmware modules and details on their functionality are available from Analog Devices. See the Writing to the ADF7241 section for details on how to download these firmware modules to program RAM.

INTERRUPT CONTROLLER

CONFIGURATION

The ADF7241 is equipped with an interrupt controller that is capable of handling up to 16 independent interrupt events. The interrupt events can be triggered either by hardware circuits or the packet manager and are captured in Register irq_src0 (0x3CB) and Register irq_src1(0x3CC).

The interrupt signals are available on two interrupt pins: IRQ1_GP4 and IRQ2_TRFS_GP2. Each of the 16 interrupt sources can be individually enabled or disabled. The irq1_en0 (0x3C7) and irq1_en1 (0x3C8) registers control the functionality of the IRQ1_GP4 interrupt pin. The irq2_en0 (0x3C9) and irq2_en1 (0x3CA) registers control the functionality of the IRQ2_TRFS_GP2 interrupt pin. Refer to Table 28 and Table 29 for details on which bits in the relevant interrupt source and interrupt enable registers correspond to the different interrupts.

The IRQ_STATUS bit of the SPI status word, is asserted if an interrupt is present on either IRQ1 or IRQ2. This is useful for host MCUs that may not have interrupt pins available.

The irq_src1 and irq_src0 registers can be read back to establish the source of an interrupt. An interrupt is cleared by writing 1 to the corresponding bit location in the appropriate interrupt source register (irq_src1 or irq_src0). If 0 is written to a bit location in the interrupt source registers, its state remains unchanged. This scheme allows interrupts to be cleared individually and facilitates hierarchical interrupt processing.

The availability of two interrupt outputs permits a flexible allocation of interrupt source to two different MCU hardware resources. For instance, an rx_sfd interrupt can be associated with a timer-capture unit of the MCU, while all other interrupts are handled by a normal interrupt handling routine. When operating in SPORT mode, Pin IRQ2_TRFS_GP2 acts as a frame synchronization signal and is disconnected from the interrupt controller.

When in the sleep state, the IRQ1_GP4 and IRQ2_TRFS_GP2 pins have high impedance.

When not in the sleep state, Pin IRQ1_GP4 and Pin IRQ2_TRFS_GP2 are configured as push-pull outputs, using positive logic polarity.

Following a power-on reset or wake-up from sleep, Register irq1_en0, Field powerup and Register irq2_en0, Field powerup are set, while all other bits in the irq1_en0, irq1_en1, irq2_en0, and irq2_en1 registers are reset. Therefore, a power-up interrupt signal is asserted on the IRQ1_GP4 and IRQ2_TRFS_GP2 pins after a power-on-reset event or wake-up from the sleep state. Provided the wake-up from sleep event is caused by the wake-up timer, the power-up interrupt signal can be used to power up the host MCU.

After the ADF7241 is powered up, the rc_ready, wake-up, and power-on reset interrupts are also asserted in the irq_src0 register. However, these interrupts are not propagated to the IRQ1_GP4 and IRQ2_TRFS_GP2 pins because the corresponding mask bits are reset. The irq_src0 and irq_src1 registers should be cleared during the initialization phase.

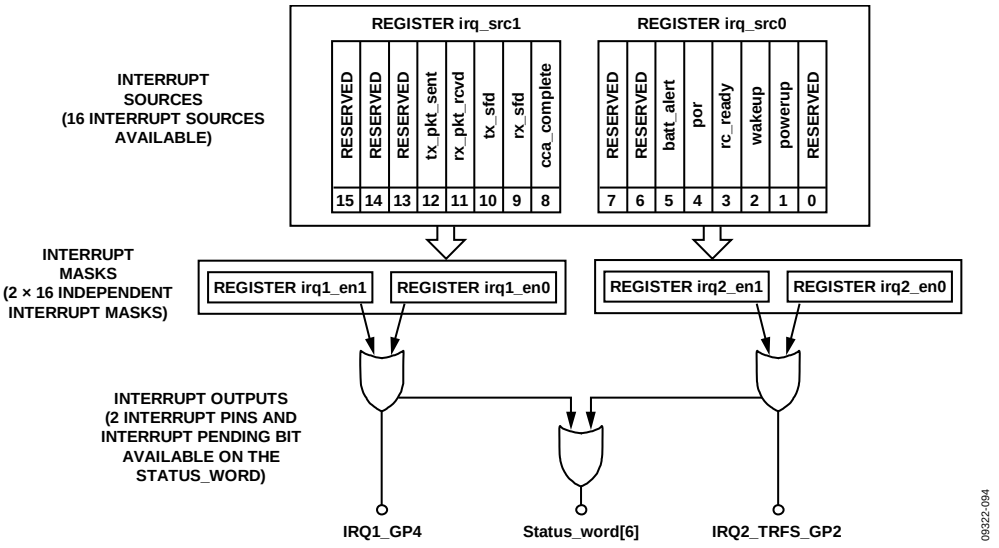


Figure 64. Interrupt Controller

Table 28. Bit Locations in the Interrupt Source Register irq_src1, with Corresponding Interrupt Enables in irq1_en1, irq2_en1

Bit	Name	Notes
7	Reserved	Don't care; set mask to 0.
6	Reserved	Don't care; set mask to 0.
5	Reserved	Don't care; set mask to 0.
4	tx_pkt_sent	TX packet transmission complete.
3	rx_pkt_rcvd	Packet received in RX_BUFFER.
2	tx_sfd	SFD has been transmitted.
1	rx_sfd	SFD has been detected.
0	cca_complete	CCA_RESULT in status word is valid.

Table 29. Bit Locations in the Interrupt Source Register irq_src0, with Corresponding Interrupt Enables in irq1_en0, irq2_en0

Bit	Name	Notes
7	Reserved	Don't care; set mask to 0.
6	Reserved	Don't care; set mask to 0.
5	batt_alert	Battery voltage has dropped below programmed threshold value.
4	por	Power-on reset event.
3	rc_ready	Radio controller ready to accept new command.
2	wakeup	Timer has timed out.
1	powerup	Chip is ready for access.
0	Reserved	Don't care; set mask to 0.

DESCRIPTION OF INTERRUPT SOURCES

tx_pkt_sent

This interrupt is asserted when in IEEE 802.15.4-2006 packet mode and the transmission of a packet in TX_BUFFER is complete.

rx_pkt_rcvd

This interrupt is asserted when in IEEE 802.15.4-2006 packet mode and a packet with a valid FCS has been received and is available in RX_BUFFER.

tx_sfd

This interrupt is asserted if the SFD is transmitted when in IEEE 802.15.4-2006 packet mode.

rx_sfd

This interrupt is asserted if a SFD is detected while in the RX state in either IEEE 802.15.4 mode.

cca_complete

The interrupt is asserted at the end of a CCA measurement following a RC_RX or RC_CCA command. The interrupt indicates that the CCA_RESULT flag in the status word is valid.

batt_alert

The interrupt is asserted if the battery monitor signals a battery alarm. This occurs when the battery voltage drops below the programmed threshold value. The battery monitor must be enabled and configured. See the Battery Monitor section for further details.

rc_ready

The interrupt is asserted if the radio controller is ready to accept a new command. This condition is equivalent to the rising edge of the RC_READY flag in the status word.

wakeup

The interrupt is asserted if the WUC timer has decremented to zero. Prior to enabling this interrupt, the WUC timer unit must be configured with the tmr_cfg0, tmr_cfg1, tmr_rld0, and tmr_rld1 registers. A wake-up interrupt can be asserted while the ADF7241 is active or has woken up from the sleep state through a timeout event. See the Wake-Up Controller (WUC) section or further details.

powerup

The interrupt is asserted if the ADF7241 is ready for SPI access following a wake-up from the sleep state. This condition reflects a rising edge of the flag SPI_READY in the status word. If the ADF7241 has been woken up from the sleep state using the $\overline{CS}$ input, this interrupt is useful to detect that the ADF7241 has powered up without the need to poll the MISO output. Register irq1_mask, Field powerup and Register irq2_mask, Field powerup are automatically set on exit from the sleep state. Therefore, this interrupt is generated when a transition from sleep is triggered by $\overline{CS}$ being pulled low or by a timeout event.

APPLICATIONS CIRCUITS

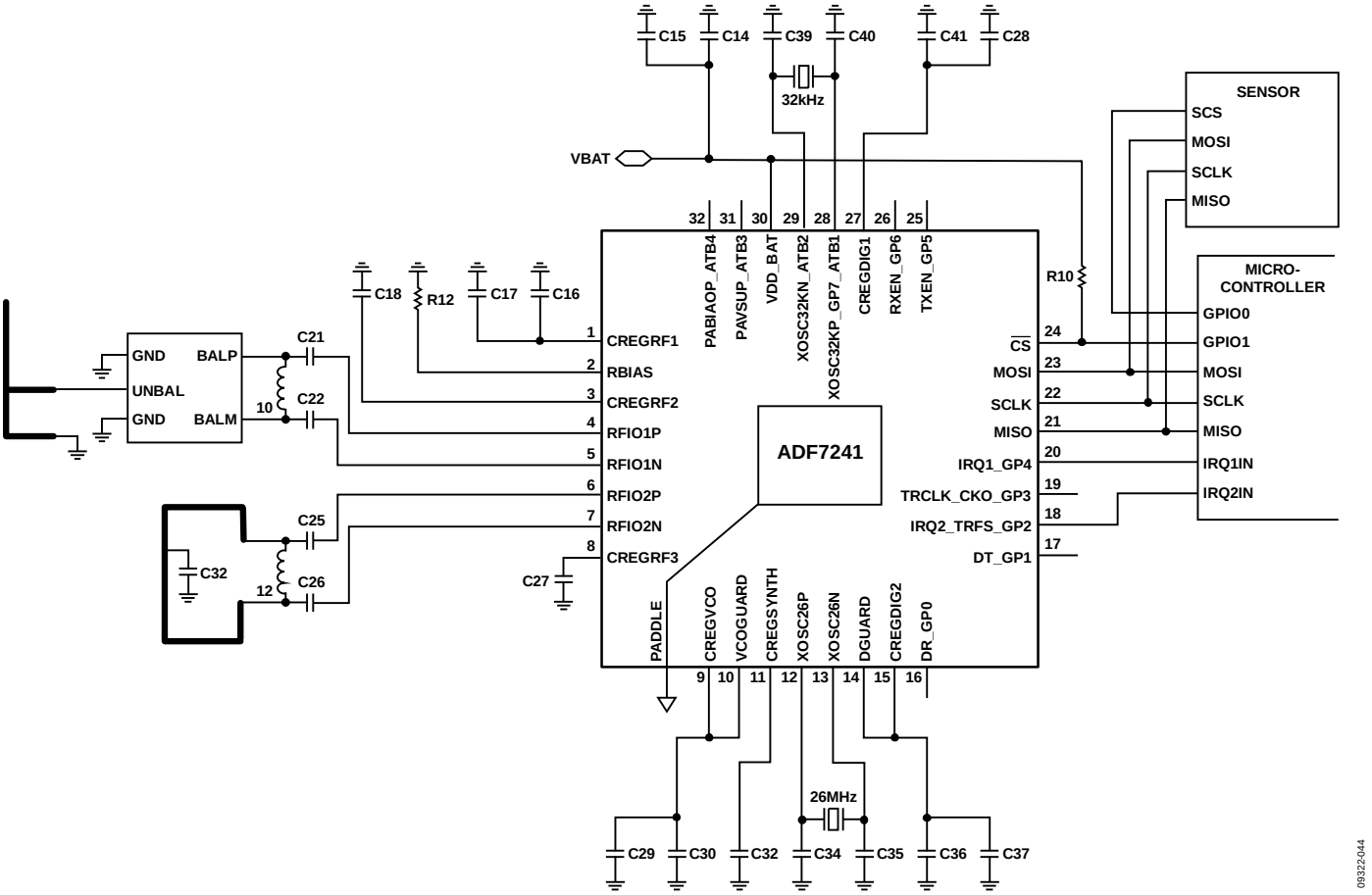


Figure 65. Typical ADF7241 Application Circuit Using Antenna Diversity

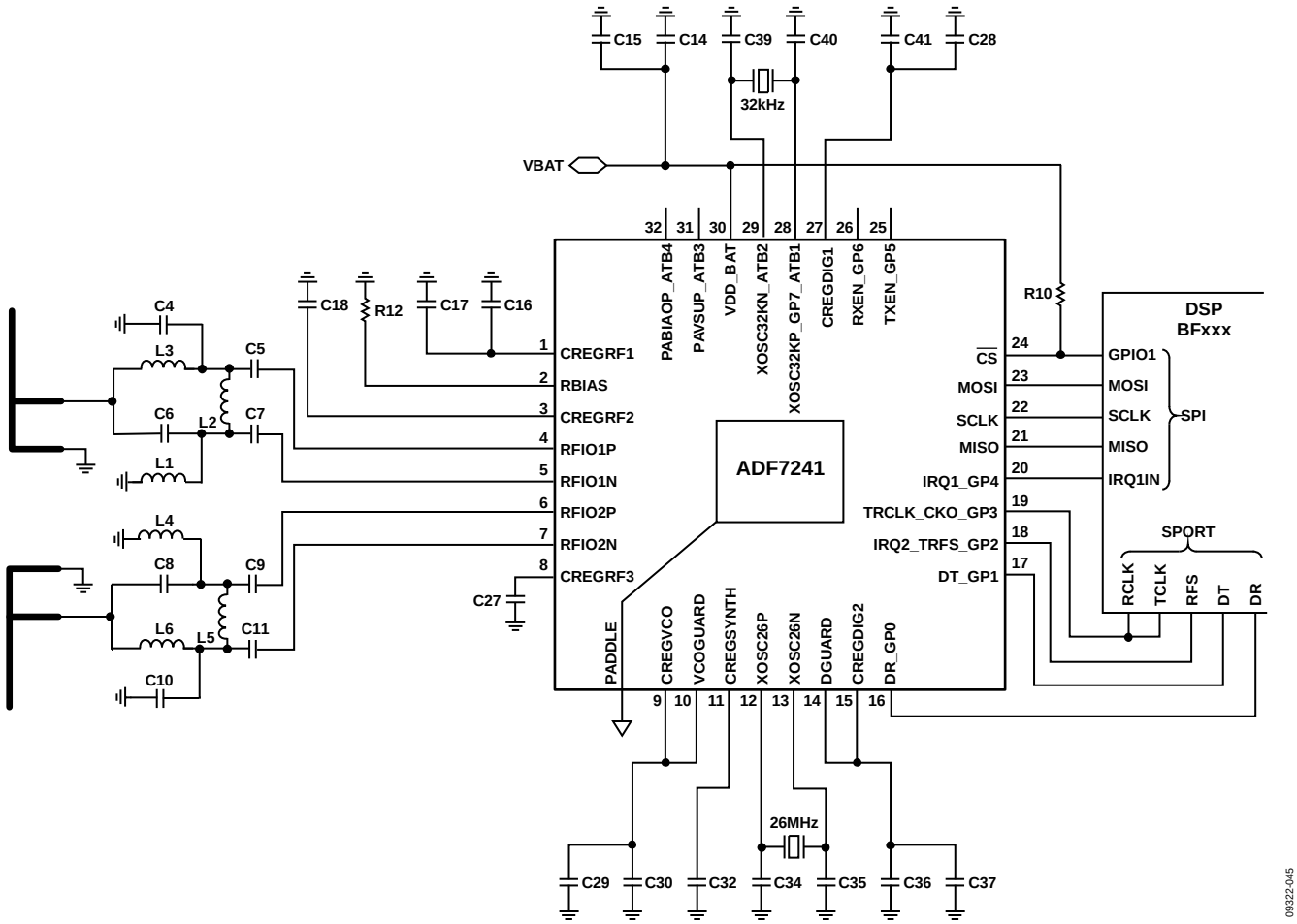


Figure 66. Typical ADF7241 Application Circuit with DSP Using Antenna Diversity

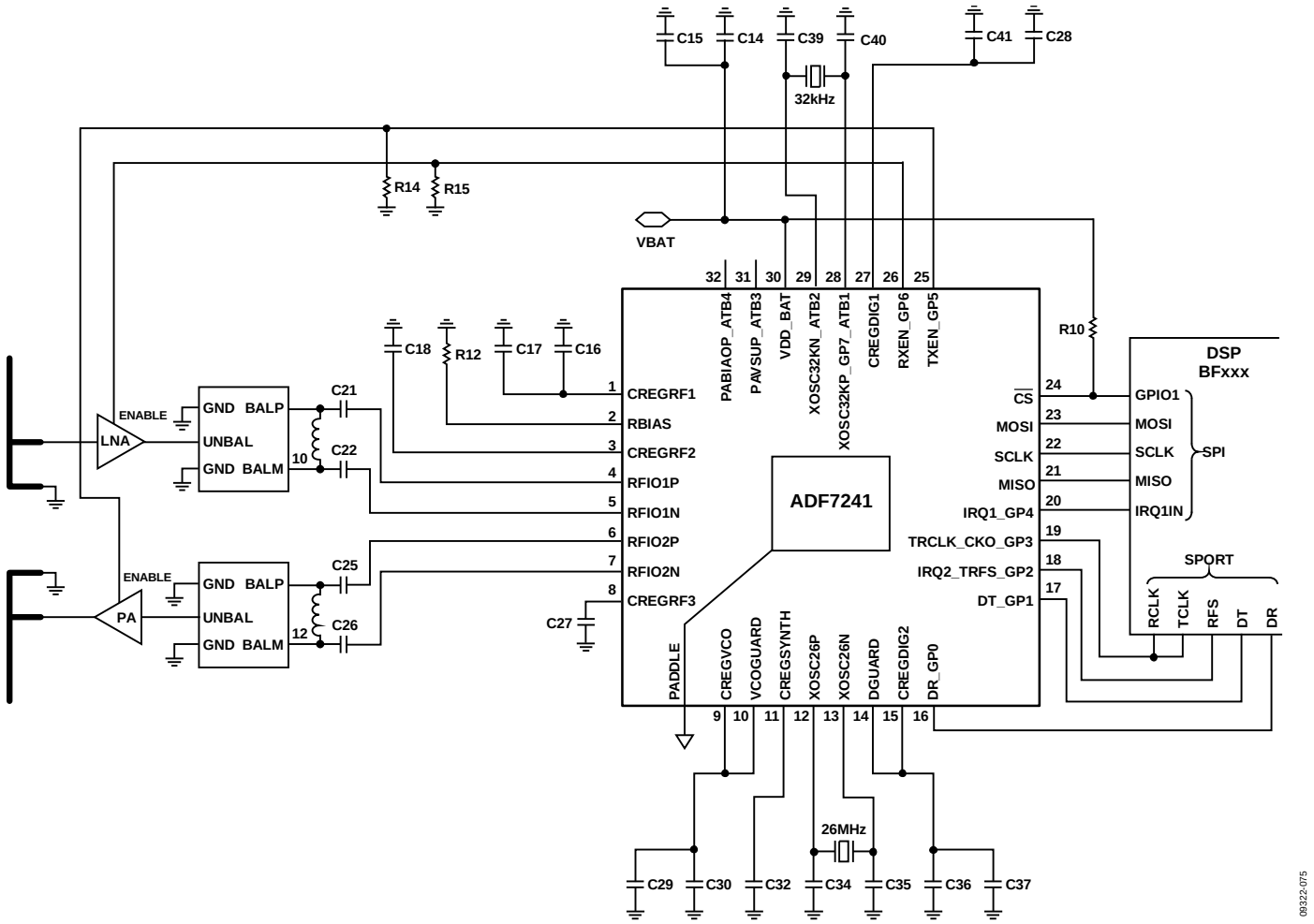


Figure 67. Typical ADF7241 Application Circuit with External LNA and External PA

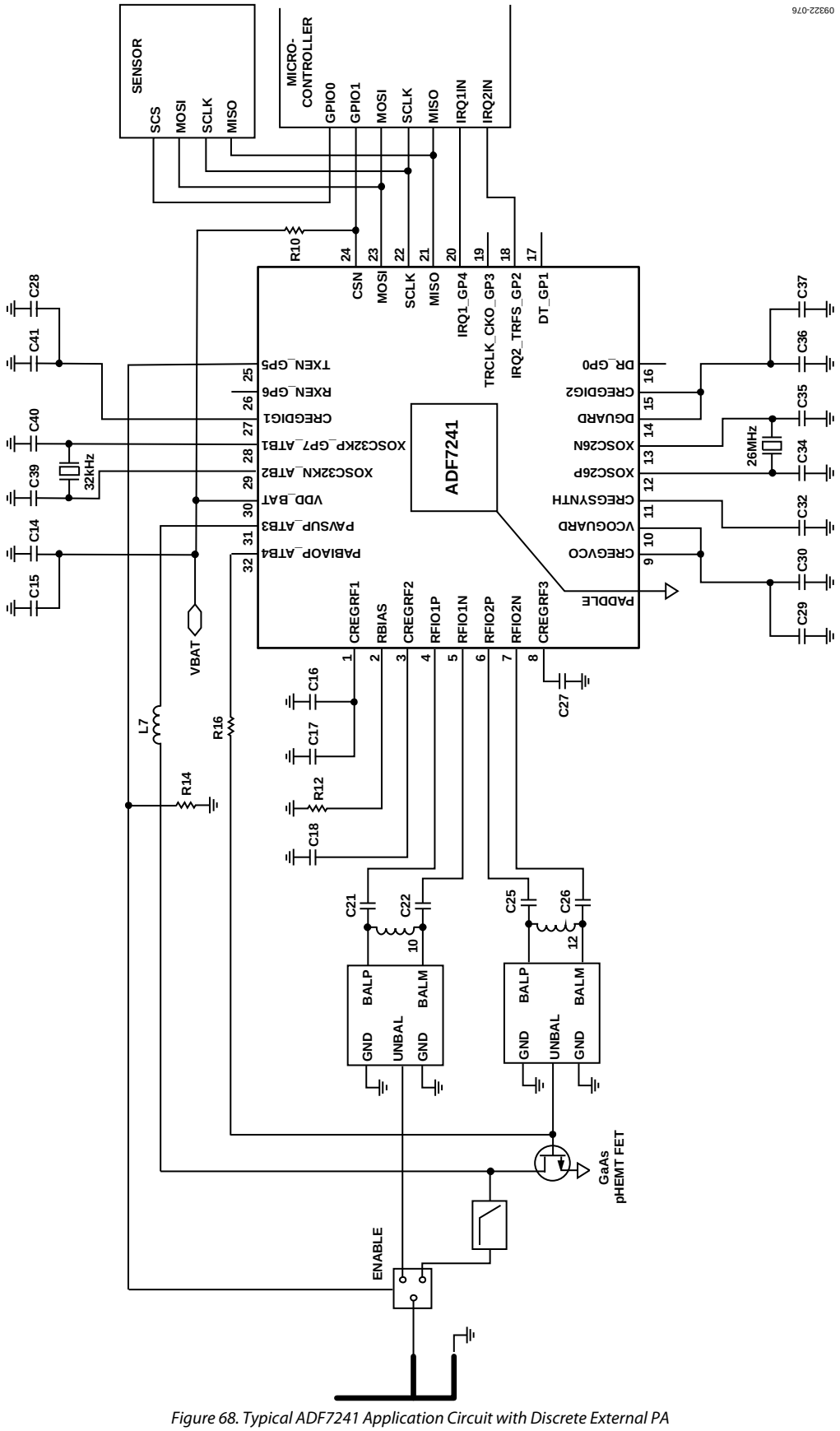


Figure 68. Typical ADF7241 Application Circuit with Discrete External PA

REGISTER MAP

It is recommended that configuration registers be programmed in the idle state. Note that all registers that include fields that are denoted as RC_CONTROLLED must be programmed in the idle state only.

Reset values are shown in decimal notation.

Table 30. Register Map Overview

Address	Register Name	Access Mode	Description
0x100	ext_ctrl	R/W	External LNA/PA and internal PA control configuration bits
0x105	cca1	R/W	RSSI threshold for CCA
0x106	cca2	R/W	CCA mode configuration
0x107	buffercfg	R/W	RX and TX buffer configuration
0x108	pkt_cfg	R/W	Firmware download module enable and FCS control
0x109	delaycfg0	R/W	RC_RX command to SFD search delay
0x10A	delaycfg1	R/W	RC_TX command to TX state delay
0x10B	delaycfg2	R/W	MAC delay extension
0x13E	rc_cfg	R/W	Packet/SPORT mode configuration
0x300	ch_freq0	R/W	Channel frequency settings—low byte
0x301	ch_freq1	R/W	Channel frequency settings—middle byte
0x302	ch_freq2	R/W	Channel frequency settings—two MSBs
0x306	tx_m	R/W	Preemphasis filter configuration
0x30C	rrb	R	RSSI readback register
0x30D	lrb	R	Signal quality indicator quality readback register
0x313	prampg	R/W	PRAM page
0x314	txpb	R/W	Transmit packet storage base address
0x315	rxpb	R/W	Receive packet storage base address
0x316	tmr_cfg0	R/W	Wake-up timer configuration register—high byte
0x317	tmr_cfg1	R/W	Wake-up timer configuration register—low byte
0x318	tmr_rld0	R/W	Wake-up timer value register—high byte
0x319	tmr_rld1	R/W	Wake-up timer value register—low byte
0x31A	tmr_ctrl	R/W	Wake-up timer timeout flag configuration register
0x31B	wuc_32khzosc_status	R	32 kHz oscillator/WUC status
0x31E	pd_aux	R/W	Battery monitor and external PA bias enable
0x32C	gp_cfg	R/W	GPIO configuration
0x32D	gp_out	R/W	GPIO configuration
0x33D	rc_cal_cfg	R/W	RC calibration setting
0x353	vco_band_ovrw	R/W	Overwrite value for the VCO frequency band
0x354	vco_idac_ovrw	R/W	Overwrite value for the VCO bias current DAC
0x355	vco_ovwr_cfg	R/W	VCO calibration settings overwrite enable
0x36E	pa_bias	R/W	PA bias control
0x36F	vco_cal_cfg	R/W	VCO calibration parameters
0x371	xto26_trim_cal	R/W	26 MHz crystal oscillator configuration
0x380	vco_band_rb	R	Readback VCO band after calibration
0x381	vco_idac_rb	R	Readback of the VCO bias current DAC after calibration
0x395	rxcal0	R/W	Receiver baseband filter calibration word, LSB
0x396	rxcal1	R/W	Receiver baseband filter calibration word, MSB
0x39B	rxfe_cfg	R/W	Receive baseband filter bandwidth and LNA selection
0x3A7	pa_rr	R/W	PA ramp rate
0x3A8	pa_cfg	R/W	PA output stage current control
0x3A9	extpa_cfg	R/W	External PA bias DAC configuration
0x3AA	extpa_msc	R/W	External PA interface circuit configuration
0x3AE	adc_rbk	R	ADC readback
0x3B9	agc_cfg5	R/W	AGC configuration parameters
0x3C7	irq1_en0	R/W	Interrupt Mask Set Bits[7:0] of Bits[15:0] for IRQ1

Address	Register Name	Access Mode	Description
0x3C8	irq1_en1	R/W	Interrupt Mask Set Bits[15:8] of [15:0] for IRQ1
0x3C9	irq2_en0	R/W	Interrupt Mask Set Bits[7:0] of [15:0] for IRQ2
0x3CA	irq2_en1	R/W	Interrupt Mask Set Bits[15:8] of [15:0] for IRQ2
0x3CB	irq_src0	R/W	Interrupt Source Bits[7:0] of [15:0] for IRQ
0x3CC	irq_src1	R/W	Interrupt Source Bits[15:8] of [15:0] for IRQ
0x3E3	gp_drv	R/W	GPIO and SPI I/O pads drive strength configuration
0x3E6	bm_cfg	R/W	Battery monitor threshold voltage setting
0x3F0	tx_test	R/W	TX test mode configuration
0x3F4	sfd_15_4	R/W	Option to set nonstandard SFD

Table 31. 0x100: ext_ctrl

Bit	Field Name	R/W	Reset Value	Description
[7]	pa_shutdown_mode	R/W	0	PA shutdown mode. 0: fast ramp-down. 1: user defined ramp-down.
[6:5]	Reserved	R/W	0	Reserved, set to default.
4	rxen_en	R/W	0	1: RXEN_GP6 is set high while in the RX state; otherwise, it is low. 0: RXEN_GP6 is under user control (refer to Register gp_out); refer to Register gp_cfg for restrictions
3	txen_en	R/W	0	1: TXEN_GP5 is set high while in the TX state; otherwise, it is low. 0: TXEN_GP5 is under user control (refer to Register gp_out); refer to Register gp_cfg for restrictions.
2	extpa_auto_en	R/W	0	1: RC enables external PA controller while in the TX state. 0: Register pd_aux, Bit extpa_bias_en (0x31E[4]) is under user control.
[1:0]	Reserved	R/W	0	Reserved, set to default.

Table 32. 0x105: cca1

Bit	Field Name	R/W	Reset Value	Description
[7:0]	cca_thres	R/W	171	RSSI threshold for CCA. Signed twos complement notation (in dBm). When CCA is completed: Status Word CCA_RESULT = 1 if Register rrb, Bit rssi_readback (0x30C[7:0]) < cca_thres Status Word CCA_RESULT = 0 if Register rrb, Bit rssi_readback (0x30C[7:0]) ≥ cca_thres

Table 33. 0x106: cca2

Bit	Field Name	R/W	Reset Value	Description
[7:3]	Reserved	R/W	0	Reserved, set to default.
2	continuous_cca	R/W	0	0: continuous CCA off. 1: generate a CCA interrupt every 128 µs.
1	rx_auto_cca	R/W	0	0: automatic CCA off. 1: generate a CCA interrupt 128 µs after entering the RX state.
0	Reserved	R/W	0	Reserved, set to default.

Table 34. 0x107: buffercfg

Bit	Field Name	R/W	Reset Value	Description
7	trx_mac_delay	R/W	0	0: tx_mac_delay (0x10A[7:0]) and rx_mac_delay (0x109[7:0]) enabled. 1: tx_mac_delay (0x10A[7:0]) and rx_mac_delay (0x109[7:0]) disabled.
6	Reserved	R/W	0	Reserved, set to default.
[5:4]	tx_buffer_mode	RW	0	0: return to PHY_RDY after frame in TX_BUFFER is transmitted once. 1: cyclic transmission of frame in TX_BUFFER after TX MAC delay with PA ramp-up/down between packets. 2: reserved. 3: cyclic transmission of frame in TX_BUFFER after TX MAC delay with PA kept on.
3	auto_tx_to_rx_turnaround	R//W	0	0: as per tx_buffer_mode setting. 1: automatically goes to RX after TX data transmitted.
2	auto_rx_to_tx_turnaround	R/W	0	0: as per rx_buffer_mode setting. 1: automatically goes to TX after RX packet received.
[1:0]	rx_buffer_mode	R/W	0	0: first frame following a RC_RX command is stored in RX_BUFFER; device returns to PHY_RDY state after reception of first frame. 1: continuous reception of frames enabled; a new frame overwrites previous frame. 2: new frames not written to buffer. 3: reserved.

Table 35. 0x108: pkt_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:5]	Reserved	R/W	0	Reserved, set to default.
4	addon_en	R/W	0	0: firmware add-on module disabled. 1: firmware add-on module enabled; module must be loaded prior to setting this bit.
3	skip_synt_settle	R/W	0	0: the RF frequency synthesizer calibration and settling phase is performed. 1: skip the RF frequency synthesizer calibration and settling phase. This must only be used when the continuous packet transmission mode is enabled. Refer to the WUC Configuration and Operation section.
[2:1]	Reserved	R/W	2	Reserved, set to default.
0	auto_fcs_off	R/W	0	The rx_pkt_rcvd interrupt is asserted. 0: receive operation—FCS automatically validated; FCS replaced with RSSI and SQI values in RX_BUFFER. Transmit operation—FCS automatically appended to transmitted packet; FCS field in TX_BUFFER is ignored. 1: receive operation—received FCS is stored in RX_BUFFER without validation. Transmit operation—FCS field in TX_BUFFER is transmitted.

Table 36. 0x109: delaycfg0

Bit	Field Name	R/W	Reset Value	Description
[7:0]	rx_mac_delay	R/W	192	Programmable delay from issue of RC_RX command to SFD search and for start of RSSI measurement window.

Table 37. 0x10A: delaycfg1

Bit	Field Name	R/W	Reset Value	Description
[7:0]	tx_mac_delay	R/W	192	Programmable delay from issue of RC_TX command to entering the TX state. Programmable in steps of 1 µs in both modes.

Table 38. 0x10B: delaycfg2

Bit	Field Name	R/W	Reset Value	Description
[7:0]	mac_delay_ext	R/W	0	Programmable MAC delay extension. Programmable in steps of 4 µs. Applies in both the RX and TX states.

Table 39. 0x13E: rc_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:0]	rc_mode	R/W	0	Configure packet format: 0: IEEE 802.15.4-2006 packet mode. 1: reserved. 2: IEEE 802.15.4-2006 receive SPORT mode. 3: IEEE 802.15.4-2006 transmit SPORT mode. 4, 5 to 255: reserved.

Table 40. 0x300: ch_freq0

Bit	Field Name	R/W	Reset Value	Description
[7:0]	ch_freq[7:0]	R/W	128	Channel frequency [Hz]/10 kHz, Bits[7:0] of Bits[23:0].

Table 41. 0x301: ch_freq1

Bit	Field Name	R/W	Reset Value	Description
[7:0]	ch_freq[15:8]	R/W	169	Channel frequency [Hz]/10 kHz, Bits[15:8] of Bits[23:0].

Table 42. 0x302: ch_freq2

Bit	Field Name	R/W	Reset Value	Description
[7:0]	ch_freq[23:16]	R/W	3	Channel frequency [Hz]/10 kHz, Bits[23:16] of Bits[23:0].

Table 43. 0x306: tx_m

Bit	Field Name	R/W	Reset Value	Description
[7:1]	RC_CONTROLLED	R/W	0	Controlled by radio controller.
0	preemp_filt	R/W	1	1: enable; 0: disable preemphasis filter.

Table 44. 0x30C: rrb

Bit	Field Name	R/W	Reset Value	Description
[7:0]	rssi_readback	R	0	Receive input power in dBm; signed twos complement.

Table 45. 0x30D: lrb

Bit	Field Name	R/W	Reset Value	Description
[7:0]	sqi_readback	R	0	Signal quality indicator readback value.

Table 46. 0x313: prampg

Bit	Field Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W	0	Reserved, set to default.
[3:0]	pram_page	R/W	0	Program PRAM page.

Table 47. 0x314: txpb

Bit	Field Name	R/W	Reset Value	Description
[7:0]	tx_pkt_base	R/W	128	Base address of TX_BUFFER in packet RAM.

Table 48. 0x315: rxpb

Bit	Field Name	R/W	Reset Value	Description
[7:0]	rx_pkt_base	R/W	0	Base address of RX_BUFFER in packet RAM.

Table 49. 0x316: tmr_cfg0

Bit	Field Name	R/W	Reset Value	Description
[7:3]	Reserved	R/W	0	Reserved, set to default.
[2:0]	timer_prescal	R/W	0	Divider factor for XTO32K or RCO. 0: ÷1. 1: ÷4. 2: ÷8. 3: ÷16. 4: ÷128. 5: ÷1024. 6: ÷8192. 7: ÷65,536. Note that this is a write-only register and should be written to prior to writing to Register tmr_cfg1. Settings become effective only after writing to Register tmr_cfg1.

Table 50. 0x317: tmr_cfg1

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Reserved, set to default.
[6:3]	sleep_config	R/W	0	1: SLEEP_BBRAM. 4: SLEEP_XTO. 5: SLEEP_BBRAM_XTO. 11: SLEEP_BBRAM_RCO. 0, 2, 3, 6 to 10, 12 to 15: reserved. Refer to note in Register tmr_cfg0.
[2:1]	Reserved	R/W	0	Reserved, set to default.
0	wake_on_timeout	R/W	0	1: enable, 0: disable wake-up on timeout event.

Table 51. 0x318: tmr_rld0

Bit	Field Name	R/W	Reset Value	Description
[7:0]	timer_reload[15:8]	R/W	0	Timer reload value, Bits[15:8] of Bits[15:0]. Note that this is a write-only register and should be written to prior to writing to Register tmr_rld1. Settings become effective only after writing to Register tmr_rld1.

Table 52. 0x319: tmr_rld1

Bit	Field Name	R/W	Reset Value	Description
[7:0]	timer_reload[7:0]	R/W	0	Timer reload value, Bits[7:0] of Bits[15:0]. Refer to note in Register tmr_rld0.

Table 53. 0x31A: tmr_ctrl

Bit	Field Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	0	Reserved, set to default.
1	wuc_rc_osc_cal	R/W	0	1: enable. 0: disable 32 kHz RC oscillator calibration.
0	wake_timer_flag_reset	R/W	0	Timer flag reset. 0: normal operation. 1: reset Field wuc_tmr_prim_toflag and Field wuc_porflag (0x31B).

Table 54. 0x31B: wuc_32khzosc_status

Bit	Field Name	R/W	Reset Value	Description
[7:6]	Reserved	R	0	Reserved, set to default.
5	rc_osc_cal_ready	R	0	32 kHz RC oscillator calibration (only valid if wuc_rc_osc_cal = 1). Calibration takes 1 ms. 0: calibration in progress. 1: calibration finished.
4	xosc32_ready	R	0	32 kHz crystal oscillator (only valid if sleep_config (0x317[6:3]) = 4 or 5). 0: oscillator not settled. 1: oscillator has settled.
3	Reserved	R	0	Reserved, set to default.
2	wuc_porflag	R	0	Chip cold start event registration. 0: not registered. 1: registered.
1	wuc_tmr_prim_toflag	R	0	WUC timeout event registration (the output of a latch triggered by a timeout event). 0: not registered. 1: registered.
0	Reserved	R	0	Reserved, set to default.

Table 55. 0x31E: pd_aux

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Reserved, set to default.
6	RC_CONTROLLED	R/W	0	Controlled by radio controller.
5	battmon_en	R/W	0	1: enable. 0: disable battery monitor.
4	extpa_bias_en	R/W	0	1: enable. 0: disable external PA biasing circuit. Controlled by radio controller when Register ext_ctrl, Field extpa_auto_en = 1 (0x100[2]).
[3:0]	RC_CONTROLLED	R/W	0	Controlled by radio controller.

Table 56. 0x32C: gp_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:0]	gpio_config	R/W	0	0: IRQ1, IRQ2 functionality. Register gp_out, Bit gpio_dout[6] controls RXEN output. Register gp_out, Bit gpio_dout[5] controls TXEN output. 1: TRCLK and data pins active in RX, gated by synchronization word detection. 1, 4: TRCLK and data pins active in TX. 7: symbol clock output on TRCLK pin and symbol data output on GP6, GP5, GP1, and GP0. Refer to Table 19 for further details of SPORT mode configurations. 2, 3, 5, 6, 8 to 255: reserved.

Table 57. 0x32D: gp_out

Bit	Field Name	R/W	Reset Value	Description
[7:0]	gpio_dout	R/W	0	GPIO output value if Register gp_cfg, Field gpio_config = 4. gpio_dout[7:0] = GP7 to GP0. If Register ext_ctrl, Field rxen_en = 1, then Register gp_out, Bit gpio_dout[6] is controlled by radio controller. If Register ext_ctrl, Field txen_en = 1, then Register gp_out, Bit gpio_dout[5] is controlled by radio controller.

Table 58. 0x33D: rc_cal_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	15	Reserved, set to default.
[1:0]	skip_rc_cal	R/W	0	0: do not skip RC calibration. This calibration is performed only when transitioning from idle to PHY_RDY. 3: skip RC calibration.

Table 59. 0x353: vco_band_ovrw

Bit	Field Name	R/W	Reset Value	Description
[7:0]	vco_band_ovrw_val	R/W	0	Overwrite value for the VCO frequency band. Enabled when vco_band_ovrw_en = 1 and Register vco_cal_cfg, Field skip_vco_cal = 15.

Table 60. 0x354: vco_idac_ovrw

Bit	Field Name	R/W	Reset Value	Description
[7:0]	vco_idac_ovrw_val	R/W	0	Overwrite value for the VCO bias current DAC. Enabled when Register vco_cal_cfg, Field skip_vco_cal = 15 and Field vco_idac_ovrw_en = 1.

Table 61. 0x355: vco_ovrw_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	2	Reserved, set to default.
1	vco_idac_ovrw_en	R/W	0	VCO bias current DAC overwrite. Effective only if Register vco_cal_cfg, Field skip_vco_cal = 15. 0: disable. 1: enable.
0	vco_band_ovrw_en	R/W	0	VCO frequency band overwrite. Effective only if Register vco_cal_cfg, Field skip_vco_cal = 15. 0: disable. 1: enable.

Table 62. 0x36E: pa_bias

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Reserved, set to default.
[6:1]	pa_bias_ctrl	R/W	55	Set to 63 if maximum PA output power of 4.8 dBm is required.
0	Reserved	R/W	1	Reserved, set to default.

Table 63. 0x36F: vco_cal_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W	0	Reserved, set to default.
[3:0]	skip_vco_cal	R/W	9	9: do not skip VCO calibration. 15: skip VCO calibration.

Table 64. 0x371: xto26_trim_cal

Bit	Field Name	R/W	Reset Value	Description
[7:6]	Reserved	R/W	0	Reserved, set to default.
[5:3]	xto26_trim	R/W	4	26 MHz crystal oscillator (XOSC26N) tuning capacitor control word. The load capacitance is adjusted according to the value of xto26_trim as follows: 0: −4 × 187.5 fF. 1: −3 × 187.5 fF. 2: −2 × 187.5 fF. 3: −1 × 187.5 fF. 4: 0 × 187.5 fF. 5: 1 × 187.5 fF. 6: 2 × 187.5 fF. 7: 3 × 187.5 fF.
[2:0]	Reserved	R/W	0	Reserved, set to default.

Table 65. 0x381: vco_band_rb

Bit	Field Name	R/W	Reset Value	Description
[7:2]	vco_band_val_rb	R	0	Readback for the VCO frequency band after calibration.

Table 66. 0x381: vco_idac_rb

Bit	Field Name	R/W	Reset Value	Description
[7:2]	vco_idac_val_rb	R	0	Readback of the VCO bias current DAC after calibration.

Table 67. 0x395: rxcal0

Bit	Field Name	R/W	Reset Value	Description
[7:0]	dcap_ovwrt_low	R/W	0	RXBB filter tuning overwrite word, LSB.

Table 68. 0x396: rxcal1

Bit	Field Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	2	Reserved, set to default.
1	dcap_ovwrt_en	R/W	0	RXBB filter tuning overwrite word enable.
0	dcap_ovwrt_high	R/W	0	RXBB filter tuning overwrite word, MSB.

Table 69. 0x39B: rxfe_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:5]	Reserved	R/W	0	Reserved, set to default.
4	lna_sel	R/W	1	Receive: 0: use LNA1. 1: use LNA2.
[3:0]	Reserved	R/W	13	Reserved, set to default.

Table 70. 0x3A7: pa_rr

Bit	Field Name	R/W	Reset Value	Description
[7:3]	Reserved	R/W	0	Reserved, set to default.
[2:0]	pa_ramp_rate	R/W	7	PA ramp rate: $2^{pa_ramp_rate} \times 2.4$ ns per PA power step.

Table 71. 0x3A8: pa_cfg

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Reserved, set to default.
[6:5]	Reserved	R/W	0	Set to default.
[4:0]	pa_bridge_dbias	R/W	13	Set to 21 if output power of 4.8 dBm is required from PA.

Table 72. 0x3A9: extpa_cfg

Bit	Field Name	R/W	Reset Value	Description
[7:5]	Reserved	R/W	0	Reserved, set to default.
[4:0]	extpa_bias	R/W	0	If Register extpa_msc, Field extpa_bias_mode = 1, 2, 3, or 4, PABIAOP_ATB4 pin DAC current = 80 µA − 2.58 µA × extpa_bias. If Register extpa_msc, Field extpa_bias_mode = 5 or 6, PAVSUP_ATB3 pin servo current set point = 22 mA − 0.349 mA × extpa_bias.

Table 73. 0x3AA: extpa_msc

Bit	Field Name	R/W	Reset Value	Description
[7:4]	pa_pwr	R/W	15	PA output power after ramping phase: 3: minimum power. 15: maximum power. Nominal power step size 2 dB per LSB.
3	extpa_bias_src	R/W	0	0: select RBIAS-referred reference current. 1: select band gap-referred reference current.
[2:0]	extpa_bias_mode	R/W	1	External PA interface configuration: 0: PAVSUP_ATB3 = on; PABIAOP_ATB4 = floating. 1: PAVSUP_ATB3 = on; PABIAOP_ATB4 = current source. 2: PAVSUP_ATB3 = on; PABIAOP_ATB4 = current sink. 3: PAVSUP_ATB3 = off; PABIAOP_ATB4 = current source. 4: PAVSUP_ATB3 = off; PABIAOP_ATB4 = current sink. 5: PAVSUP_ATB3 = on; PABIAOP_ATB4 = positive servo output. 6: PAVSUP_ATB3 = on; PABIAOP_ATB4 = negative servo output. 7: reserved.

Table 74. 0x3AE: adc_rbk

Bit	Field Name	R/W	Reset Value	Description
[7:6]	Reserved	R	0	Ignore.
[5:0]	adc_out	R	0	ADC output code.

Table 75. 0x3B9: agc_cfg5

Bit	Field Name	R/W	Reset Value	Description
[7:5]	Reserved	R/W	0	Set to 0.
[4:2]	rssi_offs	R/W	4	RSSI offset adjust, rssi_offs is added to Register rrb, Field rssi_readback.
[1:0]	Reserved	R/W	3	Reserved, set to default.

Table 76. 0x3C7: irq1_en0

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	batt_alert	R/W	0	Battery monitor interrupt.
4	por	R/W	0	Power-on reset event.
3	rc_ready	R/W	0	Radio controller ready to accept new command.
2	wakeup	R/W	0	Timer has timed out.
1	powerup	R/W	1	Chip is ready for access.
0	Reserved	R/W	0	Set to 0.

Table 77. 0x3C8: irq1_en1

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	Reserved	R/W	0	Set to 0.
4	tx_pkt_sent	R/W	0	Packet transmission complete.
3	rx_pkt_rcvd	R/W	0	Packet received in RX_BUFFER.
2	tx_sfd	R/W	0	SFD was transmitted.
1	rx_sfd	R/W	0	SFD was detected.
0	cca_complete	R/W	0	CCA_RESULT in status word is valid.

Table 78. 0x3C9: irq2_en0

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	batt_alert	R/W	0	Battery monitor interrupt.
4	por	R/W	0	Power-on reset event.
3	rc_ready	R/W	0	Radio controller ready to accept new command.
2	wakeup	R/W	0	Timer has timed out.
1	powerup	R/W	1	Chip is ready for access.
0	Reserved	R/W	0	Set to 0.

Table 79. 0x3CA: irq2_en1

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	Reserved	R/W	0	Set to 0.
4	tx_pkt_sent	R/W	0	Packet transmission complete.
3	rx_pkt_rcvd	R/W	0	Packet received in RX_BUFFER.
2	tx_sfd	R/W	0	SFD was transmitted.
1	rx_sfd	R/W	0	SFD was detected.
0	cca_complete	R/W	0	CCA_RESULT in status word is valid.

Table 80. 0x3CB: irq_src0

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	batt_alert	R/W	0	Battery monitor interrupt.
4	por	R/W	0	Power-on reset event.
3	rc_ready	R/W	0	Radio controller ready to accept new command.
2	wakeup	R/W	0	Timer has timed out.
1	powerup	R/W	0	Chip is ready for access.
0	Reserved	R/W	0	Set to 0.

Table 81. 0x3CC: irq_src1

Bit	Field Name	R/W	Reset Value	Description
7	Reserved	R/W	0	Set to 0.
6	Reserved	R/W	0	Set to 0.
5	Reserved	R/W	0	Set to 0.
4	tx_pkt_sent	R/W	0	Packet transmission complete.
3	rx_pkt_rcvd	R/W	0	Packet received in RX_BUFFER.
2	tx_sfd	R/W	0	SFD was transmitted.
1	rx_sfd	R/W	0	SFD was detected.
0	cca_complete	R/W	0	CCA_RESULT in status word is valid.

Table 82. 0x3E3: gp_drv

Bit	Field Name	R/W	Reset Value	Description
[7:4]	Reserved	R/W	0	Reserved, set to default.
[3:2]	gpio_slew	R/W	0	GPIO and SPI slew rate. 0: very slow. 1: slow. 2: very fast. 3: fast.
[1:0]	gpio_drive	R/W	0	GPIO and SPI drive strength. 0: 4 mA. 1: 8 mA. 2: >8 mA. 3: reserved.

Table 83. 0x3E6: bm_cfg

Bit	Field Name	R/W	Reset Value	Description
7:5]	Reserved	R/W	0	Reserved, set to default.
[4:0]	battmon_voltage	R/W	0	Battery monitor trip voltage: 1.7 V + 62 mV × battmon_voltage; the batt_alert interrupt is asserted when VDD_BAT drops below the trip voltage.

Table 84. 0x3F0: tx_test

Bit	Field Name	R/W	Reset Value	Description
[7:2]	Reserved	R/W	2	Reserved, set to default.
1	carrier_only	R/W	0	Transmits unmodulated tone at the programmed frequency f_{CH}.
0	Reserved	R/W	0	Reserved, set to default.

Table 85. 0x3F4: sfd_15_4

Bit	Field Name	R/W	Reset Value	Description
[7:4]	sfd_symbol_2	R/W	10	Symbol 2 of SFD note: IEEE 802.15.4-2006 requires SFD1 = 10.
[3:0]	sfd_symbol_1	R/W	7	Symbol 1 of SFD note: IEEE 802.15.4-2006 requires SFD1 = 7.

OUTLINE DIMENSIONS

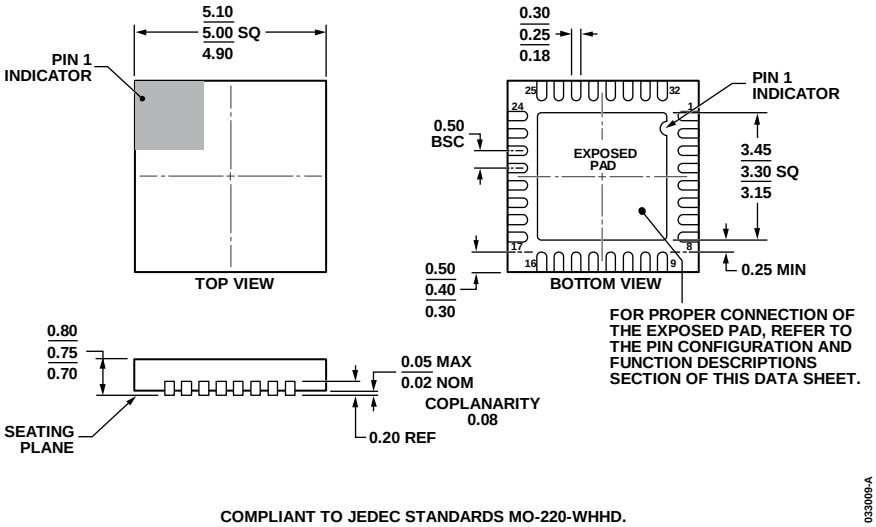


Figure 69. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF7241BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
ADF7241BCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-13
EVAL-ADF7241DB1Z		Evaluation Platform Daughterboard	
EVAL-ADF7XXXMB3Z		Evaluation Platform Motherboard	

[1] Z = RoHS Compliant Part.

NOTES

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