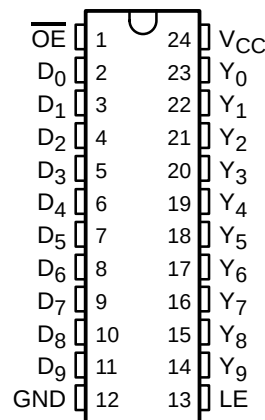


CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT, F, and AM29841 Logic
- Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- High-Speed Parallel Latches
- Buffered Common Latch-Enable Input
- 3-State Outputs
- CY54FCT841T
 - 32-mA Output Sink Current
 - 12-mA Output Source Current
- CY74FCT841T
 - 64-mA Output Sink Current
 - 32-mA Output Source Current

CY54FCT841T . . . D PACKAGE
CY74FCT841T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



description

The 'FCT841T bus-interface latches are designed to eliminate additional packages required to buffer existing latches and provide additional data width for wider address/data paths or buses carrying parity. The 'FCT841T devices are buffered 10-bit-wide versions of the FCT373 function.

The 'FCT841T devices' high-performance interface is designed for high-capacitance-load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	Latch data inputs
LE	I	Latch-enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Y	O	3-state latch outputs
$\overline{OE}$	I	Output-enable control. When $\overline{OE}$ is low, the outputs are enabled. When $\overline{OE}$ is high, the outputs are in the high-impedance (off) state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CY54FCT841T, CY74FCT841T 10-BIT LATCHES WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

ORDERING INFORMATION

T _A	PACKAGE [†]		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	5.5	CY74FCT841CTQCT	FCT841C
	SOIC – SO	Tube	5.5	CY74FCT841CTSOC	FCT841C
		Tape and reel	5.5	CY74FCT841CTSOCT	
	DIP – P	Tube	6.5	CY74FCT841BTPC	CY74FCT841BTPC
	SOIC – SO	Tube	9	CY74FCT841ATSOC	FCT841A
		Tape and reel	9	CY74FCT841ATSOCT	
-55°C to 125°C	CDIP – D	Tube	10	CY54FCT841ATDMB	

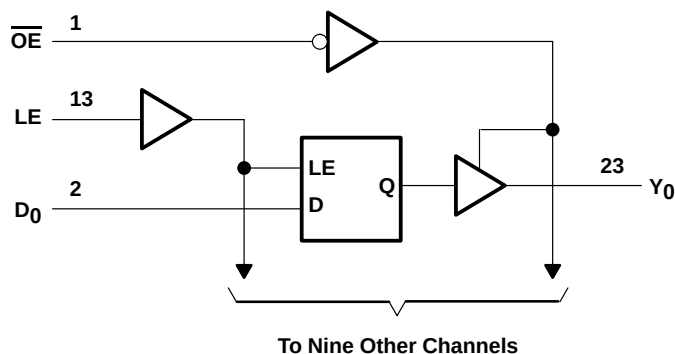
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
OE	LE	D	O	Y	
H	X	X	X	Z	Z
H	H	L	L	Z	
H	H	H	H	Z	
H	L	X	NC	Z	Latched (Z)
L	H	L	L	L	Transparent
L	H	H	H	H	
L	L	X	NC	NC	Latched

H = High logic level, L = Low logic level, X = Don't care,
NC = No change, Z = High-impedance state

logic diagram (positive logic)



CY54FCT841T, CY74FCT841T
10-BIT LATCHES
WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	CY54FCT841T			CY74FCT841T			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			–12			–32	mA
I_{OL} Low-level output current			32			64	mA
T_A Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY54FCT841T, CY74FCT841T

10-BIT LATCHES

WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT841T			CY74FCT841T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_{IN} = -18 \text{ mA}$	-0.7	-1.2					V
	$V_{CC} = 4.75 \text{ V}$, $I_{IN} = -18 \text{ mA}$				-0.7	-1.2		
V_{OH}	$V_{CC} = 4.5 \text{ V}$, $I_{OH} = -12 \text{ mA}$	2.4	3.3					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2			
	$I_{OH} = -15 \text{ mA}$				2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$, $I_{OL} = 32 \text{ mA}$	0.3	0.55					V
	$V_{CC} = 4.75 \text{ V}$, $I_{OL} = 64 \text{ mA}$				0.3	0.55		
V_{hys}	All inputs	0.2			0.2			V
I_I	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = V_{CC}$			5				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = V_{CC}$						5	
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 2.7 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 2.7 \text{ V}$						± 1	
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0.5 \text{ V}$			± 1				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0.5 \text{ V}$						± 1	
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$			10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 2.7 \text{ V}$						10	
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$			-10				μA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0.5 \text{ V}$						-10	
$I_{OS}^\ddagger$	$V_{CC} = 5.5 \text{ V}$, $V_{OUT} = 0 \text{ V}$	-60	-120	-225				mA
	$V_{CC} = 5.25 \text{ V}$, $V_{OUT} = 0 \text{ V}$				-60	-120	-225	
I_{off}	$V_{CC} = 0 \text{ V}$, $V_{OUT} = 4.5 \text{ V}$			± 1			± 1	μA
I_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.1	0.2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.1	0.2		
ΔI_{CC}	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 3.4 \text{ V}^\S$, $f_1 = 0$, Outputs open	0.5	2					mA
	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 3.4 \text{ V}^\S$, $f_1 = 0$, Outputs open				0.5	2		
$I_{CCD}^\P$	$V_{CC} = 5.5 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$	0.06	0.12					mA/ MHz
	$V_{CC} = 5.25 \text{ V}$, One input switching at 50% duty cycle, Outputs open, $\overline{OE} = \text{GND}$, $LE = V_{CC}$, $V_{IN} \leq 0.2 \text{ V}$ or $V_{IN} \geq V_{CC} - 0.2 \text{ V}$				0.06	0.12		

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.



CY54FCT841T, CY74FCT841T
10-BIT LATCHES
WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT841T		CY74FCT841T		UNIT
				MIN	TYP†	MAX	MIN	
I _C [#]	V _{CC} = 5.5 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	0.7	1.4			mA
			V _{IN} = 3.4 V or GND	1	2.4			
		10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V	1	3.2			
			V _{IN} = 3.4 V or GND	4.1	13.2			
	V _{CC} = 5.25 V, Outputs open, OE = GND, LE = V _{CC}	One bit switching at f ₁ = 10 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			0.7	1.4	
			V _{IN} = 3.4 V or GND			1	2.4	
		10 bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} – 0.2 V			1	3.2	
			V _{IN} = 3.4 V or GND			4.1	13.2	
C _i				5	10	5	10	pF
C ₀				9	12	9	12	pF

† Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT841AT		CY74FCT841AT		CY74FCT841BT		CY74FCT841CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	5		4		4		4		ns
t_{su}	Setup time, data before $LE\uparrow$	2.5		2.5		2.5		2.5		ns
t_h	Hold time, data after $LE\uparrow$	3		2.5		2.5		2.5		ns



CY54FCT841T, CY74FCT841T

10-BIT LATCHES

WITH 3-STATE OUTPUTS

SCCS035A – SEPTEMBER 1994 – REVISED OCTOBER 2001

switching characteristics over operating free-air temperature range (see Figure 1)

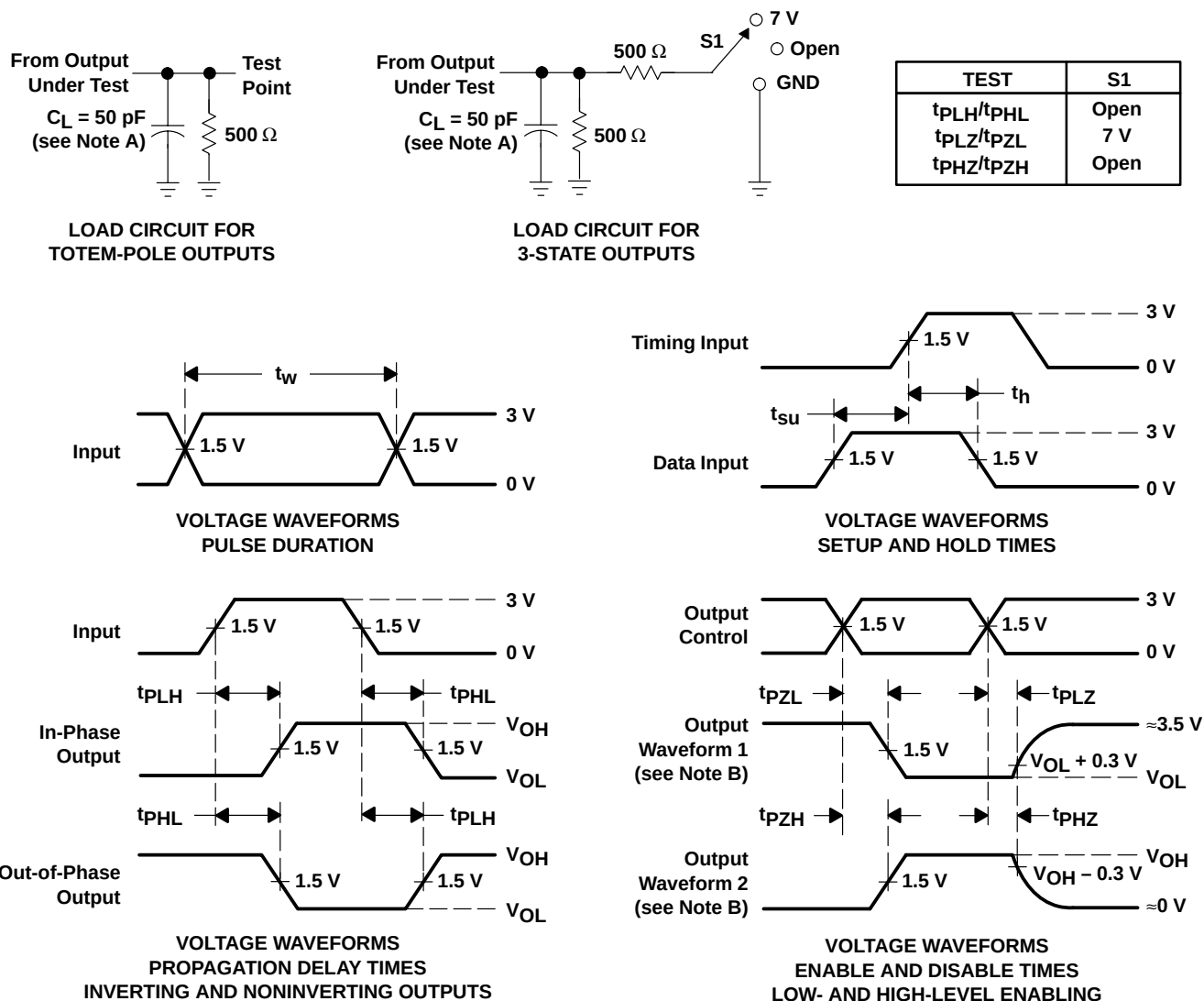
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT841AT		CY74FCT841AT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	9	ns
t _{PHL}				1.5	10	1.5	9	
t _{PLH}	D	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15	1.5	13	ns
t _{PHL}				1.5	15	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	12	ns
t _{PHL}				1.5	13	1.5	12	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	20	1.5	16	ns
t _{PHL}				1.5	20	1.5	16	
t _{PZH}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	11.5	ns
t _{PZL}				1.5	13	1.5	11.5	
t _{PZH}	$\overline{OE}$	Y	C _L = 300 pF, R _L = 500 Ω	1.5	25	1.5	23	ns
t _{PZL}				1.5	25	1.5	23	
t _{PHZ}	$\overline{OE}$	Y	C _L = 5 pF, R _L = 500 Ω	1.5	9	1.5	7	ns
t _{PLZ}				1.5	9	1.5	7	
t _{PHZ}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	10	1.5	8	ns
t _{PLZ}				1.5	10	1.5	8	

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT841BT		CY74FCT841CT		UNIT
				MIN	MAX	MIN	MAX	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	6.5	1.5	5.5	ns
t _{PHL}				1.5	6.5	1.5	5.5	
t _{PLH}	D	Y	C _L = 50 pF, R _L = 500 Ω	1.5	13	1.5	13	ns
t _{PHL}				1.5	13	1.5	13	
t _{PLH}	LE	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.4	ns
t _{PHL}				1.5	8	1.5	6.4	
t _{PLH}	LE	Y	C _L = 300 pF, R _L = 500 Ω	1.5	15.5	1.5	15	ns
t _{PHL}				1.5	15.5	1.5	15	
t _{PZH}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	8	1.5	6.5	ns
t _{PZL}				1.5	8	1.5	6.5	
t _{PZH}	$\overline{OE}$	Y	C _L = 300 pF, R _L = 500 Ω	1.5	14	1.5	12	ns
t _{PZL}				1.5	14	1.5	12	
t _{PHZ}	$\overline{OE}$	Y	C _L = 5 pF, R _L = 500 Ω	1.5	6	1.5	5.7	ns
t _{PLZ}				1.5	6	1.5	5.7	
t _{PHZ}	$\overline{OE}$	Y	C _L = 50 pF, R _L = 500 Ω	1.5	7	1.5	6	ns
t _{PLZ}				1.5	7	1.5	6	



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88575013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
CY54FCT841ATDMB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
CY54FCT841ATLMB	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
CY74FCT841ATSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841ATSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841BTPC	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT841BTPCE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CY74FCT841CTQCT	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT841CTSOC	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT841CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

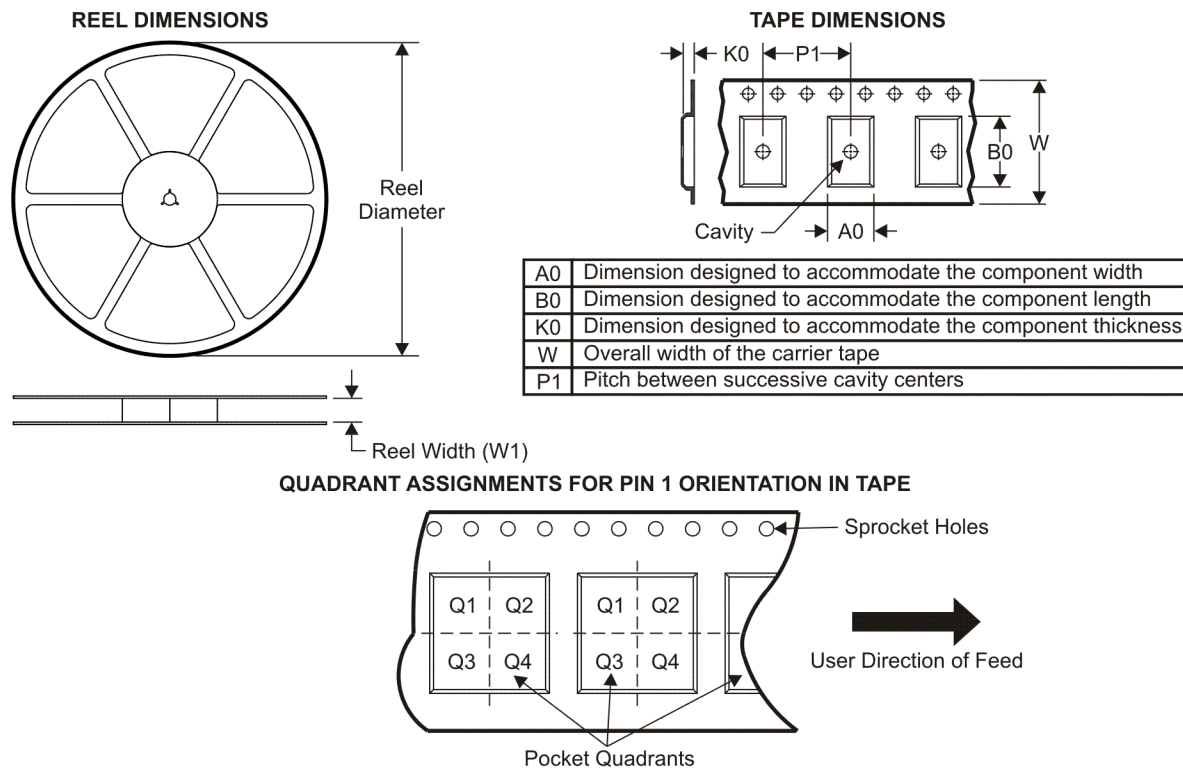
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

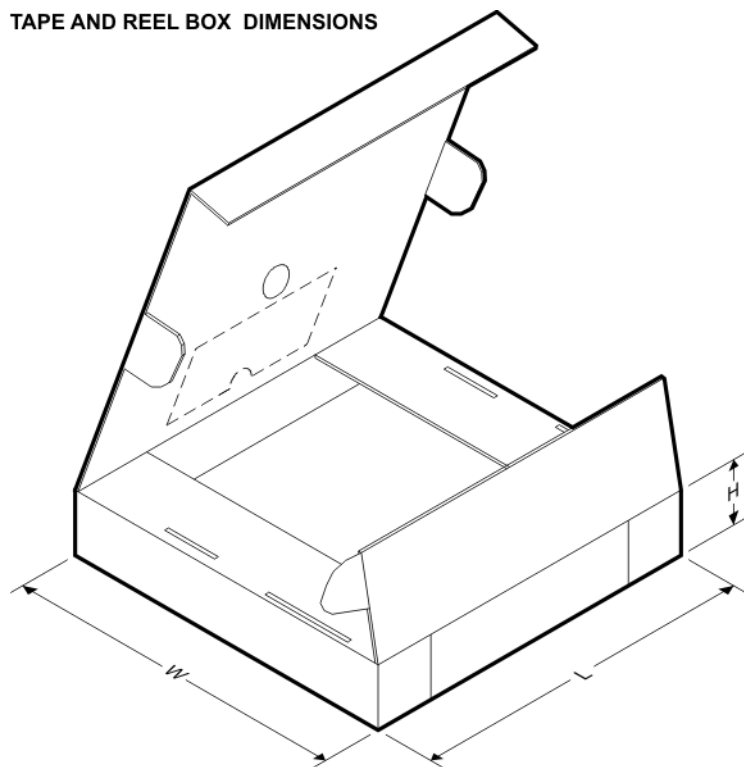
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT841ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT841CTQCT	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT841CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT841ATSOCT	SOIC	DW	24	2000	346.0	346.0	41.0
CY74FCT841CTQCT	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
CY74FCT841CTSOCT	SOIC	DW	24	2000	346.0	346.0	41.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated