SN74AVC4T245-Q1 4-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3B (JESD 22 A114-A)
  - Device CDM ESD Classification Level C5 (JESD 22 C101)
- Control Input V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- I_{off} Supports Partial Power-Down-Mode Operation
- Maximum Data Rates
  - 380 Mbps (1.8-V to 3.3-V Translation)
  - 200 Mbps (<1.8-V to 3.3-V Translation)
  - 200 Mbps (Translate to 2.5 V or 1.8 V)
  - 150 Mbps (Translate to 1.5 V)
  - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II

2 Applications

- Telematics
- Cluster
- Head Unit
- Navigation Systems

3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVC4T245-Q1 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC4T245-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC4T245-Q1 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

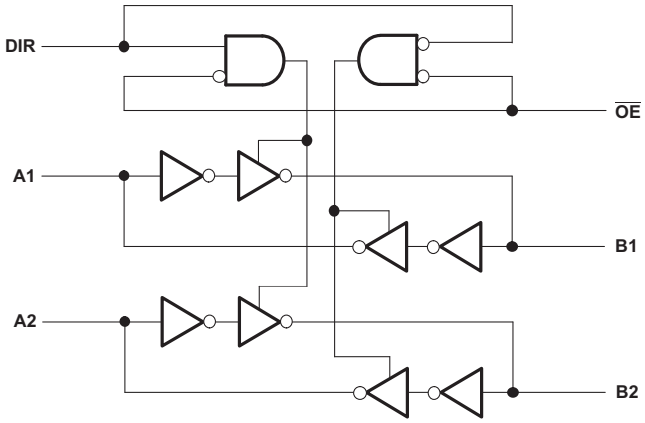
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC4T245-Q1	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245-Q1



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2012) to Revision B **Page**

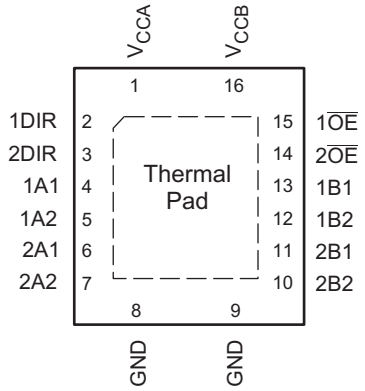
- Added *Applications* section ... 1
- Added -Q1 to the part number throughout the data sheet ... 1
- Added *Device Information* table to the data sheet ... 1
- Deleted *Ordering Information* table from the data sheet ... 1
- Added *Pin Functions* table to the data sheet ... 3
- Added *ESD Ratings* table to the data sheet ... 4
- Added *Thermal Information* table to the data sheet ... 5
- Added *Typical Characteristics* to the data sheet ... 12
- Added Figure 1 through Figure 9 from the SN74AVC8T245-Q1 data sheet over to the *Typical Characteristics* section ... 12
- Added all new content from *Application Information* through the end of the data sheet ... 15

Changes from Original (November 2009) to Revision A **Page**

- Added AEC-Q100 info to Features ... 1
- Removed ESD Protection Exceeds JESD 22, 8000-V Human-Body Model (A114-A), 1000-V Charged-Device Model (C101) from Features. ... 1

5 Pin Configuration and Functions

RGY Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1A1	4	I/O	Input/output 1A1. Referenced to V_{CCA}.
1A2	5	I/O	Input/output 1A2. Referenced to V_{CCA}.
1B1	13	I/O	Input/output 1B1. Referenced to V_{CCB}.
1B2	12	I/O	Input/output 1B2. Referenced to V_{CCB}.
1DIR	2	I	Direction-control input for 1 ports
$1\overline{OE}$	15	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘1’ outputs in 3-state mode. Referenced to V_{CCA}.
2A1	6	I/O	Input/output 2A1. Referenced to V_{CCA}.
2A2	7	I/O	Input/output 2A2. Referenced to V_{CCA}.
2B1	11	I/O	Input/output 2B1. Referenced to V_{CCB}.
2B2	10	I/O	Input/output 2B2. Referenced to V_{CCB}.
2DIR	3	I	Direction-control input for 2 ports
$2\overline{OE}$	14	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘2’ outputs in 3-state mode. Referenced to V_{CCA}.
GND	8, 9	—	Ground
Thermal pad	—	—	The exposed thermal pad must be connected as a secondary GND or be left electrically open.
V_{CCA}	1	I	A-port power supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	16	I	B-port power supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model (C101)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V

Recommended Operating Conditions(1) (2) (3) (continued)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating ambient temperature				–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T245-Q1 RGY (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics(1) (2)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C	V_{CCO} – 0.2			V
	I_{OH} = –3 mA		1.2 V	1.2 V	T_A = 25°C		0.95		
	I_{OH} = –6 mA		1.4 V	1.4 V	T_A = –40°C to 125°C	1.05			
	I_{OH} = –8 mA		1.65 V	1.65 V	T_A = –40°C to 125°C	1.2			
	I_{OH} = –9 mA		2.3 V	2.3 V	T_A = –40°C to 125°C	1.75			
	I_{OH} = –12 mA		3 V	3 V	T_A = –40°C to 125°C	2.3			

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

Electrical Characteristics[1] [2] (continued)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V	T_A = 25°C		0.25		
		I_{OL} = 6 mA		1.4 V	1.4 V	T_A = –40°C to 125°C			0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V	T_A = –40°C to 125°C			0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V	T_A = –40°C to 125°C			0.55	
		I_{OL} = 12 mA		3 V	3 V	T_A = –40°C to 125°C			0.7	
I_I[3]	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = 25°C		±0.025	±0.25	µA
						T_A = –40°C to 125°C			±1.5	
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V	T_A = 25°C		±0.1	±1	µA
						T_A = –40°C to 125°C			±5	
				0 V to 3.6 V	0 V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to 125°C			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	T_A = 25°C		±0.5	±2.5	µA
						T_A = –40°C to 125°C			±5	
I_{CCA}[3]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			8	µA
				0 V	0 V to 3.6 V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	
				0 V to 3.6 V	0 V	T_A = –40°C to 125°C			8	
I_{CCB}[3]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			8	µA
				0 V	0 V to 3.6 V	T_A = –40°C to 125°C			8	
				0 V to 3.6 V	0 V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to 125°C			16	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		3.5	4.5	pF
						T_A = –40°C to 125°C			7	
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V	T_A = 25°C		6		pF
						T_A = –40°C to 125°C				

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.6 Switching Characteristics: V_{CCA} = 1.2 V

over recommended operating ambient temperature range, V_{CCA} = 1.2 V (unless otherwise noted) (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHL}, t_{PLH}	A	B	V_{CCB} = 1.2 V	3.4	ns
			V_{CCB} = 1.5 V ± 0.1 V	2.9	
			V_{CCB} = 1.8 V ± 0.15 V	2.7	
			V_{CCB} = 2.5 V ± 0.2 V	2.6	
			V_{CCB} = 3.3 V ± 0.3 V	2.8	
t_{PHL}, t_{PLH}	B	A	V_{CCB} = 1.2 V	3.6	ns
			V_{CCB} = 1.5 V ± 0.1 V	3.1	
			V_{CCB} = 1.8 V ± 0.15 V	2.8	
			V_{CCB} = 2.5 V ± 0.2 V	2.6	
			V_{CCB} = 3.3 V ± 0.3 V	2.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V	5.6	ns
			V_{CCB} = 1.5 V ± 0.1 V	4.7	
			V_{CCB} = 1.8 V ± 0.15 V	4.3	
			V_{CCB} = 2.5 V ± 0.2 V	3.9	
			V_{CCB} = 3.3 V ± 0.3 V	3.7	
t_{PZH}	$\overline{OE}$	B	V_{CCB} = 1.2 V	5	ns
			V_{CCB} = 1.5 V ± 0.1 V	4.3	
			V_{CCB} = 1.8 V ± 0.15 V	3.9	
			V_{CCB} = 2.5 V ± 0.2 V	3.6	
			V_{CCB} = 3.3 V ± 0.3 V	36.6	
t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V	5	
			V_{CCB} = 1.5 V ± 0.1 V	4.3	
			V_{CCB} = 1.8 V ± 0.15 V	3.9	
			V_{CCB} = 2.5 V ± 0.2 V	3.6	
			V_{CCB} = 3.3 V ± 0.3 V	3.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V	6.2	ns
			V_{CCB} = 1.5 V ± 0.1 V	5.2	
			V_{CCB} = 1.8 V ± 0.15 V	5.2	
			V_{CCB} = 2.5 V ± 0.2 V	4.3	
			V_{CCB} = 3.3 V ± 0.3 V	4.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V	5.9	ns
			V_{CCB} = 1.5 V ± 0.1 V	5.1	
			V_{CCB} = 1.8 V ± 0.15 V	5	
			V_{CCB} = 2.5 V ± 0.2 V	4.7	
			V_{CCB} = 3.3 V ± 0.3 V	5.5	

6.7 Switching Characteristics, V_{CCA} = 1.5 V ± 0.1 V

over recommended operating ambient temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		3.2		ns
			V_{CCB} = 1.5 V ± 0.1 V			11.3	
			V_{CCB} = 1.8 V ± 0.15 V			10.2	
			V_{CCB} = 2.5 V ± 0.2 V			9.2	
			V_{CCB} = 3.3 V ± 0.3 V			9.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3.3		ns
			V_{CCB} = 1.5 V ± 0.1 V			11.3	
			V_{CCB} = 1.8 V ± 0.15 V			11	
			V_{CCB} = 2.5 V ± 0.2 V			10.7	
			V_{CCB} = 3.3 V ± 0.3 V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.9		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.6	
			V_{CCB} = 1.8 V ± 0.15 V			14.5	
			V_{CCB} = 2.5 V ± 0.2 V			14.4	
			V_{CCB} = 3.3 V ± 0.3 V			14.4	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.6	
			V_{CCB} = 1.8 V ± 0.15 V			12.7	
			V_{CCB} = 2.5 V ± 0.2 V			10.8	
			V_{CCB} = 3.3 V ± 0.3 V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		5.6		ns
			V_{CCB} = 1.5 V ± 0.1 V			15.2	
			V_{CCB} = 1.8 V ± 0.15 V			15.2	
			V_{CCB} = 2.5 V ± 0.2 V			15.2	
			V_{CCB} = 3.3 V ± 0.3 V			15.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		5.2		ns
			V_{CCB} = 1.5 V ± 0.1 V			15.3	
			V_{CCB} = 1.8 V ± 0.15 V			14.1	
			V_{CCB} = 2.5 V ± 0.2 V			12.4	
			V_{CCB} = 3.3 V ± 0.3 V			12.6	

6.8 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating ambient temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.9		ns
			V_{CCB} = 1.5 V ± 0.1 V			11	
			V_{CCB} = 1.8 V ± 0.15 V			9.9	
			V_{CCB} = 2.5 V ± 0.2 V			8.9	
			V_{CCB} = 3.3 V ± 0.3 V			8.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3		ns
			V_{CCB} = 1.5 V ± 0.1 V			10.3	
			V_{CCB} = 1.8 V ± 0.15 V			9.9	
			V_{CCB} = 2.5 V ± 0.2 V			9.6	
			V_{CCB} = 3.3 V ± 0.3 V			9.5	

Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V (continued)

over recommended operating ambient temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.4		ns
			V_{CCB} = 1.5 V ± 0.1 V			12.4	
			V_{CCB} = 1.8 V ± 0.15 V			12.3	
			V_{CCB} = 2.5 V ± 0.2 V			12.3	
			V_{CCB} = 3.3 V ± 0.3 V			12.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.1		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.2	
			V_{CCB} = 1.8 V ± 0.15 V			12.4	
			V_{CCB} = 2.5 V ± 0.2 V			10.3	
			V_{CCB} = 3.3 V ± 0.3 V			9.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		5.4		ns
			V_{CCB} = 1.5 V ± 0.1 V			13.6	
			V_{CCB} = 1.8 V ± 0.15 V			13.7	
			V_{CCB} = 2.5 V ± 0.2 V			13.7	
			V_{CCB} = 3.3 V ± 0.3 V			13.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		5		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.9	
			V_{CCB} = 1.8 V ± 0.15 V			13.7	
			V_{CCB} = 2.5 V ± 0.2 V			11.9	
			V_{CCB} = 3.3 V ± 0.3 V			11.9	

6.9 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating ambient temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.8		ns
			V_{CCB} = 1.5 V ± 0.1 V			10.7	
			V_{CCB} = 1.8 V ± 0.15 V			9.6	
			V_{CCB} = 2.5 V ± 0.2 V			8.5	
			V_{CCB} = 3.3 V ± 0.3 V			8.6	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		2.7		ns
			V_{CCB} = 1.5 V ± 0.1 V			9.2	
			V_{CCB} = 1.8 V ± 0.15 V			8.9	
			V_{CCB} = 2.5 V ± 0.2 V			8.4	
			V_{CCB} = 3.3 V ± 0.3 V			8.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4		ns
			V_{CCB} = 1.5 V ± 0.1 V			11.5	
			V_{CCB} = 1.8 V ± 0.15 V			10.2	
			V_{CCB} = 2.5 V ± 0.2 V			9.8	
			V_{CCB} = 3.3 V ± 0.3 V			9.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.8		ns
			V_{CCB} = 1.5 V ± 0.1 V			13.8	
			V_{CCB} = 1.8 V ± 0.15 V			12	
			V_{CCB} = 2.5 V ± 0.2 V			9.8	
			V_{CCB} = 3.3 V ± 0.3 V			9	

Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating ambient temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.7		ns
			V_{CCB} = 1.5 V ± 0.1 V			13.4	
			V_{CCB} = 1.8 V ± 0.15 V			13.4	
			V_{CCB} = 2.5 V ± 0.2 V			11.2	
			V_{CCB} = 3.3 V ± 0.3 V			11.5	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.4	
			V_{CCB} = 1.8 V ± 0.15 V			13.2	
			V_{CCB} = 2.5 V ± 0.2 V			11.2	
			V_{CCB} = 3.3 V ± 0.3 V			10.2	

6.10 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating ambient temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.9		ns
			V_{CCB} = 1.5 V ± 0.1 V			10.6	
			V_{CCB} = 1.8 V ± 0.15 V			9.5	
			V_{CCB} = 2.5 V ± 0.2 V			8.3	
			V_{CCB} = 3.3 V ± 0.3 V			7.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		2.6		ns
			V_{CCB} = 1.5 V ± 0.1 V			9.2	
			V_{CCB} = 1.8 V ± 0.15 V			8.4	
			V_{CCB} = 2.5 V ± 0.2 V			8	
			V_{CCB} = 3.3 V ± 0.3 V			7.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		3.8		ns
			V_{CCB} = 1.5 V ± 0.1 V			13.7	
			V_{CCB} = 1.8 V ± 0.15 V			10.2	
			V_{CCB} = 2.5 V ± 0.2 V			8.8	
			V_{CCB} = 3.3 V ± 0.3 V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.7		ns
			V_{CCB} = 1.5 V ± 0.1 V			13.7	
			V_{CCB} = 1.8 V ± 0.15 V			11.8	
			V_{CCB} = 2.5 V ± 0.2 V			9.7	
			V_{CCB} = 3.3 V ± 0.3 V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.8		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.3	
			V_{CCB} = 1.8 V ± 0.15 V			13.3	
			V_{CCB} = 2.5 V ± 0.2 V			10.6	
			V_{CCB} = 3.3 V ± 0.3 V			11.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		5.3		ns
			V_{CCB} = 1.5 V ± 0.1 V			14.3	
			V_{CCB} = 1.8 V ± 0.15 V			13.1	
			V_{CCB} = 2.5 V ± 0.2 V			11.4	
			V_{CCB} = 3.3 V ± 0.3 V			11.2	

6.11 Operating Characteristics

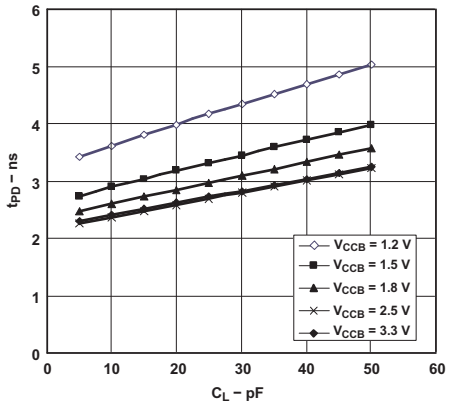
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	pF
				V_{CCA} = V_{CCB} = 1.5 V	1	
				V_{CCA} = V_{CCB} = 1.8 V	1	
				V_{CCA} =V_{CCB} = 2.5 V	1.5	
				V_{CCA} = V_{CCB} = 3.3 V	2	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} =V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	
				V_{CCA} = V_{CCB} = 1.5 V	12.5	
				V_{CCA} = V_{CCB} = 1.8 V	13	
				V_{CCA} =V_{CCB} = 2.5 V	14	
				V_{CCA} = V_{CCB} = 3.3 V	15	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} =V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	pF
				V_{CCA} = V_{CCB} = 1.5 V	12.5	
				V_{CCA} = V_{CCB} = 1.8 V	13	
				V_{CCA} =V_{CCB} = 2.5 V	14	
				V_{CCA} = V_{CCB} = 3.3 V	15	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} =V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V	1	
				V_{CCA} = V_{CCB} = 1.8 V	1	
				V_{CCA} =V_{CCB} = 2.5 V	1	
				V_{CCA} = V_{CCB} = 3.3 V	2	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} =V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		

(1) Power dissipation capacitance per transceiver

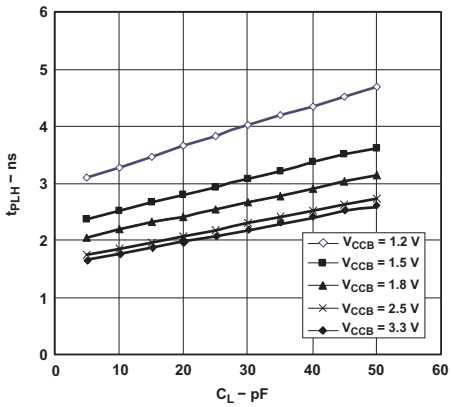
6.12 Typical Characteristics

T_A = 25°C



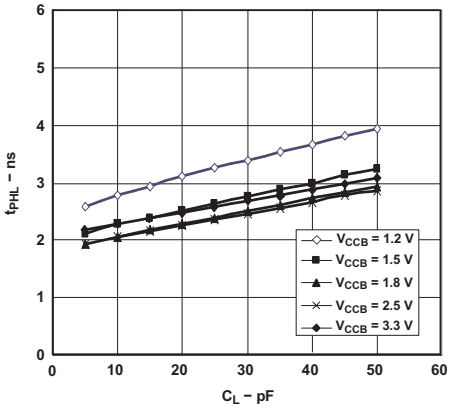
V_{CCA} = 1.2 V

Figure 1. Typical Propagation Delay (A to B) vs Load Capacitance



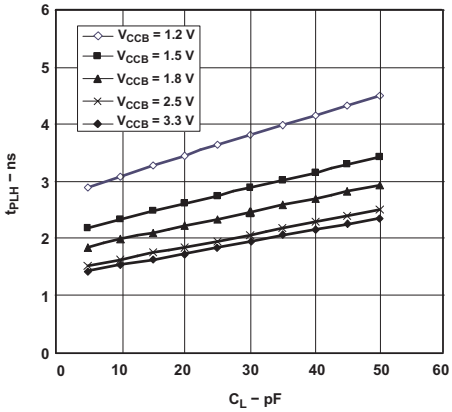
V_{CCA} = 1.5 V

Figure 2. Typical Propagation Delay (A to B) vs Load Capacitance



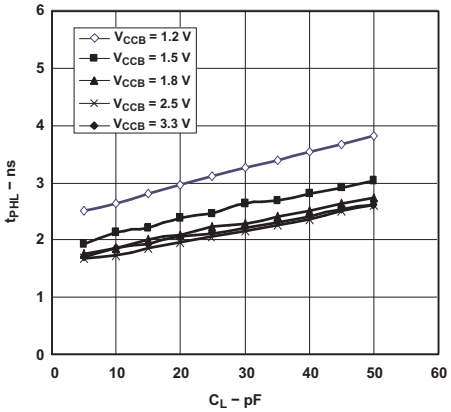
V_{CCA} = 1.5 V

Figure 3. Typical Propagation Delay (A to B) vs Load Capacitance



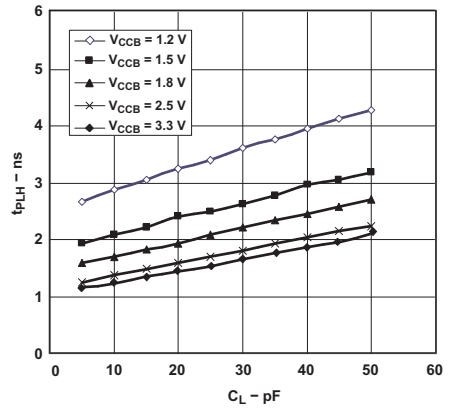
V_{CCA} = 1.8 V

Figure 4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8 V

Figure 5. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 2.5 V

Figure 6. Typical Propagation Delay (A to B) vs Load Capacitance

Typical Characteristics (continued)

T_A = 25°C

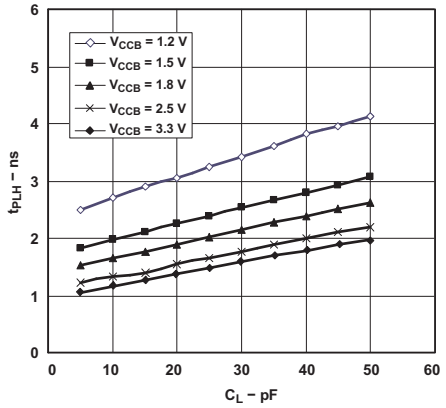


Figure 7. Typical Propagation Delay (A to B) vs Load Capacitance

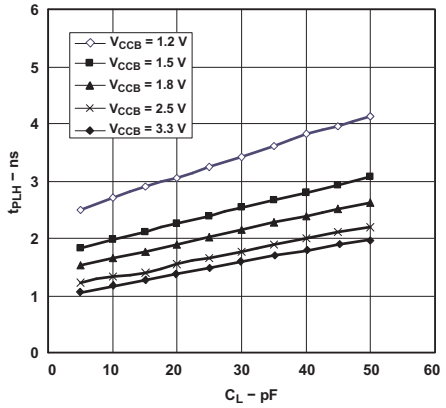


Figure 8. Typical Propagation Delay (A to B) vs Load Capacitance

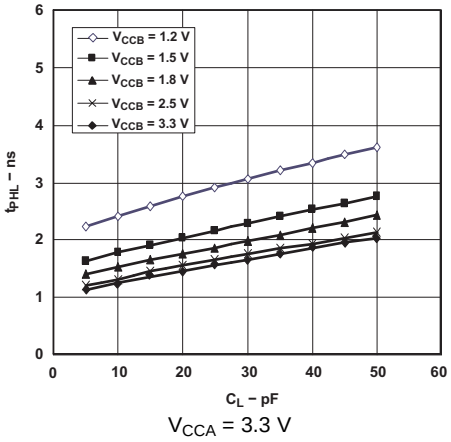


Figure 9. Typical Propagation Delay (A to B) vs Load Capacitance

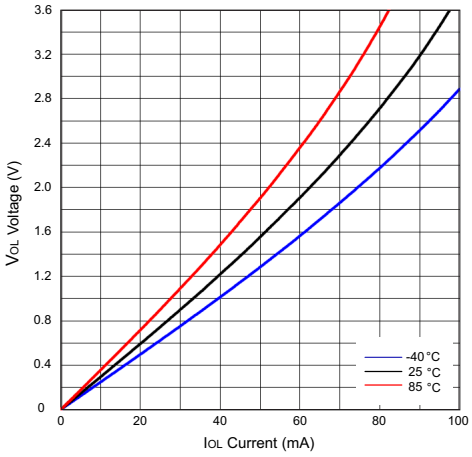


Figure 10. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL})

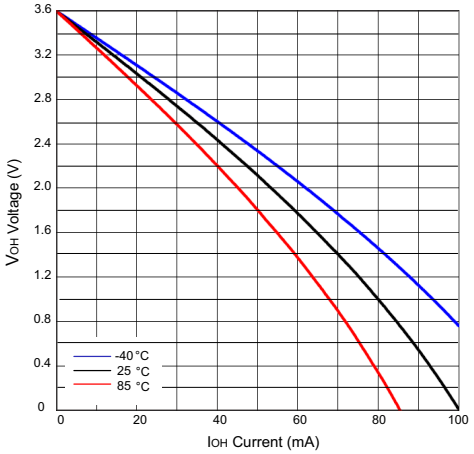
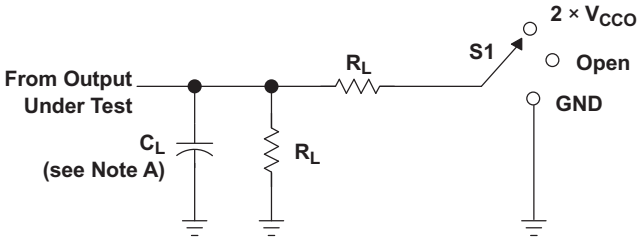


Figure 11. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH})

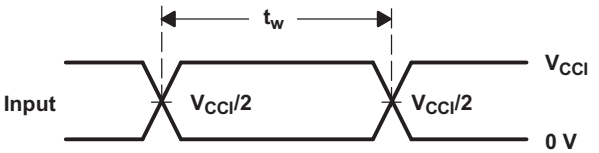
7 Parameter Measurement Information



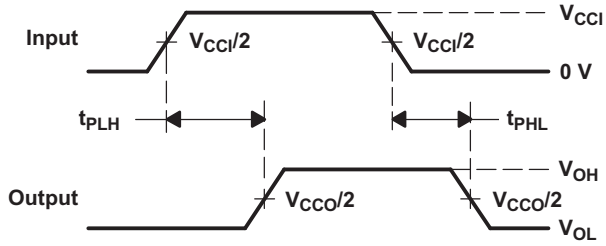
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

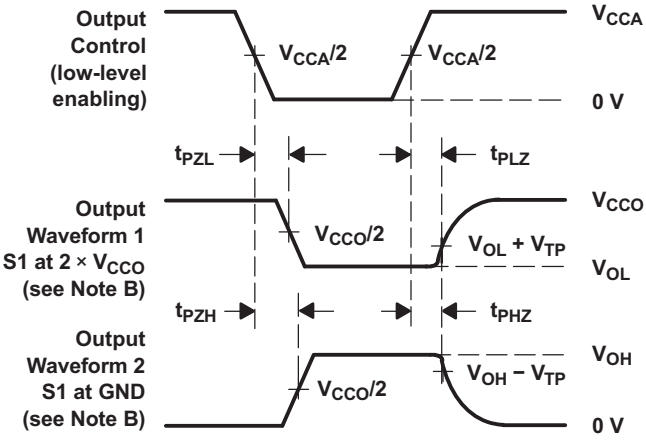
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 12. Load and Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AVC4T245-Q1 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR,1$\overline{OE}$, and 2$\overline{OE}$) are supported by V_{CCA}, and Bx pins are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

8.2 Functional Block Diagram

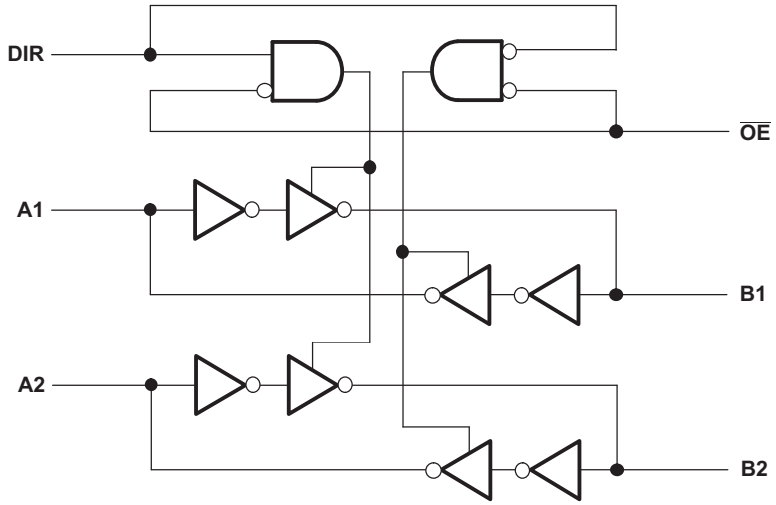


Figure 13. Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245-Q1

8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Supports High Speed Translation

The SN74AVC4T245-Q1 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AVC4T245-Q1 device.

Table 1. Function Table (Each 2-Bit Section)(1)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVC4T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T245-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380 Mbps when the device translates a signal from 1.8 V to 3.3 V.

9.2 Typical Application

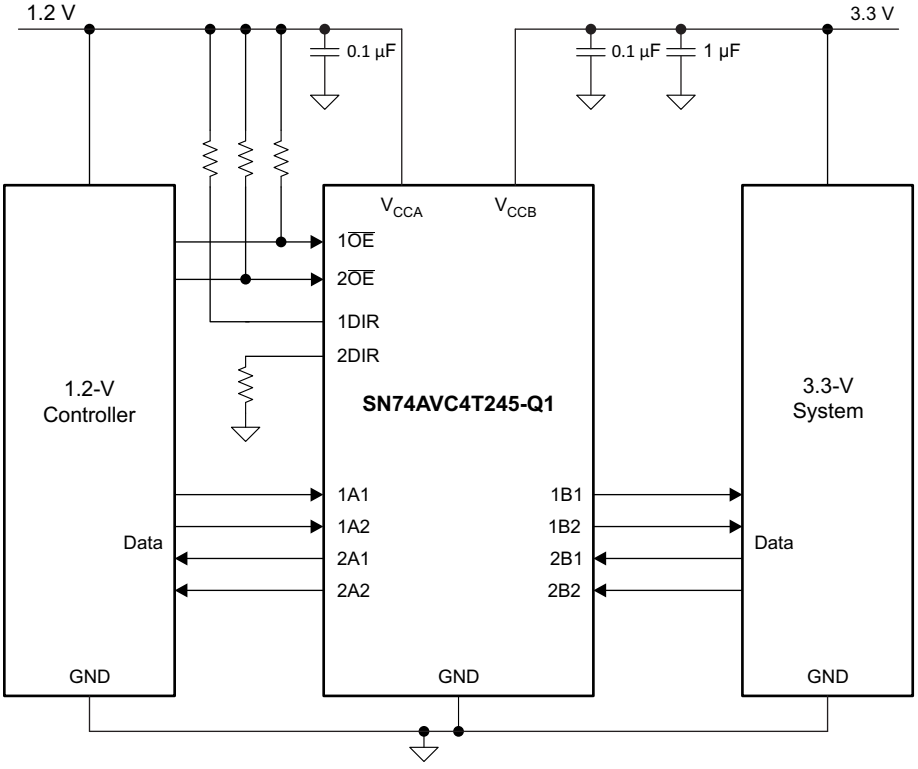


Figure 14. Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V
Output voltage range	3.3 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port. For this example, the input voltage is 1.2 V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T245-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3 V.

9.2.3 Application Curve

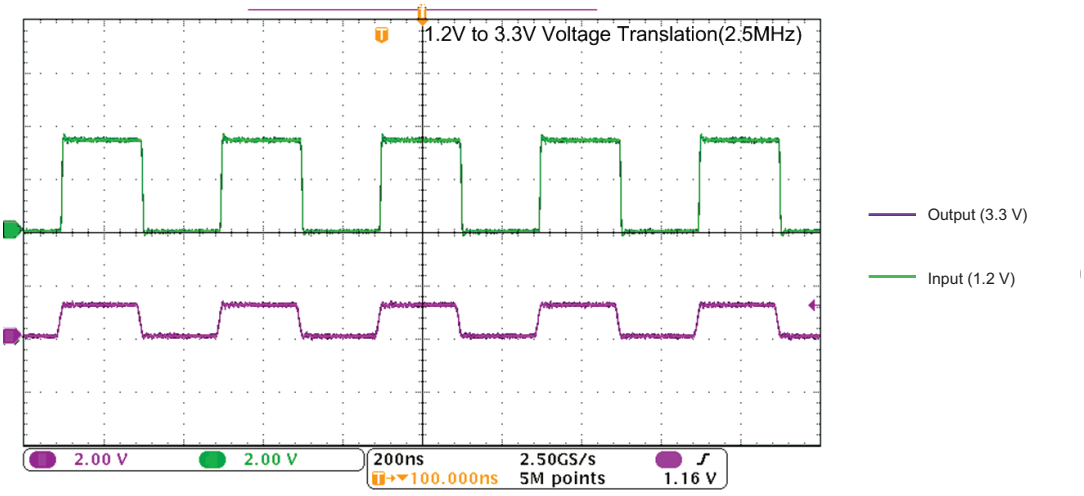


Figure 15. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

The SN74AVC4T245-Q1 device uses two separate configurable power-supply rails: V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V, and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA}; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

11.2 Layout Example

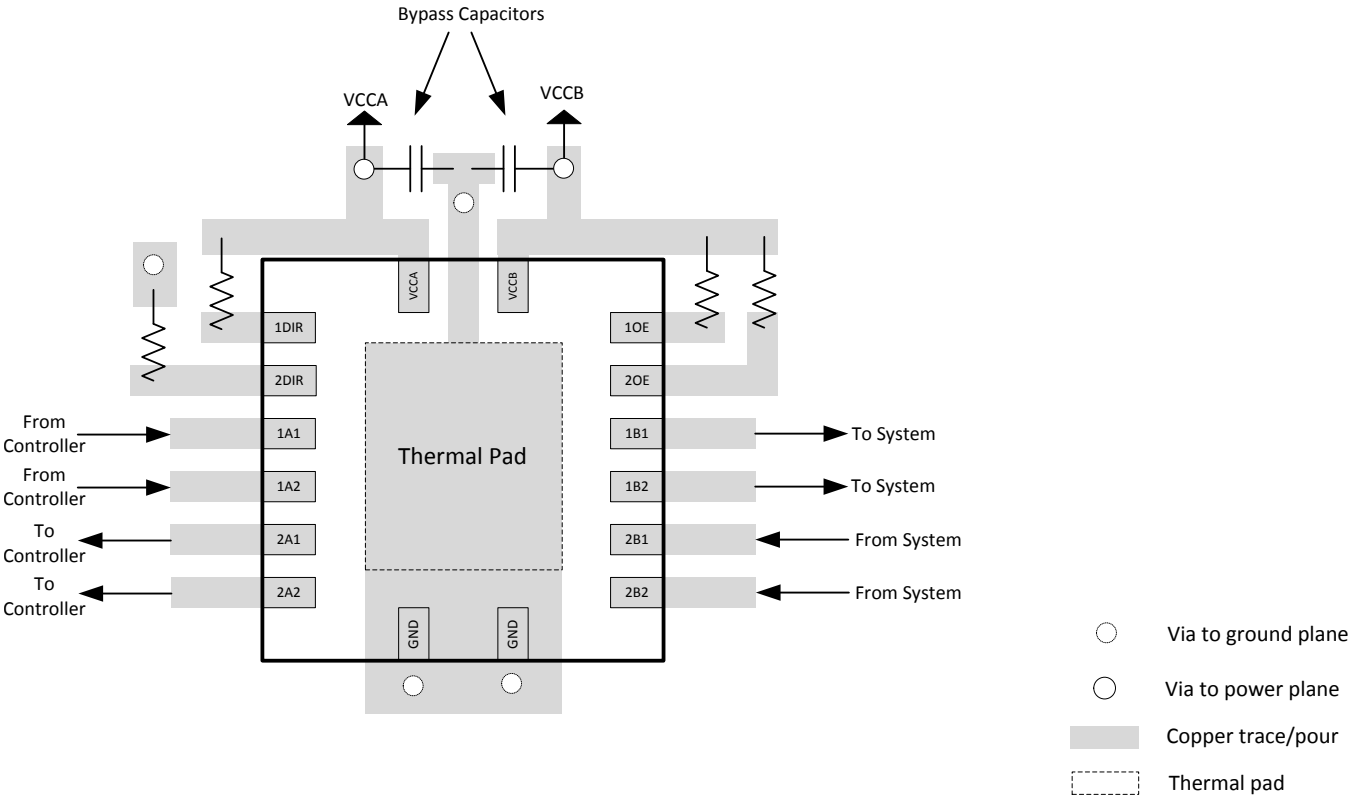


Figure 16. SN74AVC4T245-Q1 RGY Package Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

- *IC Package Thermal Metrics* application report (SPRA953)
- *Implications of Slow or Floating CMOS Inputs* application report (SCBA004)

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12.2 Trademarks

E2E is a trademark of Texas Instruments.
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12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T245QRGYRQ1	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AVC4T245-Q1 :

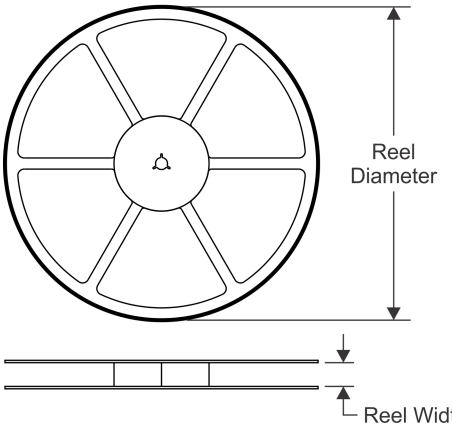
- Catalog: SN74AVC4T245

NOTE: Qualified Version Definitions:

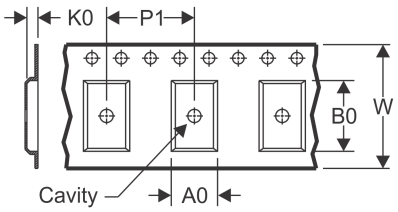
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

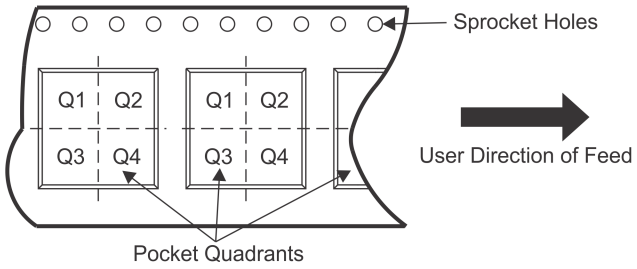


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

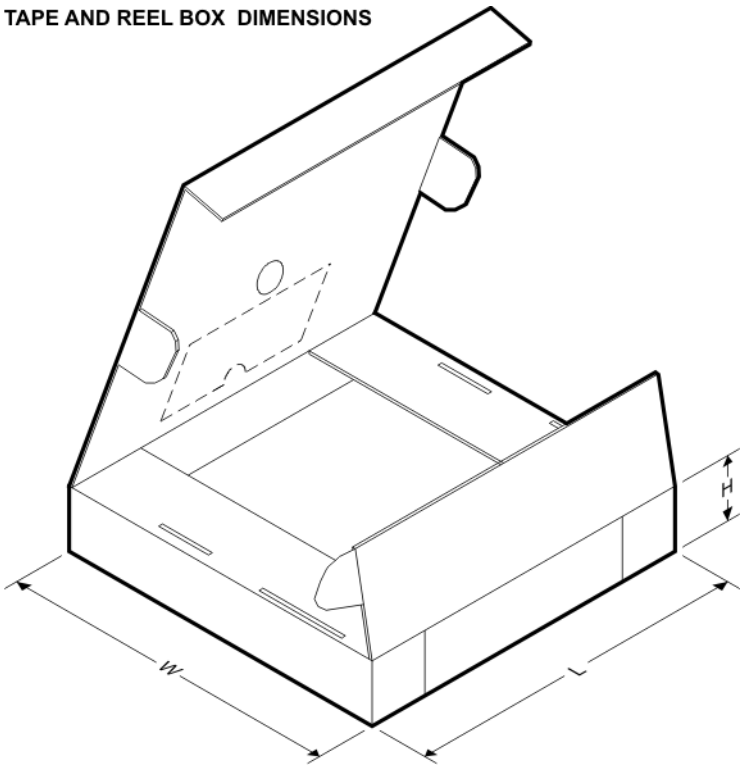
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

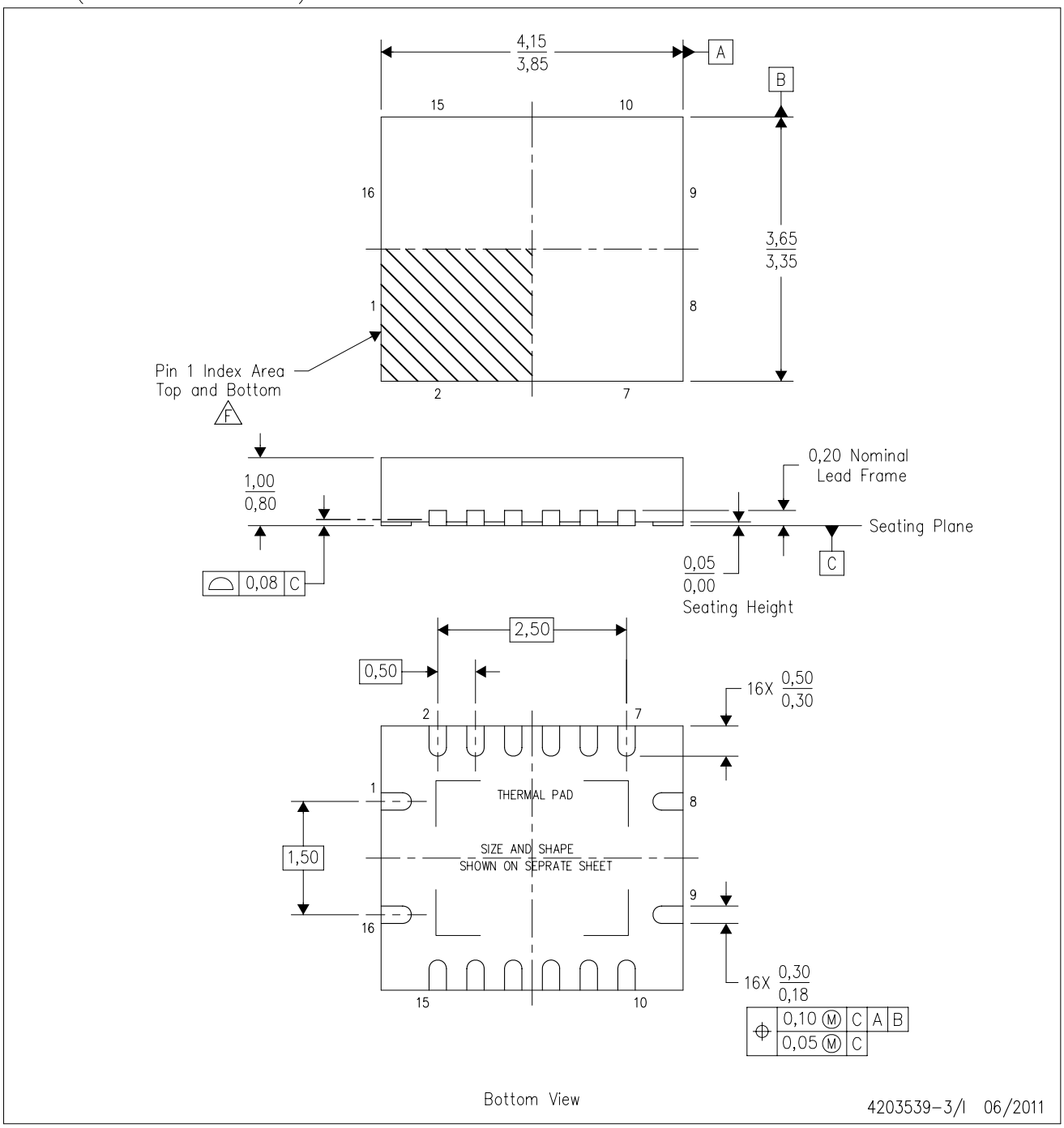
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	367.0	367.0	35.0

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

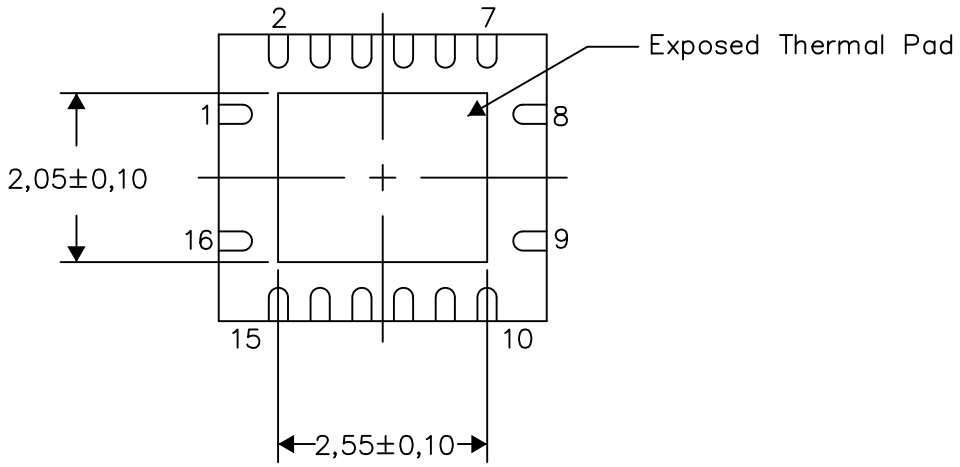
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



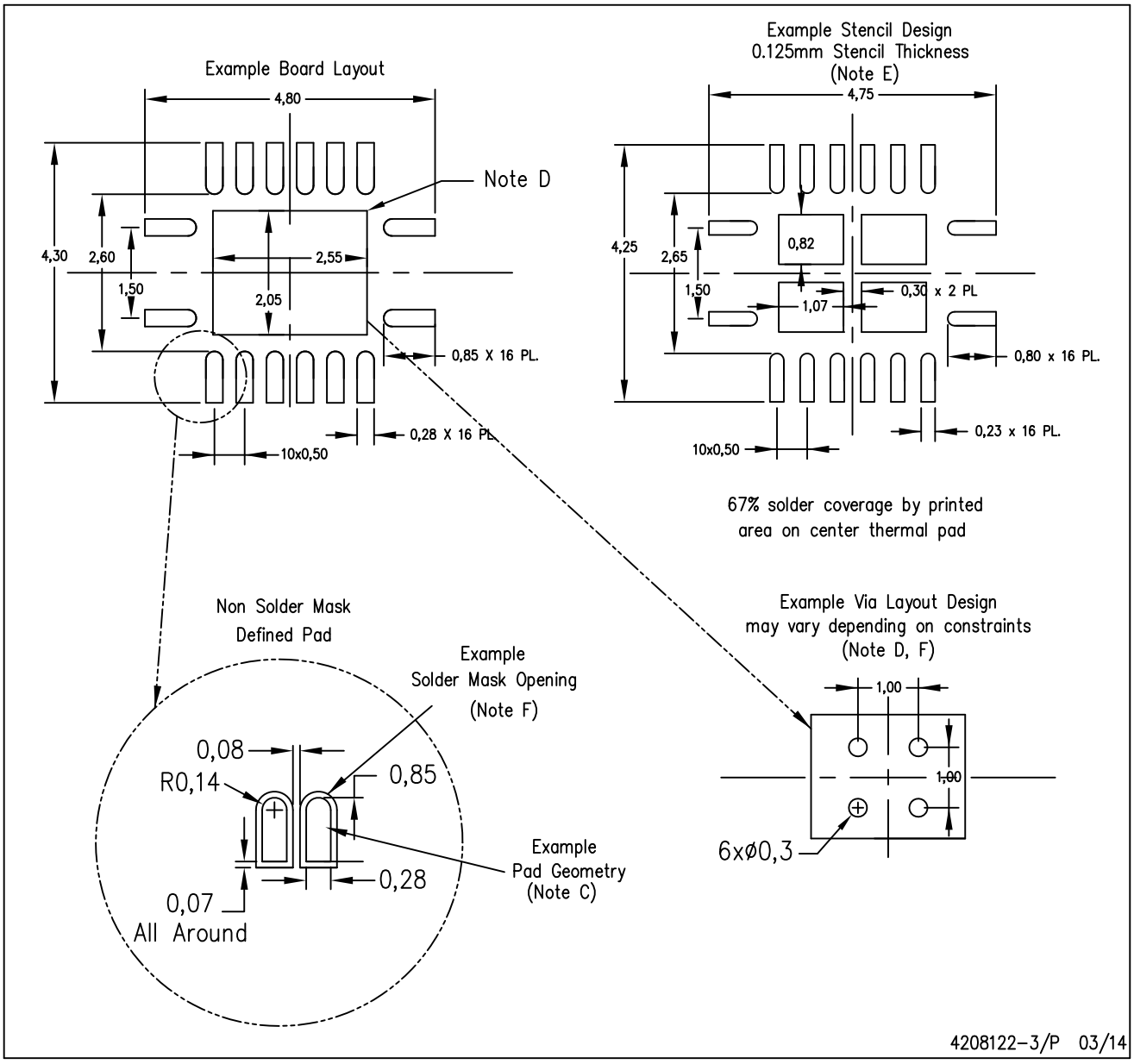
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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