STMLS05

Enhanced five-channel PMOS load switches

Datasheet - production data



UFQFPN, 3x3 mm, 16L

Features

- Five-channel PMOS switches
- Input/output voltage range: 1.05 V - 5.5 V
- V_{DD} voltage range: 1.8 V - 3.6 V
- Maximum output rated current: 100 mA
- Low R_{ON}: 120 mΩ typ. at 1.8 V
- Built-in soft-start feature for each channel programmable by I^2C (1, 2, 4, and 8 ms)
- Enable/disable function of each load switch programmed by I^2C
- Enable pin for I^2C block
- Ultra low quiescent current: 2.4 µA max.
- Output discharge circuitry
- ESD tolerance: 2 kV HBM
- Temperature range: -40 up to 70 °C
- Package: UFQFPN, 3 x3 mm, 16L
- Lead-free and Halogen-free device
- V_{DD} UVLO circuit for enhanced application robustness

Applications

- Smart phones
- Tablets
- Mobile device accessories
- Wearable devices

Description

The STMLS05 device is an array of five load switches, all featuring a soft-start turn-on to protect from high inrush current. The soft-start timing can be programmed by the I^2C. Each channel may be turned ON/OFF by the I^2C block. The I^2C block may be disabled through the EN_I2C pin.

In addition, channel 0 can be programmed ON or OFF by the EN_SW0 pin. The device is available in a UFQFPN package (3x3 mm) and its temperature range is -40 to 70 °C.

Table 1: Device summary

Order code	I^2C base address	Package marking
STMLS05ACQTR	0x5C	AS5C

This is information on a product in full production.

www.st.com

Contents

1 Functional block diagram 3

2 Pin settings 4

2.1 Pin connections 4

2.2 Pin description 4

3 Maximum ratings 5

3.1 Absolute maximum ratings 5

3.2 Recommended operating conditions 5

4 Electrical specifications 6

5 I^2C register map 9

6 Typical operating characteristics 10

7 Application information 11

7.1 Power-up sequence and UVLO functionality 11

7.2 Output discharge circuitry 11

7.3 EN_I2C (I^2C block enable) functionality 11

7.4 I^2C register auto-incrementation 11

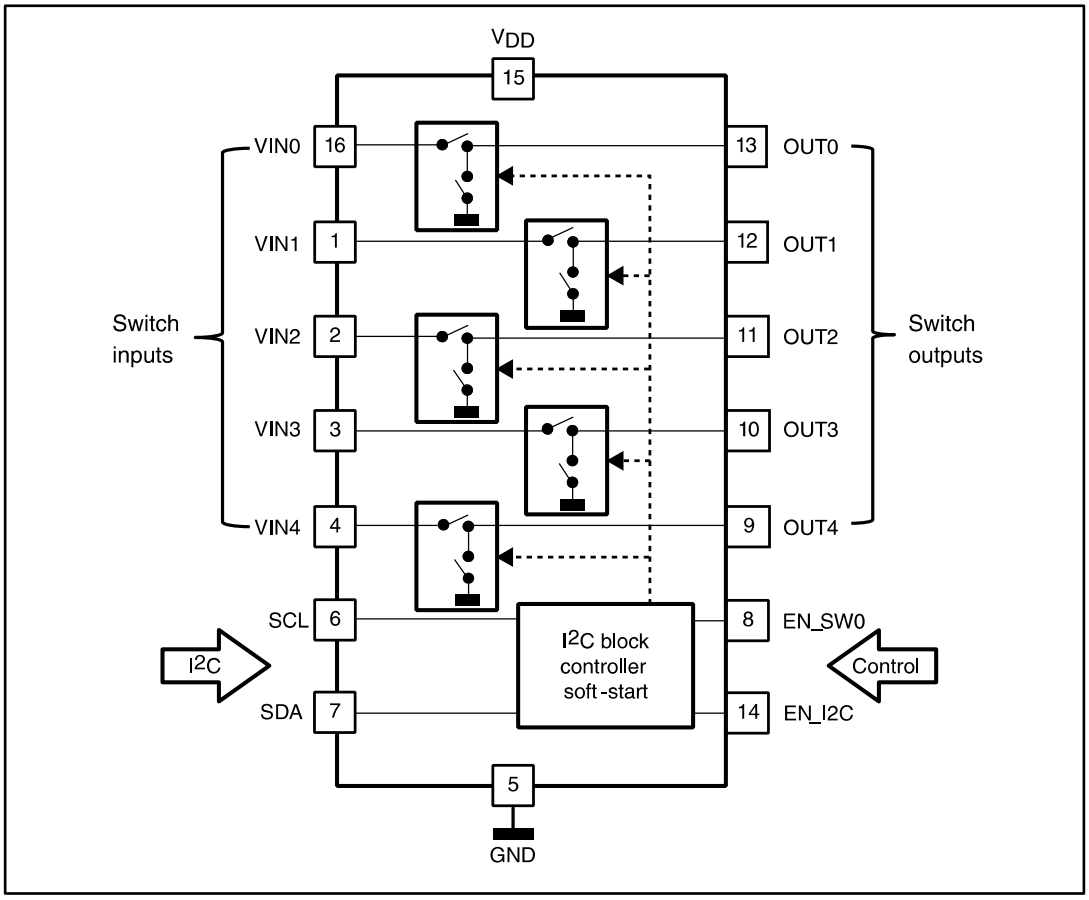
8 Package information 12

8.1 UFQFPN, 3x3mm, 16 L package information 13

9 Revision history 15

1 Functional block diagram

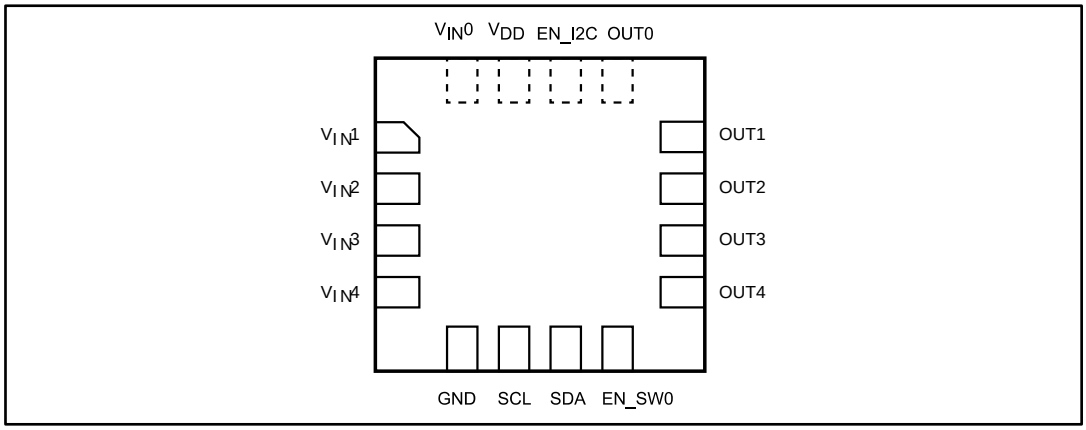
Figure 1: Functional block diagram



2 Pin settings

2.1 Pin connections

Figure 2: UFQFPN, 3x3 mm, 16L package (top view)



2.2 Pin description

Table 2: UFQFPN 3x3 mm, 16L pin description

Pin number	Name	Function
1	$V_{IN}1$	Power input
2	$V_{IN}2$	
3	$V_{IN}3$	
4	$V_{IN}4$	
5	GND	Ground
6	SCL	I^2C serial clock
7	SDA	I^2C serial data
8	EN_SW0	Enable input - switch 0
9	OUT4	Power output
10	OUT3	
11	OUT2	
12	OUT1	
13	OUT0	
14	EN_I2C	Enable input - I^2C block
15	V_{DD}	Supply voltage
16	$V_{IN}0$	Power input

3 Maximum ratings

Stressing the device beyond the rating listed in *Table 3: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in *Table 4: "Recommended operating conditions"* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage range	–0.3 to 6.0	V
V_{IN}, V_{OUT}	I/O voltage	–0.3 to 6.0	
I_{OUT}	Maximum continuous output current	500	mA
T_J	Junction operating temperature	150	°C
T_A	Operating temperature range	-40 to 70	
T_{STG}	Storage temperature	–55 to 150	
ESD	ESD protection level (all pins, HBM)	2	kV
V_{SDA}	I/O voltage	-0.3 to 6.0	V
V_{SCL}	I/O voltage	-0.3 to 6.0	
V_{EN_I2C}	I/O voltage	-0.3 to V_{DD} + 0.3	
V_{EN_SW0}	I/O voltage	-0.3 to V_{DD} + 0.3	

3.2 Recommended operating conditions

Table 4: Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	1.8	—	3.6	V
V_{IN}	Input voltage range	1.05		5.5	
V_{OUT}	Output voltage range	0		V_{IN}	
I_{OUT}	Continuous output current	—		100	mA
V_{IL}	Input logic low voltage (EN_I2C, EN_SW0, SDA, SCL)	—		0.3 V_{DD}	V
V_{IH}	Input logic high voltage (EN_I2C, EN_SW0, SDA, SCL)	0.7 V_{DD}		V_{DD}	

4 Electrical specifications

In the table below, typical values are valid for $T_A = T_J = 25$ °C.

Table 5: Electrical characteristics

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Quiescent current, switches ON, I^2C OFF	I_{OUT} = 0 mA	—	1	24	µA
	Quiescent current, switches ON, I^2C ON	I_{OUT} = 0 mA, no clock on SCL	—	—	2.4	
I_{DD}(OFF)	OFF-state supply current	V_{OUT} open	—	0.04	1	
$I_{INx(LEAKAGE)}$	OFF-state switch leakage current per switch	V_{IN} = 1.05 V, V_{OUT} = 0 V, V_{DD} = 1.8 V to 3.6 V	—	0.01	10	
		V_{IN} = 1.8 V, V_{OUT} = 0 V, V_{DD} = 1.8 V to 3.6 V	—	0.04	12	
		V_{IN} = 3.3 V, V_{OUT} = 0 V, V_{DD} = 1.8 V to 3.6 V	—	0.07	20	
		V_{IN} = 5.5 V, V_{OUT} = 0 V, V_{DD} = 1.8 V to 3.6 V	—	0.2	25	
$I_{INx(LEAKAGE)}$ (1)	OFF-state switch leakage current per switch	V_{IN} = 3.6 V, V_{OUT} floating, V_{DD} = 1.8 V to 3.6 V	—	2	75	nA
		V_{IN} = 5.5 V, V_{OUT} floating, V_{DD} = 1.8 V to 3.6 V	—	4	200	
V_{UVLO}	V_{DD} UVLO threshold (2)		0.9	1.35	1.6	V
R_{ON}	ON resistance	V_{IN} = 1.05 V, I_{OUT} = 100 mA	—	150	180	mΩ
		V_{IN} = 1.8 V, I_{OUT} = 100 mA	—	120	140	
		V_{IN} = 3.3 V, I_{OUT} = 100 mA	—	110	130	
		V_{IN} = 5.5 V, I_{OUT} = 100 mA	—	108	125	
t_{DIS}	Output discharge pulse width		1.7	4.1	8.3	ms
t_{D_ON} (3)	Delay between discharge switch turn-off and main switch turn-on to prevent cross-conduction	V_{IN} = V_{DD} = 1.8 V, C_L = 47 µF, R_L disconnected, ST2_x = 0, DEx = 1, DTx = 1	100	—	—	ns
t_{D_OFF} (3)	Delay between main switch turn-off and discharge switch turn-on to prevent cross-conduction		220	—	—	
Switching characteristics V_{IN} = 3.6 V, V_{DD} = 1.8 V, R_L = 100 Ω, C_L = 47 µF						
t_{ON}	Turn-on time: from switch enabled to V_{OUT} above 90 % of V_{IN}	No soft-start	—	80	—	µs
	Turn-on time: from switch enabled to V_{OUT} above 90 % of V_{IN}	Soft-start = 1 ms	0.5	1	1.15	ms
	Turn-on time: from switch enabled to V_{OUT} above 90 % of V_{IN}	Soft-start = 2 ms	1.2	2	2.25	
	Turn-on time: from switch enabled to V_{OUT} above 90 % of V_{IN}	Soft-start = 4 ms	2.3	4	4.3	

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
t_{ON}	Turn-on time: from switch enabled to V_{OUT} above 90 % of V_{IN}	Soft-start = 8 ms	4.35	8	10	ms
t_{OFF} (1)	Turn-off time: from switch disabled to V_{OUT} below 0.6 V	Discharge enabled (DEx = 1)	—	1.1	1.4	
		Discharge disabled (DEx = 0)	—	8.4	—	
		Discharge enabled (DEx = 1), C_L = 47 µF, R_L disconnected	—	1.3	1.7	

Notes:

(1)Based on characterization data. Not tested in production.

(2)Minimum V_{DD} fall time for proper UVLO circuit functionality is 20 µs.

(3)Guaranteed by design. Not tested in production.

Figure 3: Timing waveform

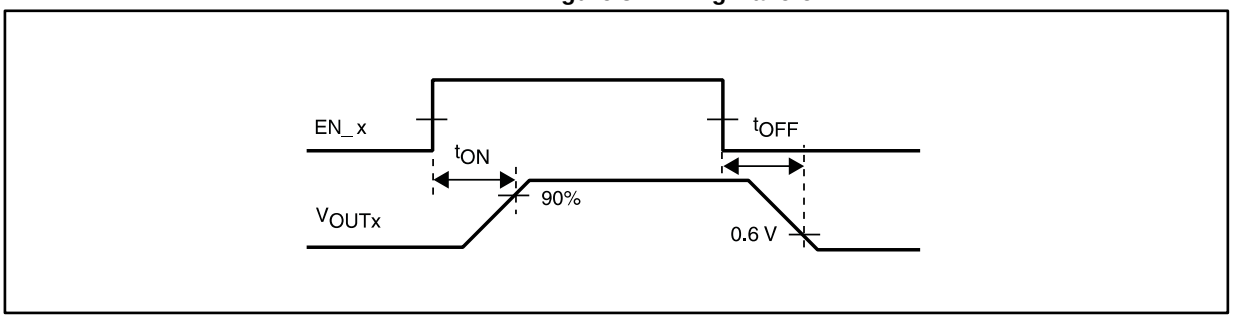
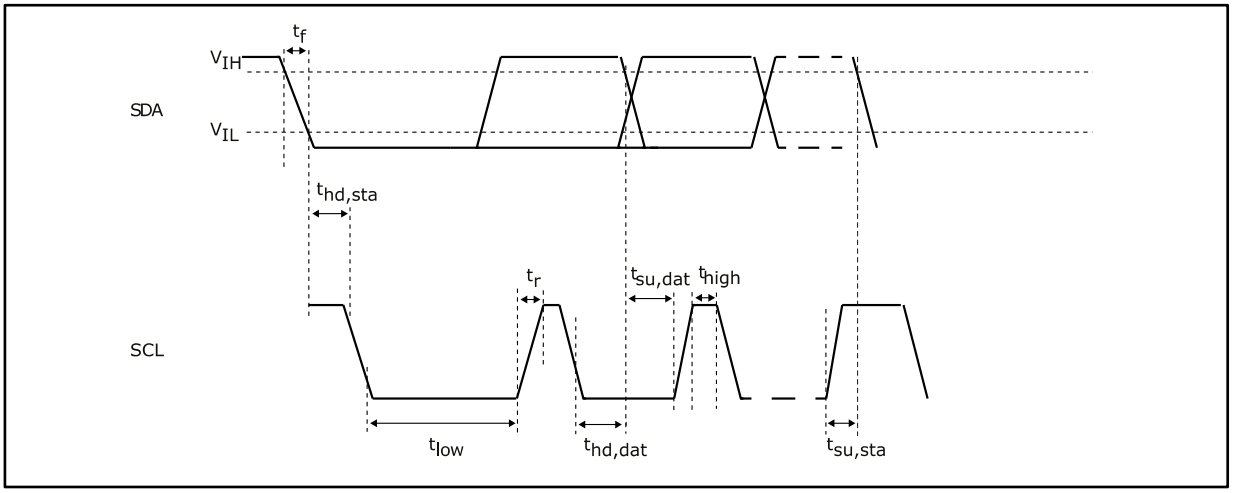


Table 6: I²C timing - V_{DD} = 1.8 V, T_A = -40 to 70 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency		0		400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition		0.6		—	
t_{low}	LOW period of the SCL clock		1.3		—	
t_{high}	HIGH period of the SCL clock		0.6		—	µs
$t_{su,dat}$	Setup time for repeated START condition		0.6		—	
$t_{hd,dat}$	Data hold time		0		0.9	
$t_{su,dat}$	Data setup time	—	100	—	—	
t_r	Rise time of both SDA and SCL signals		20 + 0.1 C_b		300	ns
t_f	Fall time of both SDA and SCL signals		20 + 0.1 C_b		300	
$t_{su,sto}$	Setup time for STOP condition		0.6		—	
t_{buf}	Bus free time between a STOP and START condition		1.3		—	µs
C_b	Capacitive load for each bus line		—		400	pF

Figure 4: I²C timing diagram



5 I²C register map

I²C base address

The I²C base address for writing to the device is 0x5C (01011100). For reading from device it is 0x5D (01011101).

Table 7: I²C register map

Address	Register purpose	b7	b6	b5	b4	b3	b2	b1	b0
0x00	Channel 0 setup	—	—	—	DT0	DE0	ST2_0	ST1_0	ST0_0
0x01	Channel 1 setup	—	—	—	DT1	DE1	ST2_1	ST1_1	ST0_1
0x02	Channel 2 setup	—	—	—	DT2	DE2	ST2_2	ST1_2	ST0_2
0x03	Channel 3 setup	—	—	—	DT3	DE3	ST2_3	ST1_3	ST0_3
0x04	Channel 4 setup	—	—	—	DT4	DE4	ST2_4	ST1_4	ST0_4
0x05	Channel enable	—	—	—	EN_4	EN_3	EN_2	EN_1	EN_0

Table 8: I²C register bit functions

Bit	Value	Function	Power-up value
EN_x (1)	0	Channel x disabled (off)	0
	1	Channel x enabled (on)	
DEx (discharge enable on channel x)	0	No discharge after channel x disable	1
	1	Discharge enabled	
DTx (discharge type on channel x)	0	Discharge during t_{DIS}	0
	1	Permanent discharge when channel x is disabled	
ST2_x	0	No soft-start time for channel x	0
	1	Soft-start for channel x defined by ST1_x, ST0_x bits	
ST1_x, ST0_x	0, 0	Soft-start 1 ms	0
	0, 1	Soft-start 2 ms	
	1, 0	Soft-start 4 ms	
	1, 1	Soft-start 8 ms	

Notes:

(1)The state-of-channel 0 is the OR function between the EN_0 bit and EN_SW0 pin

6 Typical operating characteristics

Figure 5: Output discharge circuitry performance (V_{DD} = 1.8 V, C_L = 47 µF, R_L = 100 Ω, $T_A = T_J$ = 25 °C)

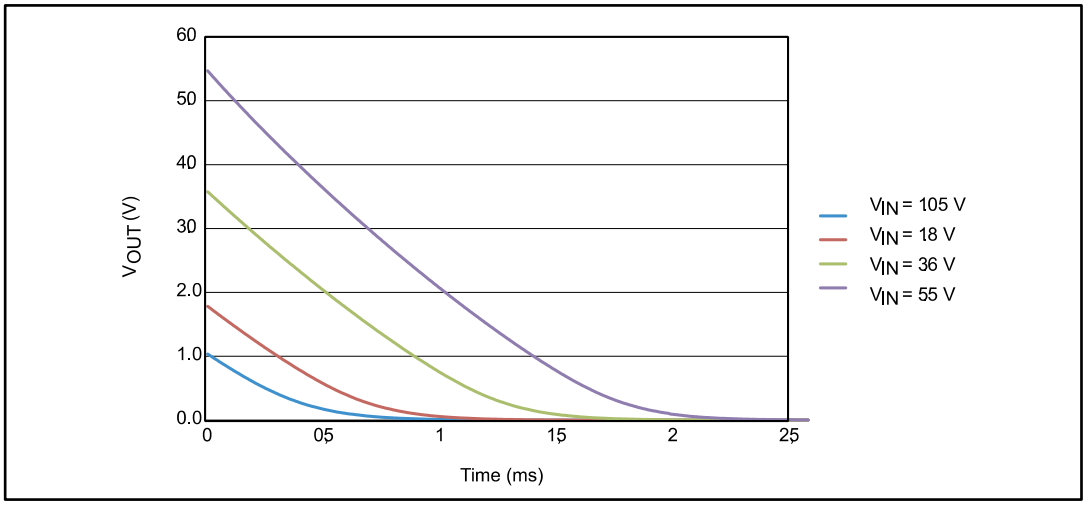
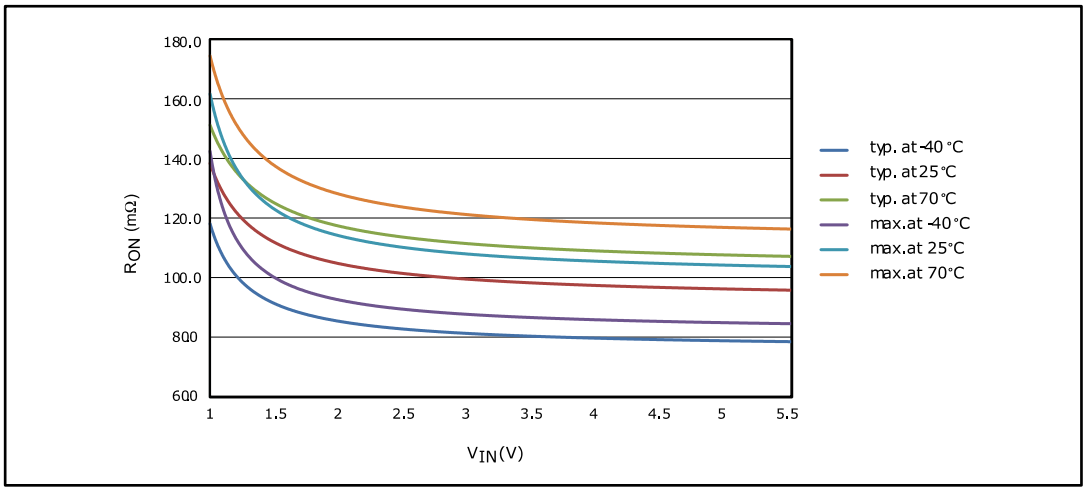


Figure 6: R_{ON} vs. V_{IN} (I_{OUT} = 100 mA)



7 Application information

7.1 Power-up sequence and UVLO functionality

The STMLS05 device is powered from the V_{DD} pin. Thus, for full device functionality a valid V_{DD} must be present.

The V_{DD} UVLO circuit enhances application robustness. If the V_{DD} is below the UVLO threshold, all main switches and discharge circuits are off and all registers are reset to their power-up values even if the V_{IN} is applied.

For proper UVLO functionality, the V_{DD} rise and fall time must be longer than 20 microseconds. In most applications this is ensured automatically otherwise a simple R-C element in the V_{DD} line (see *Figure 7: "R-C element in VDD line"*) ensures proper functionality. This R-C element also provides an excellent V_{DD} decoupling.

7.2 Output discharge circuitry

Internal output discharge circuits are activated at the moment of the main MOSFET turn-off. They are kept active for a period of 1.7 ms min. t_{DIS}, or they are kept active permanently for the whole period when the main switch is turned off, based on the DTx bit.

Output discharge can also be disabled by setting the DEx bit to 0.

It is guaranteed that the main MOSFET and the discharge circuit are never turned on at the same time. The t_{D_ON} delay shown in applies and the discharge circuit is disabled if the main MOSFET is enabled during the t_{DIS} pulse.

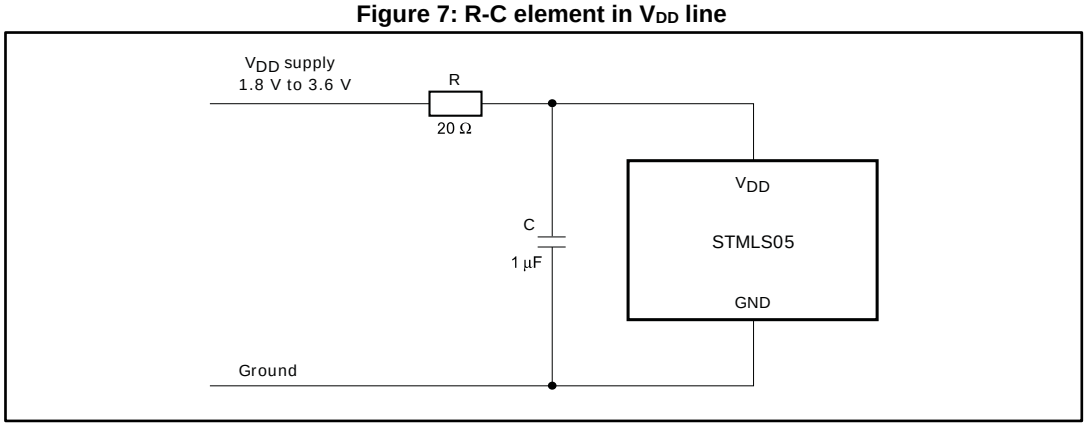
7.3 EN_I2C (I^2C block enable) functionality

The EN_I2C pin disables I^2C communication. During the I^2C block disable period (EN_I2C = 0) the last state-of-power switches are kept and I^2C commands are ignored. I^2C communication is not influenced.

7.4 I^2C register auto-incrementation

The STMLS05 device supports automatic incrementation of the I^2C register addresses. However, the automatic shift from the highest register address to the lowest address is not supported.

Figure 7: R-C element in V_{DD} line

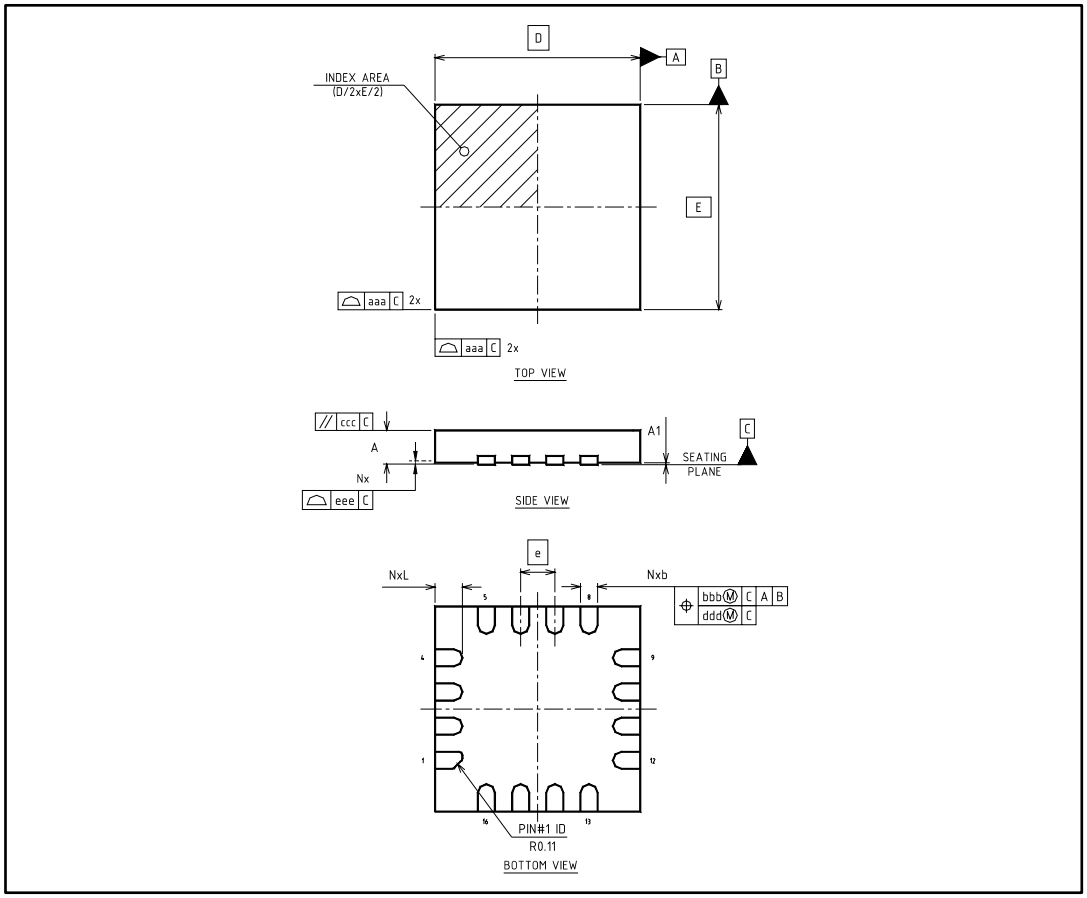


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 UFQFPN, 3x3mm, 16 L package information

Figure 8: UFQFPN, 3x3 mm, 16 L package outline



1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. The location of the terminal no.1 identifier is within the hatched area.
3. Coplanarity applies to the terminals and all other bottom surface metalization.

Table 9: UFQFPN, 3x3 mm, 16 L mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b (1)	0.18	0.25	0.30	0.007	0.010	0.012
D	3.00 BSC			0.118 BSC		
E	3.00 BSC			0.118 BSC		
e	0.5			0.020		
L	0.30	0.40	0.50	0.012	0.016	0.020
aaa			0.05			0.002
bbb			0.10			0.004
ccc			0.05			0.002
ddd			0.05			0.002
eee			0.05			0.002
N (2)	16			0.630		
ND (3)	4			0.157		
NE (3)	4			0.157		

Notes:

(1)Dimension b applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.

(2)N is the total number of terminals.

(3)ND and NE refer to the number of terminals on the D and E side respectively.

9 Revision history

Table 10: Document revision history

Date	Revision	Changes
13-Dec-2016	1	Initial release
10-Feb-2017	2	Typo corrections

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved