MP5034

USB Charging Port Controller Integrating QC 3.0 Protocol

The Future of Analog IC Technology

DESCRIPTION

The MP5034 supports DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick-charge specification (QC 3.0) without the need for outside user interaction.

Full protection features include input over-voltage protection (OVP) and thermal shutdown.

The MP5034 requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MP5034 is available in an 8-pin TSOT23 package.

FEATURES

- Wide 3.6V to 14V Operating Input Voltage Range
- Supports QC 3.0 (3.6V - 12Vbus with 1% Accuracy) and DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- Input Discharge during High Voltage to Low Voltage Change
- Compatible with Buck, Boost, and AC/DC Converters
- Available in a TSOT23-8 Package

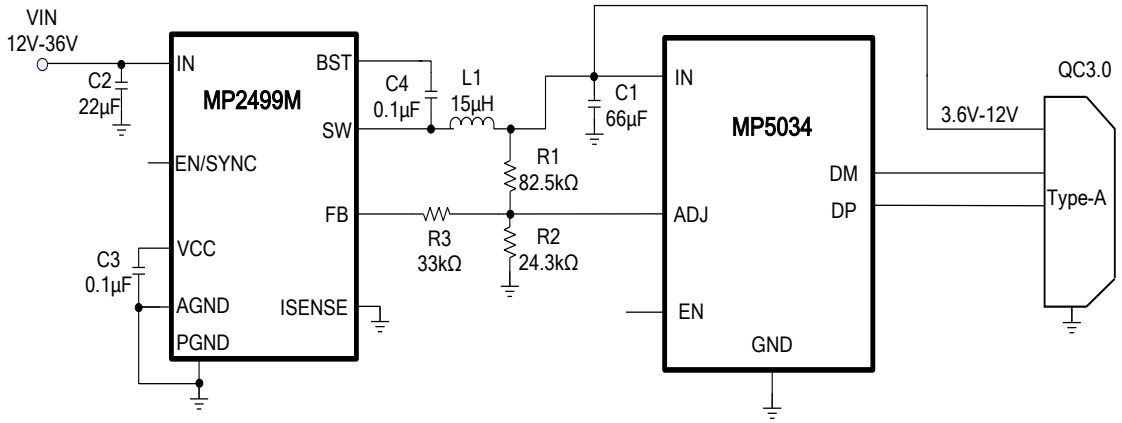
APPLICATIONS

- USB Charger Controller
- AC/DC Wall Adapter with USB Ports
- Power Bank Controller

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TYPICAL APPLICATION

Note: Set MP2499M original output to 3.5V by R1 and R2.



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5034GJ	TSOT23-8	*See Below*

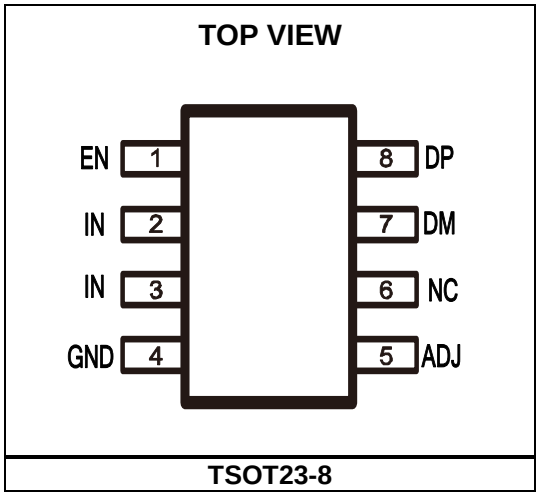
* For Tape & Reel, add suffix –Z (e.g.MP5034GJ-Z)

TOP MARKING

|AYQY

AYQ: Product code of MP5034GJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +16V
All other pins..... -0.3V to +6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2)(5)
..... 1.89W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.6V to 14V (4)
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance

TSOT23-8	***θ_{JA}***	***θ_{JC}***	
EV5034-J-00A (5)	66	23	°C/W
JESD51-7 (6)	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section.
5) Measured on EV5034-J-00A, 2-layer PCB, 58mmx32mm, 2Oz copper.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}	ADJ starts to work	2.7	3.0	3.3	V
UVLO hysteresis	$V_{UVLOHYS}$			880		mV
EN rising threshold	V_{EN_R}		1.17	1.21	1.25	V
EN hysteresis	V_{EN_HYS}			200		mV
EN auto pull-up current	I_{EN_UP}		7	11.5	16	µA
Shutdown current	I_{Q_STD}	EN = 0, V_{IN} = 5V		280		µA
Supply current	I_Q	V_{IN} = 5V, no load		250	320	µA
Voltage Control						
Default V_{IN} voltage	V_{IN_Def1}	I_{OUT} = 0A, T_J = 25°C	5.05	5.10	5.15	V
	V_{IN_Def2}	I_{OUT} = 0A, T_J = -40°C to 125°C	5	5.10	5.2	V
9V_{IN} voltage	V_{IN_9}		8.82	9	9.18	V
12V_{IN} voltage	V_{IN_12}		11.76	12	12.24	V
V_{ADJ} sink current capability		V_{ADJ} = 0.8V	500			µA
Protection						
V_{IN} OVP threshold	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
		V_{IN} rising edge, V_{IN} = 9V	110	115	120	
		V_{IN} rising edge, V_{IN} = 12V	110	115	120	
V_{IN} OVP recovery threshold	$V_{OV_Recovery}$	Reset mode to 5V default	5.35	5.5	5.65	V
Shutdown temperature (8)	T_{STD}			160		°C
Hysteresis (8)	T_{HYS}			35		°C
BC 1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA			50	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM_1.2V}$		200	300	400	kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = 5V	2.5	2.7	2.85	V
DP/DM output impendence	$R_{DP/DM}$		18	22	28	kΩ
Quick Charge 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.25	0.3	0.4	V
DP/DM high voltage	V_{QC_High}		1.8	2	2.2	V
DP output impendence	R_{DP_QC}		250	400	450	kΩ
DM output impendence	R_{DM_QC}		15	20	25	kΩ
DM low glitch time (8)	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		1000		1500	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bus voltage change glitch time	$T_{Glitch_V_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS_CONT_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V [8]	T_{V_UNPLUG}				500	ms

NOTES:

7) Guaranteed by over-temperature correlation, not tested in production.
8) Guaranteed by engineering sample characterization.

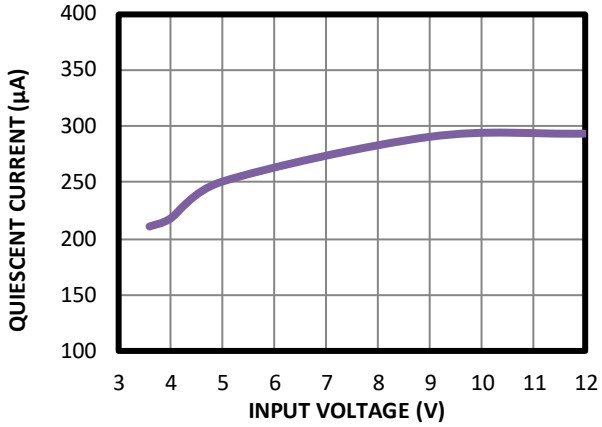
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TYPICAL CHARACTERISTICS

V_{IN_MP5034} = 5V, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

EN floating



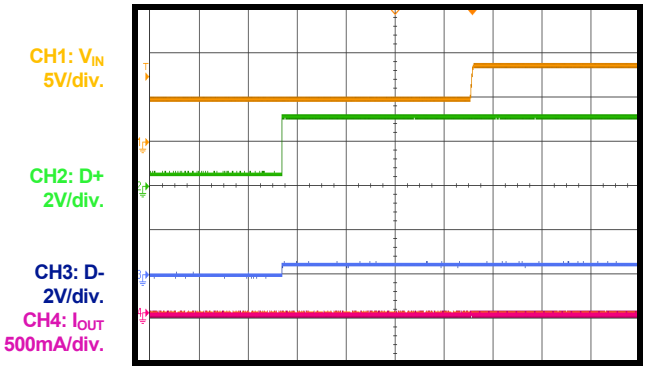
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TYPICAL CHARACTERISTICS *(continued)*

V_{IN_MP5034} = 5V, T_A = 25°C, unless otherwise noted.

MODE Transition from 5V to 9V

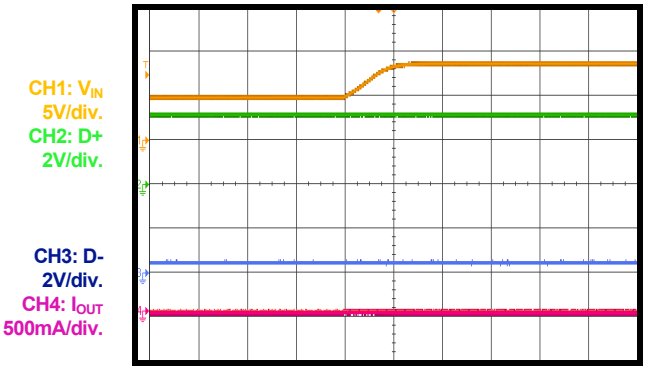
I_{OUT} = 0A, from QC 2.0_5V to 9V



10ms/div.

MODE Transition from 5V to 9V

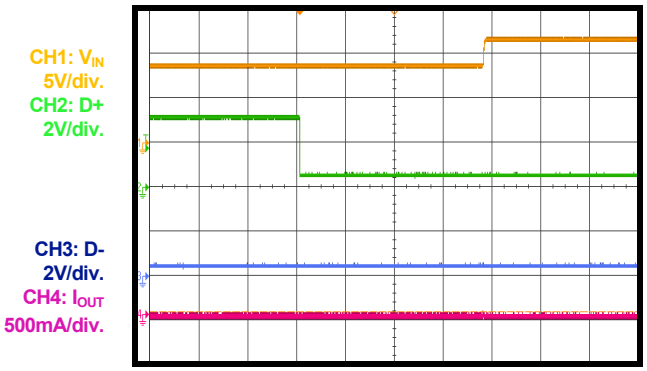
Zoom in 5V to 9V slew rate



500µs/div.

MODE Transition from 9V to 12V

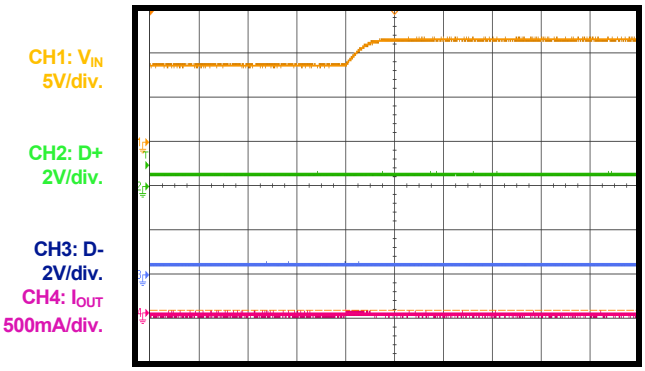
I_{OUT} = 0A, from QC 2.0_9V to 12V



10ms/div.

MODE Transition from 9V to 12V

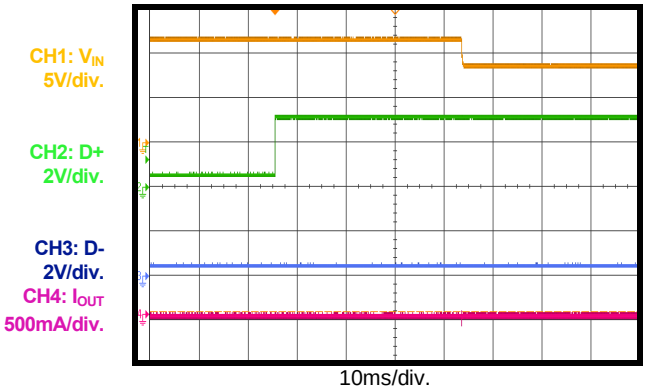
Zoom in 9V to 12V slew rate



500µs/div.

MODE Transition from 12V to 9V

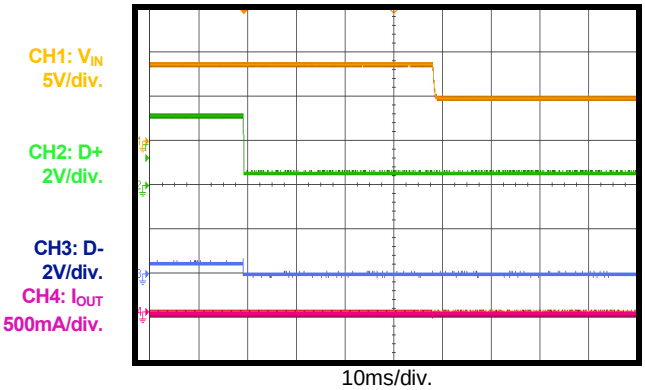
I_{OUT} = 0A, from QC 2.0_12V to 9V



10ms/div.

MODE Transition from 9V to 5V

I_{OUT} = 0A, from QC 2.0_9V to 5V



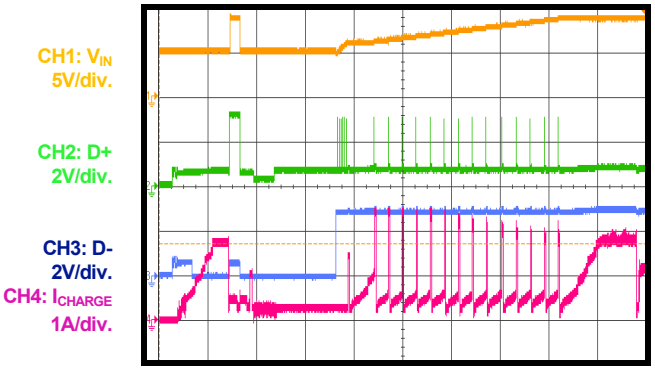
10ms/div.

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TYPICAL CHARACTERISTICS *(continued)*

V_{IN_MP5034} = 5V, T_A = 25°C, unless otherwise noted.

QC 3.0 Device Charging Test



2s/div.

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PIN FUNCTIONS

Package Pin #	Name	Description
1	EN	**Enable control.** EN has an internal auto pull-up current to 5V. Float EN or apply a logic high voltage to EN to enable the IC. Pull EN to logic low to disable the IC.
2, 3	IN	**Supply voltage.** The two input voltage pins must be connected together on the PCB.
4	GND	**Ground.**
5	ADJ	**Input voltage adjustment.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage.
6	NC	**No connection.** Connect NC to ground during application in the PCB layout. Do not connect NC to any other >500mV pin.
7	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
8	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.

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BLOCK DIAGRAM

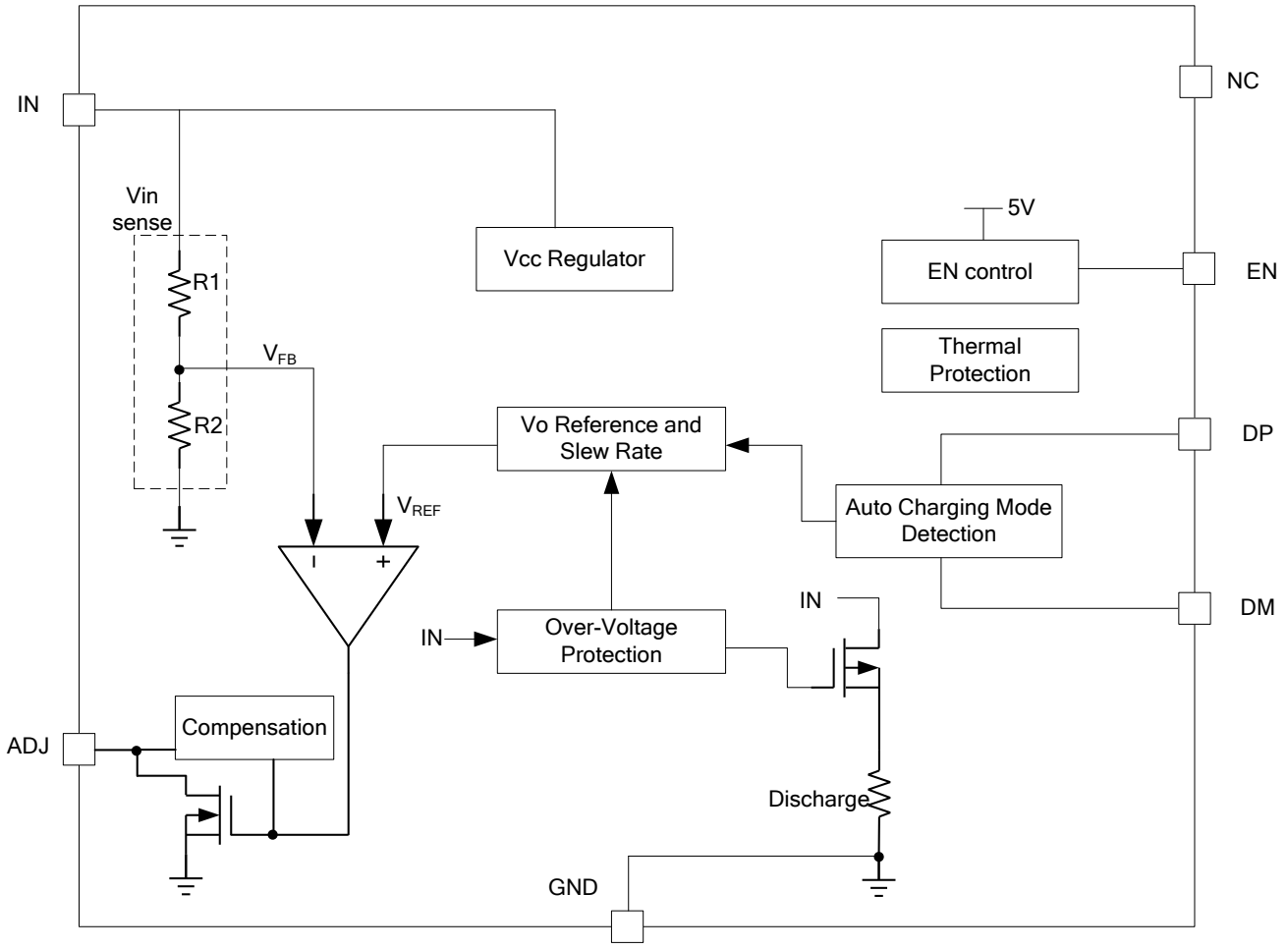


Figure 1: Functional Block Diagram

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OPERATION

The MP5034 supports the latest quick-charge specification (QC 3.0) and is back-compatible with QC 2.0, DCP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for outside user interaction.

Fault condition protection includes input over-voltage protection (OVP) and thermal shutdown.

Operation Supply Voltage

The MP5034's input voltage threshold is around 3V. When V_{IN} is higher than the threshold, MP5034's ADJ block begins working, which sinks a current to adjust the upstream regulator's output to an accurate 5.1V.

QC Mode Voltage Transition - Class A

If the downstream device of the MP5034 supports QC specification, the device can require a higher USB bus voltage than 5V by DM and DP communication. If a higher bus voltage is required, ADJ must be used. ADJ is connected to the feedback pin (FB) of an upstream voltage converter, typically. After the handshake, the MP5034 sinks a controlled current gradually via ADJ to adjust the V_{BUS} value to 9V, 12V, or another voltage (200mV step-by-step). Because of smart controller mode, only one ADJ pin can set a different high voltage, which meets the QC specification. The bus voltage transition is smooth and has no undershoot/overshoot (see Figure 2 and Table 1).

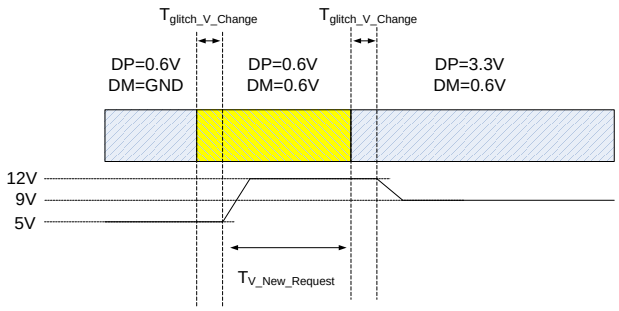


Figure 2: QC Mode Transition

Table 1: QC Mode Definition

Portable Device		USB Bus Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V - 12V, 200mV step according to QC3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, the bus voltage returns to the default 5V automatically. The input-to-ground discharge resistor helps quicken this procedure.

Input Voltage Adjust

In no-load condition, if the input voltage is lower than 5.1V (typical), ADJ sinks a current to regulate the upstream regulator's output voltage to 5.1V. If the input voltage is higher than 5.1V, the MP5034 stops regulating the input voltage.

Figure 3 shows the typical ADJ usage. The ADJ sink current capability is 500μA. The feedback current through R1 must be less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{V_{OUT}(V) - V_{FB}(V)}{0.5} \quad (1)$$

Where V_{OUT} is the maximum output voltage that can be adjusted to.

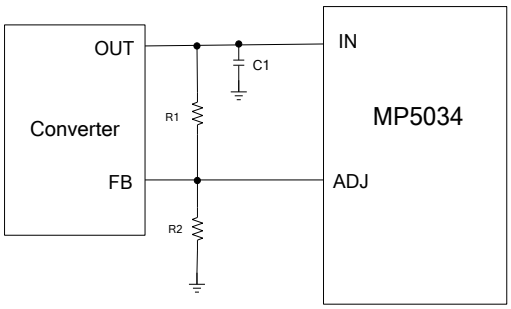


Figure 3: ADJ Configure

Input Over-Voltage Protection (OVP) and Discharge

To protect the downstream device over-voltage, the MP5034 provides an input OVP discharge function. Because the MP5034 supports the QC 3.0 protocol, it has a dynamic OVP threshold.

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An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the input-to-ground discharge path is active. When the input voltage falls below 5.5V (typical), the MP5034 exits OVP mode.

The input-to-ground discharge resistance is always active during the high-to-low voltage mode change period. The discharge path is turned off when FB becomes less than 108% * V_{REF} with 20ms of additional delay (see Figure 4).

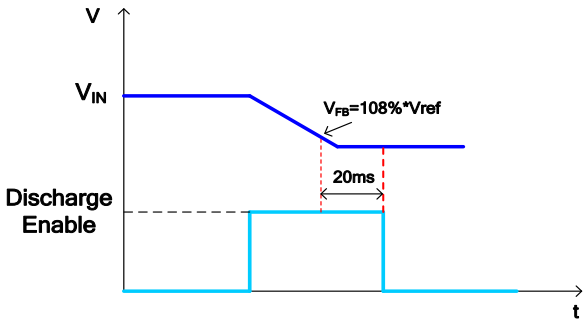


Figure 4: Input Discharge during the High Voltage to Low Voltage Transition

Auto Detection

The MP5034 integrates a USB-dedicated charging port auto-detect function, which recognizes most mainstream portable devices. The MP5034 supports the following charging schemes:

- USB battery charging specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Qualcomm quick-charge mode 3.0 and 2.0

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

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APPLICATION INFORMATION

Selecting Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications. When selecting the input capacitor, also consider the pre-stage converter stability. The input capacitor of the MP5034 is the output capacitor of the converter. Ensure that the converter is stable with additional output capacitors.

Selecting V_{ADJ} Resistor

ADJ has an internal, controlled, current sink. A QC mode transition can be achieved through ADJ. The ADJ sink current capability is 500µA. For the pre-side converter, it is recommended to use a kΩ-level feedback resistor. Limit the current through the high-side feedback resistor below 500µA (see Figure 5).

There is another V_{ADJ} configuration value to limit the maximum output voltage and insert a resistor (R3) between FB and ADJ. With R3, the maximum output voltage can be limited with Equation (3):

$$V_{OUT_MAX}(V) = \frac{R_1 + R_2 // R_3}{R_2 // R_3} \times V_{FB}(V) \quad (3)$$

The required feedback resistor value of R1 must be greater than 30kΩ.

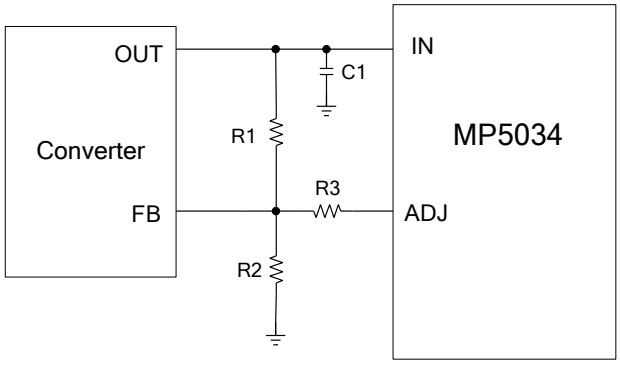


Figure 5: V_{ADJ} Set Maximum V_{OUT}

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 6 and follow the guidelines below.

1. Use short, direct, and wide traces to connect the IC's IN pin.
2. Keep the ADJ trace to the upstream converter FB pin as short as possible and routed far from the switching node to prevent noise injection.

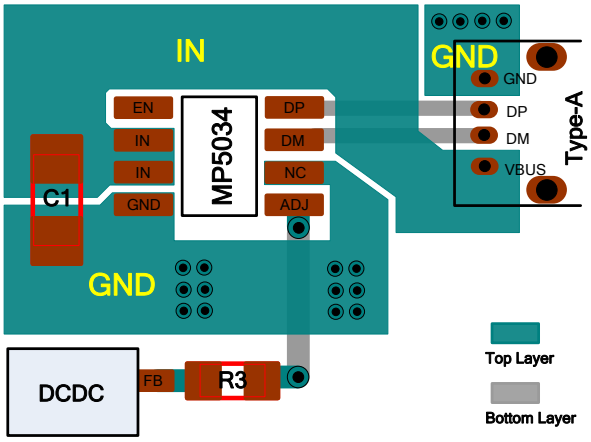


Figure 6: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the given specifications.

Table 3: Design Example

V_{IN} (V)	3.6 - 12
Current (A)	3

The detailed application schematic is shown in Figure 7 through Figure 9. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

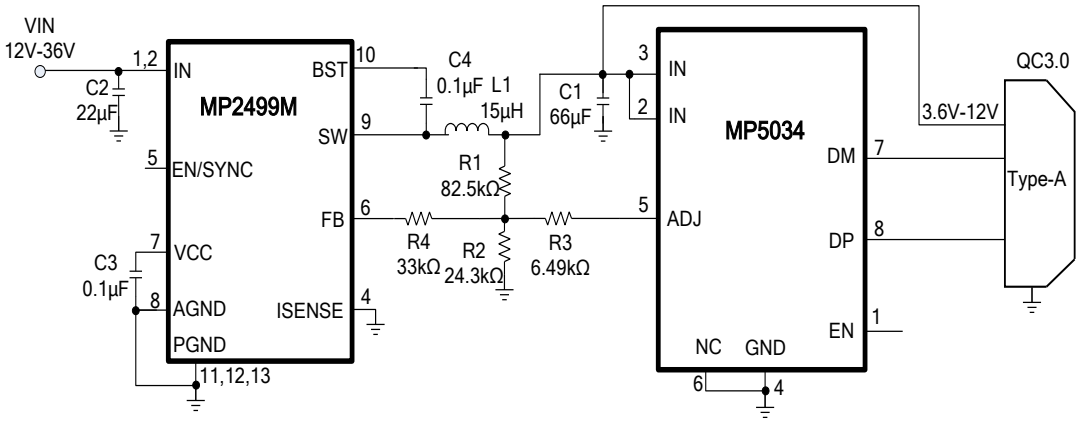


Figure 7: MP5034 + MP2499M for CLA Car Charger

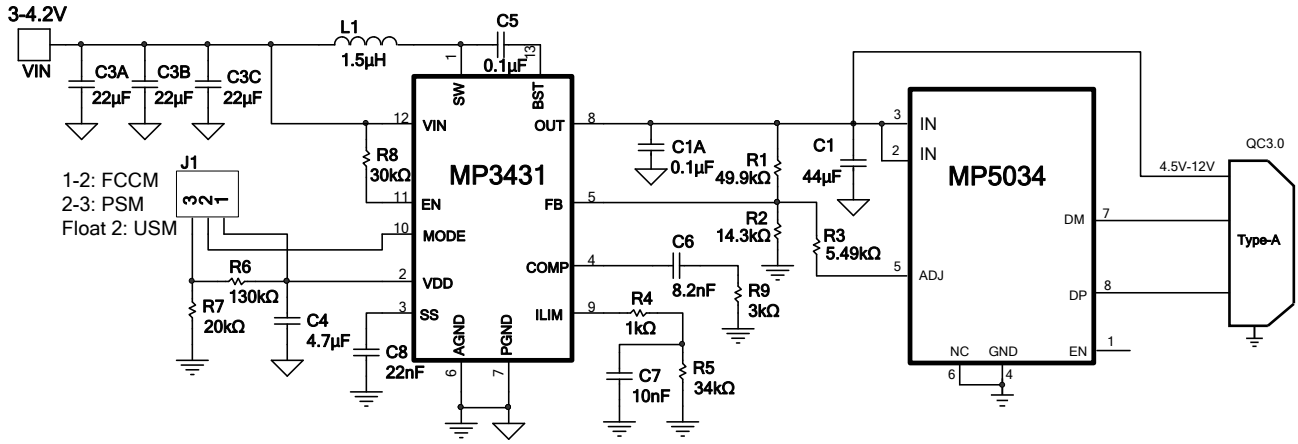


Figure 8: MP5034 + MP3431 for Power Bank

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TYPICAL APPLICATION CIRCUITS *(continued)*

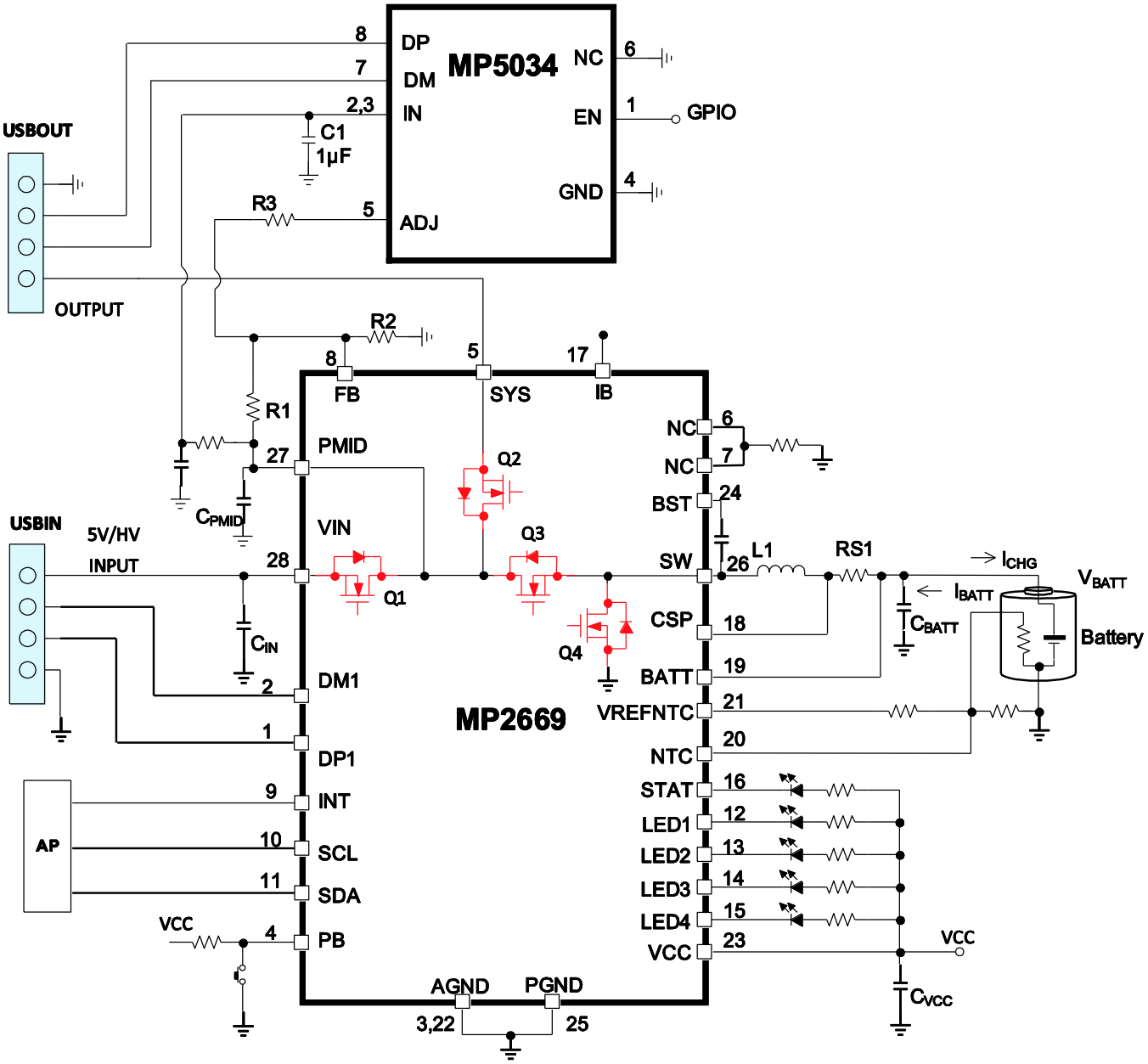
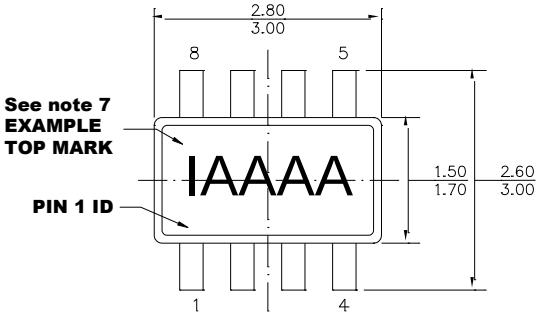


Figure 9: MP5034 + MP2669 for Power Bank

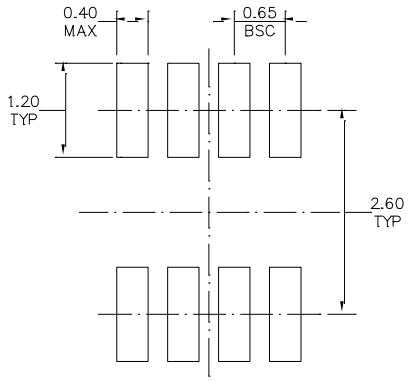
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PACKAGE INFORMATION

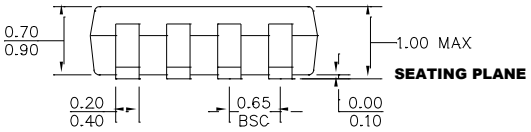
TSOT23-8



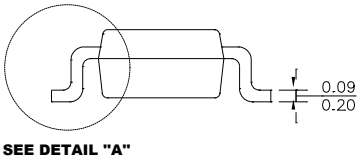
TOP VIEW



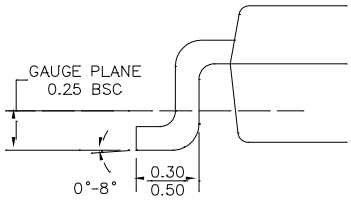
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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