16 Input, 16 Output Analog I/O Port with Integrated Amplifiers

AD5590

FEATURES

Input channels
- 12-bit successive approximation ADC
- 16 inputs with sequencer
- Fast throughput rate: 1 MSPS
- Wide input bandwidth: 70 dB SNR at f_{IN} = 50 kHz

Output channels
- 16 outputs with 12-bit DACs
- On-chip 2.5 V reference
- Hardware $\overline{LDAC}$ and $\overline{LDAC}$ override function
- $\overline{CLR}$ function to programmable code
- Rail-to-rail operation

Operational amplifiers

Offset voltage: 2.2 mV maximum

Low input bias current: 1 pA maximum

Single supply operation

Low noise: 22 nV/√Hz

Unity gain stable

Flexible serial interface
- SPI-/QSPI-/MICROWIRE-/DSP-compatible

−40°C to +85°C operation

Available in 80-ball CSP_BGA package

APPLICATIONS

Optical line cards

Base stations

General-purpose analog I/O

Monitoring and control

FUNCTIONAL BLOCK DIAGRAM

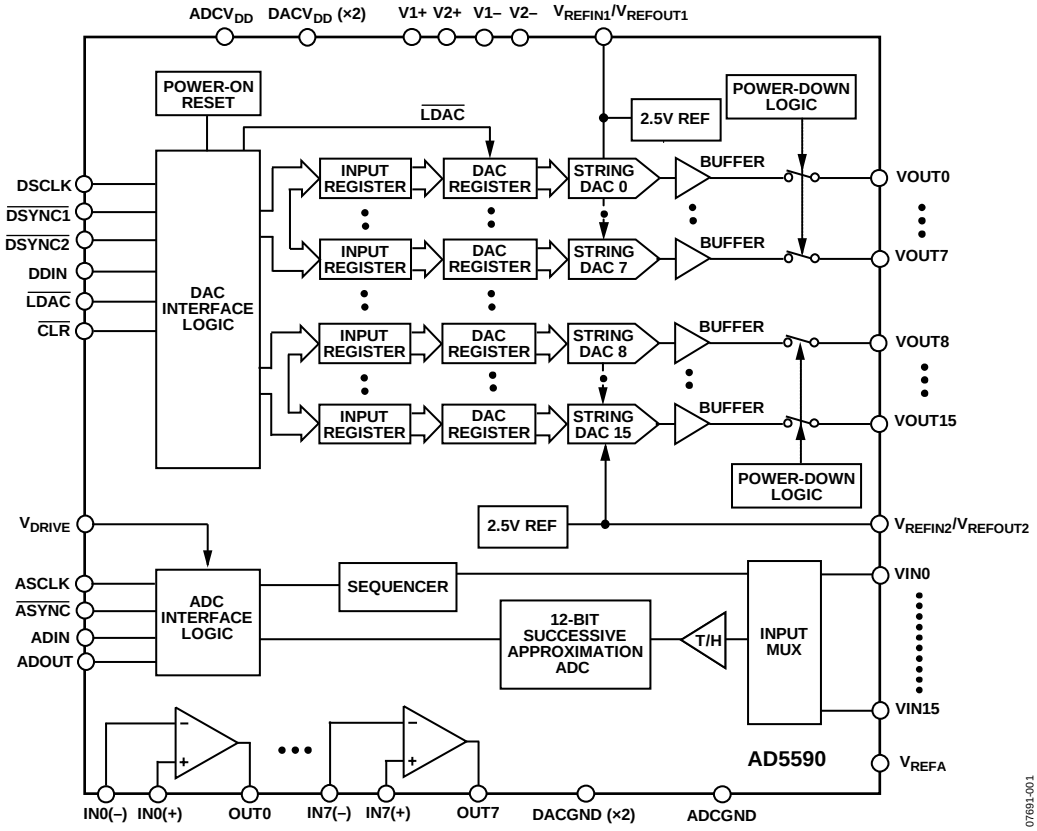


Figure 1.

Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

Fax: 781.461.3113 ©2008–2011 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
Revision History ... 2
General Description ... 3
Specifications ... 4
ADC Specifications ... 4
DAC Specifications ... 6
Operational Amplifier Specifications ... 8
Timing Specifications ... 9
Absolute Maximum Ratings ... 11
Thermal Resistance ... 11
ESD Caution ... 11
Pin Configuration and Function Descriptions ... 12
Typical Performance Characteristics ... 14
DAC ... 14
ADC ... 18
Amplifier ... 19
Terminology ... 23
Theory of Operation ... 26
DAC Section ... 26
ADC Section ... 27
ADC Converter Operation ... 27
Amplifier Section ... 29
Serial Interface ... 30
Accessing the DAC Block ... 30
Accessing the ADC Block ... 34
Outline Dimensions ... 42
Ordering Guide ... 42

REVISION HISTORY

7/11—Rev. 0 to Rev. A

Changes to Features Section and Figure 1 ... 1
Changes to VOUT10 Pin Number in Table 10 ... 13

10/08—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5590 is a 16-channel input and 16-channel output analog I/O port with eight uncommitted amplifiers, operating from a single 4.5 V to 5.25 V supply. The AD5590 comprises 16 input channels multiplexed into a 1 MSPS, 12-bit successive approximation ADC with a sequencer to allow a preprogrammed selection of channels to be converted sequentially. The ADC contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{\text{ASYNC}}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{ASYNC}}$ and conversion is also initiated at this point. There are no pipeline delays associated with the ADC. By setting the relevant bits in the control register, the analog input range for the ADC can be selected to be a 0 V to V_{REFA} input or a 0 V to $2 \times V_{REFA}$ with either straight binary or twos complement output coding. The conversion time is determined by the ASCLK frequency because it is also used as the master clock to control the conversion.

The DAC section of the AD5590 comprises sixteen 12-bit DACs divided into two groups of eight. Each group has an on-chip reference. The on-board references are off at power-up, allowing the use of external references. The internal references are enabled via a software write.

The AD5590 incorporates a power-on reset circuit that ensures that the DAC outputs power up to 0 V and remain powered up at this level until a valid write takes place. The DAC contains a power-down feature that reduces the current consumption of the device and provides software-selectable output loads while in power-down mode for any or all DAC channels. The outputs of all DACs can be updated simultaneously using the $\overline{\text{LDAC}}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{\text{CLR}}$ that updates all DACs to a user-programmable code: zero scale, midscale, or full scale.

The AD5590 contains eight low noise, single-supply amplifiers. These amplifiers can be used for signal conditioning for the ADCs, DACs, or other independent circuitry, if required.

SPECIFICATIONS

ADC SPECIFICATIONS

$ADCV_{DD}$ = V_{DRIVE} = 2.7 V to 5.25 V_{REFA} = 2.5 V, f_{SCLK}[1] = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[2]
DYNAMIC PERFORMANCE					f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[3]	68.5	70		dB	@ 5 V
		70.5		dB	@ 3 V
Signal-to-Noise Ratio (SNR)[3]	69	70		dB	@ 5 V
		70.5		dB	@ 3 V
Total Harmonic Distortion (THD)[3]	−74	−82		dB	@ 5 V
		−82		dB	@ 3 V
Peak Harmonic or Spurious Noise (SFDR)[3]	−75	−86		dB	@ 5 V
		−80		dB	@ 3 V
Intermodulation Distortion (IMD)[3, 4]					fa = 40.1 kHz, fb = 41.5 kHz
Second-Order Terms		−85		dB	
Third-Order Terms		−85		dB	
Aperture Delay[4]		10		ns	
Aperture Jitter[4]		50		ps	
Channel-to-Channel Isolation[3, 4]		−82		dB	f_{IN} = 400 kHz
Full Power Bandwidth[4]		8.2		MHz	@ 3 dB
		1.6		MHz	@ 0.1 dB
DC ACCURACY[3]					
Resolution		12		Bits	
Integral Nonlinearity	−1		+1	LSB	
Differential Nonlinearity	−1		+1.5	LSB	Guaranteed no missing codes to 12 bits
0 V to V_{REFA} Input Range					Straight binary output coding
Offset Error	−10	±0.6	+10	LSB	
Offset Error Match			3.5	LSB	
Gain Error	−2		+2	LSB	
Gain Error Match	−0.8		+0.8	LSB	
0 V to 2 × V_{REFA} Input Range					−V_{REFA} to +V_{REFA} biased about V_{REFA} with twos complement output coding offset
Positive Gain Error	−2		+2	LSB	
Positive Gain Error Match	−0.8		+0.8	LSB	
Zero-Code Error	−8	±0.6	+8	LSB	
Zero-Code Error Match			2	LSB	
Negative Gain Error	−1		+1	LSB	
Negative Gain Error Match	−0.8		+0.8	LSB	
ANALOG INPUT					
Input Voltage Ranges		0 to V_{REFA}		V	Range bit set to 1
		0 to 2 × V_{REFA}		V	Range bit set to 0, $ADCV_{DD}/V_{DRIVE}$ = 4.75 V to 5.25 V for 0 V to 2 × V_{REFAS}
DC Leakage Current	−1		+1	µA	
Input Capacitance[4]		20		pF	
REFERENCE INPUT					
V_{REFA} Input Voltage		2.5		V	±1% specified performance
DC Leakage Current	−1		+1	µA	
V_{REFA} Input Impedance[4]		36		kΩ	f_{SAMPLE} = 1 MSPS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[2]
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage, V_{INL}			$0.3 \times V_{DRIVE}$	V	
Input Current, I_{IN}	−1		+1	µA	Typically 10 nA
Input Capacitance, C_{IN}[1, 4]			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$			V	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating State Leakage Current		±10		µA	weak/$\overline{TRI}$ bit set to 0
Floating State Output Capacitance[4]		10		pF	weak/$\overline{TRI}$ bit set to 0
Output Coding		Straight (Natural) Binary			coding bit set to 1
		Twos Complement			coding bit set to 0
CONVERSION RATE[4]					
Conversion Time			800	ns	16 ASCLK cycles, ASCLK = 20 MHz
Track-and-Hold Acquisition Time[3]			300	ns	Sine wave input
			300	ns	Full-scale step input
Throughput Rate			1	MSPS	@ 5 V (see the Serial Interface section)
POWER REQUIREMENTS					
$ADCV_{DD}$	2.7		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{DRIVE}			0.15	µA	
I_{DD}[5]					Digital inputs = 0 V or V_{DRIVE}
Normal Mode, Static		750		µA	V_{DD} = 4.75 V to 5.25 V, ASCLK on or off
Normal Mode, Operational (f_S = Maximum Throughput)			2.5	mA	V_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
Autostandby Mode		1.55		mA	f_{SAMPLE} = 500 kSPS
			100	µA	Static
Autoshutdown Mode		960		µA	f_{SAMPLE} = 250 kSPS
			0.5	µA	Static
Full Shutdown Mode		0.02	0.5	µA	ASCLK on or off
Power Dissipation					
Normal Mode, Operational			12.5	mW	$ADCV_{DD}$ = 5 V, f_{SCLK} = 20 MHz
Autostandby Mode, Static			500	µW	$ADCV_{DD}$ = 5 V
Autoshutdown Mode, Static			2.5	µW	$ADCV_{DD}$ = 5 V
Full Shutdown Mode			2.5	µW	$ADCV_{DD}$ = 5 V

[1] Specifications apply for f_{SCLK} up to 20 MHz. For serial interfacing requirements, see the Timing Specifications section.
[2] Temperature range: −40°C to +85°C.
[3] See the Terminology section.
[4] Guaranteed by design and characterization. Not production tested.
[5] See the ADC Power vs. Throughput Rate section.

DAC SPECIFICATIONS

$DACV_{DD}$ = 4.5 V to 5.25 V, R_L = 2 kΩ to DACGND, C_L = 200 pF to DACGND, V_{REFIN1} = V_{REFIN1} = $DACV_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions/Comments[1]
STATIC PERFORMANCE[2]					
Resolution	12			Bits	
Integrated Nonlinearity (INL)	−3	±0.5	+3	LSB	See Figure 6
Differential Nonlinearity (DNL)	−0.25		+0.25	LSB	Guaranteed monotonic by design; see Figure 7
Zero-Code Error		1	12	mV	All 0s loaded to DAC register; see Figure 11
Zero-Code Error Drift[3]		±2		µV/°C	
Full-Scale Error	−1	−0.2		% FSR	All 1s loaded to DAC register
Gain Error	−1		+1	% FSR	
Gain Temperature Coefficient[3]		±2.5		ppm	Of FSR/°C
Offset Error	−11	±5	+11	mV	
DC Power Supply Rejection Ratio[3]		−80		dB	$DACV_{DD}$ ± 10%
DC Crosstalk[3]					
External Reference		10		µV	Due to full-scale output change, R_L = 2 kΩ to DACGND or $DACV_{DD}$
		5		µV/mA	Due to load current change
		10		µV	Due to powering down (per channel)
Internal Reference		25		µV	Due to full-scale output change, R_L = 2 kΩ to DACGND or $DACV_{DD}$
		10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		$DACV_{DD}$	V	
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
DC Output Impedance		0.5		Ω	
Short-Circuit Current		30		mA	$DACV_{DD}$ = 5 V
Power-Up Time		4		µs	Coming out of power-down mode, $DACV_{DD}$ = 5 V
REFERENCE INPUTS					
Reference Current		40	50	µA	V_{REFINx} = $DACV_{DD}$ = 5.5 V (per DAC channel)
Reference Input Range	0		$DACV_{DD}$	V	
Reference Input Impedance[3]		14.6		kΩ	
REFERENCE OUTPUT					
Output Voltage	2.495		2.505	V	At ambient
Reference Temperature Coefficient[3]		±10		ppm/°C	
Reference Output Impedance[3]		7.5		kΩ	
LOGIC INPUTS					
Input Current	−3		+3	µA	All digital inputs
Input Low Voltage, V_{INL}			0.8	V	$DACV_{DD}$ = 5 V
Input High Voltage, V_{INH}	2			V	$DACV_{DD}$ = 5 V
Pin Capacitance[3]		5		pF	

Parameter	Min	Typ	Max	Unit	Conditions/Comments[1]
POWER REQUIREMENTS					
$DACV_{DD}$	4.5		5.5	V	All digital inputs at 0 or $DACV_{DD}$, DAC active, excludes load current
I_{DD} (Normal Mode)[4]					V_{IH} = $DACV_{DD}$ = 4.5 V to 5.5 V, V_{IL} = DACGND
		2.6	3.2	mA	Internal reference off
		4	5	mA	Internal reference on
$DACI_{DD}$ (All Power-Down Modes)[5]					
$DACV_{DD}$		0.8	2	µA	V_{IH} = $DACV_{DD}$ = 4.5 V to 5.5 V, V_{IL} = DACGND

[1] Temperature range is −40°C to +85°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of Code 32 to Code 4064. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All sixteen DACs powered down.

DAC AC Characteristics

$DACV_{DD}$ = 4.5 V to 5.25 V, R_L = 2 kΩ to DACGND, C_L = 200 pF to DACGND, V_{REFIN1} = V_{REFIN1} = $DACV_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		6	10	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-sec	1 LSB change around major carry (see Figure 17)
Digital Feedthrough		0.1		nV-sec	
Reference Feedthrough		−90		dB	V_{REFIN1} = V_{REFIN2} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
Digital Crosstalk		0.5		nV-sec	
Analog Crosstalk		2.5		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		340		kHz	V_{REFIN1} = V_{REFIN2} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REFIN1} = V_{REFIN2} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC Code = 0x8400, 1 kHz
		100		nV/√Hz	DAC Code = 0x8400, 10 kHz
Output Noise		15		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +85°C, typical at 25°C.

OPERATIONAL AMPLIFIER SPECIFICATIONS

Electrical characteristics @ V_{SY} = 5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		0.4	2.2	mV	−0.3 V < V_{CM} < +5.3 V
				2.2	mV	−40°C < T_A < +85°C, −0.3 V < V_{CM} < +5.2 V
Offset Voltage Drift[1]	$\Delta V_{OS}/\Delta T$		1	4.5	µV/°C	−40°C < T_A < +85°C
Input Bias Current[1]	I_B		0.2	1	pA	
				110	pA	−40°C < T_A < +85°C
Input Offset Current[1]	I_{OS}		0.1	0.5	pA	
				50	pA	−40°C < T_A < +85°C
Common-Mode Rejection Ratio	CMRR		95		dB	0 V < V_{CM} < 5 V
		68			dB	−40°C < T_A < +85°C
Large Signal Voltage Gain	A_{VO}	235	400		V/mV	R_L = 10 kΩ, 0.5 V < V_{OUT} < 4.5 V
Input Capacitance[1]	C_{DIFF}		2		pF	
	C_{CM}		7		pF	
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	4.95	4.98		V	I_L = 1 mA
		4.9			V	−40°C to +85°C
			4.7		V	I_L = 10 mA
		4.50			V	−40°C to +85°C
Output Voltage Low	V_{OL}		20	30	mV	I_L = 1 mA
				50	mV	−40°C to +85°C
			190	275	mV	I_L = 10 mA
				335	mV	−40°C to +85°C
Short-Circuit Current[1]	I_{SC}		±80		mA	
Closed-Loop Output Impedance[1]	Z_{OUT}		15		Ω	f = 10 kHz, A_V = 1
POWER SUPPLY						
Power Supply Span (V+ to V−)			5		V	
Power Supply Rejection Ratio	PSRR	67	94		dB	1.8 V < V_{SY} < 5 V
		64			dB	−40°C < T_A < +85°C
Supply Current per Amplifier	I_{SY}		38		µA	V_{OUT} = V_{SY}/2
			50	60	µA	−40°C <T_A < +85°C
DYNAMIC PERFORMANCE[1]						
Slew Rate	SR		0.1		V/µs	R_L = 10 kΩ
Settling Time 0.1%	t_S		23		µs	G = ±1, 2 V step, C_L = 20 pF, R_L = 1 kΩ
Gain Bandwidth Product	GBP		400		kHz	R_L = 100 kΩ
			350		kHz	R_L = 10 kΩ
Phase Margin	$Ø_O$		70		Degrees	R_L = 10 kΩ, R_L = 100 kΩ, C_L = 20 pF
NOISE PERFORMANCE[1]						
Peak-to-Peak Noise			2.3	3.5	µV	
Voltage Noise Density	e_n		25		nV/√Hz	f = 1 kHz
			22		nV/√Hz	f = 10 kHz
Current Noise Density	i_n		0.05		pA/√Hz	f = 1 kHz

[1] Guaranteed by design and characterization. Not production tested.

TIMING SPECIFICATIONS

ADC Timing Characteristics

$ADCV_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE} \leq ADCV_{DD}$, V_{REFA} = 2.5 V; All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1]	Limit at T_{MIN}, T_{MAX}; $ADCV_{DD}$ = 5 V	Unit	Conditions/Comments
f_{SCLK}[2]	10	kHz min	
	20	MHz min	
$t_{CONVERT}$	16 × t_{ASCLK}	MHz max	
t_{QUIET}	50	ns min	
t_2	10	ns min	$\overline{ASYNC}$ to ASCLK setup time
t_3[3]	14	ns max	Delay from $\overline{ASYNC}$ until ADOUT three-state disabled
t_3b[4]	20	ns min	Data hold time
t_4[3]	40	ns max	Data access time after ASCLK falling edge
t_5	0.4 × t_{ASCLK}	ns min	ASCLK low pulse width
t_6	0.4 × t_{ASCLK}	ns min	ASCLK high pulse width
t_7	15	ns min	ASCLK to ADOUT valid hold time
t_8[5]	15/50	ns min/max	ASCLK falling edge to ADOUT high impedance
t_9	20	ns min	ADIN setup time prior to ASCLK falling edge
t_{10}	5	ns min	ADIN Hold time prior to ASCLK falling edge
t_{11}	20	ns min	16th ASCLK falling edge to $\overline{ASYNC}$ high
t_{12}	1	µs max	Power-up time from full power-down/autoshutdown/ autostandby modes

[1] Guaranteed by design and characterization. Not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of $ADCV_{DD}$) and timed from a voltage level of 1.6 V.

[2] Maximum ASCLK frequency is 50 MHz at $ADCV_{DD}$ = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.

[3] Measured with the load circuit of Figure 3 and defined as the time required for the output to cross 0.4 V or 0.7 × V_{DRIVE}.

[4] t_3b represents a worst-case figure for having ADD3 available on the ADOUT line, that is, if the ADC goes back into three-state at the end of a conversion and some other device takes control of the bus between conversions, the user needs to wait a maximum time of t_3b before having ADD3 valid on the ADOUT line. If the ADOUT line is weakly driven to ADD3 between conversions, then the user typically needs to wait 17 ns at 3 V and 12 ns at 5 V after the $\overline{ASYNC}$ falling edge before seeing ADD3 valid on ADOUT.

[5] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of bus loading.

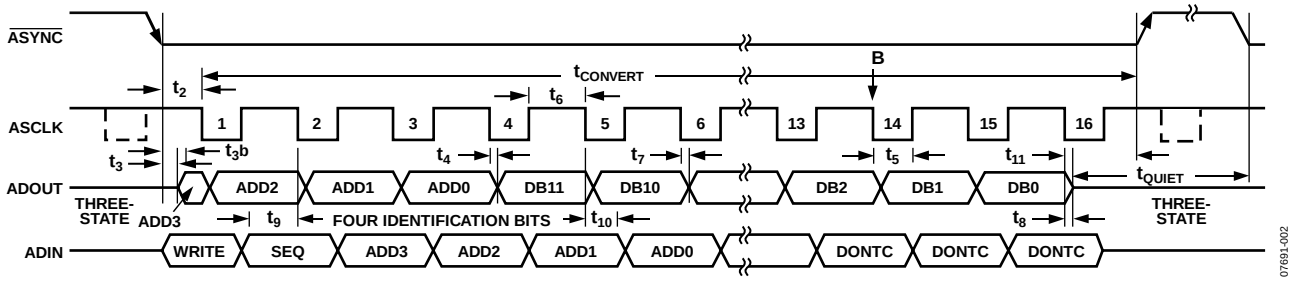


Figure 2. ADC Timing Characteristics

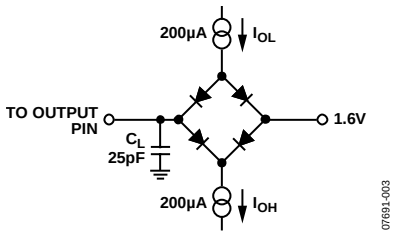


Figure 3. Load Circuit for ADC Digital Output Timing Specifications

DAC Timing Characteristics

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 4. $DACV_{DD}$ = 4.5 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6.

Parameter[1]	Limit at T_{MIN}, T_{MAX}; $DACV_{DD}$ = 2.7 V to 5.5 V	Unit	Conditions/Comments
t_1[2]	20	ns min	DSCLK cycle time
t_2	8	ns min	DSCLK high time
t_3	8	ns min	DSCLK low time
t_4	13	ns min	$\overline{\text{DSYNC}}$ to DSCLK falling edge setup time
t_5	4	ns min	Data setup time
t_6	4	ns min	Data hold time
t_7	0	ns min	DSCLK falling edge to $\overline{\text{DSYNC}}$ rising edge
t_8	15	ns min	Minimum $\overline{\text{DSYNC}}$ high time
t_9	13	ns min	$\overline{\text{DSYNC}}$ rising edge to DSCLK fall ignore
t_{10}	0	ns min	DSCLK falling edge to $\overline{\text{DSYNC}}$ fall ignore
t_{11}	10	ns min	$\overline{\text{LDAC}}$ pulse width low
t_{12}	15	ns min	DSCLK falling edge to $\overline{\text{LDAC}}$ rising edge
t_{13}	5	ns min	$\overline{\text{CLR}}$ pulse width low
t_{14}	0	ns min	DSCLK falling edge to $\overline{\text{LDAC}}$ falling edge
t_{15}	300	ns typ	$\overline{\text{CLR}}$ pulse activation time

[1] Sample tested at 25°C to ensure compliance.
[2] Maximum DSCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.

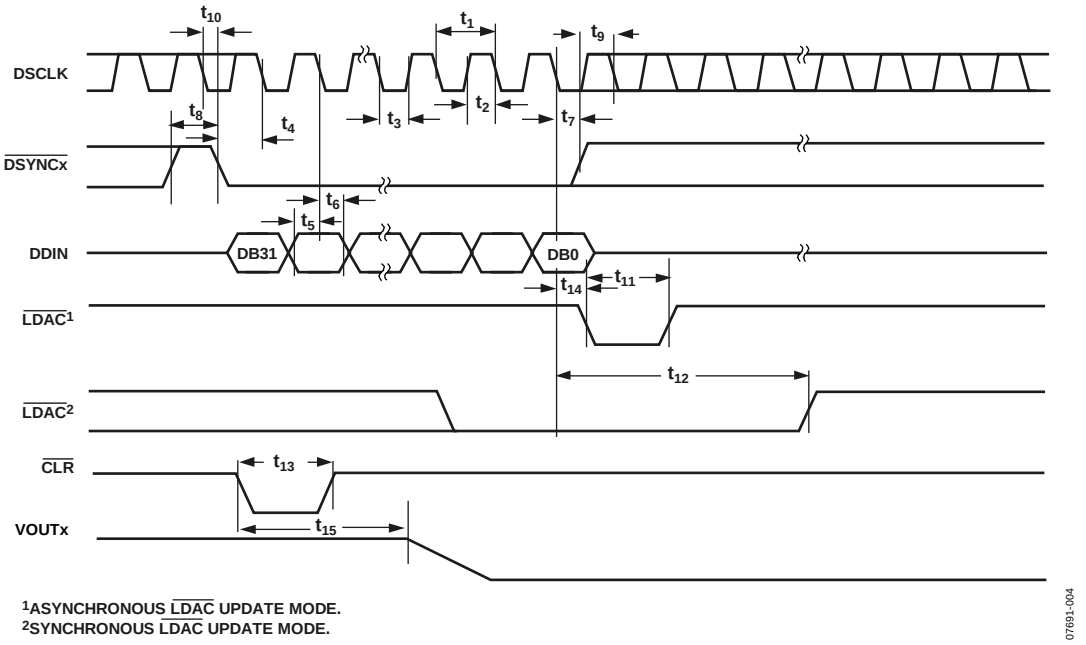


Figure 4. DAC Timing Characteristics

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted. V_{DD} refers to $DACV_{DD}$ or $ADCV_{DD}$. GND refers to DACGND or ADCGND.

Table 7.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to V_{DD} + 0.3 V
Op Amp Supply Voltage	6 V
Op Amp Input Voltage	(V1− or V2−) − 0.3 V to (V1+ or V2+) + 0.3 V
Op Amp Differential Input Voltage	±6 V
Op Amp Output Short-Circuit Duration to GND	Indefinite
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} +0.3 V
V_{REFA} to GND	−0.3 V to V_{DD} +0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} +0.3 V
Input Current to Any ADC Pin Except Supplies	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a 4-layer JEDEC thermal test board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
80-Ball CSP_BGA	40	°C/W

Table 9. Junction Temperature

Parameter	Max	Unit	Comments
Junction Temperature[1, 2]	130	°C	$T_J = T_A + P_{TOTAL} \times \theta_{JA}$

[1] P_{TOTAL} is the sum of ADC, DAC, and operational amplifier supply currents.
[2] θ_{JA} is the package thermal resistance.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

12	11	10	9	8	7	6	5	4	3	2	1	
VOUT14	VOUT10	VOUT8	DACGND	$\overline{\text{LDAC}}$	DDIN	DSCLK	$\overline{\text{DSYNC1}}$	$DACV_{DD}$	VOUT5	VOUT7	VOUT0	A
VIN12	VIN10	VOUT12	VOUT1	$DACV_{DD}$	$\overline{\text{DSYNC2}}$	$\overline{\text{CLR}}$	DACGND	VOUT3	VIN9	VIN8	OUT2	B
OUT7	VOUT9									VOUT2	IN2(+)	C
IN7(–)	VOUT11									VOUT4	IN2(–)	D
IN7(+)	VOUT13									VOUT6	IN3(+)	E
IN6(+)	VOUT15									V_{REFIN1}/ $V_{REFOUT1}$	IN3(–)	F
IN6(–)	V_{REFIN2}/ $V_{REFOUT2}$									VIN5	OUT3	G
V2–	VIN15									V1–	OUT1	H
OUT6	V_{REFA}									VIN7	IN1(–)	J
OUT5	VIN14									VIN6	IN1(+)	K
IN5(–)	VIN11	VIN13	V2+	ADIN	ASCLK	V_{DRIVE}	VIN1	VIN3	VIN2	VIN4	OUT0	L
IN5(+)	IN4(+)	IN4(–)	OUT4	$ADCV_{DD}$	$\overline{\text{ASYNC}}$	ADOUT	ADCGND	VIN0	V1+	IN0(+)	IN0(–)	M

07691-005

Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
M7	$\overline{\text{ASYNC}}$	Frame Synchronization Signal. Active low logic input. This input provides the dual function of initiating ADC conversions and also frames the serial data transfer.
J11	V_{REFA}	Reference Input for the ADC Block. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
M8	$ADCV_{DD}$	Power Supply Input for the ADC Block. The ADC can operate from 4.5 V to 5.25 V, and the supply should be decoupled with a 10 µF in parallel with a 0.1 µF capacitor to ADCGND.
M5	ADCGND	Ground Reference Point for the ADC Block. All ADC analog/digital input/output signals and any external reference signal should be referred to this ADCGND voltage.
M4, L5, L3, L4, L2, G2, K2, J2, B2, B3, B11, L11, B12, L10, K11, H11	VIN0 to VIN15	Analog Input 0 through Analog Input 15. Sixteen single-ended analog input channels that are multiplexed into the on-chip track and hold. The analog input channel to be converted is selected by using the ADD3 through ADD0 address bits of the control register. The address bits in conjunction with the SEQ and shadow bits allow the sequence register to be programmed. The input range for all input channels can extend from 0 V to V_{REFA} or 0 V to 2 × V_{REFA}, as selected via the range bit in the control register. Any unused input channels should be connected to GND to avoid noise pickup.
L8	ADIN	ADC Data In. Logic input. Data to be written to the control register of the ADC is provided on this input and is clocked into the register on the falling edge of ASCLK (see the Accessing the ADC Block section).
M6	ADOUT	Data Out. Logic output. The conversion result from the ADC block is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the ASCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided MSB first. The output coding can be selected as straight binary or twos complement via the coding bit in the control register.

Pin No.	Mnemonic	Description
L7	ASCLK	Serial Clock. Logic input. ASCLK provides the serial clock for accessing data from the ADC block. This clock input is also used as the clock source for the conversion process of the ADC.
L6	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the ADC block operates.
A4, B8	$DACV_{DD}$	Power Supply Input for the DAC Block. The DAC can operate from 4.5 V to 5.25 V, and the supply should be decoupled with a 10 µF in parallel with a 0.1 µF capacitor to DACGND. The two $DACV_{DD}$ pins must be connected together.
A9, B5	DACGND	Ground Reference Point for the DAC Block. All DAC analog/digital input/output signals and any external reference signal should be referred to this DACGND voltage. The two DACGND pins should be connected together.
A8	$\overline{LDAC}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
A5	$\overline{DSYNC1}$	Active Low Control Input. This is the frame synchronization signal for the input data of DAC channels VOUT0 to VOUT7. When $\overline{DSYNC1}$ goes low, it powers on the DSCLK and DDIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{DSYNC1}$ is taken high before the 32nd falling edge, the rising edge of $\overline{DSYNC1}$ acts as an interrupt and the write sequence is ignored by the device.
B7	$\overline{DSYNC2}$	Active Low Control Input. This is the frame synchronization signal for the input data of DAC channels VOUT8 to VOUT15. When $\overline{DSYNC2}$ goes low, it powers on the DSCLK and DDIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{DSYNC2}$ is taken high before the 32nd falling edge, the rising edge of $\overline{DSYNC2}$ acts as an interrupt and the write sequence is ignored by the device.
B6	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{CLR}$ code register—zero scale, midscale, or full scale. Default setting clears the output to 0 V.
A7	DDIN	DAC Data Input. This DAC has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
A6	DSCLK	DAC Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
A1, B9, C2, B4, D2, A3, E2, A2	VOUT0 to VOUT7	Analog Output Voltage from DAC0 to DAC7. $\overline{DSYNC1}$ is the frame synchronization signal for writing data to these DACs. The DAC is updated automatically if $\overline{LDAC}$ is low, or on the falling edge of $\overline{LDAC}$ if it is high. The output amplifiers have rail-to-rail operation.
A10, C11, A11, D11, B10, E11, A12, F11	VOUT8 to VOUT15	Analog Output Voltage from DAC8 to DAC15. $\overline{DSYNC2}$ is the frame synchronization signal for writing data to these DACs. The DAC is updated automatically if $\overline{LDAC}$ is low, or on the falling edge of $\overline{LDAC}$ if it is high. The output amplifiers have rail to rail operation.
F2	V_{REFIN1}/ $V_{REFOUT1}$	Reference Input/Output Pin for DAC0 to DAC7. The DACs have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
G11	V_{REFIN2}/ $V_{REFOUT2}$	Reference Input/Output Pin for DAC8 to DAC15. The DACs have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
M3	V1+	Positive Supply Input for the amplifier 0 to amplifier 3. The supply for these amplifiers is independent of other supplies and can be operated with a different supply if required. The pin should be decoupled to V1− with a 10 µF in parallel with a 0.1 µF capacitor.
H2	V1−	Negative Supply Input for Amplifier 0 to Amplifier 3.
L9	V2+	Positive Supply Input for Amplifier 4 to Amplifier 7. The supply for these amplifiers is independent of other supplies and can be operated with a different supply if required. The pin should be decoupled to V2− with a 10 µF in parallel with a 0.1 µF capacitor.
H12	V2−	Negative Supply Input for Amplifier 4 to Amplifier 7.
M1, J1, D1, F1, M10, L12, G12, D12	IN0(−) to IN7(−)	Inverting Input Terminals for Operational Amplifier 0 to Amplifier 7.
M2, K1, C1, E1, M11, M12, F12, E12	IN0(+) to IN7(+)	Noninverting Input Terminals for Operational Amplifier 0 to Amplifier 7.
L1, H1, B1, G1, M9, K12, J12, C12	OUT0 to OUT7	Output Terminals for Operational Amplifier 0 to Amplifier 7.

TYPICAL PERFORMANCE CHARACTERISTICS

DAC

$DACV_{DD}$ and $ADCV_{DD}$ = 5 V, V_{SY} = 5 V, unless otherwise noted.

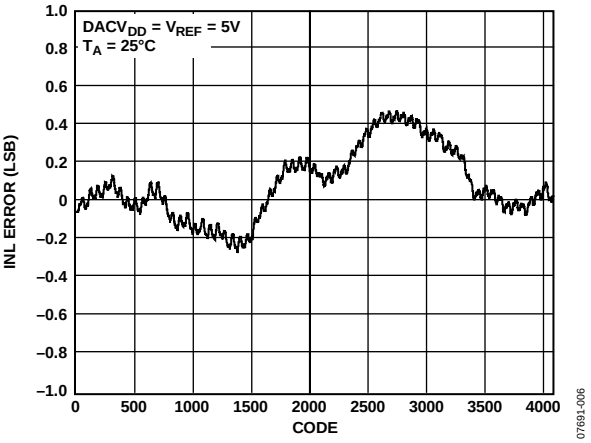


Figure 6. DAC INL, External Reference

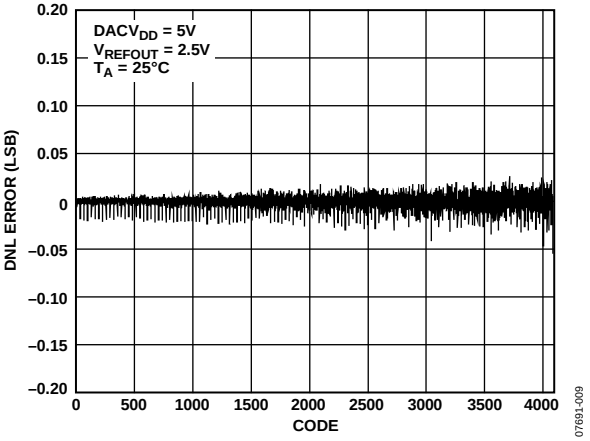


Figure 9. DAC DNL, Internal Reference

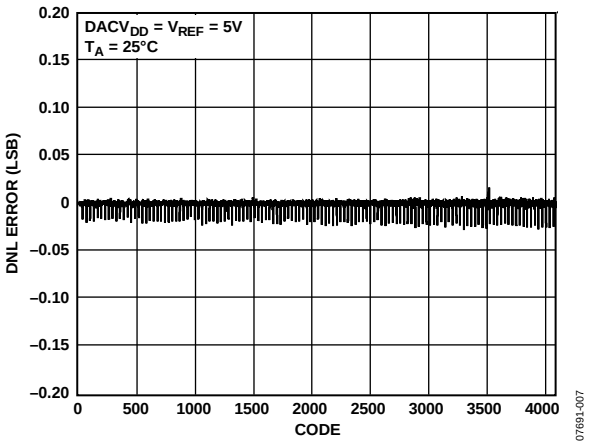


Figure 7. DAC DNL, External Reference

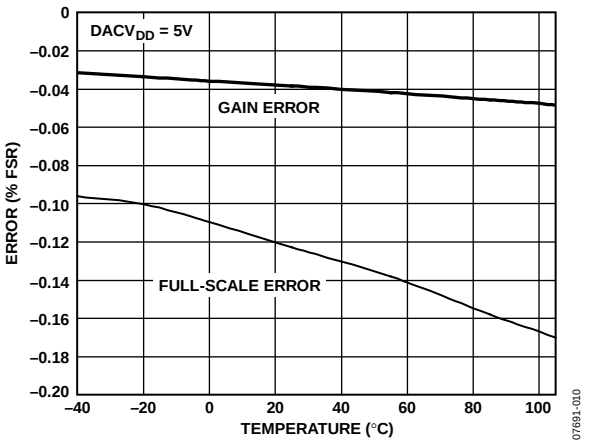


Figure 10. DAC Gain Error and Full-Scale Error vs. Temperature

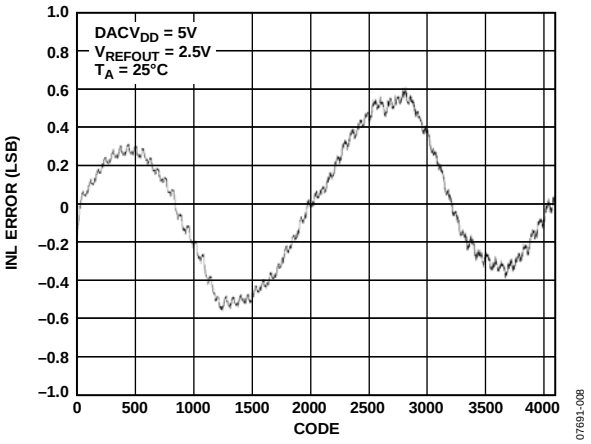


Figure 8. DAC INL, Internal Reference

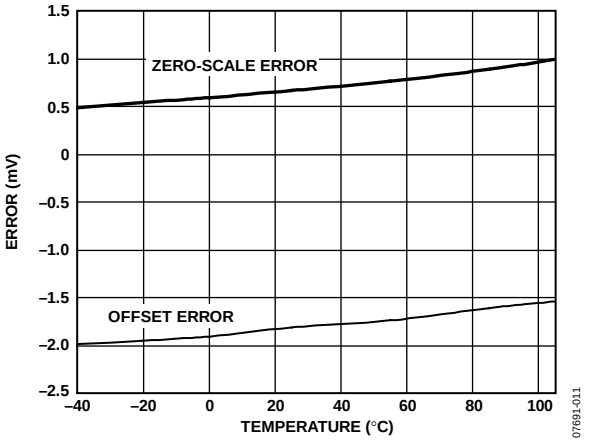


Figure 11. DAC Zero-Scale Error and Offset Error vs. Temperature

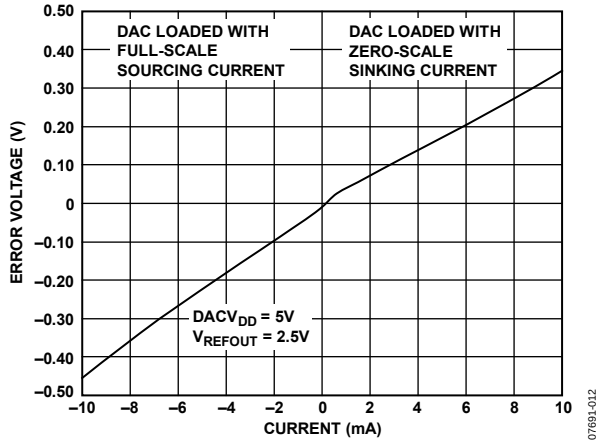


Figure 12. DAC Headroom at Rails vs. Source and Sink

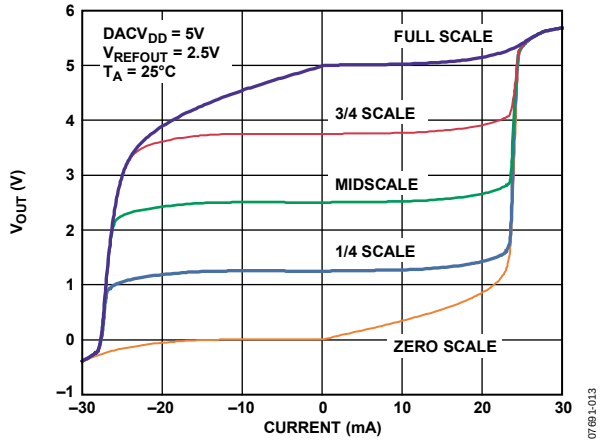


Figure 13. DAC Sink and Source Capability

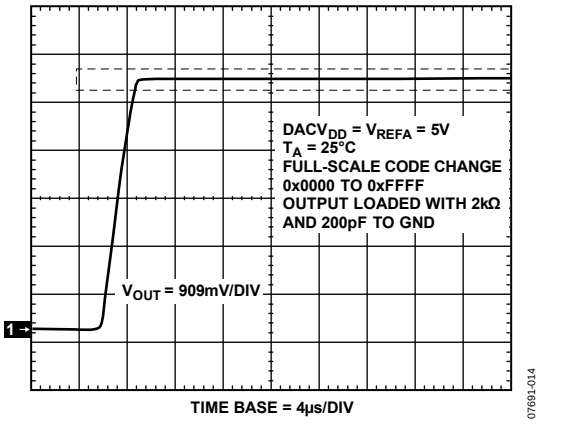


Figure 14. DAC Full-Scale Settling Time

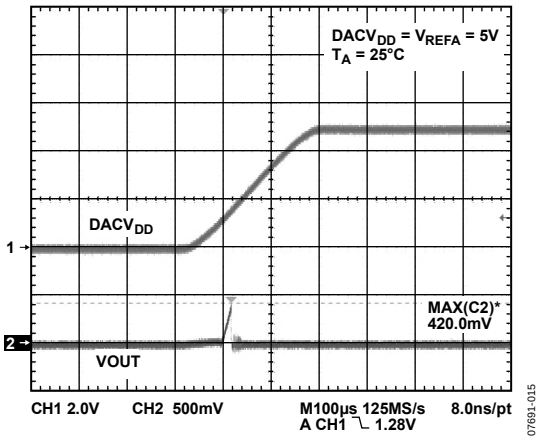


Figure 15. DAC Power-On Reset to 0 V

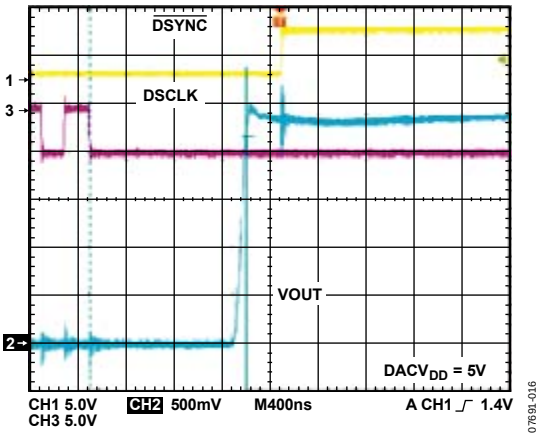


Figure 16. DAC Exiting Power-Down to Midscale

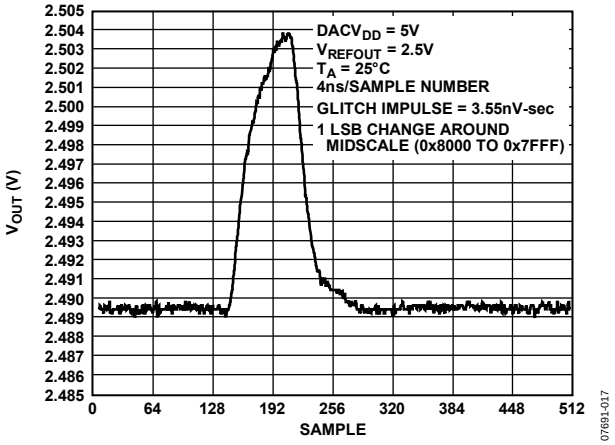


Figure 17. DAC Digital-to-Analog Glitch Impulse (Negative)

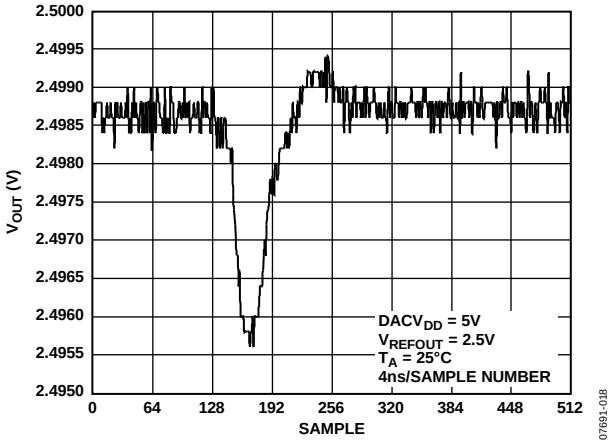


Figure 18. DAC Analog Crosstalk

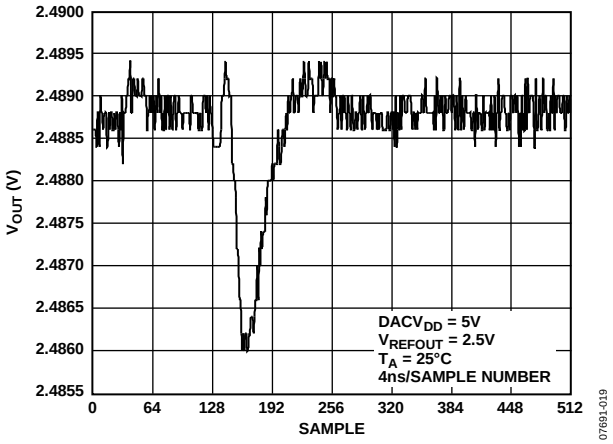


Figure 19. DAC-to-DAC Crosstalk

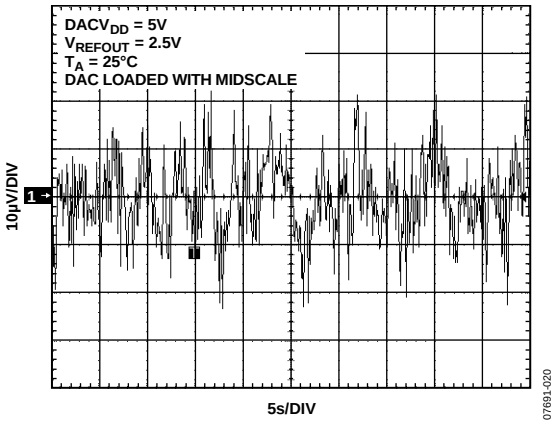


Figure 20. 0.1 Hz to 10 Hz DAC Output Noise Plot, Internal Reference

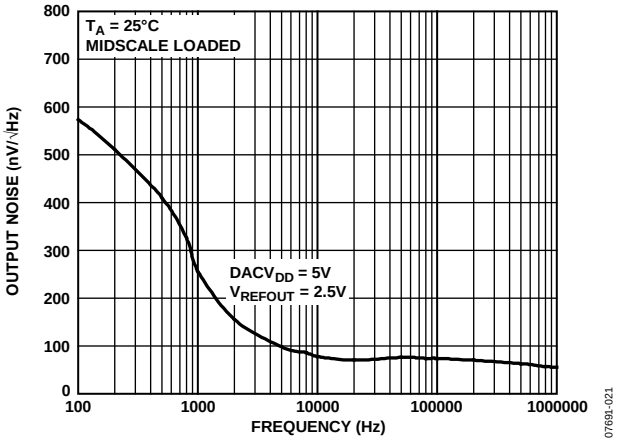


Figure 21. DAC Noise Spectral Density, Internal Reference

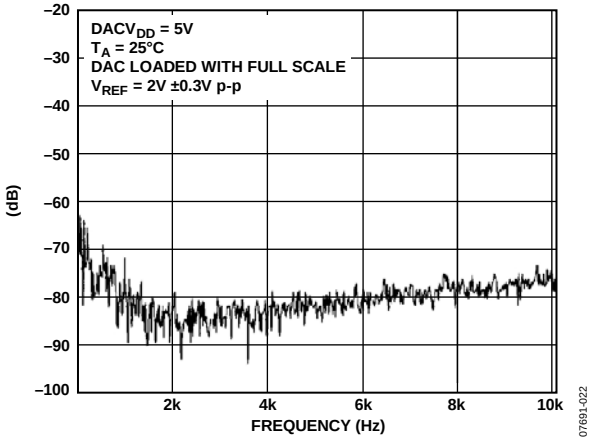


Figure 22. DAC Total Harmonic Distortion

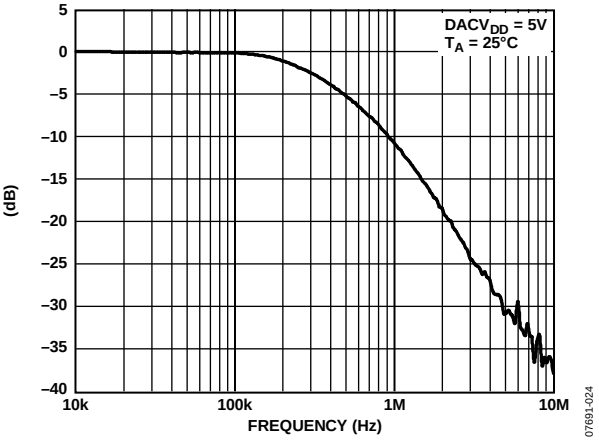


Figure 24. DAC Multiplying Bandwidth

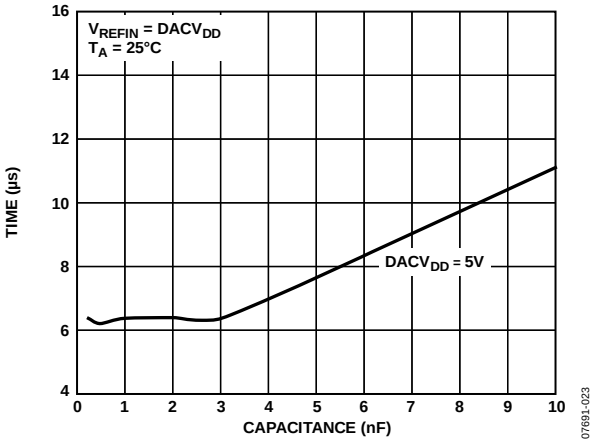


Figure 23. DAC Settling Time vs. Capacitive Load

ADC

$DACV_{DD}$ and $ADCV_{DD}$ = 5 V, V_{SY} = 5 V, unless otherwise noted.

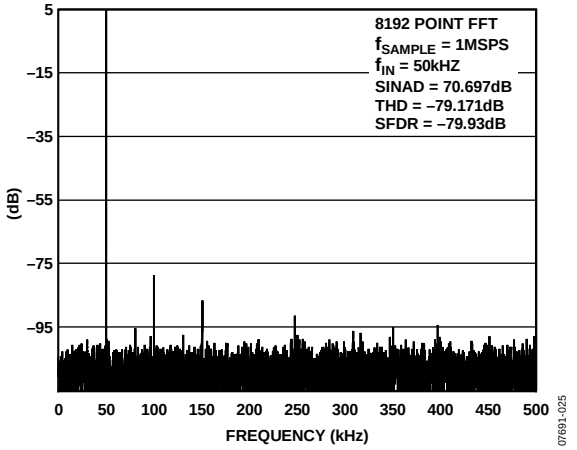


Figure 25. ADC Dynamic Performance at 1 MSPS

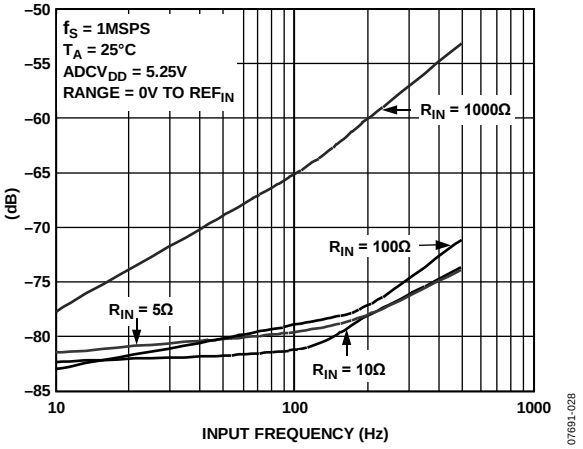


Figure 28. ADC THD vs. Input Frequency for Various Analog Source Impedances

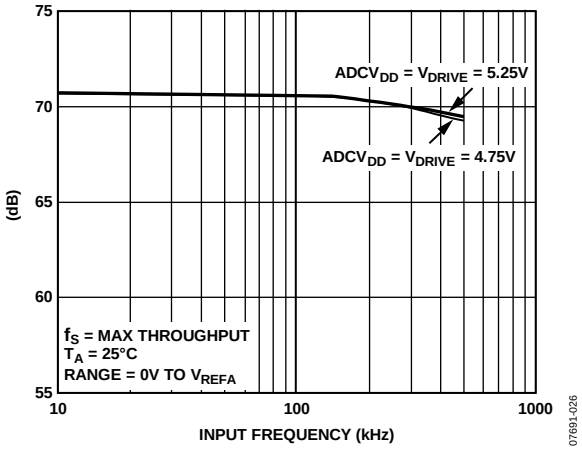


Figure 26. ADC SINAD vs. Analog Input Frequency for Various Supply Voltages at 1 MSPS

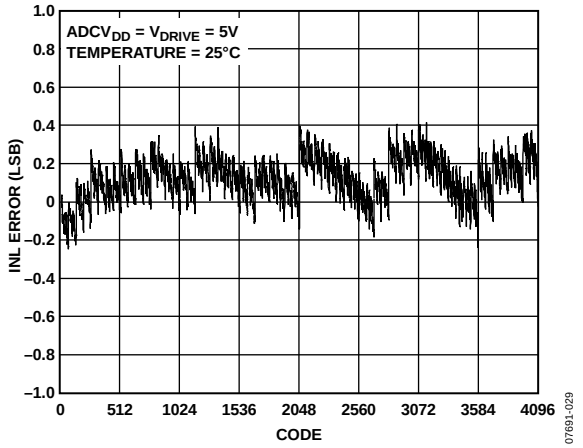


Figure 29. ADC Typical INL

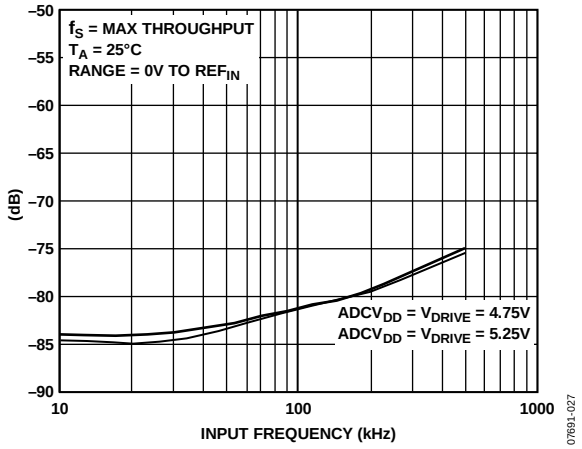


Figure 27. THD vs. Analog Input Frequency for Various Supplies at 1 MSPS

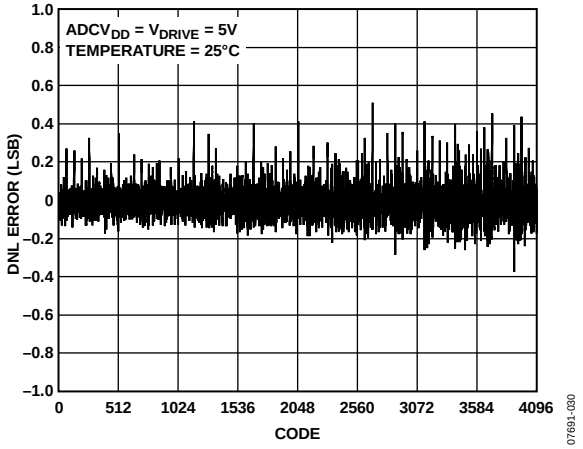


Figure 30. ADC Typical DNL

AMPLIFIER

$DACV_{DD}$ and $ADCV_{DD}$ = 5 V, V_{SY} = 5 V, unless otherwise noted.

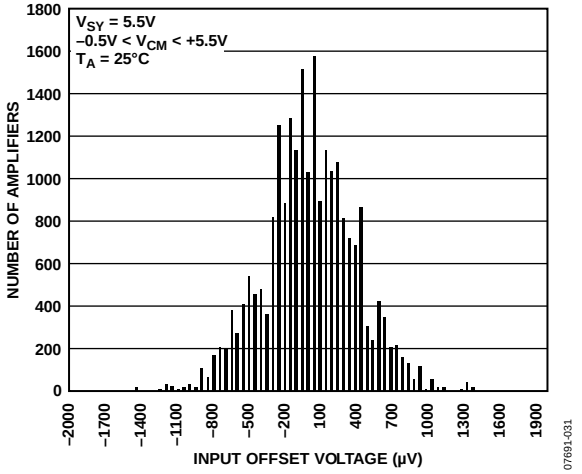


Figure 31. Amplifier Input Offset Voltage Distribution

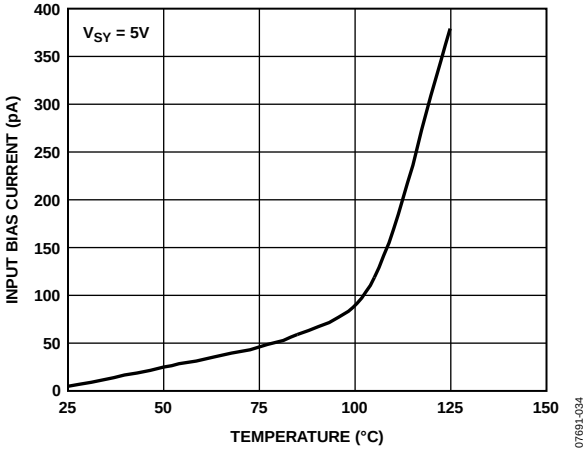


Figure 34. Amplifier Input Bias Current vs. Temperature

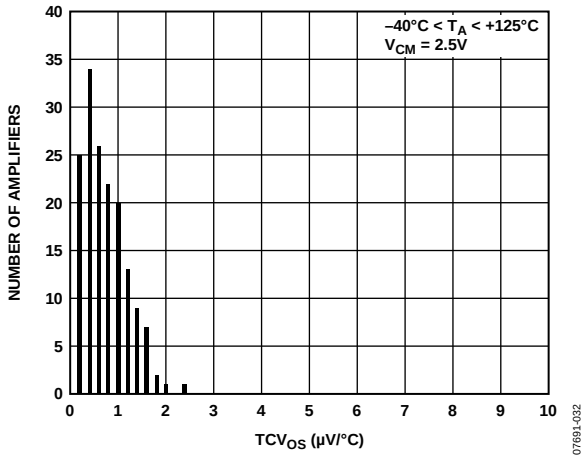


Figure 32. Amplifier Input Offset Voltage Drift Distribution

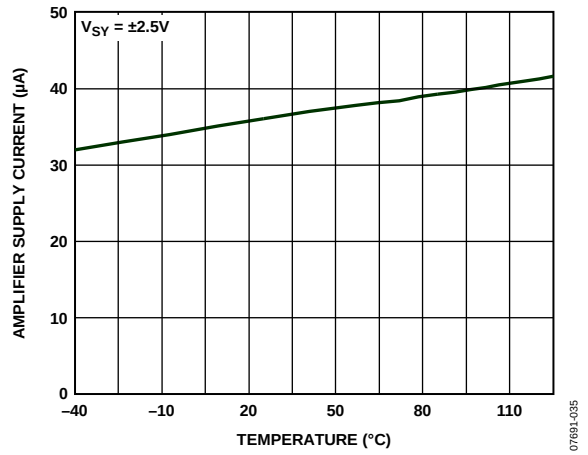


Figure 35. Amplifier Supply Current vs. Temperature

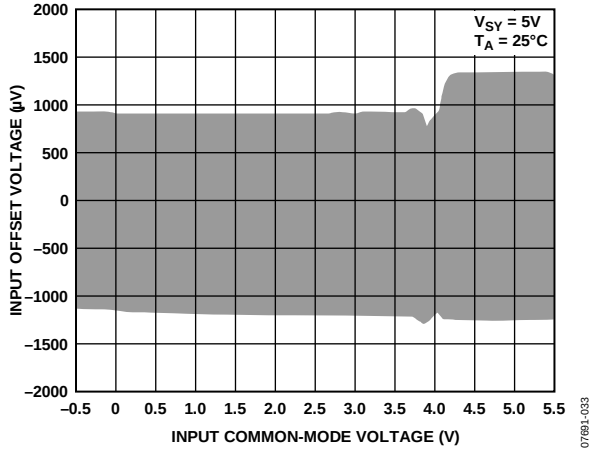


Figure 33. Amplifier Input Offset Voltage vs. Input Common-Mode Voltage

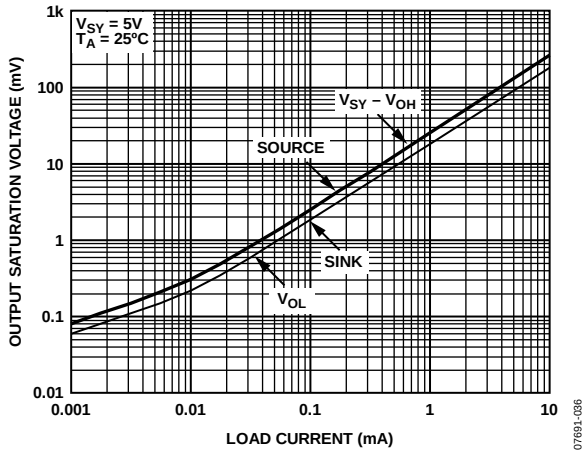


Figure 36. Amplifier Output Saturation Voltage vs. Load Current

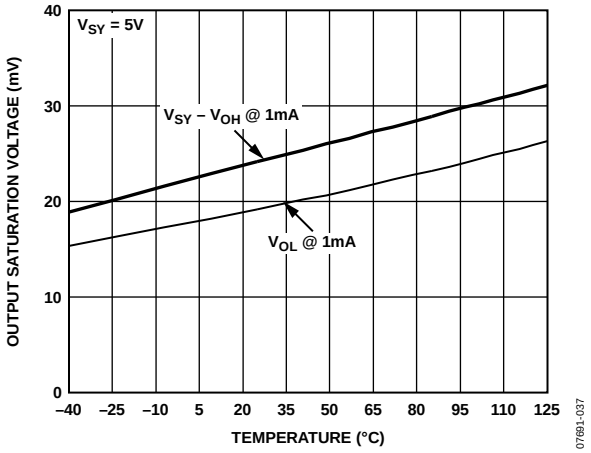


Figure 37. Amplifier Output Saturation Voltage vs. Temperature (I_L = 1 mA)

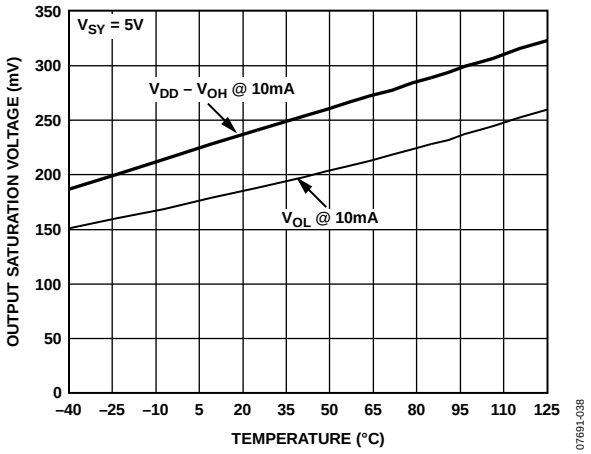


Figure 38. Amplifier Output Saturation Voltage vs. Temperature (I_L = 10 mA)

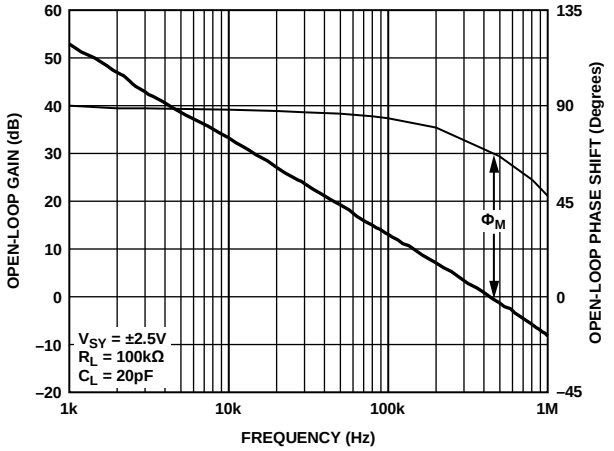


Figure 39. Amplifier Open-Loop Gain and Phase vs. Frequency

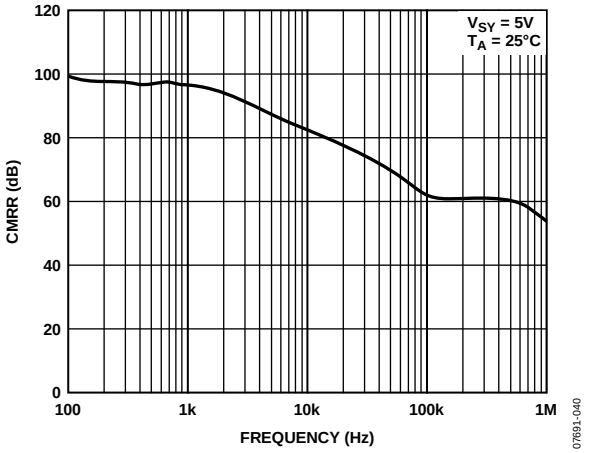


Figure 40. Amplifier CMRR vs. Frequency

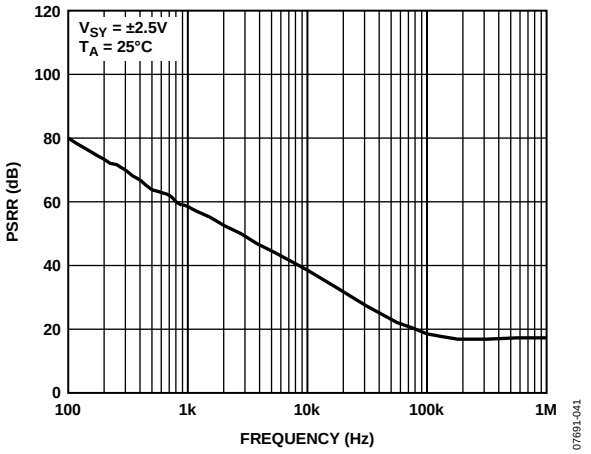


Figure 41. Amplifier PSRR vs. Frequency

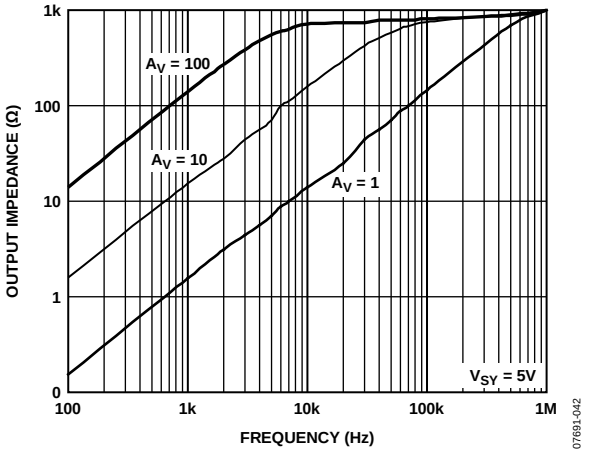


Figure 42. Amplifier Closed-Loop Output Impedance vs. Frequency

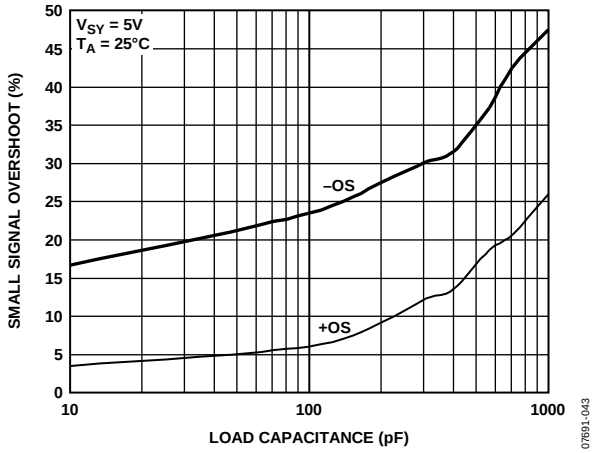


Figure 43. Small Signal Overshoot vs. Load Capacitance

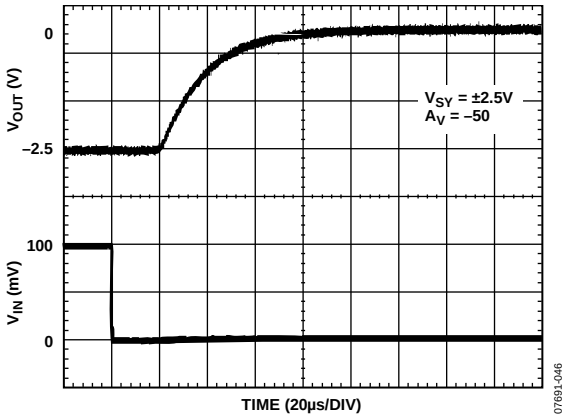


Figure 46. Amplifier Positive Overload Recovery

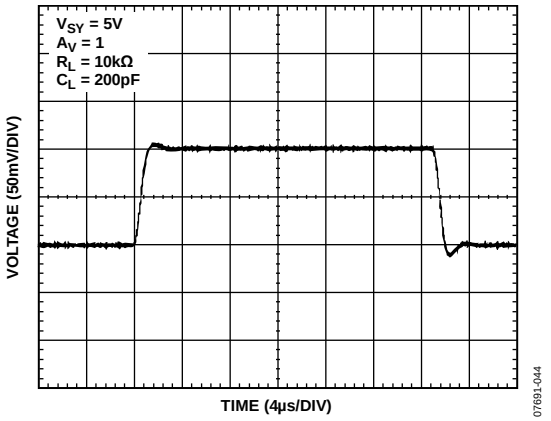


Figure 44. Amplifier Small Signal Transient Response

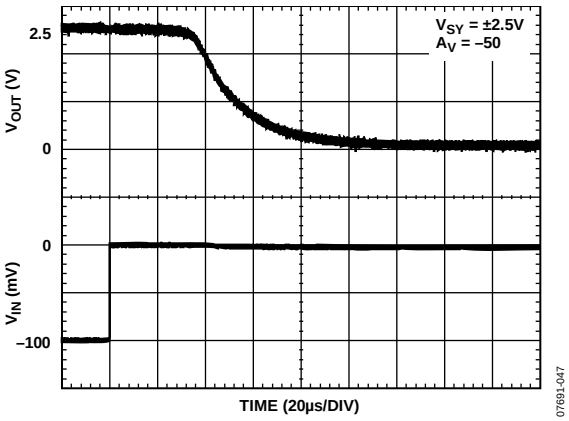


Figure 47. Amplifier Negative Overload Recovery

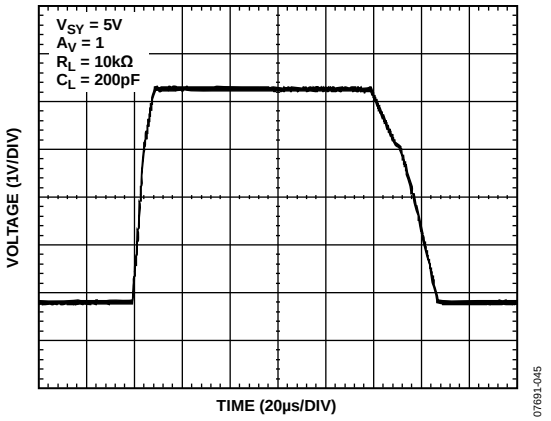


Figure 45. Amplifier Large Signal Transient Response

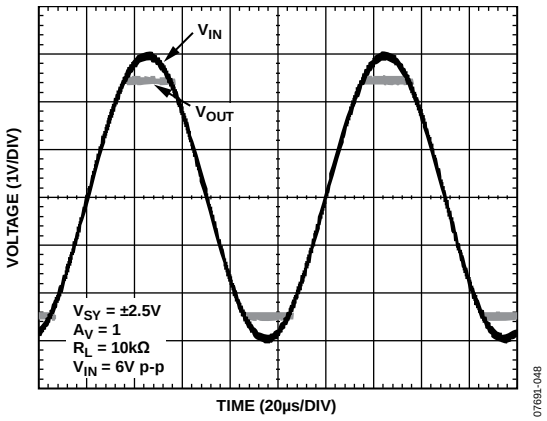


Figure 48. Amplifier, No Phase Reversal

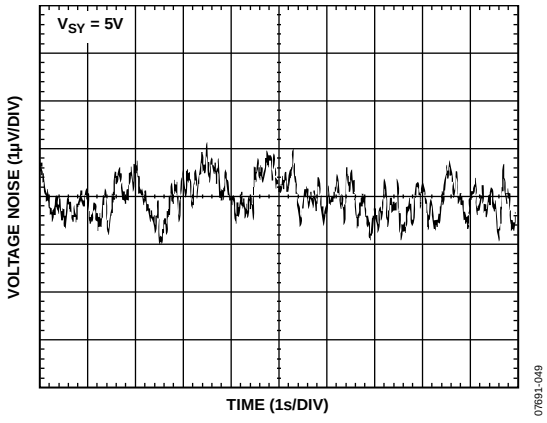


Figure 49. Amplifier 0.1 Hz to 10 Hz Input Voltage Noise

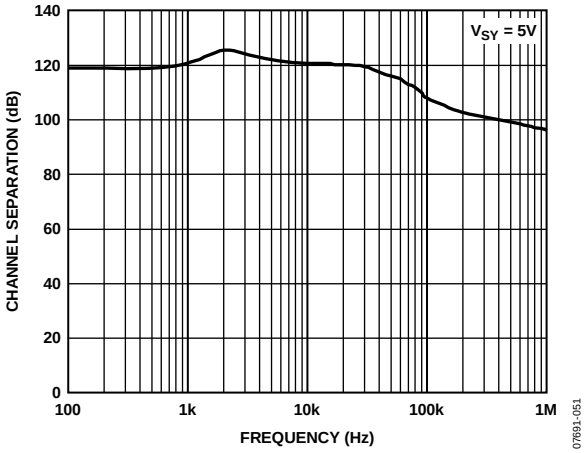


Figure 51. Amplifier Channel Separation

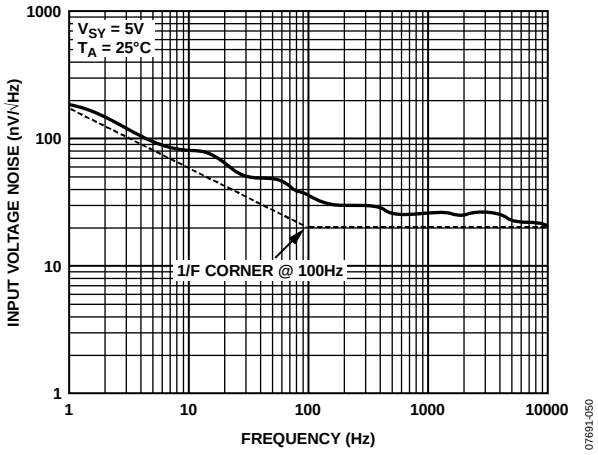


Figure 50. Amplifier Voltage Noise Density

TERMINOLOGY

DAC Integrated Nonlinearity
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function.

DAC Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The DAC is guaranteed monotonic by design.

DAC Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. It can be negative or positive and is expressed in millivolts.

DAC Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts.

DAC Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

DAC Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in microvolts per degree Celsius.

DAC Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in ppm of full-scale range per degree Celsius.

DAC Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 10 shows a plot of typical full-scale error vs. temperature.

DAC Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000).

DAC DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in $DACV_{DD}$ for full-scale output of the DAC. It is measured in decibels. V_{REFIN} is held at 2 V, and $DACV_{DD}$ is varied ±10%.

DAC DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (that is, $\overline{\text{LDAC}}$ is high). It is expressed in decibels.

DAC Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{SYNC}}$ held high). It is specified in nV-sec and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

DAC Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

DAC Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high, and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

DAC Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

ADC Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

ADC Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

ADC Offset Error
This is the deviation of the first code transition (00…000 to 00…001) from the ideal, that is, ADCGND + 1 LSB.

ADC Offset Error Match
This is the difference in offset error between any two channels.

ADC Gain Error
This is the deviation of the last code transition (111…110 to 111…111) from the ideal (that is, V_{REFA} − 1 LSB) after the offset error has been adjusted out.

ADC Gain Error Match
This is the difference in gain error between any two channels.

ADC Zero-Code Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REFA} input range with−V_{REFA} to +V_{REFA} biased about the V_{REFA} point. It is the deviation of the midscale transition (all 0s to all 1s) from the ideal V_{IN} voltage, that is, V_{REFA} − 1 LSB.

ADC Zero-Code Error Match
This is the difference in ADC zero-code error between any two channels.

ADC Positive Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REFA} input range with −V_{REFA} to +V_{REFA} biased about the V_{REFA} point. It is the deviation of the last code transition (011…110 to 011…111) from the ideal (that is, +V_{REFA} − 1 LSB) after the zero-code error has been adjusted out.

ADC Positive Gain Error Match
This is the difference in ADC positive gain error between any two channels.

ADC Negative Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × V_{REFA} input range with −V_{REFA} to +V_{REFA} biased about the V_{REFA} point. It is the deviation of the first code transition (100…000 to 100…001) from the ideal (that is, −V_{REFA} + 1 LSB) after the ADC zero-code error has been adjusted out.

ADC Negative Gain Error Match
This is the difference in negative gain error between any two channels.

ADC Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all 15 nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure is given worst case across all 16 channels for the ADC.

ADC PSR (Power Supply Rejection)
Variations in power supply affect the full scale transition, but not the linearity of the converter. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

ADC Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track on the 14th ASCLK falling edge. Track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

ADC Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal-to-(Noise+Distortion)=6.02N+1.76\ [\text{dB}]$$

Thus, for a 12-bit converter, this is 74 dB.

ADC Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the ADC, it is defined as

$$THD[\text{dB}]=20\times\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

ADC Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

ADC Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), while the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The ADC is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves whereas the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

THEORY OF OPERATION

The AD5590 is an analog I/O module. The output port contains sixteen 12-bit voltage output DAC channels. The DAC channels are divided into two groups of eight DACs, each of which can be programmed independently. Each group of DACs contains its own internal 2.5 V reference. The references are powered down by default allowing the use of external references, if required.

Either internal reference can be powered up and used as a reference for the ADC section. This is achieved by connecting the appropriate $V_{REFINx}/V_{REFOUTx}$ pin to V_{REFA}. Because the $V_{REFINx}/V_{REFOUTx}$ pins have different input and output impedances it is not possible to use one internal reference for both DAC groups without buffering.

The input port comprises a single, 12-bit, 1 MSPS ADC with 16 multiplexed input channels. The ADC contains a sequencer that allows it to sample any combination of the sixteen channels.

The AD5590 also contains eight rail-to-rail low noise amplifiers. These amplifiers can be used independently or as part of signal condition for the input or output ports.

DAC SECTION

Sixteen DACs make up the output port of the AD5590. Each DAC consists of a string of resistors followed by an output buffer amplifier. The sixteen DACs are divided into two groups of eight with each group having its own internal 2.5 V reference with an internal gain of 2. Figure 52 shows a block diagram of the DAC architecture.

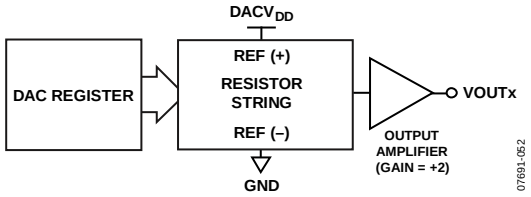


Figure 52. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register (0 to 4095).
N = 12.

Resistor String

The resistor string section is shown in Figure 53. It is simply a string of resistors, each of Value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

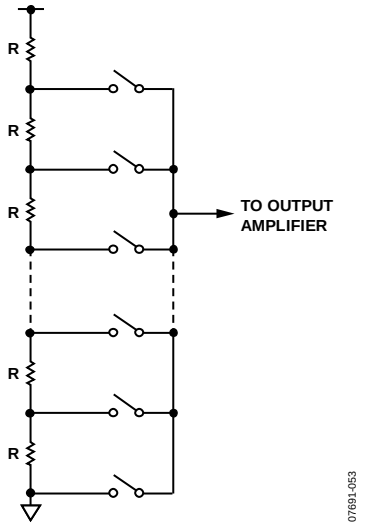


Figure 53. Resistor String

DAC Internal Reference

The DAC section has two on-chip 2.5 V references with an internal gain of 2, giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal references are enabled via a write to the appropriate control register (see Table 11).

The internal references associated with each group of DACs are available at the $V_{REFIN1}/V_{REFOUT1}$ and $V_{REFIN2}/V_{REFOUT2}$ pins. A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and DACGND for reference stability.

Individual channel power-down is not supported while using the internal reference.

DAC Output Amplifier

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to $DACV_{DD}$. The amplifier is capable of driving a load of 2 kΩ in parallel with 1000 pF to DACGND. The source and sink capabilities of the output amplifier can be seen in Figure 13. The slew rate is 1.5 V/μs with a ¼ to ¾ scale settling time of 10 μs.

ADC SECTION

The ADC section is a fast, 16-channel, 12-bit, single-supply, analog-to-digital converter. The ADC is capable of throughput rates of up to 1 MSPS when provided with a 20 MHz clock.

The ADC section provides the user with an on-chip track-and-hold, analog-to-digital converter. The ADC section has 16 single-ended input channels with a channel sequencer, allowing the user to select a sequence of channels through which the ADC can cycle with each consecutive $\overline{\text{ASYNC}}$ falling edge. The serial clock input accesses data from the ADC, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC converter. The analog input range for the ADC is 0 V to V_{REFA} or 0 V to 2 × V_{REFA} depending on the status of Bit 1 in the control register. The ADC provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits in the ADC control register.

ADC CONVERTER OPERATION

The ADC is a 12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The ADC can convert analog input signals in the range 0 V to V_{REFA} or 0 V to 2 × V_{REFA}. Figure 54 and Figure 55 show simplified schematics of the ADC. The ADC comprises control logic, SAR, and a capacitive DAC, which are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 54 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected VIN channel.

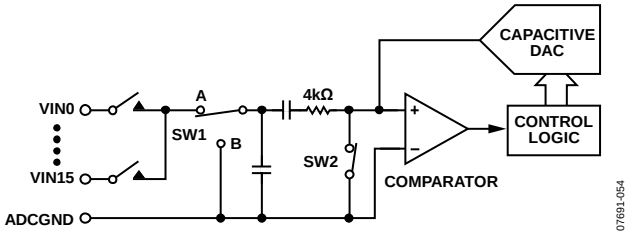


Figure 54. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 55), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 57 shows the ADC transfer function.

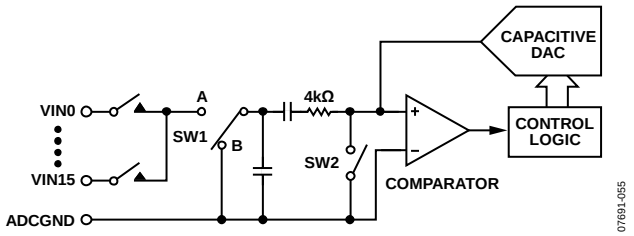


Figure 55. ADC Conversion Phase

Analog Input

Figure 56 shows an equivalent circuit of the analog input structure of the ADC. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceed the supply rails by more than 200 mV. This causes these diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the ADC. Capacitor C1 in Figure 56 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and also includes the on resistance of the input multiplexer.

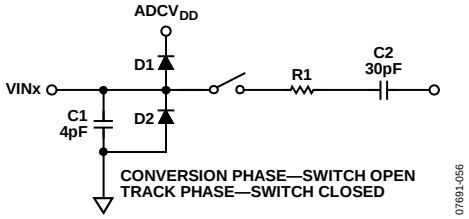


Figure 56. Equivalent Analog Input Circuit

The total resistance is typically about 400 Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF. For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, drive the analog input from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, limit the source impedance to low values. The maximum source impedance depends on the amount of total harmonic distortion (THD) that can be tolerated. The THD increases as the source impedance increases, and performance degrades (see Figure 28).

ADC Transfer Function

The output coding of the ADC is either straight binary or twos complement, depending on the status of the LSB (range bit) in the ADC control register. The designed code transitions occur midway between successive LSB values (that is, 1 LSB, 2 LSBs, and so on). The LSB size is equal to $V_{REFA}/4096$. The ideal transfer characteristic for the ADC when straight binary coding is selected is shown in Figure 57.

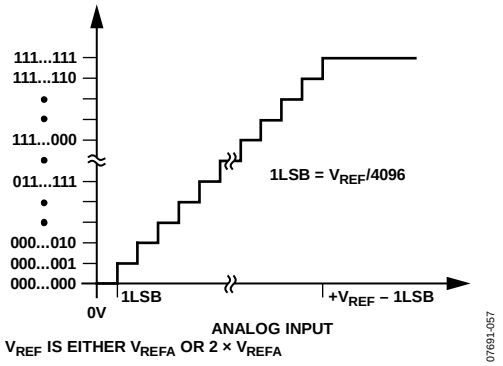


Figure 57. Straight Binary Transfer Characteristic

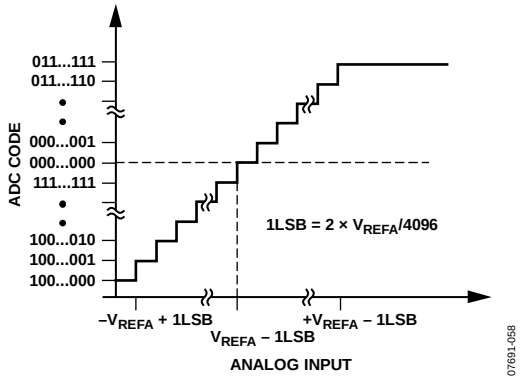


Figure 58. Twos Complement Transfer Characteristic with $V_{REFA} \pm V_{REFA}$ Input Range

Analog Input Selection

Any one of 16 analog input channels can be selected for conversion by programming the multiplexer with the ADD3 to ADD0 address bits in the ADC control register. The channel configurations are shown in Table 23. The ADC can also be configured to automatically cycle through a number of channels as selected. The sequencer feature is accessed via the SEQ and shadow bits in the ADC control register (see Table 21). The ADC can be programmed to continuously convert on a selection of channels in ascending order. The analog input channels to be converted on are selected through programming the relevant bits in the shadow register (see Table 26). The next serial transfer then acts on the sequence programmed by executing a conversion on the lowest channel in the selection.

The next serial transfer results in a conversion on the next highest channel in the sequence, and so on. It is not necessary to write to the ADC control register once a sequencer operation has been initiated. The write bit must be set to 0 to ensure the ADC control register is not accidentally overwritten, or the sequence operation interrupted. If the ADC control register is written to at any time during the sequence, then it must be ensured that the SEQ and shadow bits are set to 1 and 0, respectively to avoid interrupting the automatic conversion sequence. This pattern continues until the ADC is written to and the SEQ and shadow bits are configured with any bit combination except 1, 0. On completion of the sequence, the ADC sequencer returns to the first selected channel in the shadow register and commence the sequence again if uninterrupted.

Rather than selecting a particular sequence of channels, a number of consecutive channels beginning with Channel 0 can also be programmed via the control register alone, without needing to write to the shadow register. This is possible if the SEQ and shadow bits are set to 1, 1. The channel address bits, ADD3 through ADD0, then determine the final channel in the consecutive sequence. The next conversion is on Channel 0, then Channel 1, and so on until the channel selected via the ADD3 through ADD0 address bits is reached. The cycle begins again on the next serial transfer provided the write bit is set to low or, if high, that the SEQ and shadow bits are set to 1, 0; then, the ADC continues its preprogrammed automatic sequence uninterrupted. Regardless of which channel selection method is used, the 16-bit word output from the ADC during each conversion always contains the channel address that the conversion result corresponds to, followed by the 12-bit conversion result (see the Serial Interface section).

Digital Inputs

The digital inputs applied to the ADC are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the $ADCV_{DD}$ + 0.3 V limit found on the analog inputs.

Another advantage of ASCLK, ADIN, and $\overline{\text{ASYNC}}$ not being restricted by the $ADCV_{DD}$ + 0.3 V limit is the fact that power supply sequencing issues are avoided. If $\overline{\text{ASYNC}}$, ADIN, or ASCLK is applied before $ADCV_{DD}$, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to $ADCV_{DD}$.

V_{DRIVE}

The ADC has the V_{DRIVE} feature, which controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the ADC is operated with a V_{DD} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply. The ADC has better dynamic performance with a V_{DD} of 5 V while still being able to interface to 3 V processors. Care should be taken to ensure that V_{DRIVE} does not exceed $ADCV_{DD}$ by more than 0.3 V (see the Absolute Maximum Ratings section).

Reference Section

An external reference source should be used to supply the 2.5 V reference to the ADC. Errors in the reference source results in gain errors in the ADC transfer function and adds to the specified full-scale errors of the ADC. A capacitor of at least 0.1 µF should be placed on the V_{REFA} pin. Suitable reference sources for the ADC include the AD780, REF193, and the AD1852.

If 2.5 V is applied to the V_{REFA} pin, the analog input range can either be 0 V to 2.5 V or 0 V to 5 V, depending on the range bit in the control register.

AMPLIFIER SECTION

The operational amplifiers in the AD5590 are micropower, rail-to-rail input and output amplifiers that feature low supply current, low input voltage, and low current noise.

The parts are fully specified to operate from a single 5.0 V supply, or ±2.5 V dual supplies. The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems. The amplifiers in the AD5590 are fully independent of the DAC and ADC sections. If some or all of the amplifiers are not required, connect them as a grounded unity-gain buffer, as shown in Figure 59.

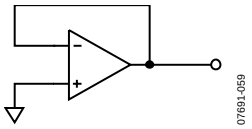


Figure 59. Configuration for Unused Amplifiers

SERIAL INTERFACE

The AD5590 contains independent serial interfaces for the ADC and DAC sections. The ADC uses the $\overline{\text{ASYNC}}$, ASCLK, ADIN, and ADOUT pins. The V_{DRIVE} pin allows the user to determine the output voltage of logic high signals. The DAC uses DSCLK, DDIN, $\overline{\text{DSYNC1}}$, $\overline{\text{DSYNC2}}$, $\overline{\text{LDAC}}$, and $\overline{\text{CLR}}$.

The 16 analog input channels use the ADC interface. The 16 output channels use the DAC interface. The 16 output channels are divided into two groups of eight channels, which can be controlled independently. Each group has its own set of control registers. When addressing the DAC control registers, the serial data should be framed by $\overline{\text{DSYNC1}}$ to access the control registers for DAC0 to DAC7 and framed by $\overline{\text{DSYNC2}}$ to access the control registers for DAC8 to DAC15.

The interfaces are compatible with SPI®, QSPI™, MICROWIRE™, and most DSPs.

ACCESSING THE DAC BLOCK

Figure 4 shows a timing diagram of a typical write sequence to the DAC block. The write sequence begins by bringing one or both of the $\overline{\text{DSYNC}}$ lines low. If $\overline{\text{DSYNC1}}$ is brought low, the data is written to the DAC block containing DAC0 to DAC7. If $\overline{\text{DSYNC2}}$ is brought low, the data is written to the DAC block containing DAC8 to DAC15. If both $\overline{\text{DSYNC1}}$ and $\overline{\text{DSYNC2}}$ are brought low, the data is written into both blocks simultaneously. Figure 60 shows how the serial interface is arranged.

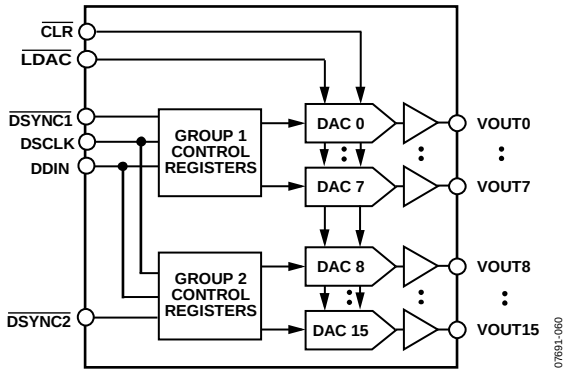


Figure 60. DAC Serial Interface Configuration

Data from the DDIN line is clocked into the 32-bit shift register on the falling edge of DSCLK. The serial clock frequency can be as high as 50 MHz, making the AD5590 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{\text{DSYNCx}}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{\text{DSYNCx}}$ can initiate the next write sequence.

DAC Input Shift Register

The input shift register is 32 bits wide (see Figure 61). The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 11), followed by the 4-bit DAC address, A3 to A0 (see Table 12), and finally the 12-bit data-word. The data-word comprises the 12-bit input code followed by eight don't care bits. These data bits are transferred to the DAC register on the 32nd falling edge of DSCLK.

Table 11. DAC Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (Software $\overline{\text{LDAC}}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{\text{LDAC}}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up internal REF register
1	0	0	1	Reserved
…	…	…	…	Reserved
1	1	1	1	Reserved

Table 12. DAC Address Commands

Address (n)				Selected DAC Channel	
A3	**A2**	**A1**	**A0**	**$\overline{\text{DSYNC1}}$ Low**	**$\overline{\text{DSYNC2}}$ Low**
0	0	0	0	DAC0	DAC8
0	0	0	1	DAC1	DAC9
0	0	1	0	DAC2	DAC10
0	0	1	1	DAC3	DAC11
0	1	0	0	DAC4	DAC12
0	1	0	1	DAC5	DAC13
0	1	1	0	DAC6	DAC14
0	1	1	1	DAC7	DAC15
1	1	1	1	DAC0 to DAC7	DAC8 to DAC15

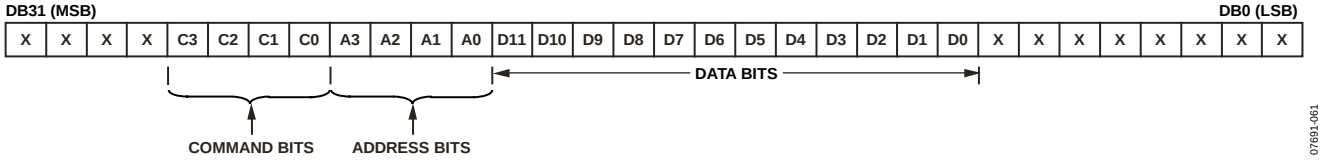


Figure 61. DAC Input Register Contents

$\overline{\text{DSYNC}}$ Interrupt

In a normal write sequence, the $\overline{\text{DSYNCx}}$ line is kept low for 32 falling edges of DSCLK, and the DAC is updated on the 32nd falling edge and rising edge of $\overline{\text{DSYNCx}}$. However, if $\overline{\text{DSYNCx}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 63).

DAC Internal Reference Register

The on-board references in the DAC blocks are off at power-up by default. This allows the use of an external reference if the application requires it. The on-board references can be turned on or off by a user-programmable internal REF register by setting Bit DB0 high or low (see Table 13). Command 1000 is reserved for setting the internal REF register (see Table 11).

DAC Power-On Reset

The DAC blocks contain a power-on reset circuit that controls the output voltage during power-up. The DAC outputs power up to 0 V. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 11). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

DAC Power-Down Modes

The DAC block contains four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 11). These modes are software-programmable by setting Bit DB9 and Bit DB8 in the control register.

Table 15 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC0 to DAC7 in Block 1 or DAC8 to DAC15 in Block 2) can be powered down to the selected mode by setting the corresponding eight bits to 1. See Table 16 for the contents of the input shift register during power-down/power-up operation. When using the internal reference, only all channel power-down to the selected modes is supported.

When both bits are set to 0, each block works normally with its normal power consumption of 1.3 mA at 5 V. However, for the three power-down modes, the supply current of each block falls to 0.4 μA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the DAC is known while it is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 62.

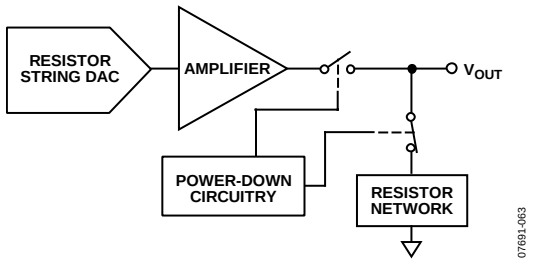


Figure 62. Output Stage During Power-Down

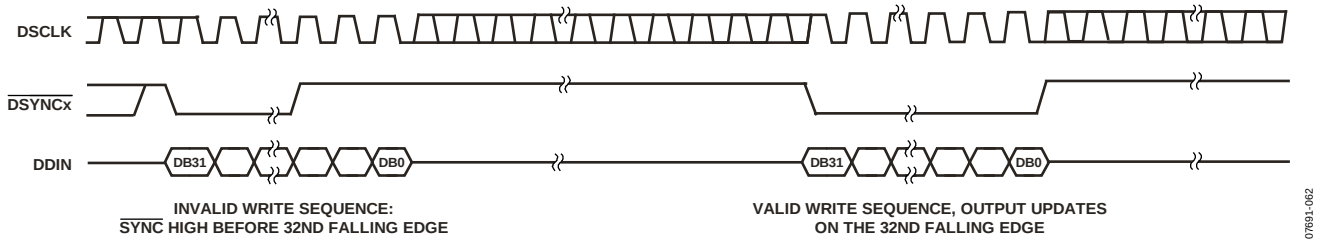


Figure 63. $\overline{\text{SYNC}}$ Interrupt Facility

Table 13. DAC Internal Reference Register

Internal REF Register (DB0)	Action
0	Reference off (default)
1	Reference on

Table 14. DAC 32-Bit Input Shift Register Contents for Reference Setup Command

MSB										LSB
DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB1	DB0
X	1	0	0	0	X	X	X	X	X	1/0
Don't care	Command bits (C3 to C0)				Address bits (A3 to A0)—don't care				Don't care	Internal REF register

The bias generator of the selected DAC(s), output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. The internal reference is powered down only when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for $DACV_{DD}$ = 5 V.

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{LDAC}$ low) or to the value in the DAC register before powering down ($\overline{LDAC}$ high).

DAC Clear Code Register

The DAC blocks have a hardware $\overline{CLR}$ pin that is an asynchronous clear input for all 16 DACs. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly. This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting Bit DB1 and Bit DB0 in the $\overline{CLR}$ control register (see Table 17). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 11).

The DAC exits clear code mode on the 32nd falling edge of the next write to the DAC. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time—the falling edge of $\overline{CLR}$ to when the output starts to change—is typically 280 ns. However, if outside the DAC linear region, it typically takes 520 ns after executing $\overline{CLR}$ for the output to start changing.

See Table 18 for contents of the input shift register during the loading clear code register operation.

Table 15. DAC Power-Down Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Table 16. DAC 32-Bit Input Shift Register Contents for Power-Down/Power-Up Function

MSB **LSB**

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	1	0	0	X	X	X	X	X	PD1	PD0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't care	Command bits (C3 to C0)				Address bits (A3 to A0)—don't care				Don't care	Power-down mode		Power-down/power-up channel selection—set bit to 1 to select							

Table 17. DAC Clear Code Register

Clear Code Register		
DB1	DB0	
CR1	CR0	Clears to Code
0	0	0x0000
0	1	0x0800
1	0	0x0FFF
1	1	No operation

Table 18. DAC 32-Bit Input Shift Register Contents for Clear Code Function

MSB **LSB**

DB31 to DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB2	DB1	DB0
X	0	1	0	1	X	X	X	X	X	CR1	CR0
Don't care	Command bits (C3 to C0)				Address bits (A3 to A0)—don't care				Don't care	Clear code register	

$\overline{\text{LDAC}}$ Function

The outputs of all DACs can be updated simultaneously using the hardware $\overline{\text{LDAC}}$ pin.

Synchronous $\overline{\text{LDAC}}$: After new data is read, the DAC registers are updated on the falling edge of the 32nd DSCLK pulse. $\overline{\text{LDAC}}$ can be permanently low or pulsed as in Figure 4.

Asynchronous $\overline{\text{LDAC}}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{\text{LDAC}}$ function by writing to Input Register n and updating all DAC registers. Command 0011 is reserved for this software $\overline{\text{LDAC}}$ function.

An $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin. This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{\text{LDAC}}$ pin is executed. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that this channel's update is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel updates synchronously; that is, the DAC register is updated after new data is read, regardless of the state of the $\overline{\text{LDAC}}$ pin. It effectively registers the $\overline{\text{LDAC}}$ pin as being tied low. (See Table 19 for the $\overline{\text{LDAC}}$ register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using Command 0110 loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means the DAC channel is updated regardless of the state of the $\overline{\text{LDAC}}$ pin. See Table 20 for the contents of the input shift register during the $\overline{\text{LDAC}}$ register mode of operation.

Table 19. $\overline{\text{LDAC}}$ Register

$\overline{\text{LDAC}}$ Bits (DB7 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
0	1/0	Determined by $\overline{\text{LDAC}}$ pin.
1	X—don't care	DAC channels update, overriding the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 0.

Table 20. DAC 32-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Register Function

MSB **LSB**

DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB19 to DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	1	0	X	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't care	Command bits (C3 to C0)				Address bits (A3 to A0)—don't care				Don't care	Setting $\overline{\text{LDAC}}$ bit to 1 overrides $\overline{\text{LDAC}}$ pin							

ACCESSING THE ADC BLOCK

The ADC register can be accessed via the serial interface using the ASCLK , ADIN, ADOUT, and $\overline{\text{ASYNC}}$ pins. The V_{DRIVE} pin can be used to dictate the logic levels of the output pins, allowing the ADC to be interfaced to a 3 V DSP while the ADC is operating at 5 V.

ADC Modes of Operation

The ADC has a number of different modes of operation. These modes are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The mode of operation of the ADC is controlled by the power management bits, PM1 and PM0, in the ADC control register, as detailed in Table 21. When power supplies are first applied to the ADC, ensure that the ADC is placed in the required mode of operation (see the Powering Up the ADC section).

Normal Mode (PM1 = PM0 = 1)

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times with the ADC remaining fully powered at all times. Figure 64 shows the general diagram of the operation of the ADC in this mode.

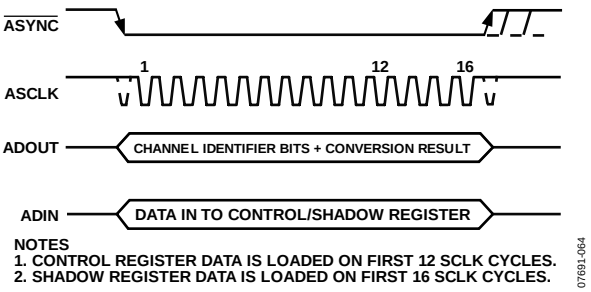


Figure 64. ADC Normal Mode Operation

The conversion is initiated on the falling edge of $\overline{\text{ASYNC}}$ and the track-and-hold enters hold mode as described in the Serial Interface section. The data presented to the ADC on the ADIN line during the first 12 clock cycles of the data transfer is loaded to the ADC control register (provided the write bit is 1). If the previous write had SEQ = 0 and shadow = 1, the data presented on the ADIN line on the next 16 ASCLK cycles is loaded into the shadow register. The ADC remains fully powered up in normal mode at the end of the conversion as long as PM1 and PM0 are set to 1 in the write transfer during that conversion. To ensure continued operation in normal mode, PM1 and PM0 are both loaded with 1 on every data transfer. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The track-and-hold returns to track on the 14th ASCLK falling edge. $\overline{\text{ASYNC}}$ can then idle high until the next conversion or can idle low until sometime prior to the next conversion, (effectively idling $\overline{\text{ASYNC}}$ low).

When a data transfer is complete (ADOUT has returned to three-state, weak/$\overline{\text{TRI}}$ bit = 0), another conversion can be initiated by bringing $\overline{\text{ASYNC}}$ low again after the quiet time, t_{QUIET}, has elapsed.

Full Shutdown (PM1 = 1, PM0 = 0)

In this mode, all internal circuitry on the ADC is powered down. The ADC retains information in the ADC control register during full shutdown. The ADC remains in full shutdown until the power management bits in the control register, PM1 and PM0, are changed.

If a write to the ADC control register occurs while the ADC is in full shutdown, with the power management bits changed to PM0 = PM1 = 1, normal mode, the ADC begins to power up on the $\overline{\text{ASYNC}}$ rising edge. The track-and-hold that was in hold while the ADC was in full shutdown return to track on the 14th ASCLK falling edge.

To ensure that the ADC is fully powered up, $t_{POWER-UP}$ (t_{12}) should elapse before the next $\overline{\text{ASYNC}}$ falling edge. Figure 65 shows the general diagram for this sequence.

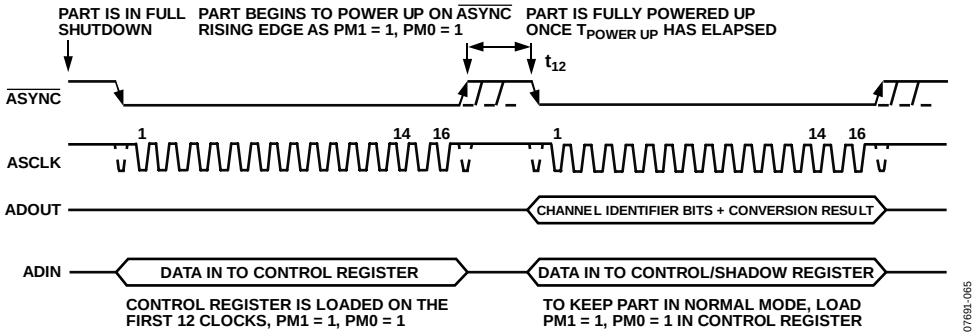


Figure 65. Full Shutdown Mode Operation

AutoShutdown (PM1 = 0, PM0 = 1)

In this mode, the ADC automatically enters shutdown at the end of each conversion when the ADC control register is updated. When the ADC is in shutdown, the track-and-hold is in hold mode. Figure 66 shows the general diagram of the operation of the ADC in this mode. In shutdown mode, all internal circuitry on the ADC is powered down. The ADC retains information in the ADC control register during shutdown. The ADC remains in shutdown until the next $\overline{\text{ASYNC}}$ falling edge it receives. On this $\overline{\text{ASYNC}}$ falling edge, the track-and-hold that was in hold while the ADC was in shutdown returns to track. Wake-up time from autoshutdown is 1 µs, and the user should ensure that 1 µs has elapsed before attempting a valid conversion. When running the ADC with a 20 MHz clock, one dummy cycle of 16 × ASCLKs should be sufficient to ensure that the ADC is fully powered up. During this dummy cycle, the contents of the ADC control register should remain unchanged; therefore, the write bit should be 0 on the ADIN line. This dummy cycle effectively halves the throughput rate of the ADC, with every other conversion result being valid. In this mode, the power consumption of the ADC is greatly reduced with the ADC entering shutdown at the end of each conversion. When the ADC control register is programmed to move into autoshutdown, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{\text{ASYNC}}$ signal.

Autostandby (PM1 = PM0 = 0)

In this mode, the ADC automatically enters standby mode at the end of each conversion when the ADC control register is updated. Figure 67 shows the general diagram of the operation of the ADC in this mode. When the ADC is in standby, portions of the ADC are powered down, but the on-chip bias generator remains powered up. The ADC retains information in the ADC control register during standby. The ADC remains in standby until it receives the next $\overline{\text{ASYNC}}$ falling edge. On this $\overline{\text{ASYNC}}$ falling edge, the track and hold that was in hold while the ADC was in standby returns to track. Wake-up time from standby is 1 µs; the user should ensure that 1 µs has elapsed before attempting a valid conversion on the ADC in this mode. When running the ADC with a 20 MHz clock, one dummy cycle of 16 × ASCLKs should be sufficient to ensure the ADC is fully powered up. During this dummy cycle, the contents of the ADC control register should remain unchanged; therefore, the write bit should be set to 0 on the ADIN line. This dummy cycle effectively halves the throughput rate of the ADC with every other conversion result being valid. In this mode, the power consumption of the ADC is greatly reduced with the ADC entering standby at the end of each conversion. When the ADC control register is programmed to move into autostandby, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{\text{ASYNC}}$ signal.

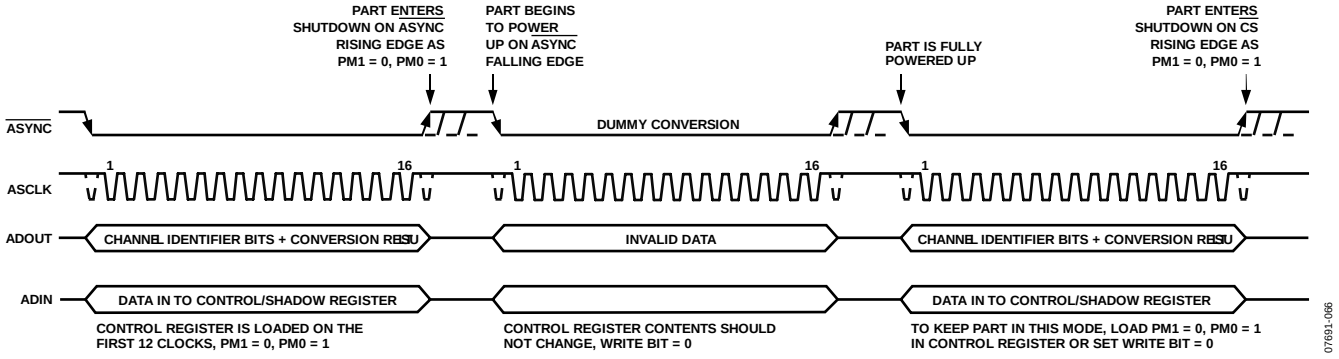


Figure 66. Autoshutdown Mode Operation

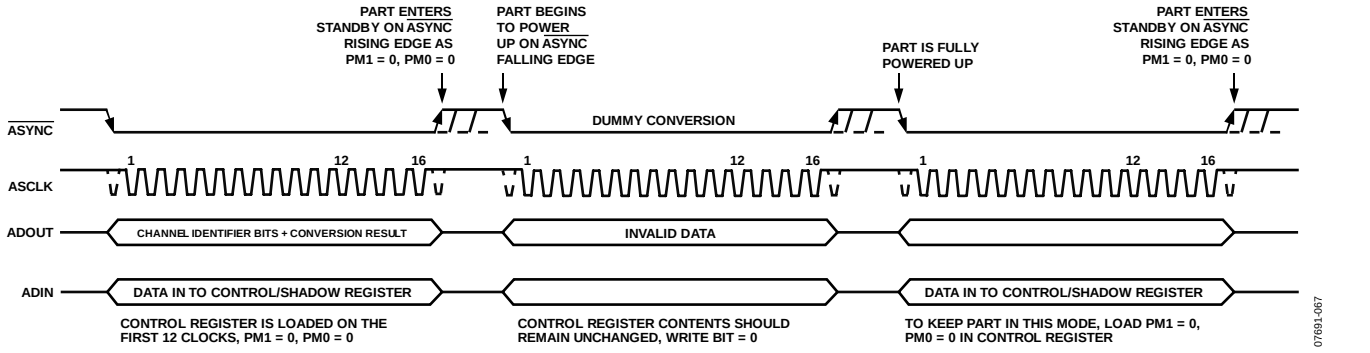


Figure 67. Autostandby Mode Operation

Powering Up the ADC

When supplies are first applied to the ADC, the ADC can power up in any of the operating modes of the ADC. To ensure that the ADC is placed into the required operating mode, the user should perform a dummy cycle operation, as outlined in Figure 68.

The three dummy conversion operations outlined in Figure 68 must be performed to place the ADC into either of the automatic modes. The first two conversions of this dummy cycle operation are performed with the ADIN line tied high, and for the third conversion of the dummy cycle operation, the user writes the desired control register configuration to the ADC to place the ADC into the required automode. On the third $\overline{\text{ASYNC}}$ rising edge after the supplies are applied, the control register contains the correct information and valid data results from the next conversion.

Therefore, to ensure the ADC is placed into the correct operating mode when supplies are first applied to the ADC, the user must first issue two serial write operations with the ADIN line tied high. On the third conversion cycle, the user can then write to the ADC control register to place the ADC into any of the operating modes. To guarantee that the ADC control register contains the correct data, do not write to the shadow register until the fourth conversion cycle after the supplies are applied to the ADC.

If the user wants to place the ADC into either normal mode or full shutdown mode, the second dummy cycle with ADIN tied high can be omitted from the three dummy conversion operation outlined in Figure 68.

Interfacing to the ADC

Figure 2 shows the detailed timing diagram for serial interfacing to the ADC. The serial clock provides the conversion clock and also controls the transfer of information to and from the ADC during each conversion.

The $\overline{\text{ASYNC}}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{\text{ASYNC}}$ puts the track and hold into hold mode, takes the bus out of three-state, and the analog input is sampled at this point. The conversion is also initiated at this point and requires 16 ASCLK cycles to complete. The track and hold returns to track on the 14th ASCLK falling edge as shown in Figure 2 at Point B, except when the write is to the shadow register, in which case the track and hold does not return to track until the rising edge of $\overline{\text{ASYNC}}$, that is, Point C in Figure 72. On the 16th ASCLK falling edge, the ADOUT line goes back into three-state (assuming the weak/$\overline{\text{TRI}}$ bit is set to 0). Sixteen serial clock cycles are required to perform the conversion process and to access data from the ADC. The 12 bits of data are preceded by the four channel address bits (ADD3 to ADD0), identifying which channel the conversion result corresponds to. $\overline{\text{ASYNC}}$ going low provides Address Bit ADD3 to be read in by the microprocessor or DSP. The remaining address bits and data bits are then clocked out by subsequent ASCLK falling edges beginning with the second Address Bit ADD2; thus, the first ASCLK falling edge on the serial clock has Address Bit ADD3 provided and also clocks out Address Bit ADD2. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

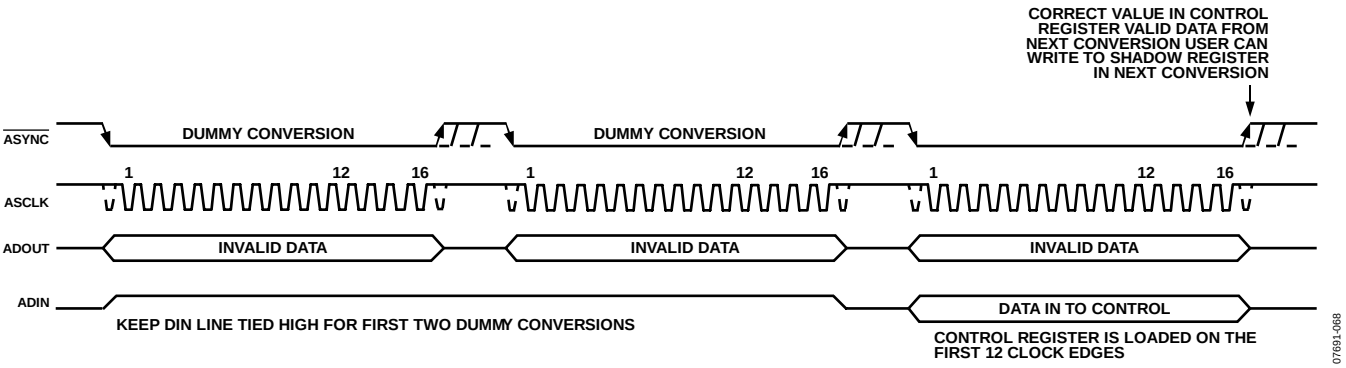


Figure 68. Placing the ADC into the Required Operating Mode after Supplies are Applied

ADC Control Register

The control register on the ADC is a 12-bit, write-only register. Data is loaded from the ADIN pin of the ADC on the falling edge of ASCLK. The data is transferred on the ADIN line at the same time as the conversion result is read from the ADC. The data transferred on the ADIN line corresponds to the ADC configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after $\overline{\text{ASYNC}}$ falling edge) is loaded to the ADC control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 21. Writing of information to the ADC control register takes place on the first 12 falling edges of ASCLK in a data transfer, assuming the MSB, that is, the write bit, has been set to 1. If the ADC control register is programmed to use the shadow register, writing of information to the shadow register takes place on all 16 ASCLK falling edges in the next serial transfer (see Figure 72). The shadow register is updated on the rising edge of $\overline{\text{ASYNC}}$ and the track-and-hold begins to track the first channel selected in the sequence.

If the weak/$\overline{\text{TRI}}$ bit in the ADC control register is set to 1, rather than returning to true three-state upon the 16th ASCLK falling edge, the ADOUT line is instead pulled weakly to the logic level corresponding to ADD3 of the next serial transfer. This is done to ensure that the MSB of the next serial transfer is set up in time for the first ASCLK falling edge after the $\overline{\text{ASYNC}}$ falling edge. If the weak/$\overline{\text{TRI}}$ bit is set to 0 and the ADOUT line has been in true three-state between conversions, then depending on the particular DSP or microcontroller interfacing to the ADC, the ADD3 address bit may not be set up in time for the DSP/microcontroller to clock it in successfully. In this case, ADD3 is only driven from the falling edge of $\overline{\text{ASYNC}}$ and must then be clocked in by the DSP on the following falling edge of ASCLK. However, if the weak/$\overline{\text{TRI}}$ bit had been set to 1, then although ADOUT is driven with the ADD3 address bit from the last conversion, it is nevertheless so weakly driven that another device may still take control of the bus. It does not lead to a bus contention (for example, a 10 kΩ pull-up or pull-down resistor would be sufficient to overdrive the logic level of ADD3 between conversions), and all 16 channels may be identified. However, if this does happen and another device takes control of the bus, it is not guaranteed that ADOUT becomes fully driven to ADD3 again in time for the read operation when control of the bus is taken back.

This is especially useful if using an automatic sequence mode to identify to which channel each result corresponds. Obviously, if only the first eight channels are in use, the ADD3 address bit does not need to be decoded, and whether it is successfully clocked in as a 1 or 0 does not matter as long as it is still counted by the DSP/microcontroller as the MSB of the 16-bit serial transfer.

Table 21. ADC Control Register

MSB											LSB
DB11	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
Write	SEQ	ADD3	ADD2	ADD1	ADD0	PM1	PM0	Shadow	Weak/$\overline{\text{TRI}}$	Range	Coding

Table 22. ADC Control Register Bit Functions

Bit	Name	Description
11	Write	The value written to this bit of the control register determines whether the following 11 bits are loaded to the control register or not. If this bit is a 1, the following 11 bits are written to the control register; if it is a 0, the remaining 11 bits are not loaded to the control register, therefore it remains unchanged.
10	SEQ	The SEQ bit in the control register is used in conjunction with the shadow bit to control the use of the sequencer function and to access the shadow register (see Table 25).
9:6	ADD3:ADD0	These four address bits are loaded at the end of the current conversion sequence and select which analog input channel is to be converted on in the next serial transfer, or can select the final channel in a consecutive sequence, as described in Table 25. The selected input channel is decoded as shown in Table 23. The address bits corresponding to the conversion result are also output on ADOUT prior to the 12 bits of data (see the Serial Interface section). The next channel to be converted on is selected by the mux on the 14th ASCLK falling edge.
5, 4	PM1, PM0	These two power management bits decode the mode of operation of the ADC, as shown in Table 24.
3	Shadow	The shadow bit in the control register is used in conjunction with the SEQ bit to control the use of the sequencer function and access the shadow register (see Table 25).
2	Weak/$\overline{\text{TRI}}$	This bit selects the state of the ADOUT line at the end of the current serial transfer. If it is set to 1, the ADOUT line is weakly driven to the ADD3 channel address bit of the ensuing conversion. If this bit is set to 0, ADOUT returns to three-state at the end of the serial transfer. See the Serial Interface section for more details.
1	Range	This bit selects the analog input range to be used on the ADC. If it is set to 0, then the analog input range extends from 0 V to $2 \times V_{REFA}$. If it is set to 1, then the analog input range extends from 0 V to V_{REFA} (for the next conversion). For 0 V to $2 \times V_{REFA}$, $ADCV_{DD}$ = 4.75 V to 5.25 V.
0	Coding	This bit selects the type of output coding the ADC uses for the conversion result. If this bit is set to 0, the output coding for the ADC is twos complement. If this bit is set to 1, the output coding from the ADC is straight binary (for the next conversion).

Table 23. ADC Channel Selection

ADD3	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	VIN0
0	0	0	1	VIN1
0	0	1	0	VIN2
0	0	1	1	VIN3
0	1	0	0	VIN4
0	1	0	1	VIN5
0	1	1	0	VIN6
0	1	1	1	VIN7
1	0	0	0	VIN8
1	0	0	1	VIN9
1	0	1	0	VIN10
1	0	1	1	VIN11
1	1	0	0	VIN12
1	1	0	1	VIN13
1	1	1	0	VIN14
1	1	1	1	VIN15

Table 24. ADC Power Mode Selection

PM1	PM0	Mode
1	1	Normal operation. In this mode, the ADC remains in full power mode regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the ADC.
1	0	Full shutdown. In this mode, the ADC is in full shut down mode, with all circuitry on the ADC powered down. The ADC retains the information in the control register while in full shutdown. The ADC remains in full shutdown until these bits are changed in the control register.
0	1	Autoshutdown. In this mode, the ADC automatically enters shutdown mode at the end of each conversion when the control register is updated. Wake-up time from shutdown is 1 µs and the user should ensure that 1 µs has elapsed before attempting to perform a valid conversion on the ADC in this mode.
0	0	Autostandby. In this standby mode, portions of the ADC are powered down, but the on-chip bias generator remains powered up. This mode is similar to autoshutdown and allows the ADC to power up within one dummy cycle, that is, 1 µs with a 20 MHz ASCLK.

ADC Sequencer Operation

The configuration of the SEQ and shadow bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table 25 outlines the four modes of operation of the sequencer.

Table 25. ADC Sequence Selection

SEQ	Shadow	Sequence Type
0	0	This configuration means the sequence function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits, ADD0 to ADD3, in each prior write operation. This mode of operation reflects the normal operation of a multichannel ADC, without sequencer function being used, where each write to the ADC selects the next channel for conversion (see Figure 69).
0	1	This configuration selects the shadow register for programming. After the write to the control register, the following write operation loads the contents of the shadow register. This programs the sequence of channels to be converted on continuously with each successive valid $\overline{\text{ASYNC}}$ falling edge (see the shadow register, Table 26, and Figure 70). The channels selected need not be consecutive.
1	0	If the SEQ and shadow bits are set in this way, the sequence function is not interrupted upon completion of the write operation. This allows other bits in the control register to be altered while in a sequence without terminating the cycle.
1	1	This configuration is used in conjunction with the channel address bits, ADD3 to ADD0, to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel, as determined by the channel address bits in the control register (see Figure 71).

ADC Shadow Register

The shadow register on the ADC is a 16-bit, write-only register. Data is loaded from the ADIN pin of the ADC on the falling edge of ASCLK. The data is transferred on the ADIN line at the same time as a conversion result is read from the ADC. This requires 16 serial falling edges for the data transfer. The information is clocked into the shadow register, provided that the SEQ and shadow bits were set to 0 and 1, respectively, in the previous write to the control register. MSB denotes the first bit in the data stream. Each bit represents an analog input from Channel 0 through to Channel 15. A sequence of channels can be selected through which the ADC cycles with each consecutive $\overline{\text{ASYNC}}$ falling edge after the write to the shadow register. To select a sequence of channels, the associated channel bit must be set for each analog input. The ADC continuously cycles through the selected channels in ascending order, beginning with the lowest channel, until a write operation occurs (that is, the write bit is set to 1) with the SEQ and shadow bits configured in any way except 1, 0 (see Table 25). The bit functions are outlined in Table 26.

Figure 69 reflects the normal operation of a multichannel ADC, where each serial transfer selects the next channel for conversion. In this mode of operation, the sequencer function is not used.

Figure 70 shows how to program the ADC to continuously convert on a particular sequence of channels. To exit this mode of operation and revert back to the normal mode of operation of a multichannel ADC (as outlined in Figure 69), ensure the write bit = 1 and the SEQ = shadow = 0 on the next serial transfer.

Figure 71 shows how a sequence of consecutive channels can be converted without having to program the shadow register or write to the ADC on each serial transfer. Again, to exit this mode of operation and revert back to the normal mode of operation of a multichannel ADC (as outlined in Figure 69), ensure the write bit = 1 and the SEQ = shadow = 0 on the next serial transfer.

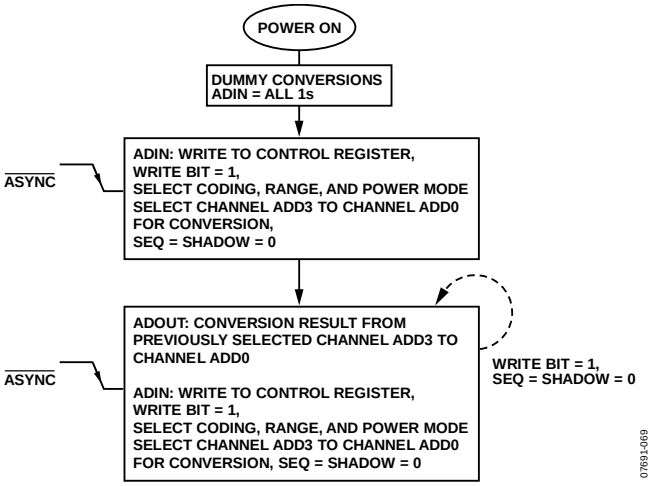


Figure 69. Sequence Function Not Used

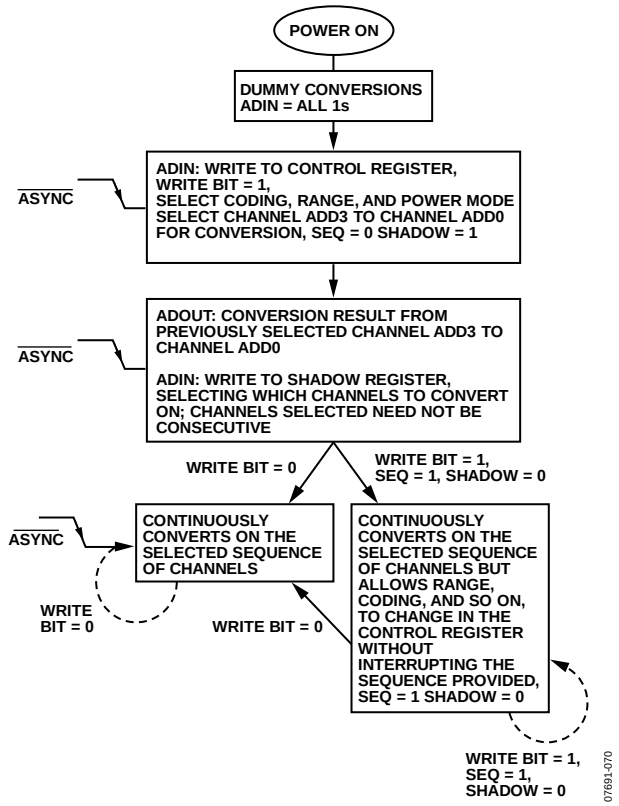


Figure 70. Continuous Conversions

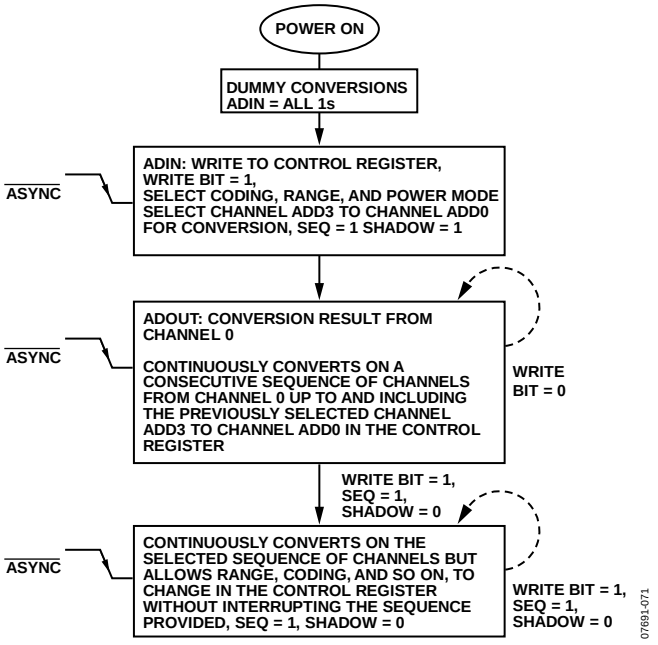


Figure 71. Continuous Conversion Without Programming the Shadow Register

Table 26. ADC Shadow Register Bits

MSB															LSB
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
VIN0	VIN1	VIN2	VIN3	VIN4	VIN5	VIN6	VIN7	VIN8	VIN9	VIN10	VIN11	VIN12	VIN13	VIN14	VIN15

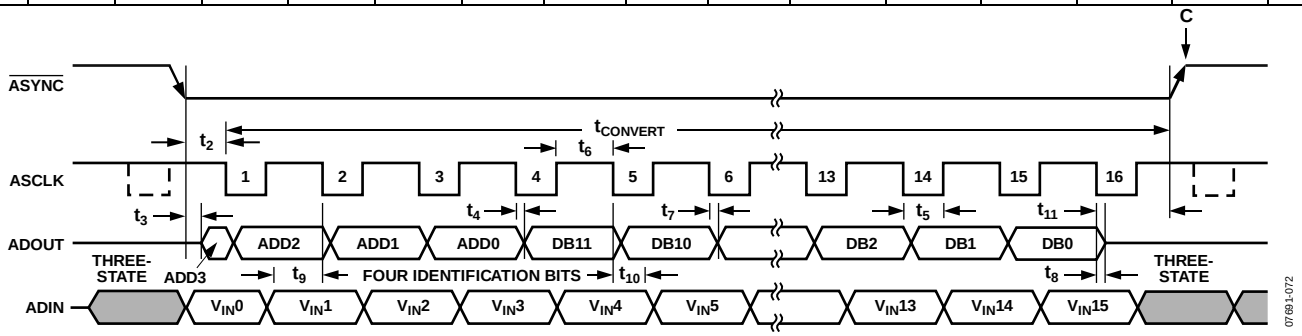


Figure 72. Writing to Shadow Register Timing Diagram

ADC Power vs. Throughput Rate

By operating the ADC in autoshutdown or autostandby mode, the average power consumption of the ADC decreases at lower throughput rates. Figure 73 shows how, as the throughput rate is reduced, the ADC remains in its shutdown state longer and the average power consumption over time drops accordingly.

For example, if the ADC is operated in a continuous sampling mode with a throughput rate of 100 kSPS and an ASCLK of 20 MHz, with PM1 = 0 and PM0 = 1 (that is, the device is in autoshutdown mode), the power consumption is calculated as follows: the maximum power dissipation during normal operation is 12.5 mW. If the power-up time from autoshutdown is one dummy cycle, that is, 1 µs, and the remaining conversion time is another cycle, that is, 1 µs, the ADC dissipates 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the ADC remains in shutdown mode. The ADC dissipates 2.5 µW for the remaining 8 µs of the conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is

$$\frac{2}{10} \times 12.5\,\text{mW} + \frac{8}{10} \times 2.5\,\mu\text{W} = 2.502\,\text{mW}$$

When operating the ADC in autostandby mode, PM1 = PM0 = 0 at 5 V, 100 kSPS, the ADC power dissipation is calculated as follows: the maximum power dissipation is 12.5 mW at 5 V during normal operation. The power-up time from autostandby is one dummy cycle, 1 µs, and the remaining conversion time is another dummy cycle, 1 µs. The ADC dissipates 12.5 mW for 2 µs during each conversion cycle. For the remainder of the conversion cycle, 8 µs, the ADC remains in standby mode dissipating 460 µW for 8 µs. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each conversion cycle is

$$\frac{2}{10} \times 12.5\,\text{mW} + \frac{8}{10} \times \mu\text{W} = 2.868\,\text{mW}$$

Figure 73 shows the power vs. throughput rate when using the autoshutdown mode and autostandby mode with 5 V supplies. At the lower throughput rates, power consumption for the autoshutdown mode is lower than that for the autostandby mode, with the ADC dissipating less power when in shutdown compared to standby. However, as the throughput rate is increased, the ADC spends less time in power-down states; thus, the difference in power dissipated is negligible between modes.

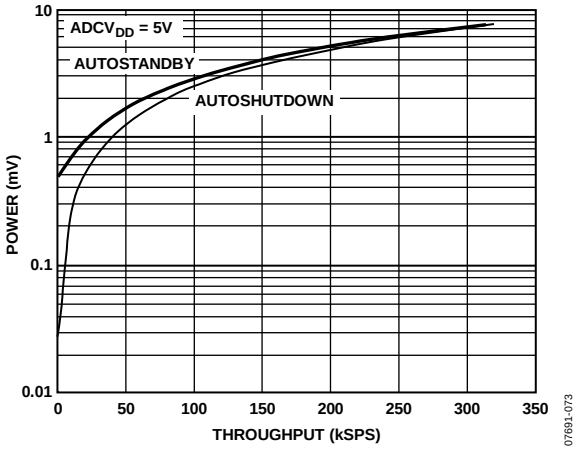


Figure 73. Power vs. Throughput Rate in Autoshutdown and Autostandby Mode

OUTLINE DIMENSIONS

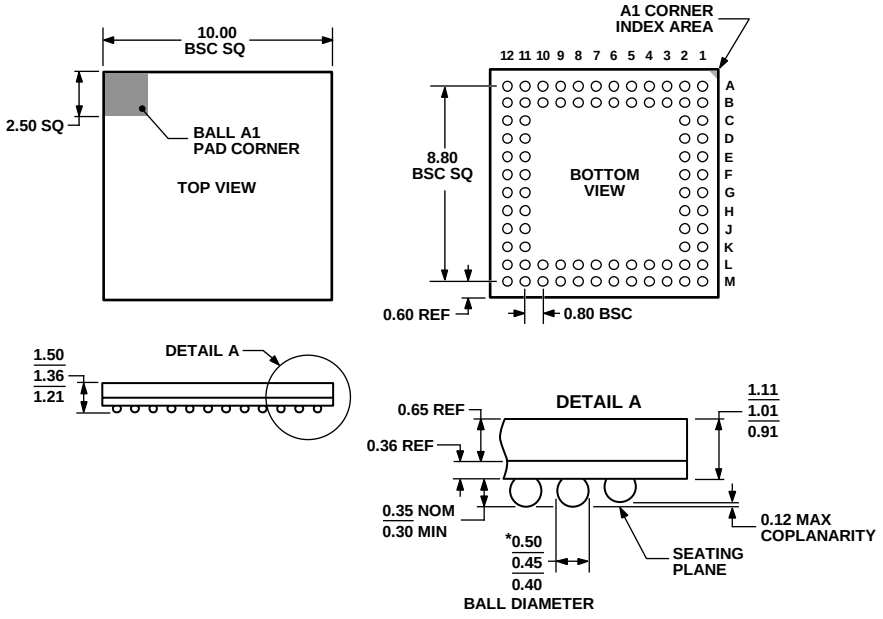


Figure 74. 80-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5590BBC	−40°C to +85°C	80-Ball CSP_BGA	BC-80-2
AD5590BBCZ	−40°C to +85°C	80-Ball CSP_BGA	BC-80-2
EVAL-AD5590EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

©2008–2011 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D07691-0-7/11(A)