LMV82x Single/Dual/Quad, Low Voltage, Low Power, RRO, 5 MHz Operational Amplifiers

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - LMV822-Q1 And LMV824-Q1 Are Available in Automotive AEC-Q100 Grade 1 Version
- For Vs = 5 V, Typical Supply Values Unless Otherwise Noted
- LMV824 Available With Extended Temperature Range to 125°C
- Small SC70-5 Package 2.0 x 1.25 x 0.95 mm
- Specified Performance At 2.5 V, 2.7 V and 5 V
- V_{OS} 3.5 mV (Max)
- TCV_{OS} 1 uV/°C
- Gain Bandwidth Product At 2.7 V, 5 MHz
- I_{Supply} At 2.7 V Supply, 220 µA per Amplifier
- Slew Rate 1.4 V/µs (Min)
- CMRR 90 dB
- PSRR 85 dB
- V_{CM} At 5 V Supply, -0.3 V to 4.3 V
- Rail to Rail Output (RRO)
  - 600 Ω Load, 160 mV From Rail
  - 10 kΩ Load, 55 mV From Rail
- Stable Performance with Capacitive Loads

2 Applications

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

3 Description

The LMV821/LMV822/LMV824 op amps bring performance and economy to low voltage, low power systems. With a 5 MHz unity-gain frequency, at 2.7 V supply, and a 1.4 V/µs slew rate, the quiescent current is only 220 µA per amplifier. They provide rail to rail output (RRO) swing into 600 Ω load. The input common-mode voltage range includes ground and the maximum input offset voltage is 3.5 mV. They are also capable of easily driving large capacitive loads as indicated in the applications section.

The LMV821 single op amp is available in the tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5. The LMV824NDGV is specified over the extended industrial temperature range and is in a TVSOP package.

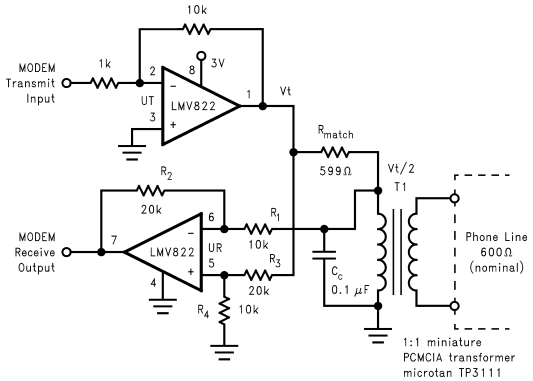
Overall, the LMV821/LMV822/LMV824 devices are low voltage, low power and performance op amps designed for a wide range of applications at an economical price.

Device Information(1)

DEVICE NAME	PACKAGE	BODY SIZE
LMV821-N	SOT23 (5)	2.92 mm x 1.60 mm
	SC70 (5)	2.00 mm x 1.25 mm
LMV822-N	SOIC (8)	4.90 mm x 3.91 mm
	VSSOP (8)	3.00 mm x 3.00 mm
LMV822-N-Q1	VSSOP (8)	3.00 mm x 3.00 mm
LMV824-N	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm x 4.40 mm
LMV824-N-Q1	TSSOP (14)	5.00 mm x 4.40 mm
LMV824I	TVSOP (14)	4.40 mm x 3.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Telephone Line Transceiver for PCMCIA Modem Card



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2014) to Revision I — **Page**

- Changed Features Section ... 1
- Moved Storage Temperature from Handling Ratings Table which has been renamed ESD Table ... 5
- Changed Handling Ratings Table to ESD Ratings Table Format - no data changed ... 5
- Added Thermal Information ... 5
- Changed and updated Electrical Tables ... 9

Changes from Revision G (November 2013) to Revision H — **Page**

- Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, Mechanical, Packaging, and Orderable Information ... 1
- Added Added new LMV824I throughout datasheet ... 1
- Deleted "Refer to application note AN-397 for detailed explanation." - no such appnote ... 23
- Added Added Section ... 28
- Added Added Section ... 28

Changes from Revision D (February 2013) to Revision G — **Page**

- Added new part ... 1
- Added new device ... 1
- Added new device ... 5
- Added new device ... 6
- Added new device ... 9
- Added new device ... 9

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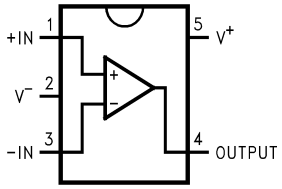
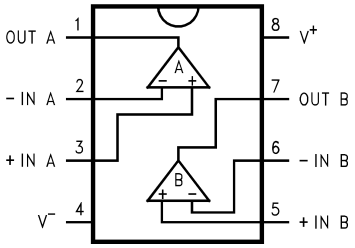
5 Pin Configuration and Functions

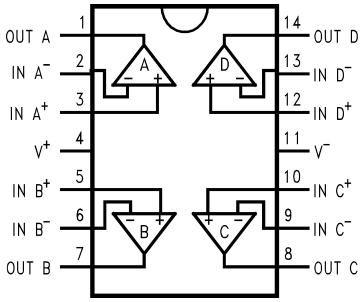
5-Pin SC70-5/SOT23-5
DCK0005A, DBV0005A Packages
Top View



8-Pin SOIC/VSSOP
D0008A, DGK0008A Packages
Top View



14-Pin SOIC/TSSOP/TVSOP
D0014A, PW0014A, DGV0014A Packages
Top View



Pin Functions

PIN NAME	I/O	DESCRIPTION
+IN	I	Non-Inverting Input
-IN	I	Inverting Input
OUT	O	Output
V-	P	Negative Supply
V+	P	Positive Supply

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6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

	MIN	MAX	UNIT
Differential Input Voltage	V^-	V^+	V
Supply Voltage ($V^+ - V^-$)	–0.3	5.5	V
Output Short Circuit to V^+ (3)		See (3)	
Output Short Circuit to V^- (3)		See (3)	
Soldering Information			
Infrared or Convection (20 sec)		235	°C
Junction Temperature (4)		150	°C
Storage Temperature T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) (2)(3)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1) LMV821	±1500	
		Machine Model (MM) (4)	±200	

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series wth 100 pF.
(3) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification for Q grade devices.
(4) Machine model, 200Ω in series with 100 pF.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage		2.5		5.5	V
Temperature Range	LMV821, LMV822, LMV824	–40		85	°C
	LMV822-Q1, LMV824I and LMV824-Q1	–40		125	

6.4 Thermal Information, 5 Pins (1)

THERMAL METRIC (1)		DCK SC70-5 PACKAGE	DBV SOT23-5 PACKAGE	UNIT
		5 PIN	5 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	263.4	217.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.8	142.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	49.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	29.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.2	48.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Thermal Information, 8 Pins(1)

THERMAL METRIC(1)		D SOIC PACKAGE	DGK VSSOP PACKAGE	UNIT
		8 PIN	8 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.6	193.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.9	84.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	114.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.0	21.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.6	113.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information, 14 Pins(1)

THERMAL METRIC(1)		D SOIC PACKAGE	PW TSSOP PACKAGE	DGV TVSOP PACKAGE	UNIT
		14 PIN	14 PIN	14 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.7	135.6	148.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.9	63.8	67.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.1	77.4	77.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.5	13.0	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	76.8	76.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 DC Electrical Characteristics 2.7V

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage	LMV821/822/822-Q1/824		1	3.5	mV
		LMV821/822/822-Q1/824, Over Temperature			4	
		LMV824-Q1/LMV824I		1		
		LMV824-Q1/LMV824I, Over Tempeature			5.5	
TCV_{OS}	Input Offset Voltage Average Drift			1		µV/°C
I_B	Input Bias Current			30	90	nA
		Over Temperature			140	
I_{OS}	Input Offset Current			0.5	30	nA
		Over Temperature			50	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	70	85		dB
		0V ≤ V_{CM} ≤ 1.7V, Over Temperature	68			
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/LMV824I	75	85		dB
		1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/LMV824I, Over Temperature	70			
		LMV822-Q1	75	85		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

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DC Electrical Characteristics 2.7V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/LMV824I	73	85		dB
		-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/LMV824I, Over Temperature	70			
		LMV822-Q1	73	85		
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		–0.3	–0.2	V
			1.9	2.0		
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 1.35V, V_O = 1.35V to 2.2V; LMV821/822/824	90	100		dB
		Sourcing, R_L = 600Ω to 1.35V, V_O = 1.35V to 2.2V; LMV821/822/824, Over Temperature	85			
		LMV822-Q1/LMV824-Q1/LMV824I	90	100		
		Sinking, R_L = 600Ω to 1.35V, V_O = 1.35V to 0.5V LMV821/822/824	85	90		dB
		Sinking, R_L = 600Ω to 1.35V, V_O = 1.35V to 0.5V LMV821/822/824, Over Temperature	80			
		LMV824I	85	90		
		LMV824I, Over Temperature	78			
		LMV822-Q1/LMV824-Q1	85	90		
		Sourcing, R_L =2kΩ to 1.35V, V_O = 1.35V to 2.2V; LMV821/822/824	95	100		dB
		Sourcing, R_L =2kΩ to 1.35V, V_O = 1.35V to 2.2V; LMV821/822/824, Over Temperature	90			
		LMV822-Q1/LMV824-Q1/LMV824I	95	100		
		Sinking, R_L = 2kΩ to 1.35V, V_O = 1.35V to 0.5V LMV821/822/824	90	95		dB
		Sinking, R_L = 2kΩ to 1.35V, V_O = 1.35V to 0.5V LMV821/822/824, Over Temperature	85			
		LMV822-Q1/LMV824-Q1/LMV824I	90	95		
V_O	Output Swing	V^+ = 2.7V, R_L= 600Ω to 1.35V	2.50	2.58		V
				0.13	0.20	
		V^+ = 2.7V, R_L= 600Ω to 1.35V, Over Temp	2.40		0.30	
		V^+ = 2.7V, R_L= 2kΩ to 1.35V	2.60	2.66		V
				0.08	0.120	
		V^+ = 2.7V, R_L= 2kΩ to 1.35V, Over Temp	2.50		0.200	
I_O	Output Current	Sourcing, V_O = 0V	12	16		mA
		Sinking, V_O = 2.7V	12	26		

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DC Electrical Characteristics 2.7V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_S	Supply Current	LMV821 (Single)		0.22	0.3	mA
		LMV821, Over Temperature			0.5	
		LMV822 (Dual)		0.45	0.6	mA
		LMV822, Over Temperature			0.8	
		LMV824 (Quad)		0.72	1.0	mA
		LMV824, Over Temperature			1.2	

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6.8 DC Electrical Characteristics 2.5V

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.5V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.25V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		CONDITION	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage	LMV821/822/822-Q1/824		1	3.5	mV
		LMV821/822/822-Q1/824, Over Temperature			4	
		LMV824-Q1/LMV824I		1		
		LMV824-Q1/LMV824I, Over Temperature			5.5	
V_O	Output Swing	V^+ = 2.5V, R_L = 600Ω to 1.25V	2.30	2.37		V
				0.13	0.20	
		V^+ = 2.5V, R_L = 600Ω to 1.25V, Over Temperature	2.20		0.30	
		V^+ = 2.5V, R_L = 2kΩ to 1.25V	2.40	2.46		V
				0.08	0.12	
		V^+ = 2.5V, R_L = 2kΩ to 1.25V, Over Temperature	2.30		0.20	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

6.9 AC Electrical Characteristics 2.7V

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
SR	Slew Rate	See (3)		1.5		V/µs
GBW	Gain-Bandwdth Product			5		MHz
Φ_m	Phase Margin			61		Deg.
G_m	Gain Margin			10		dB
	Amp-to-Amp Isolation	See (4)		135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V		28		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		0.1		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}		0.01%		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) V^+ = 5V. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, V^+ = 5V and R_L = 100kΩ connected to 2.5V. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}.

6.10 DC Electrical Characteristics 5V

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5 V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{OS}	Input Offset Voltage	LMV821/822/822-Q1/824		1	3.5	mV
		LMV821/822/822-Q1/824, Over Temperature			4.0	
		LMV824-Q1/LMV824I		1		
		LMV824-Q1/ LMV824I, Over Temperature			5.5	
TCV_{OS}	Input Offset Voltage Average Drift			1		µV/°C

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.

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DC Electrical Characteristics 5V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5 V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
I_B	Input Bias Current			40	100	nA
		Over Temperature			150	
I_{OS}	Input Offset Current			0.5	30	nA
		Over Temperature			50	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V	72	90		dB
		0V ≤ V_{CM} ≤ 4.0V, Over Temperature	70			
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/824I		85	75	dB
		1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/824I, Over Temperature			70	
		LMV822-Q1	75	85		
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/824I	73	85		dB
		-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V LMV821/822/824/824-Q1/824I	70			
		LMV822-Q1	73	85		
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		-0.3	-0.2	V
			4.2	4.3		V
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 2.5V, V_O = 2.5V to 4.5V; LMV821/822/824	95	105		dB
		Sourcing, R_L = 600Ω to 2.5V, V_O = 2.5V to 4.5V; LMV821/822/824, Over Temperature	90			
		LMV822-Q1/LMV824-Q1/LMV824I	95	105		
		Sinking, R_L = 600Ω to 2.5V, V_O = 2.5V to 0.5V LMV821/822/824	95	105		dB
		Sinking, R_L = 600Ω to 2.5V, V_O = 2.5V to 0.5V LMV821/822/824, Over Temperature	90			
		LMV824I	95	105		
		LMV824I, Over Temperature	82			
		LMV822-Q1/LMV824-Q1	95	105		
		Sourcing, R_L =2kΩ to 2.5V, V_O = 2.5V to 4.5V; LMV821/822/824	95	105		dB
		Sourcing, R_L =2kΩ to 2.5V, V_O = 2.5V to 4.5V; LMV821/822/824, Over Temperature	90			
		LMV822-Q1/LMV824-Q1/LMV824I	95	105		
		Sinking, R_L = 2kΩ to 2.5V, V_O = 2.5V to 0.5V LMV821/822/824	95	105		dB
		Sinking, R_L = 2kΩ to 2.5V, V_O = 2.5V to 0.5V LMV821/822/824, Over Temperature	90			
		LMV822-Q1/LMV824-Q1/LMV824I	95	105		

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DC Electrical Characteristics 5V (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5 V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_O	Output Swing	V^+ = 5V, R_L = 600Ω to 2.5V	4.75	4.84		V
		V^+ = 5V, R_L = 600Ω to 2.5V, Over Temperature	4.70			
		V^+ = 5V, R_L = 600Ω to 2.5V (LMV824-Q1, LMV824I)		4.84		
		V^+ = 5V, R_L = 600Ω to 2.5V (LMV824-Q1, LMV824I), Over Temperature	4.60			
		V^+ = 5V, R_L = 600Ω to 2.5V		0.17	0.250	V
		V^+ = 5V, R_L = 600Ω to 2.5V, Over Temperature			0.30	
		V^+ = 5V, R_L = 600Ω to 2.5V (LMV824-Q1, LMV824I)		0.17		
		V^+ = 5V, R_L = 600Ω to 2.5V (LMV824-Q1, LMV824I), Over Temperature			0.40	
		V^+ = 5V, R_L = 2kΩ to 2.5V	4.85	4.90		V
				0.10	0.15	
		V^+ = 5V, R_L = 2kΩ to 2.5V, Over Temperature	4.80		0.20	
I_O	Output Current	Sourcing, V_O = 0V	20	45		mA
		Sourcing, V_O = 0V, Over Temperature	15			
		Sourcing, V_O = 0V LMV824I	20	45		mA
		Sourcing, V_O = 0V LMV824I, Over Temperature	10			
		Sinking, V_O = 5V	20	40		mA
		Sinking, V_O = 5V, Over Temperature	15			
		Sinking, V_O = 5V LMV824I	20	40		mA
		Sinking, V_O = 5V LMV824I, Over Temperature	10			
I_S	Supply Current	LMV821 (Single)		0.30	0.4	mA
		LMV821, Over Temperature			0.6	
		LMV822 (Dual)		0.5	0.7	mA
		LMV822, Over Temperature			0.9	
		LMV824 (Quad)		1.0	1.3	mA
		LMV824, Over Temperature			1.5	
		LMV824I (Quad)		1.0	1.3	mA
		LMV824I, Over Temperature			1.6	

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6.11 AC Electrical Characteristics 5V

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5 V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. Temperature extremes are −40°C ≤ T_J ≤ 85°C for LMV821/822/824, and −40°C ≤ T_J ≤ 125°C for LMV822-Q1/LMV824-Q1/LMV824I.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
SR	Slew Rate	See (3)	1.4	2.0		V/μs min
GBW	Gain-Bandwdth Product			5.6		MHz
Φ_m	Phase Margin			67		Deg.
G_m	Gain Margin			15		dB
	Amp-to-Amp Isolation	See (4)		135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V		24		nV/√Hz
i_n	Input-Referred Current Noise	f = 1 kHz		0.25		pA/√Hz
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}		0.01%		

(1) All limits are ensured by testing or statistical analysis.
(2) Typical Values represent the most likely parametric norm.
(3) V^+ = 5V. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, V^+ = 5V and R_L = 100kΩ connected to 2.5V. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}.

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6.12 Typical Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

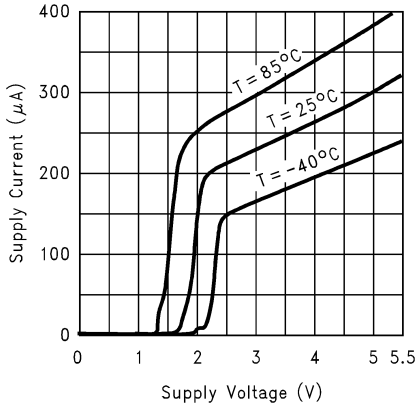

Figure 1. Supply Current vs. Supply Voltage (LMV821)

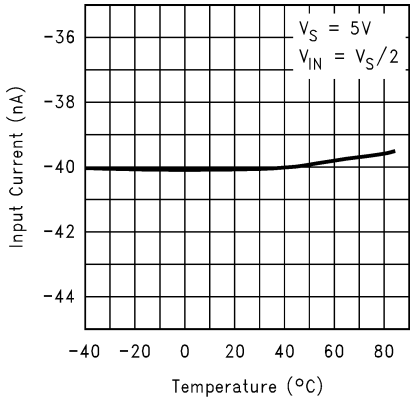

Figure 2. Input Current vs. Temperature

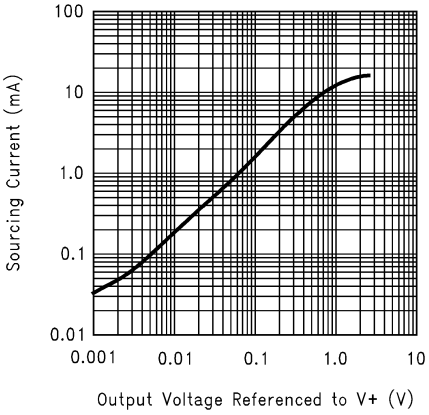

Figure 3. Sourcing Current vs. Output Voltage (V_S = 2.7V)

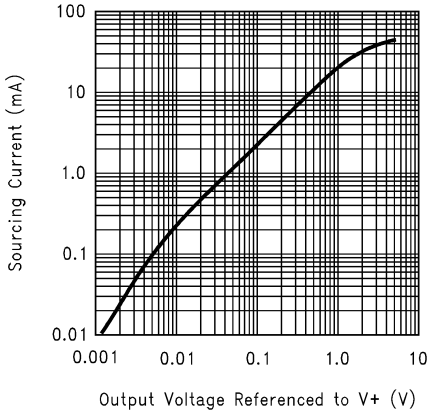

Figure 4. Sourcing Current vs Output Voltage (V_S = 5V)

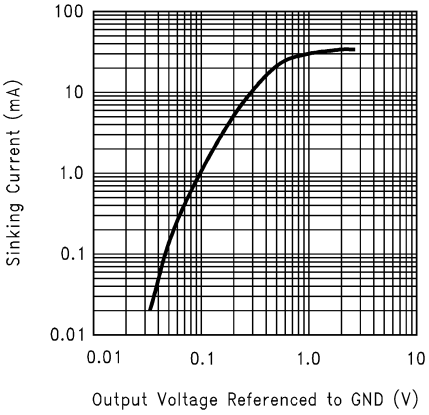

Figure 5. Sinking Current vs. Output Voltage (V_S = 2.7V)

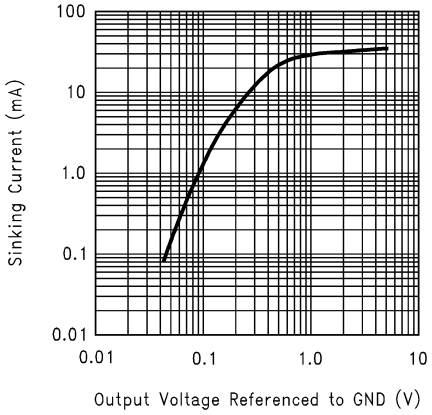

Figure 6. Sinking Current vs. Output Voltage (V_S = 5V)

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Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

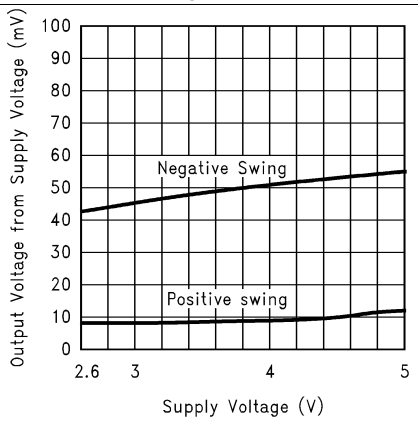

Figure 7. Output Voltage Swing vs. Supply Voltage (R_L = 10kΩ)

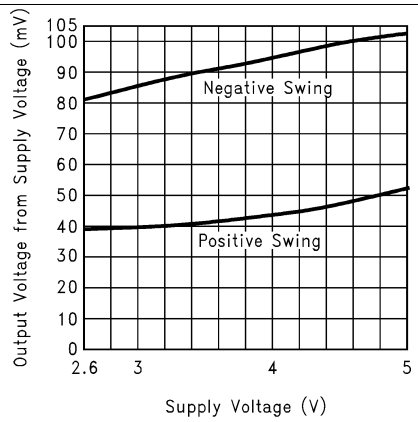

Figure 8. Output Voltage Swing vs. Supply Voltage (R_L = 2kΩ)

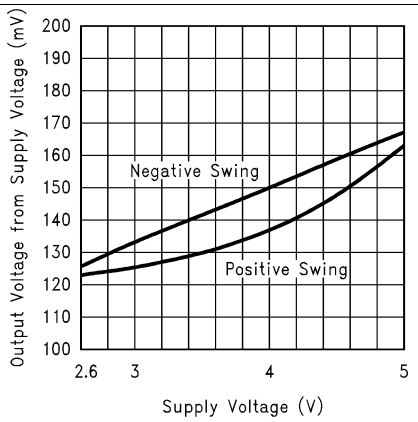

Figure 9. Output Voltage Swing vs. Supply Voltage (R_L = 600Ω)

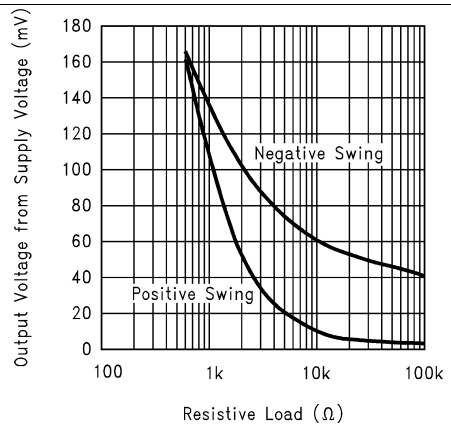

Figure 10. Output Voltage Swing vs. Load Resistance

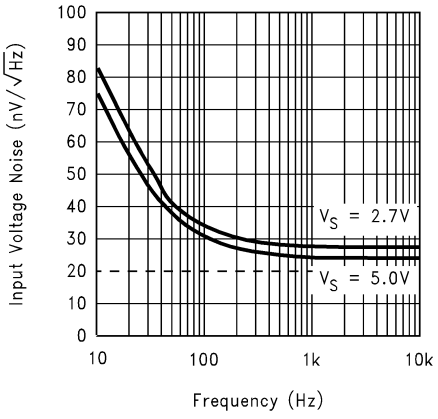

Figure 11. Input Voltage Noise vs. Frequency

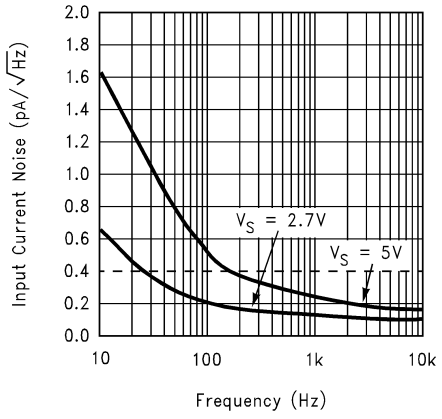

Figure 12. Input Current Noise vs. Frequency

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Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

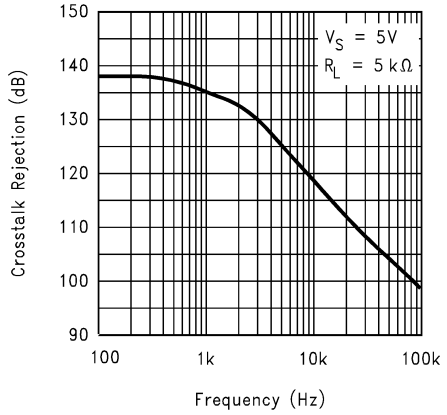

Figure 13. Crosstalk Rejection vs. Frequency

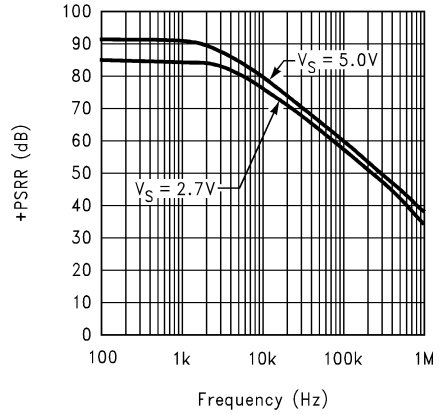

Figure 14. +PSRR vs. Frequency

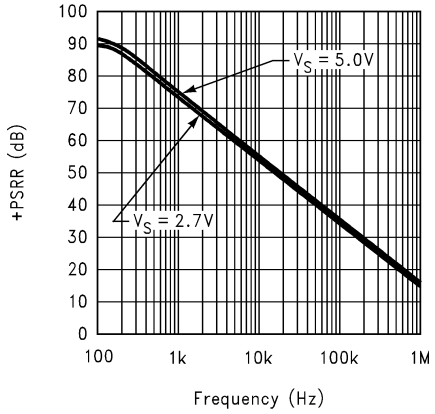

Figure 15. -PSRR vs. Frequency

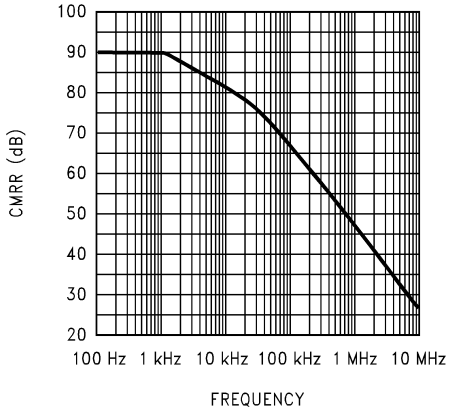

Figure 16. CMRR vs. Frequency

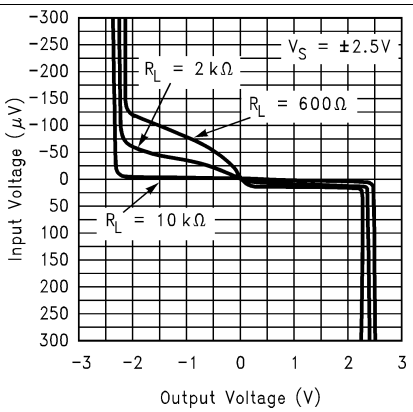

Figure 17. Input Voltage vs. Output Voltage

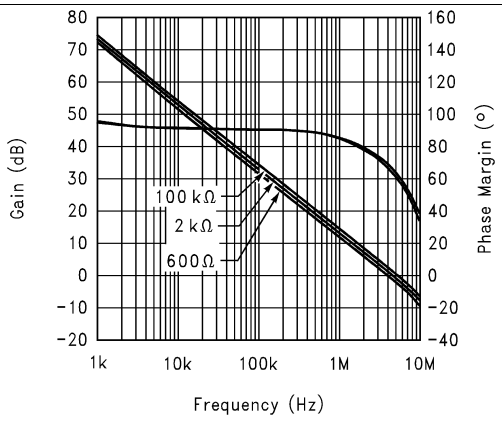

Figure 18. Gain and Phase Margin vs. Frequency (R_L = 100kΩ, 2kΩ, 600Ω) at 2.7V

Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

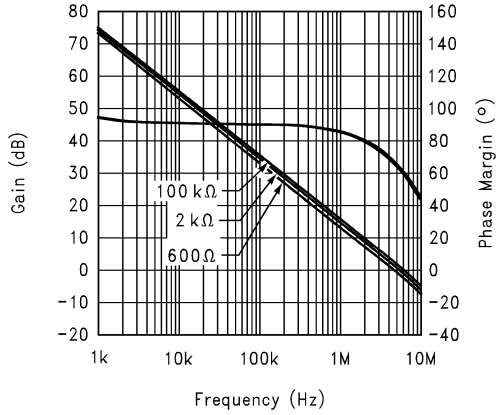

Figure 19. Gain and Phase Margin vs. Frequency (R_L = 100kΩ, 2kΩ, 600Ω) at 5V

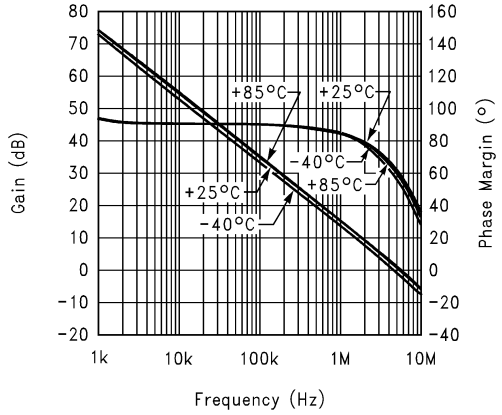

Figure 20. Gain and Phase Margin vs. Frequency (Temp.= 25, -40, 85°C, R_L = 10kΩ) at 2.7V

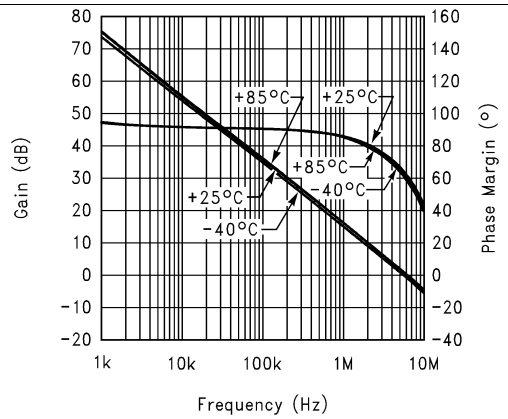

Figure 21. Gain and Phase Margin vs. Frequency (Temp.= 25, -40, 85 °C, R_L = 10kΩ) at 5V

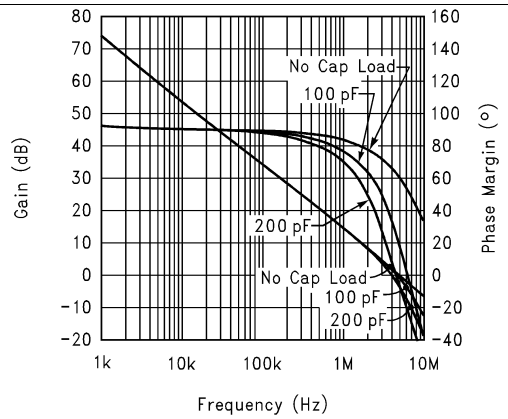

Figure 22. Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF, R_L = 10kΩ) at 2.7V

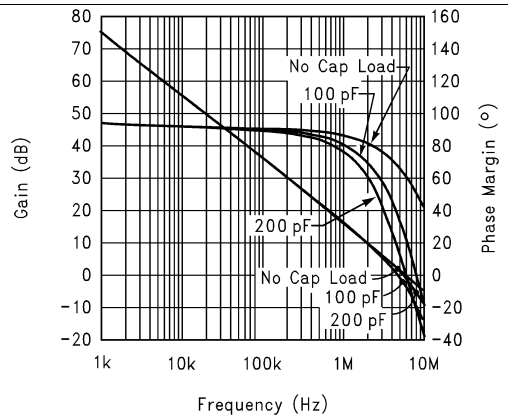

Figure 23. Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 10kΩ) at 5V

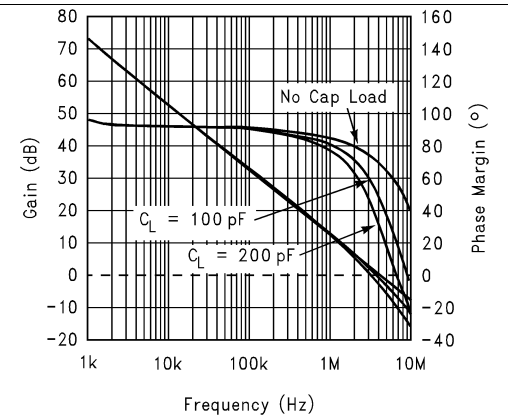

Figure 24. Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 600Ω) at 2.7V

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Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

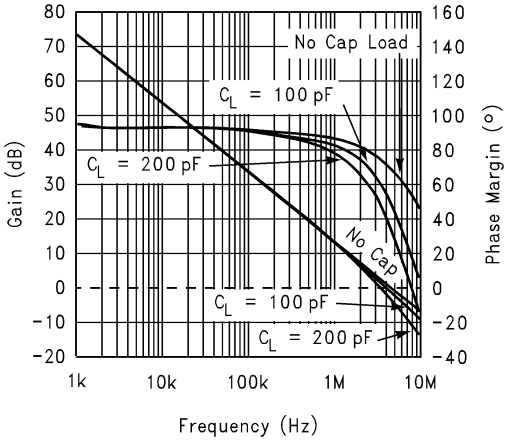

Figure 25. Gain and Phase Margin vs. Frequency (C_L = 100pF, 200pF, 0pF R_L = 600Ω) at 5V

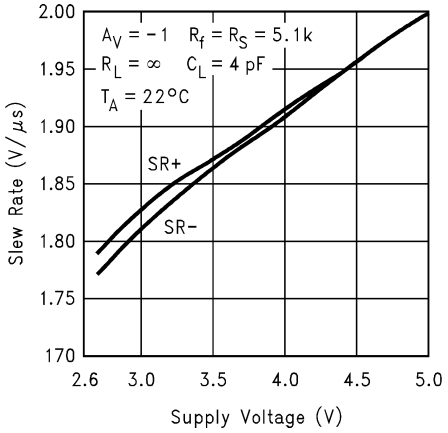

Figure 26. Slew Rate vs. Supply Voltage

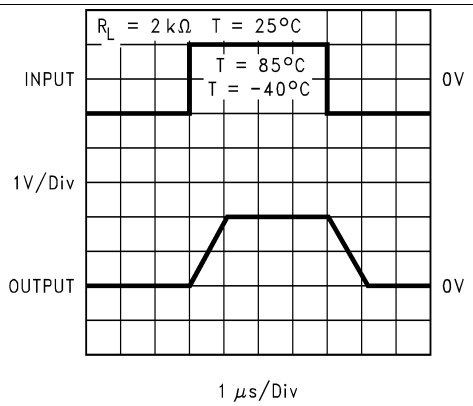

Figure 27. Non-Inverting Large Signal Pulse Response

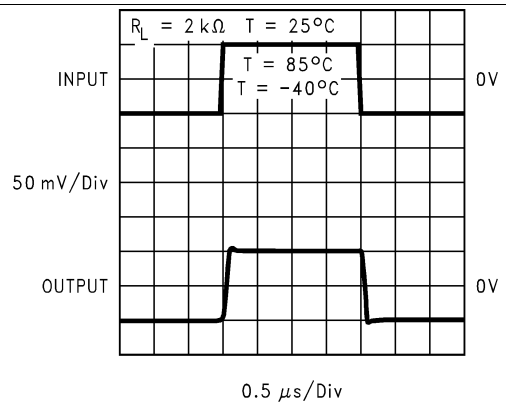

Figure 28. Non-Inverting Small Signal Pulse Response

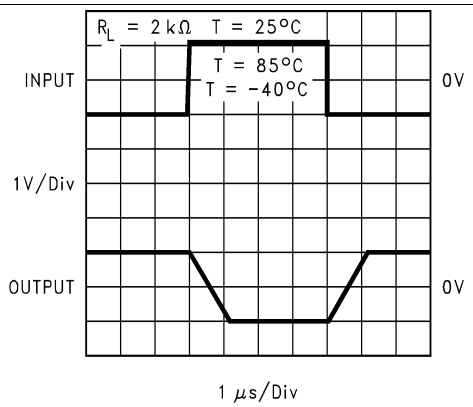

Figure 29. Inverting Large Signal Pulse Response

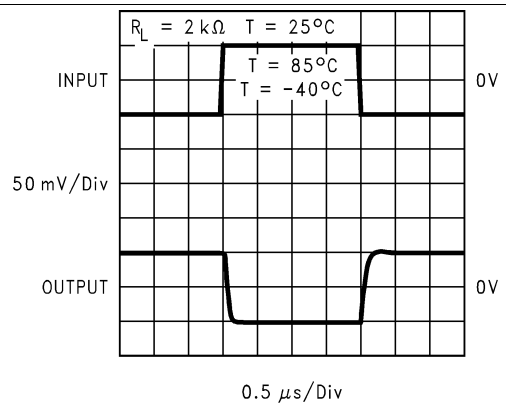

Figure 30. Inverting Small Signal Pulse Response

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Typical Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

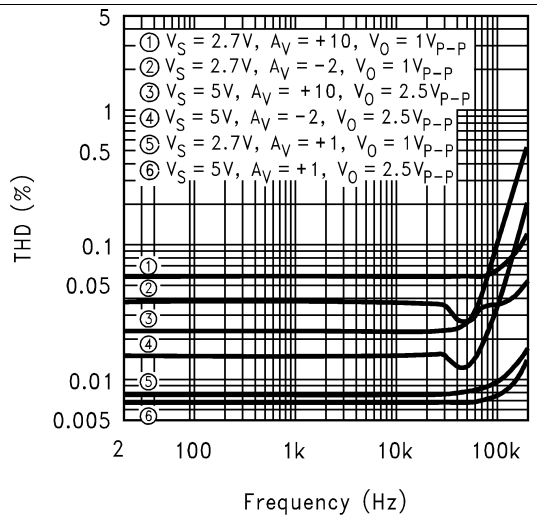

Figure 31. THD vs. Frequency

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7 Detailed Description

7.1 Overview

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a specified 1.4 V/µs slew rate, the quiescent current is only 220 µA/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600 Ω specified). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5 mV.

7.2 Functional Block Diagram

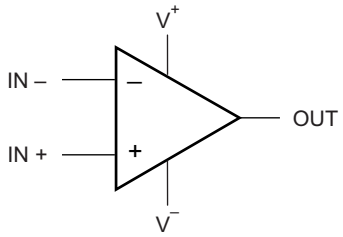

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Figure 32. (Each Amplifier)

7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (–IN). The amplifer amplifies only the difference in voltage between the two inpus, which is called the differential input voltage. The output voltage of the op-amp Vout is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \quad (1)$$

where A_{OL} is the open-loop gain of the amplifier, typically around 100dB (100,000x, or 10uV per Volt).

7.4 Device Functional Modes

This section covers the following design considerations:

1. Frequency and Phase Response Considerations
2. Unity-Gain Pulse Response Considerations
3. Input Bias Current Considerations

7.4.1 Frequency and Phase Response Considerations

The relationship between open-loop frequency response and open-loop phase response determines the closed-loop stability performance (negative feedback). The open-loop phase response causes the feedback signal to shift towards becoming positive feedback, thus becoming unstable. The further the output phase angle is from the input phase angle, the more stable the negative feedback will operate. Phase Margin (φ_m) specifies this output-to-input phase relationship at the unity-gain crossover point. Zero degrees of phase-margin means that the input and output are completely in phase with each other and will sustain oscillation at the unity-gain frequency.

The AC tables show φ_m for a no load condition. But φ_m changes with load. The Gain and Phase margin vs Frequency plots in the curve section can be used to graphically determine the φ_m for various loaded conditions. To do this, examine the phase angle portion of the plot, find the phase margin point at the unity-gain frequency, and determine how far this point is from zero degree of phase-margin. The larger the phase-margin, the more stable the circuit operation.

Device Functional Modes (continued)

The bandwidth is also affected by load. The graphs of Figure 33 and Figure 34 provide a quick look at how various loads affect the φ_m and the bandwidth of the LMV821/822/824 family. These graphs show capacitive loads reducing both φ_m and bandwidth, while resistive loads reduce the bandwidth but increase the φ_m. Notice how a 600Ω resistor can be added in parallel with 220 picofarads capacitance, to increase the φ_m 20°(approx.), but at the price of about a 100 kHz of bandwidth.

Overall, the LMV821/822/824 family provides good stability for loaded condition.

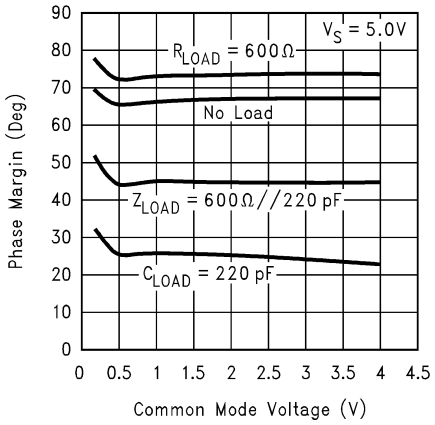

Figure 33. Phase Margin vs Common Mode Voltage for Various Loads

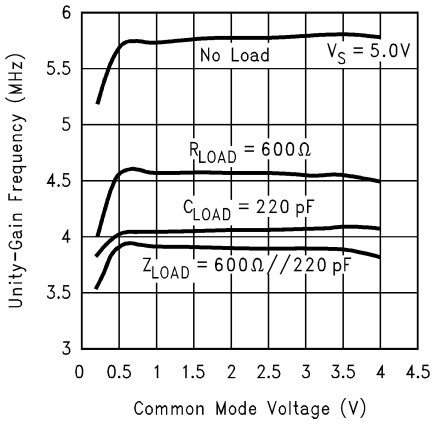

Figure 34. Unity-Gain Frequency vs Common Mode Voltage for Various Loads

7.4.2 Unity Gain Pulse Response Consideration

A pull-up resistor is well suited for increasing unity-gain, pulse response stability. For example, a 600 Ω pull-up resistor reduces the overshoot voltage by about 50%, when driving a 220 pF load. Figure 35 shows how to implement the pull-up resistor for more pulse response stability.

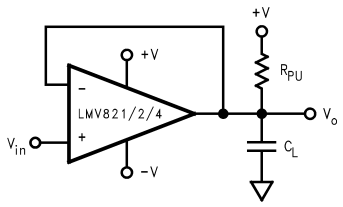

Figure 35. Using a Pull-up Resistor at the Output for Stabilizing Capacitive Loads

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Device Functional Modes (continued)

Higher capacitances can be driven by decreasing the value of the pull-up resistor, but its value shouldn't be reduced beyond the sinking capability of the part. An alternate approach is to use an isolation resistor as illustrated in Figure 36.

Figure 37 shows the resulting pulse response from a LMV824, while driving a 10,000 pF load through a 20Ω isolation resistor.

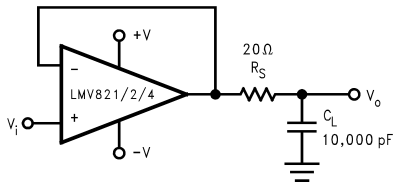

Figure 36. Using an Isolation Resistor to Drive Heavy Capacitive Loads

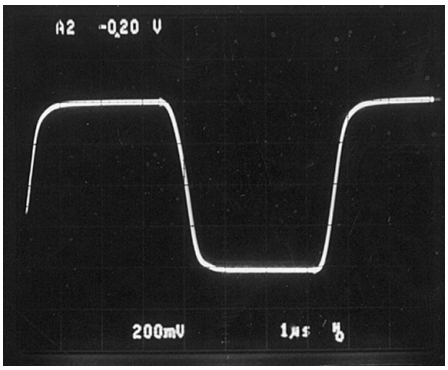

Figure 37. Pulse Response per Figure 36

7.4.3 Input Bias Current Consideration

Input bias current (I_B) can develop a somewhat significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 90 nA (max @ room) and R_F is 100 kΩ, then an offset of 9 mV will be developed (V_{OS}= I_B x R_F).Using a compensation resistor (R_C), as shown in Figure 38, cancels out this affect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner - typically 0.05 mV at room temp.

Device Functional Modes (continued)

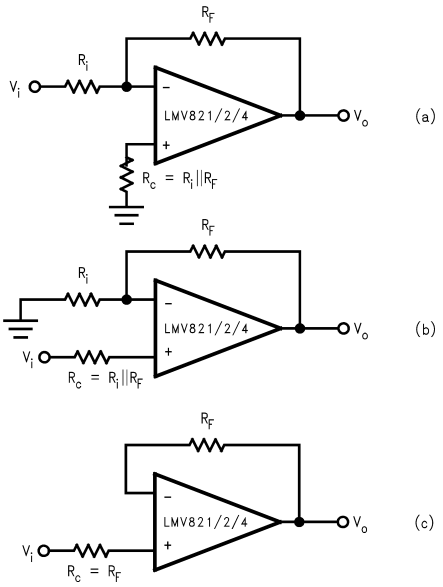

Figure 38. Canceling the Voltage Offset Effect of Input Bias Current

8 Application and Implementation

8.1 Application Information

The LMV82x bring performance and economy to low voltage/low power systems. They provide rail-to-rail output swing into heavy loads and are capable of driving large capacitive loads.

8.2 Typical Applications

8.2.1 Telephone-Line Transceiver

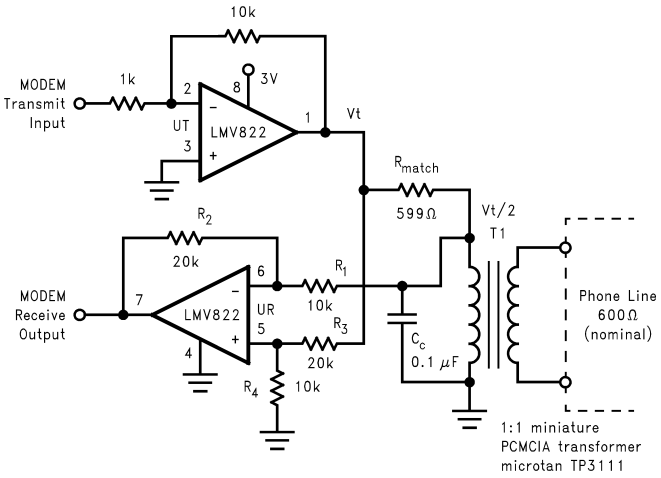

Figure 39. Telephone-Line Transceiver for a PCMCIA Modem Card

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Typical Applications (continued)

8.2.1.1 Design Requirements

The telephone-line transceiver of Figure 39 provides a full-duplexed connection through a PCMCIA, miniature transformer. The differential configuration of receiver portion (UR), cancels reception from the transmitter portion (UT). Note that the input signals for the differential configuration of UR, are the transmit voltage (V_T) and $V_T/2$. This is because R_{match} is chosen to match the coupled telephone-line impedance; therefore dividing V_T by two (assuming R1 >> R_{match}).

8.2.1.2 Detailed Design Procedure

The differential configuration of UR has its resistors chosen to cancel the V_T and $V_T/2$ inputs according to the following equation:

$$V_O = V_T \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) - \frac{V_T}{2}\left(\frac{R_2}{R_1}\right) = V_T \frac{1}{3}(3) - \frac{V_T}{2}(2) = 0 \quad (2)$$

Note that Cc is included for canceling out the inadequacies of the lossy, miniature transformer.

8.2.2 "Simple" Mixer (Amplitude Modulator)

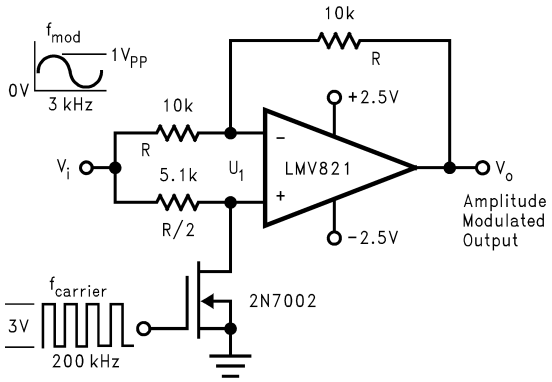

Figure 40. Amplitude Modulator Circuit

8.2.2.1 Design Requirements

The simple mixer can be applied to applications that utilize the Doppler Effect to measure the velocity of an object. The difference frequency is one of its output frequency components. This difference frequency magnitude ($/F_M$-$F_C/$) is the key factor for determining an object's velocity per the Doppler Effect. If a signal is transmitted to a moving object, the reflected frequency will be a different frequency. This difference in transmit and receive frequency is directly proportional to an object's velocity.

8.2.2.2 Detailed Design Procedure

The mixer of Figure 40 is simple and provides a unique form of amplitude modulation. Vi is the modulation frequency (F_M), while a +3V square-wave at the gate of Q1, induces a carrier frequency (F_C). Q1 switches (toggles) U1 between inverting and non-inverting unity gain configurations. Offsetting a sine wave above ground at Vi results in the oscilloscope photo of Figure 41.

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Typical Applications (continued)

8.2.2.3 Application Performance Plot

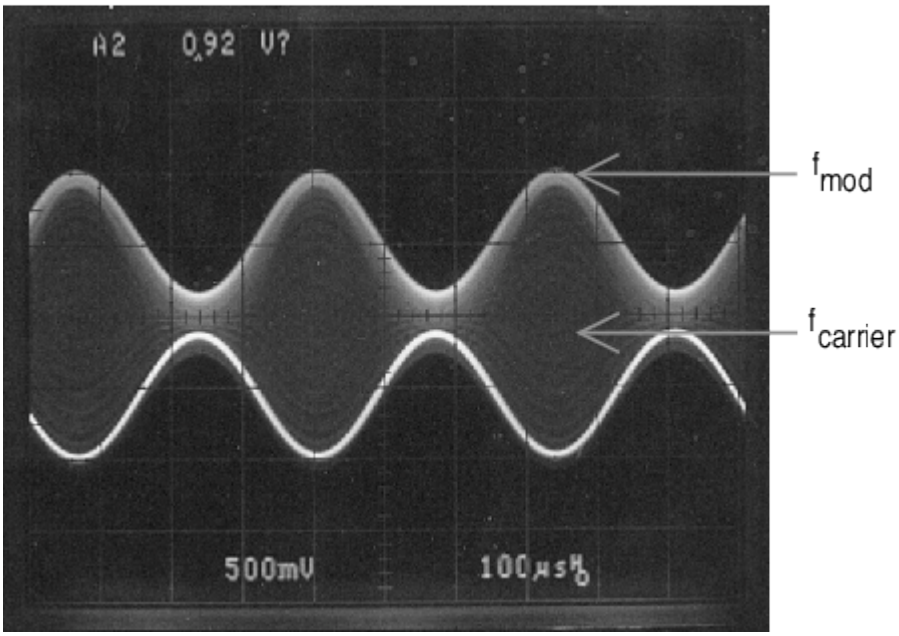

Figure 41. Output signal of Figure 40

8.2.3 Tri-Level Voltage Detector

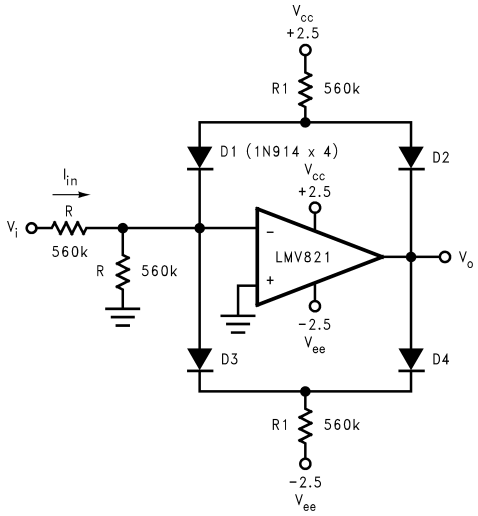

Figure 42. Tri-level Voltage Detector

8.2.3.1 Design Requirements

The tri-level voltage detector of Figure 42 provides a type of window comparator function. It detects three different input voltage ranges: Min-range, Mid-range, and Max-range. The output voltage (V_O) is at V_{CC} for the Min-range. V_O is clamped at GND for the Mid-range. For the Max-range, V_O is at V_{ee}. Figure 43 shows a V_O vs. V_I oscilloscope photo per the circuit of Figure 42.

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Typical Applications (continued)

Its operation is as follows: V_I deviating from GND, causes the diode bridge to absorb I_{IN} to maintain a clamped condition (V_O= 0V). Eventually, I_{IN} reaches the bias limit of the diode bridge. When this limit is reached, the clamping effect stops and the op amp responds open loop. The design equation directly preceding Figure 43, shows how to determine the clamping range. The equation solves for the input voltage band on each side GND. The mid-range is twice this voltage band.

8.2.3.2 Detailed Design Procedure

$$\Delta V = \frac{R}{R_1}(V_{CC} - V_{Diode}) \quad (3)$$

8.2.3.3 Application Performance Plot

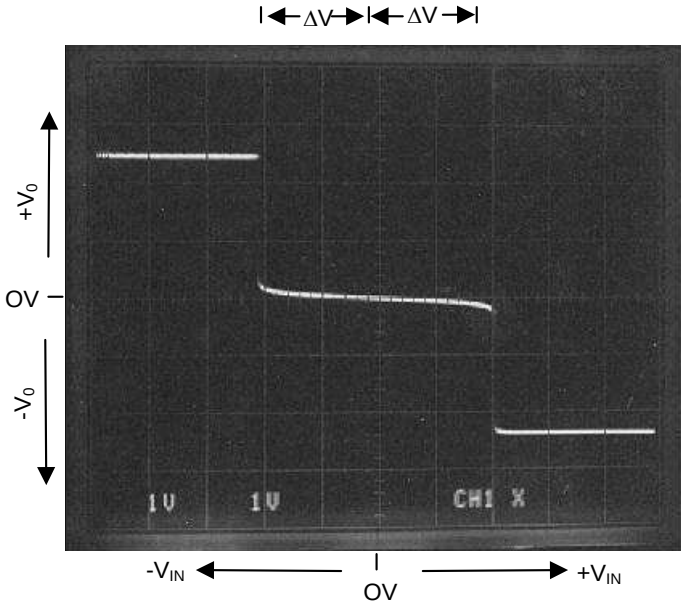
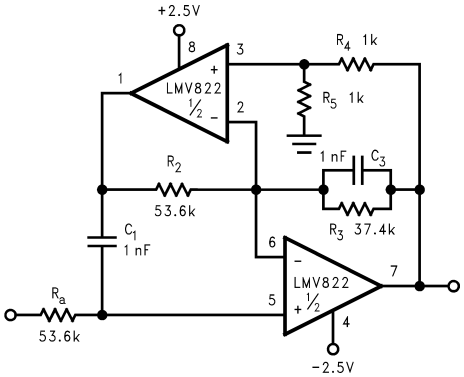


Figure 43. X, Y Oscilloscope Trace showing V_{OUT} vs V_{IN} per the Circuit of Tri-Level Voltage Detector

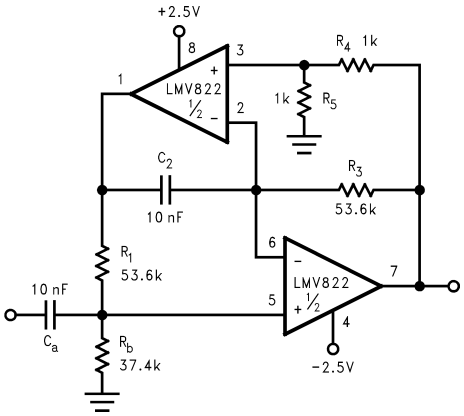
8.2.4 Dual Amplifier Active Filters (DAAFs)



3 kHz Low-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Figure 44. Dual Amplifier Active Low-Pass Filter

Typical Applications (continued)



300 Hz High-Pass Active Filter with a Butterworth Response and a Pass Band Gain of Times Two

Figure 45. Dual Active Amplifier High-Pass Filter

8.2.4.1 Design Requirements

The LMV822/24 bring economy and performance to DAAFs. The low-pass and the high-pass filters of Figure 44 and Figure 45 (respectively), offer one key feature: excellent sensitivity performance. Good sensitivity is when deviations in component values cause relatively small deviations in a filter's parameter such as cutoff frequency (Fc). Single amplifier active filters like the Sallen-Key provide relatively poor sensitivity performance that sometimes cause problems for high production runs; their parameters are much more likely to deviate out of specification than a DAAF would. The DAAFs of Figure 44 and Figure 45 are well suited for high volume production.

8.2.4.2 Detailed Design Procedure

Active filters are also sensitive to an op amp's parameters -Gain and Bandwidth, in particular. The LMV822/24 provide a large gain and wide bandwidth. And DAAFs make excellent use of these feature specifications.

Single Amplifier versions require a large open-loop to closed-loop gain ratio - approximately 50 to 1, at the Fc of the filter response.

In addition to performance, DAAFs are relatively easy to design and implement. The design equations for the low-pass and high-pass DAAFs are shown below. The first two equation calculate the Fc and the circuit Quality Factor (Q) for the LPF (Figure 44). The second two equations calculate the Fc and Q for the HPF (Figure 45).

$$\text{(LPF)} \quad F_C = \frac{\sqrt{R_5}}{2\pi\sqrt{R_a}\cdot\sqrt{R_2}\cdot\sqrt{R_4}\cdot\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$Q = 2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}$$

$$\text{(HPF)} \quad F_C = \frac{\sqrt{R_4}}{2\pi\sqrt{R_1}\cdot\sqrt{R_3}\cdot\sqrt{R_5}\cdot\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$Q = 2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2} \tag{4}$$

To simplify the design process, certain components are set equal to each other. Refer to Figure 44 and Figure 45. These equal component values help to simplify the design equations as follows:

$$\text{(LPF)} \quad R_a = R_2 = \frac{1}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$R_3 = \frac{Q}{2\pi F_C\sqrt{C_1}\cdot\sqrt{C_3}}$$

$$\text{(HPF)} \quad R_1 = R_3 = \frac{1}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}}$$

$$R_b = \frac{Q}{2\pi F_C\sqrt{C_a}\cdot\sqrt{C_2}} \tag{5}$$

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Typical Applications (continued)

To illustrate the design process/implementation, a 3 kHz, Butterworth response, low-pass filter DAAF (Figure 44) is designed as follows:

1. Choose $C_1 = C_3 = C = 1$ nF

2. Choose $R_4 = R_5 = 1$ kΩ

3. Calculate R_a and R_2 for the desired Fc as follows:

$$R_a = R_2 = \frac{1}{2\pi(F_C)C}$$

$$= \frac{1}{2\pi(3\text{ kHz})1\text{nF}}$$

$$= 53.1\text{ k}\Omega$$

$$\cong 53.6\text{ k}\Omega \text{ (Practical Value)} \quad (6)$$

4. Calculate R_3 for the desired Q. The desired Q for a Butterworth (Maximally Flat) response is 0.707 (45 degrees into the s-plane). R_3 calculates as follows:

$$R_3 = \frac{Q}{2\pi(F_C)C}$$

$$= \frac{0.707}{2\pi(3\text{ kHz})1\text{nF}}$$

$$= 37.5\text{ k}\Omega$$

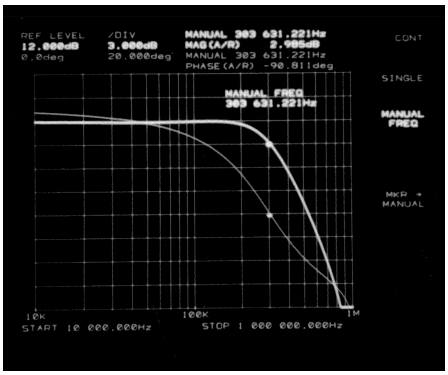
$$\cong 37.4\text{ k}\Omega \text{ (Practical Value)} \quad (7)$$

Notice that R_3 could also be calculated as 0.707 of R_a or R_2.

The circuit was implemented and its cutoff frequency measured. The cutoff frequency measured at 2.92 kHz.

The circuit also showed good repeatability. Ten different LMV822 samples were placed in the circuit. The corresponding change in the cutoff frequency was less than a percent.

8.2.4.3 Application Perfromance Plots



Butterworth Response as Measured by the HP3577A Network Analyzer

Figure 46. 300 kHz, DAAF Low-Pass Filter Measurement Results

Figure 46 shows an impressive photograph of a network analyzer measurement (HP3577A). The measurement was taken from a 300 kHz version of Figure 44. At 300 kHz, the open-loop to closed-loop gain ratio @ Fc is about 5 to 1. This is 10 times lower than the 50 to 1 “rule of thumb” for Single Amplifier Active Filters.

Table 1 provides sensitivity measurements for a 10 MΩ load condition. The left column shows the passive components for the 3 kHz low-pass DAAF. The third column shows the components for the 300 Hz high-pass DAAF. Their respective sensitivity measurements are shown to the right of each component column. Their values consists of the percent change in cutoff frequency (Fc) divided by the percent change in component value. The lower the sensitivity value, the better the performance.

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Typical Applications (continued)

Each resistor value was changed by about 10 percent, and this measured change was divided into the measured change in Fc. A positive or negative sign in front of the measured value, represents the direction Fc changes relative to components' direction of change. For example, a sensitivity value of negative 1.2, means that for a 1 percent increase in component value, Fc decreases by 1.2 percent.

Note that this information provides insight on how to fine tune the cutoff frequency, if necessary. It should be also noted that R_4 and R_5 of each circuit also caused variations in the pass band gain. Increasing R_4 by ten percent, increased the gain by 0.4 dB, while increasing R_5 by ten percent, decreased the gain by 0.4 dB.

Table 1. Component Sensitivity Measurements

Component (LPF)	Sensitivity (LPF)	Component (HPF)	Sensitivity (HPF)
R_a	-1.2	C_a	-0.7
C_1	-0.1	R_b	-1.0
R_2	-1.1	R_1	+0.1
R_3	+0.7	C_2	-0.1
C_3	-1.5	R_3	+0.1
R_4	-0.6	R_4	-0.1
R_5	+0.6	R_5	+0.1

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistence to the oputput when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do not exceed the input common mode range. The input is not "Rail to Rail" and will limit upper output swing when configured as followers or other low-gain applications. See the Input Common Mode Voltage Range section of the Electrical Table.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

For proper operation, the power supplies bust be properly decoupled. For decoupling the supply lines it is suggested that 10 nF capacitors be placed as close as possible to the op amp power supply pins. For single supply, place a capacitor between V^+ and V^-supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

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10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible minimizing strays.

10.2 Layout Example

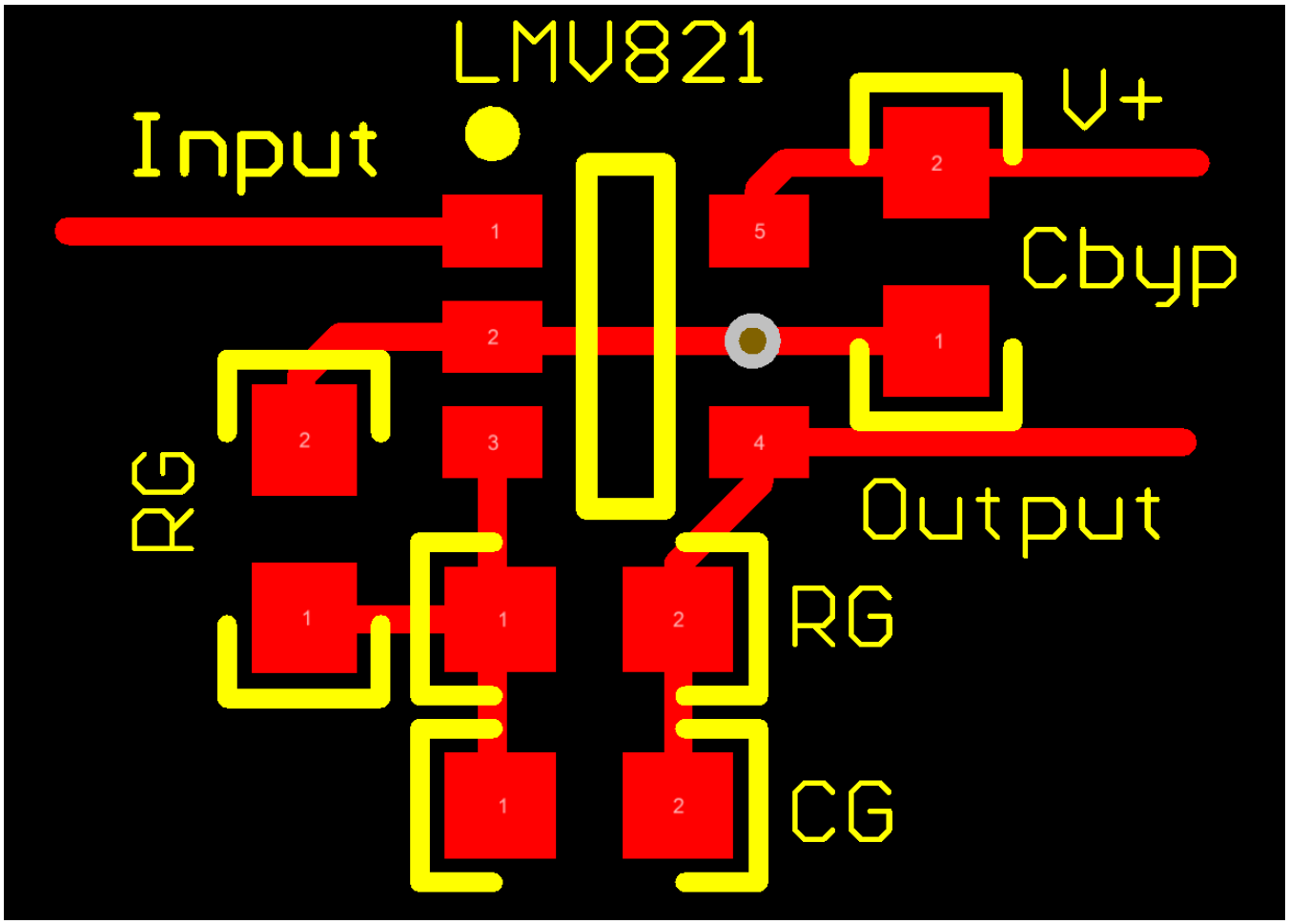

Figure 47. 2-D Layout

Layout Example (continued)

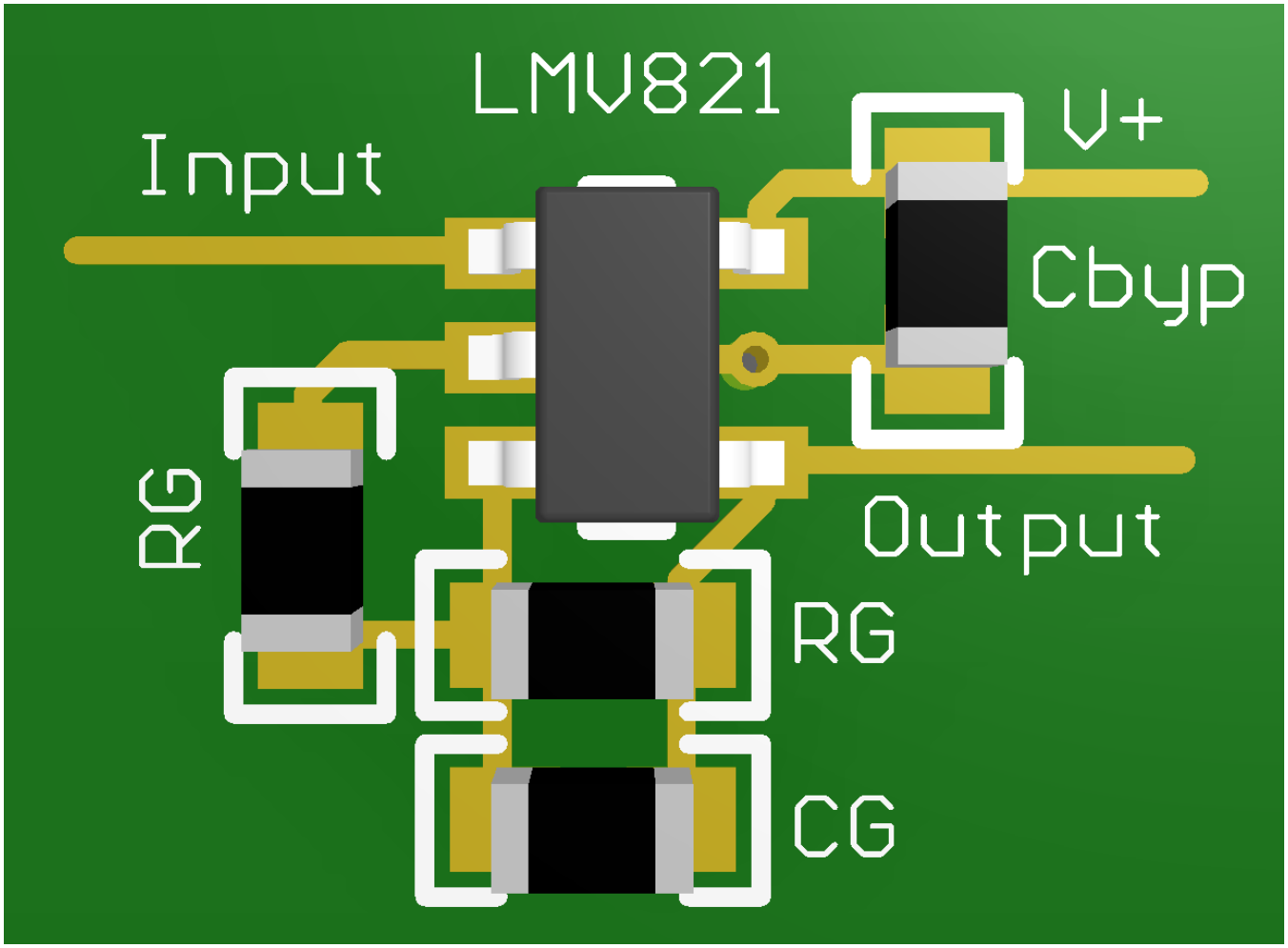

Figure 48. 3-D Layout

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- TI Filterpro Software
- TI Universal Operational Amplifier Evaluation Module
- TINA-TI SPICE-Based Analog Simulation Program

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV821-N	Click here	Click here	Click here	Click here	Click here
LMV822-N	Click here	Click here	Click here	Click here	Click here
LMV822-N-Q1	Click here	Click here	Click here	Click here	Click here
LMV824-N	Click here	Click here	Click here	Click here	Click here
LMV824-N-Q1	Click here	Click here	Click here	Click here	Click here

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV821M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A14	
LMV821M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A14	
LMV821M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A14	Samples
LMV821M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A15	
LMV821M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV821M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A15	Samples
LMV822M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMV 822M	
LMV822M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	Samples
LMV822MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	V822	
LMV822MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 85	V822	Samples
LMV822MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMV 822M	
LMV822MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMV 822M	Samples
LMV822Q1MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AKAA	Samples
LMV822Q1MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	AKAA	Samples
LMV824M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	Samples
LMV824MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MTX	NRND	TSSOP	PW	14	2500	TBD	Call TI	Call TI	-40 to 85	LMV824 MT	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV824MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMV824 MT	Samples
LMV824MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMV824M	Samples
LMV824NDGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV824N	Samples
LMV824Q1MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMV824Q1 MA	Samples
LMV824Q1MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LMV824Q1 MA	Samples
LMV824Q1MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	LMV824 Q1MT	Samples
LMV824Q1MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	LMV824 Q1MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV822-N, LMV822-N-Q1, LMV824-N, LMV824-N-Q1 :

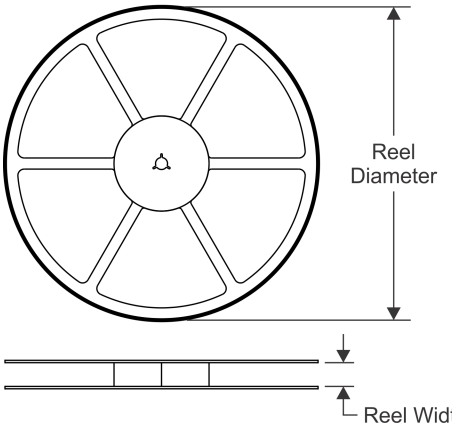
- Catalog: LMV822-N, LMV824-N
- Automotive: LMV822-N-Q1, LMV824-N-Q1

NOTE: Qualified Version Definitions:

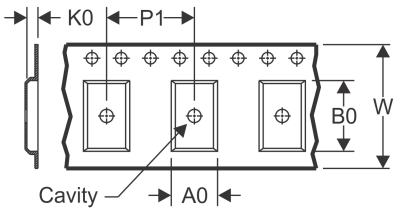
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

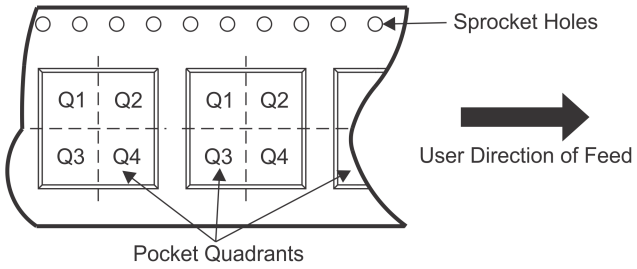


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

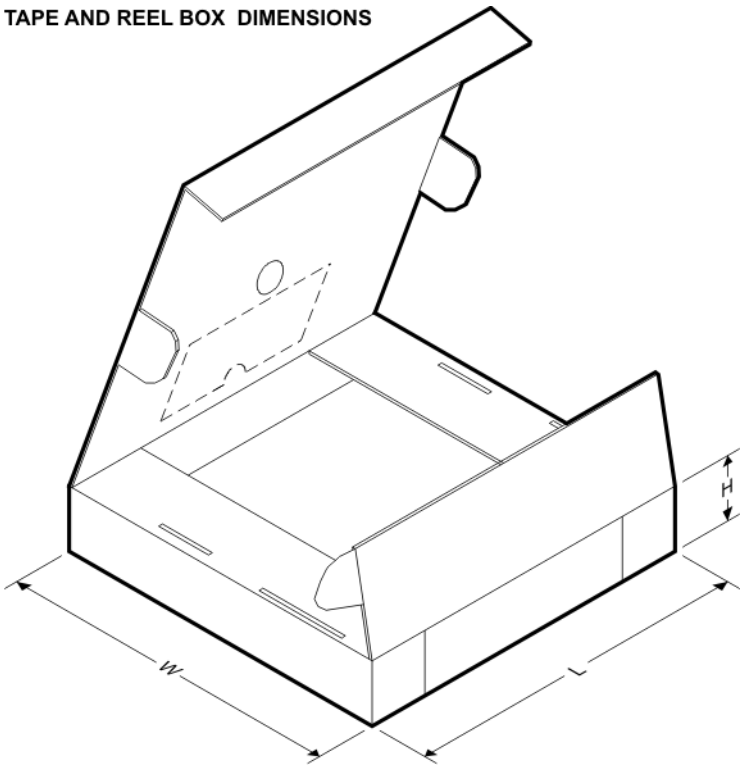


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV821M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV821M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV821M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV822MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV822MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV822Q1MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV822Q1MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV824MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV824MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV824MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV824MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV824NDGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
LMV824Q1MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV824Q1MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

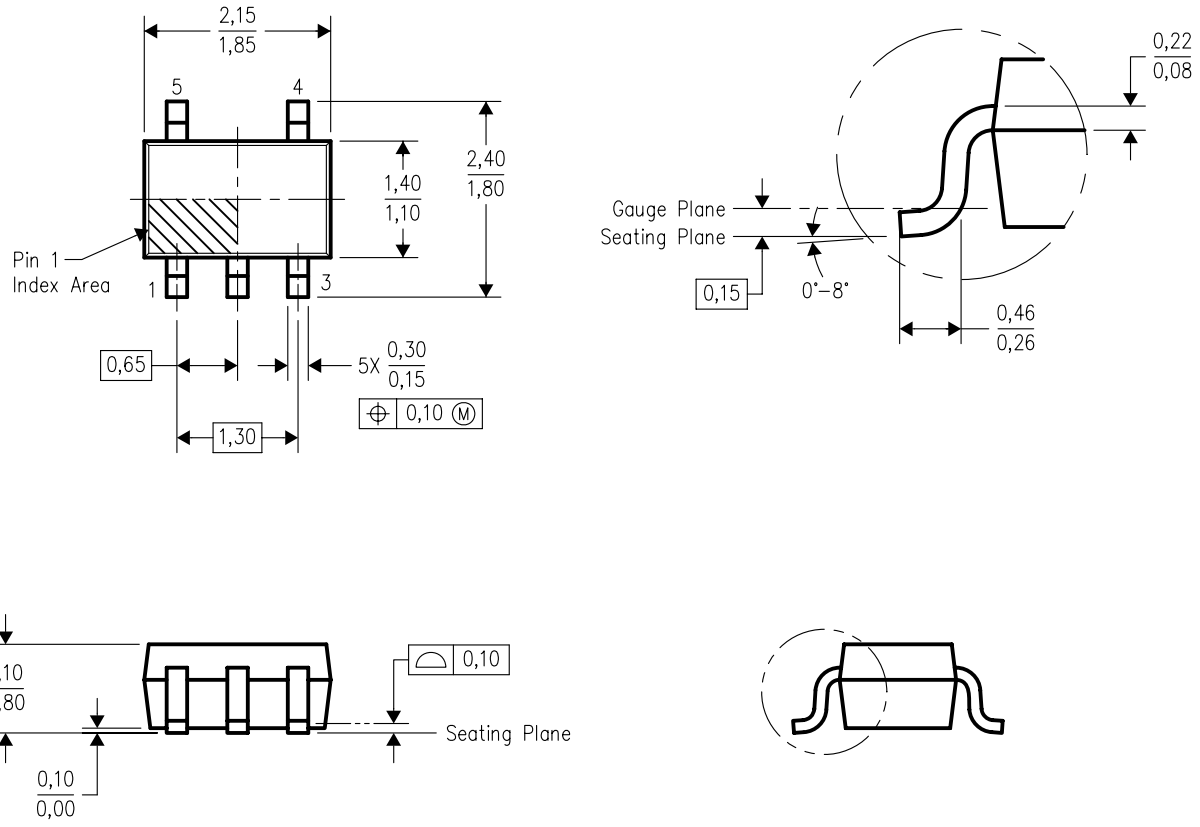


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV821M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV821M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV821M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV821M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV821M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV821M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV821M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV822MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV822MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV822MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV822MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV822MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV822Q1MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV822Q1MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV824MTX	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV824MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV824MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV824MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV824NDGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
LMV824Q1MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV824Q1MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

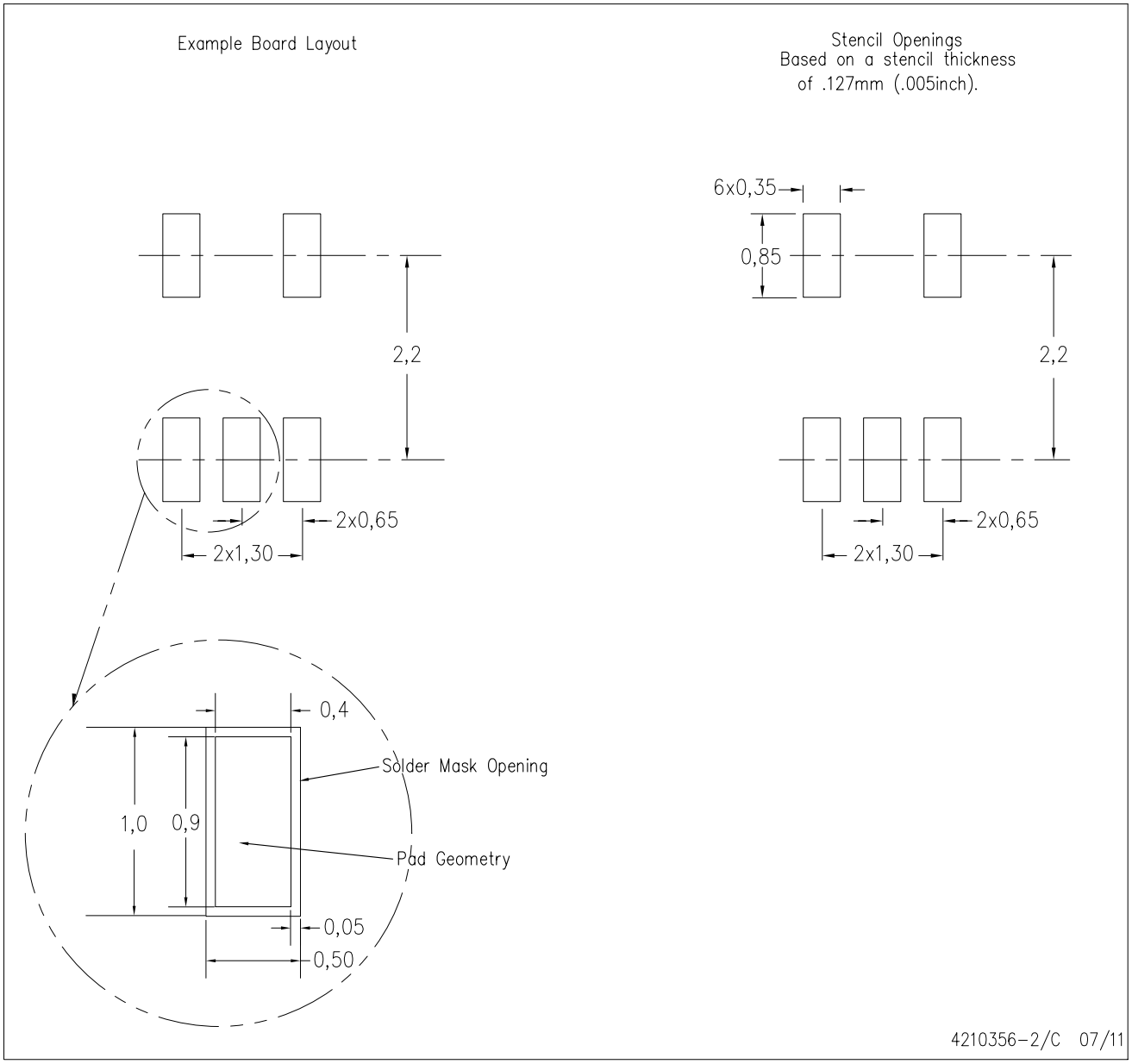
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



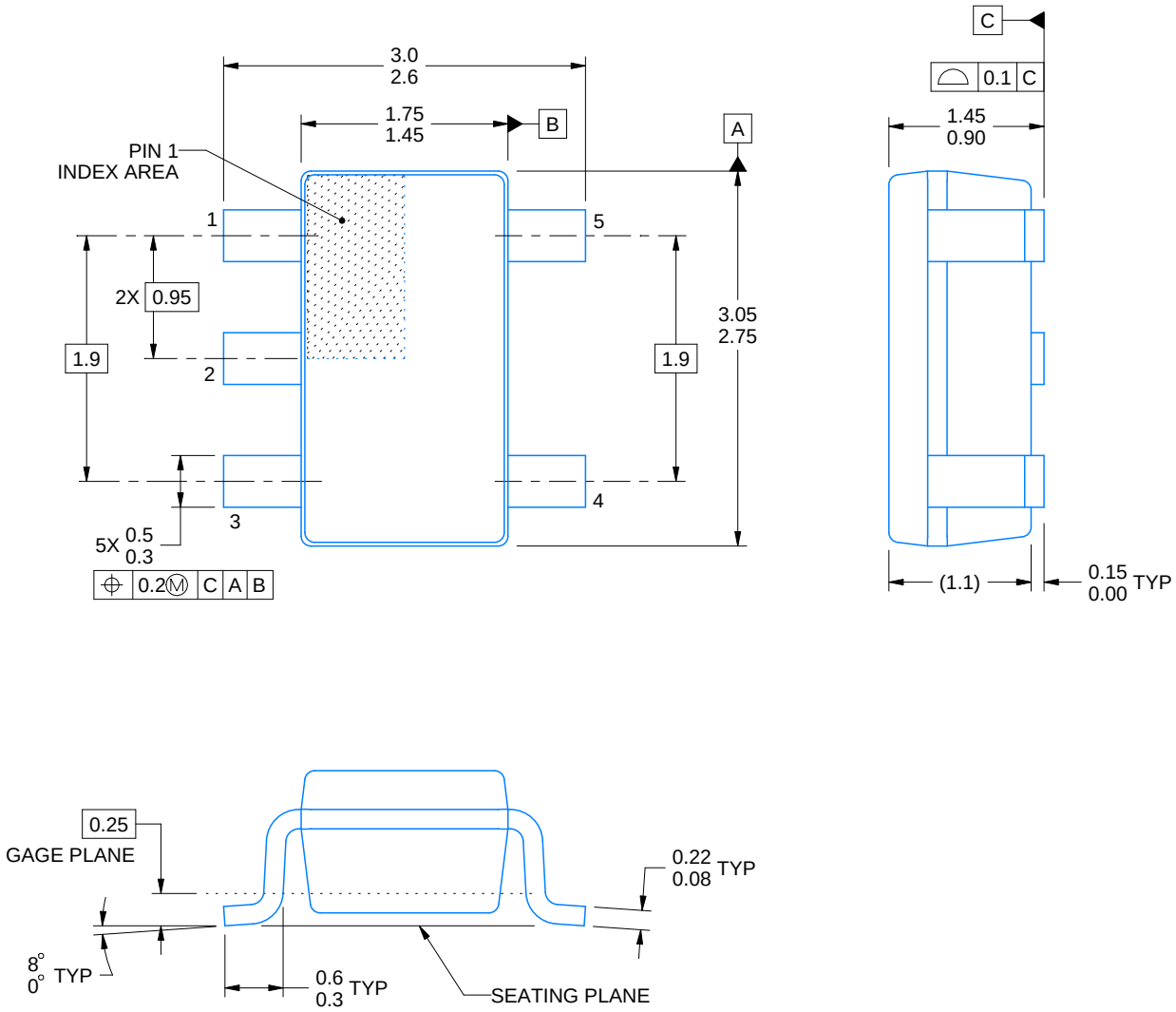
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

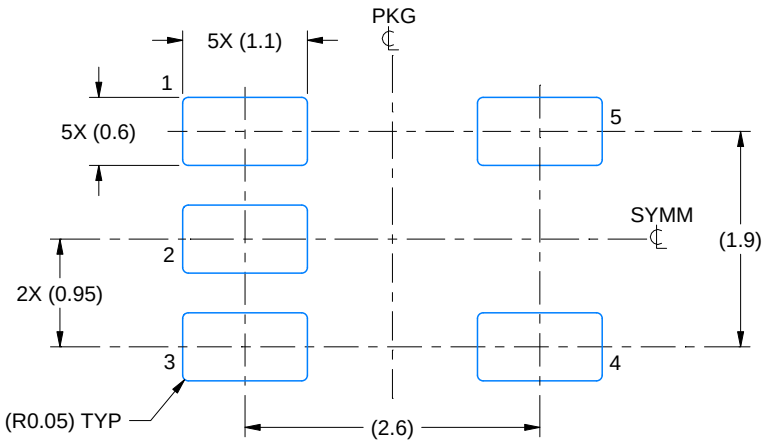
SMALL OUTLINE TRANSISTOR



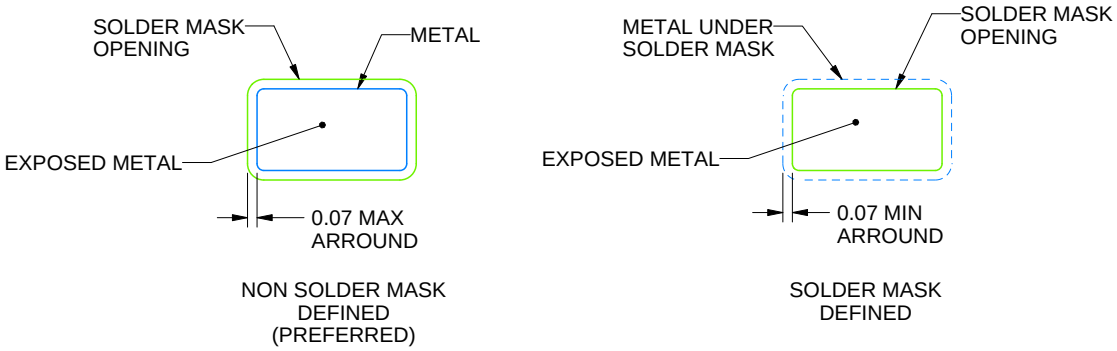
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

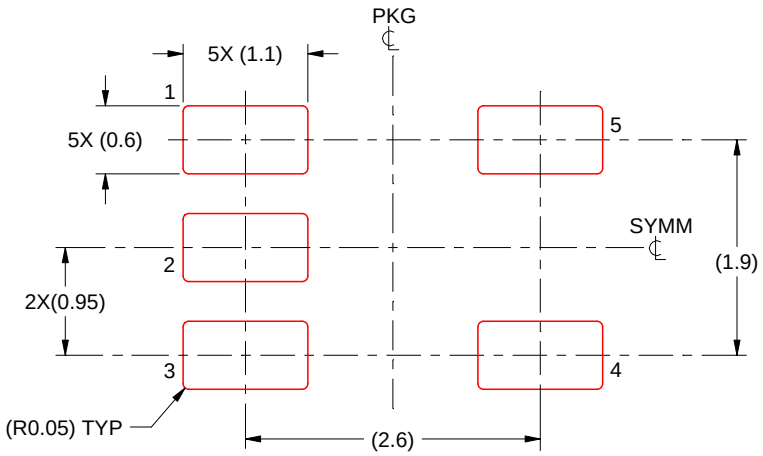


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



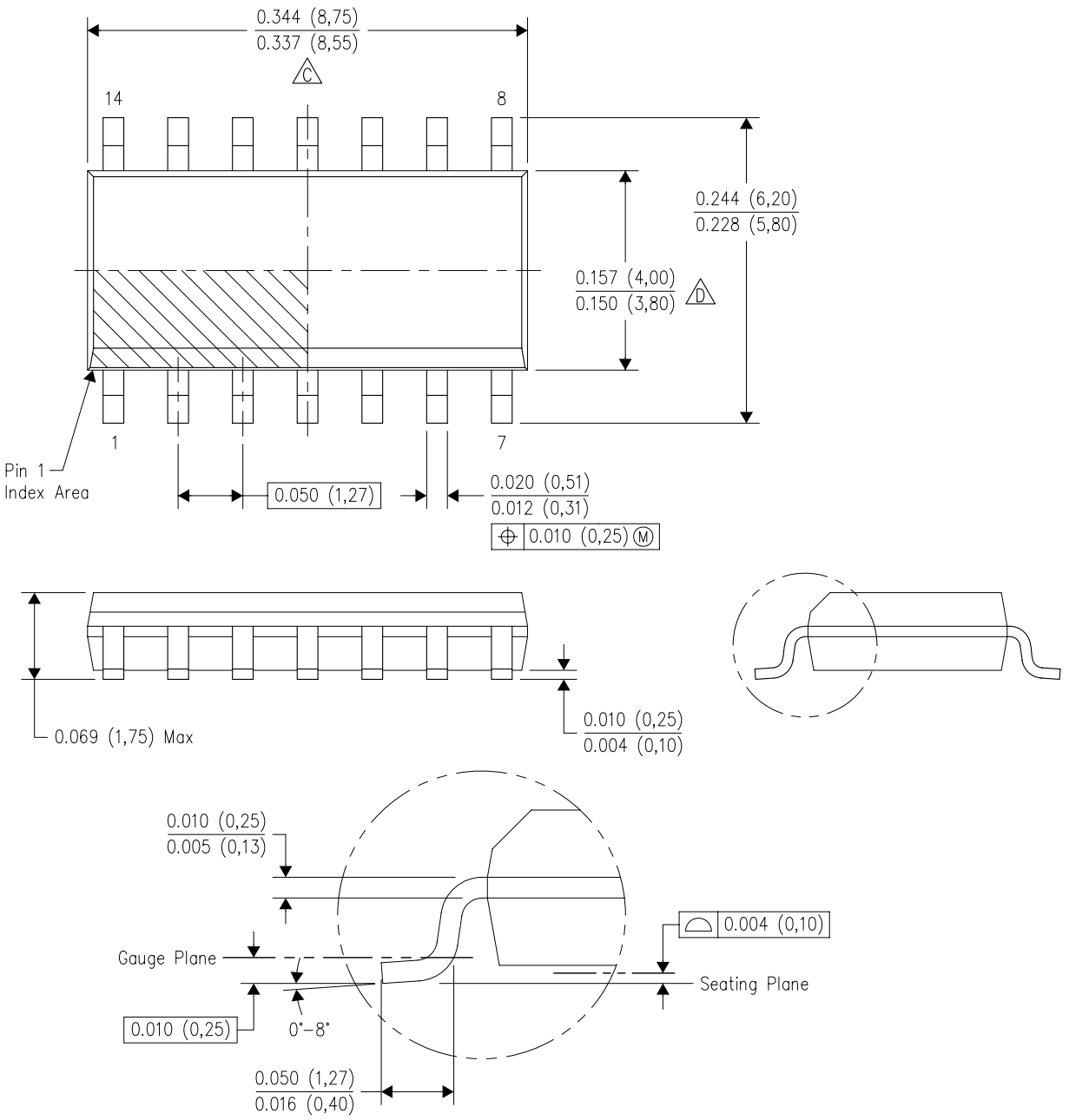
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

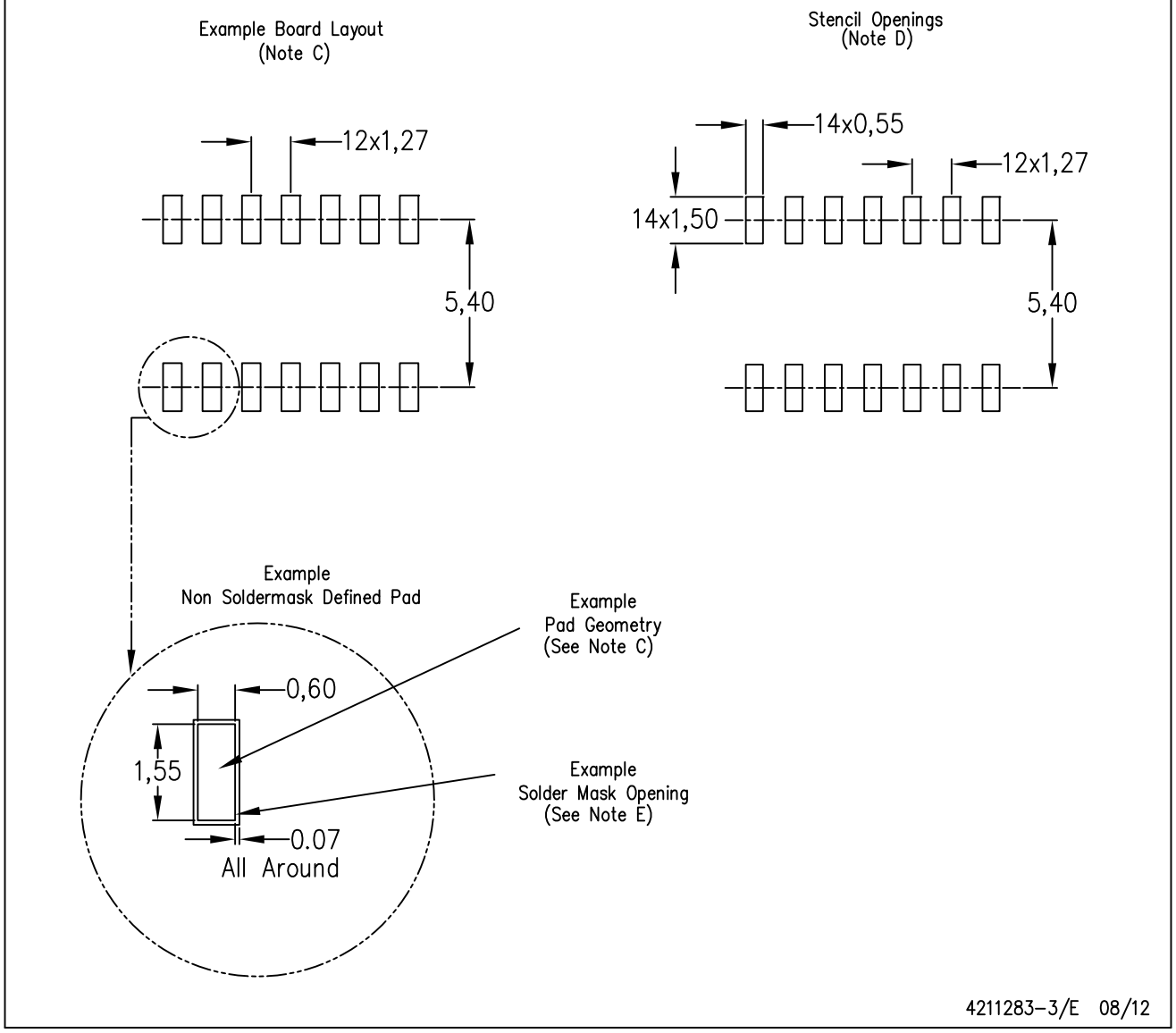
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



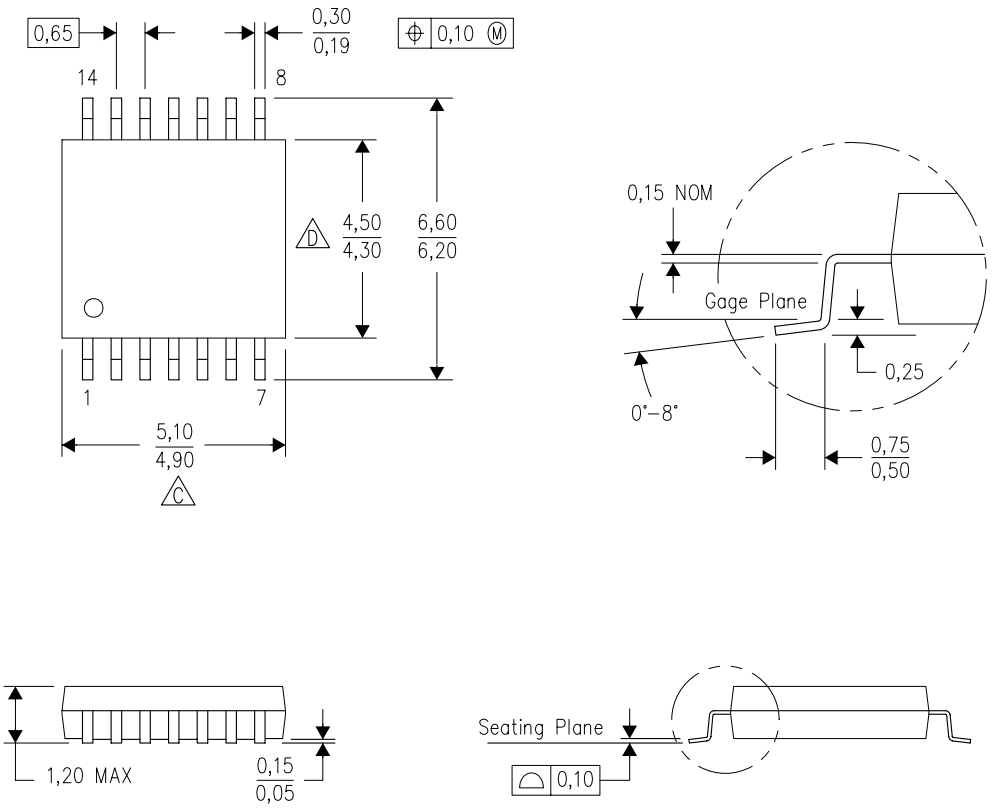
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

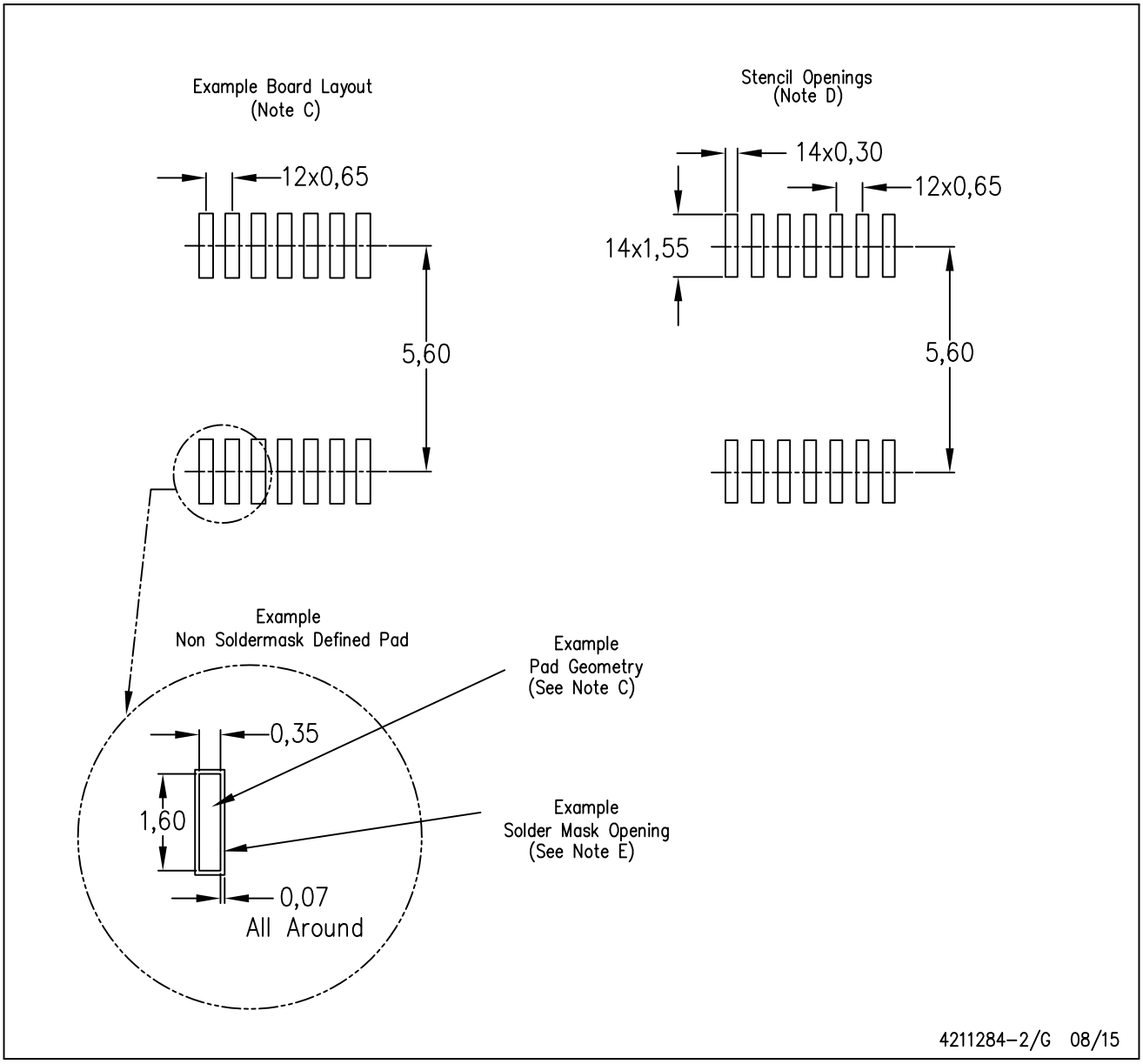
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



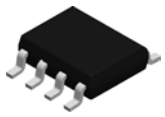
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

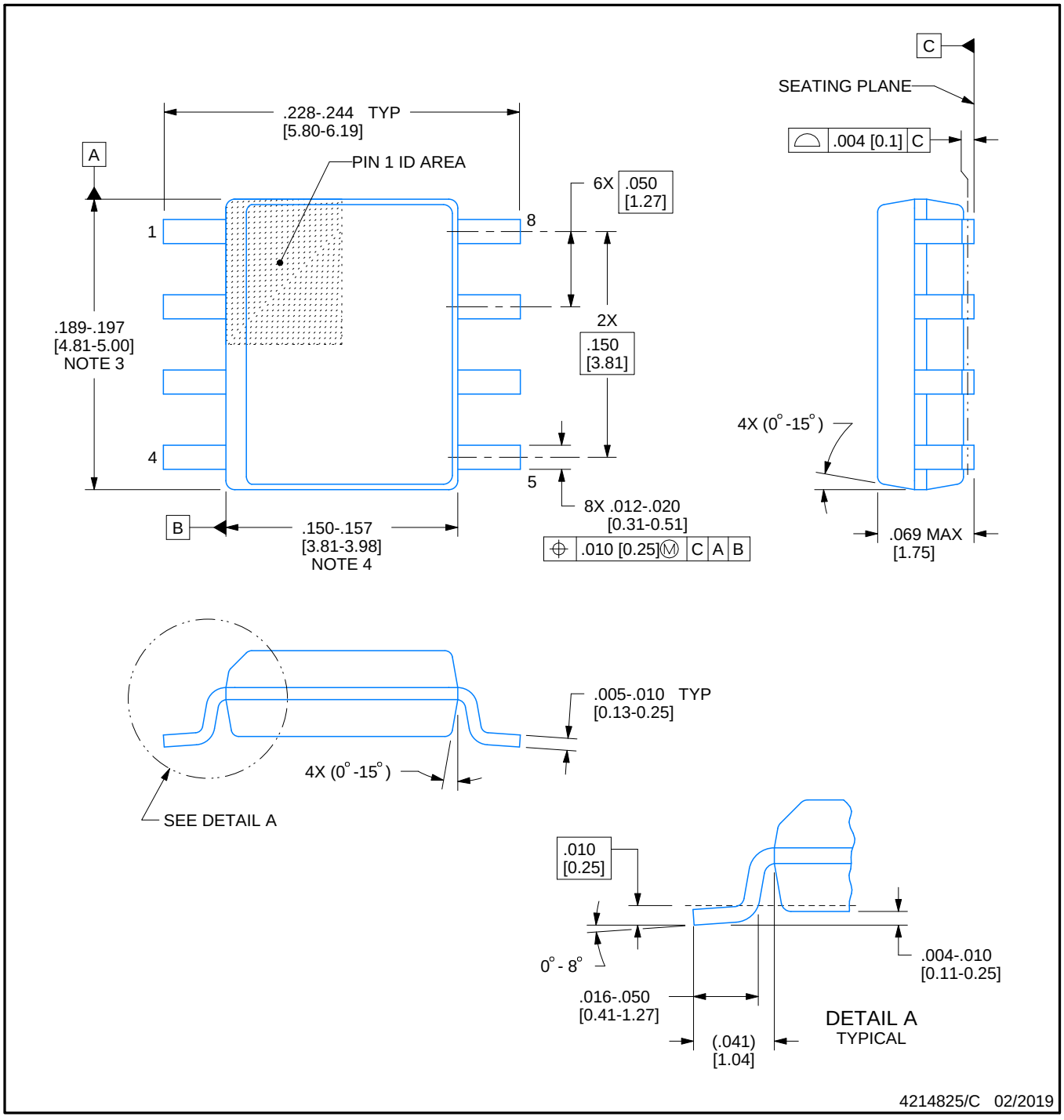


PACKAGE OUTLINE

D0008A

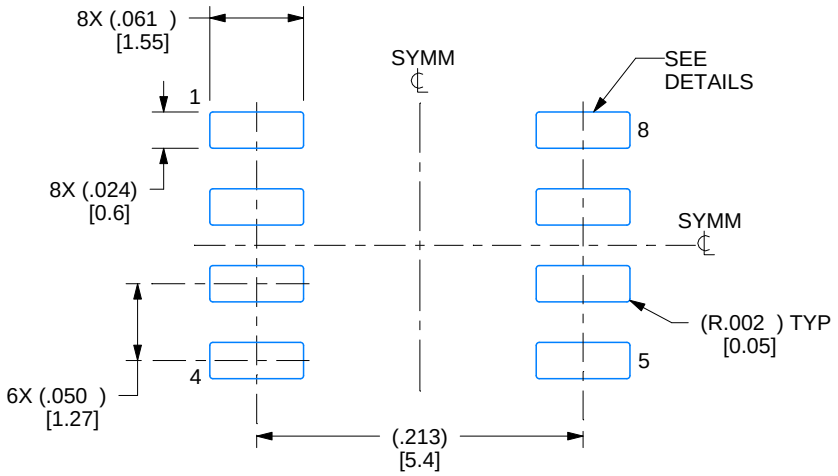
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

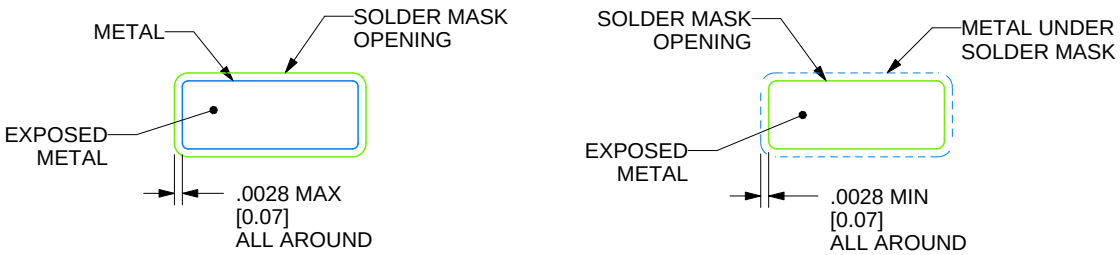


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

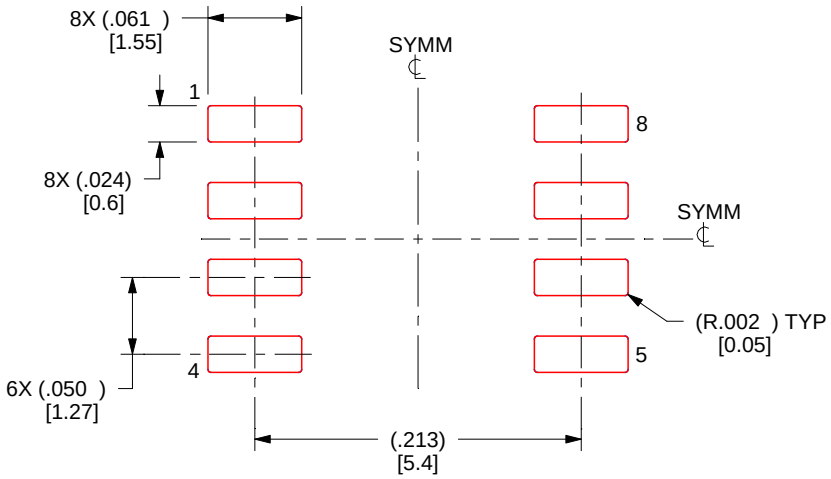
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



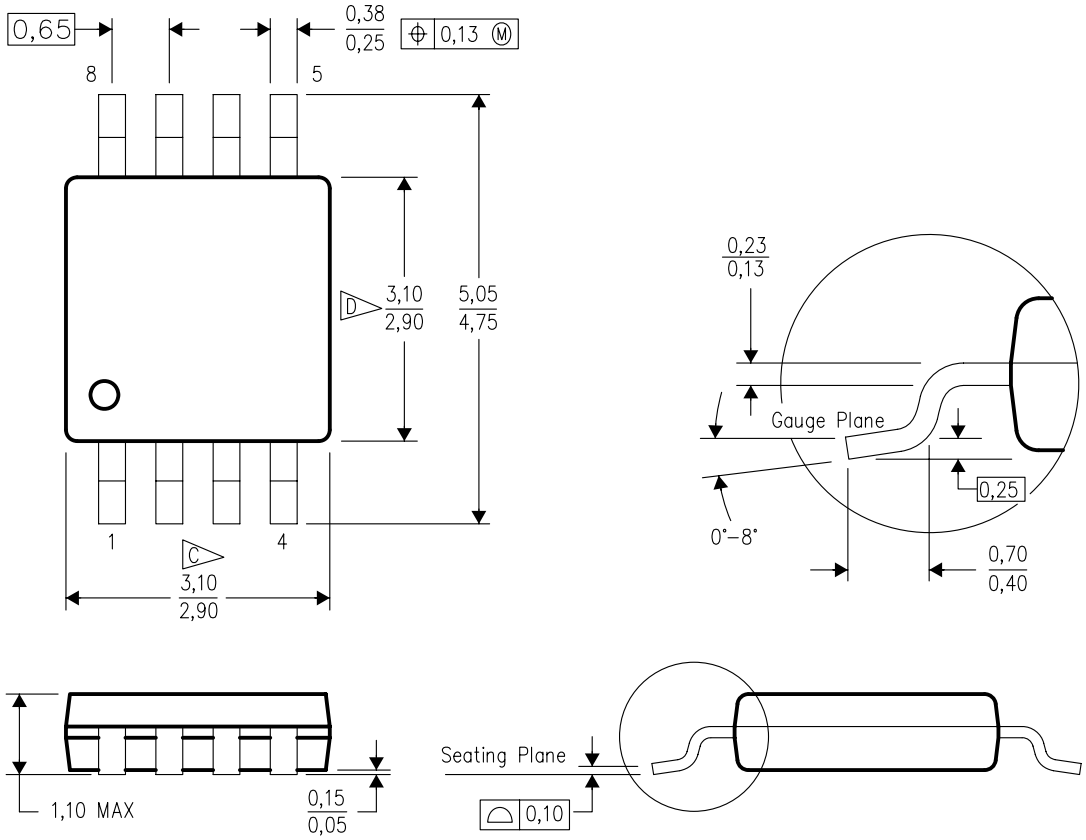
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

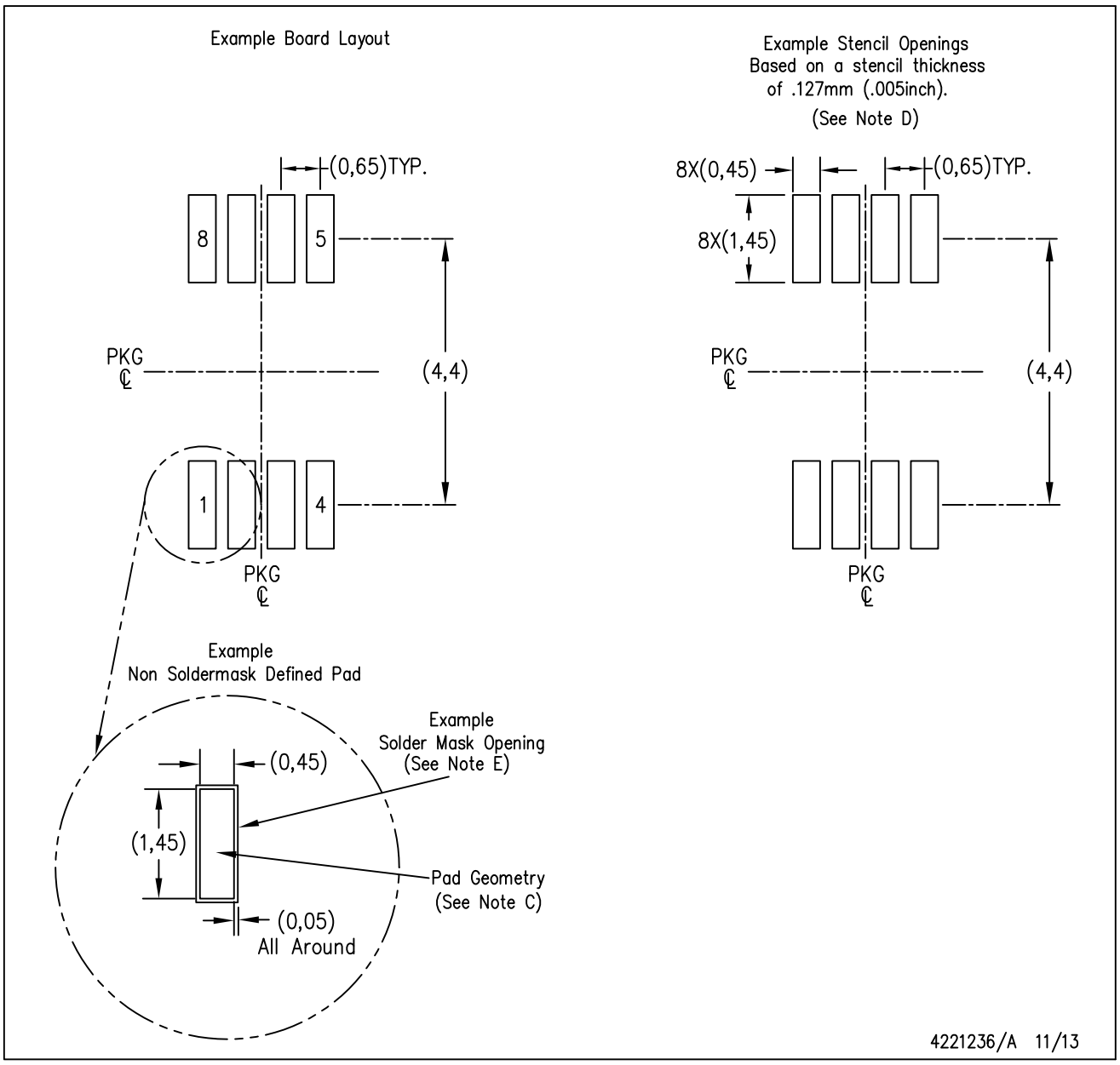
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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