IWR1443 Device Errata
Silicon Revision 1.0, 2.0, and 3.0

1 Introduction

This document describes the known exceptions to the functional and performance specifications to TI CMOS Radar Devices (IWR1443).

2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of Radar / milli-meter Wave sensor devices. Each of the Radar devices has one of the two prefixes: XIx or IWRx (for example: **IWR1443**FQAGABL). These prefixes represent evolutionary stages of product development from engineering prototypes (XI) through fully qualified production devices (IWR).

Device development evolutionary flow:

XI — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

IWR — Production version of the silicon die that is fully qualified.

XI devices are shipped with the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Texas Instruments recommends that these devices not to be used in any production system as their expected end –use failure rate is still undefined.

3 Device Markings

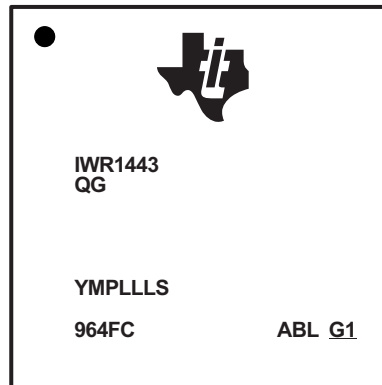Figure 1 shows an example of the IWR1443 Radar Device's package symbolization.

Figure 1. Example of Device Part Markings

This identifying number contains the following information:
- **Line 1:** Device Number
- **Line 2:** Temperature and Security Grade
- **Line 3:** Lot Trace Code
  - YM = Year/Month Code
  - PLLL = Assembly Lot
  - S = Assembly Site Code
- **Line 4:**
  - 964 = IWR1443 Identifier
  - D = ES2.0
  - FC = ES3.0
  - BLANK = ES1.0
  - ABL = Package Identifier
  - G1 = "Green" Package Build (must be underlined)

4 Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These usage notes will be incorporated into future documentation updates for the device (such as the device-specific data sheet), and the behaviors they describe will not be altered in future silicon revisions.

4.1 MSS: SPI Speed in 3-Wire Mode Usage Note

The maximum SPI speed under 3-wire operation was only tested up to 33 MHz. This affects IWR1443 ES2.0.

4.2 Identification

The JTAG identification code for this device is the same as the device ICEPick Identification code.

Table 1. Device Identification

Silicon Revision	ID
ES1.0	0x0BB1F02F
ES2.0	0x1BB1F02F
ES3.0	0x3BB1F02F

5 Advisory to Silicon Variant / Revision Map

Table 2. Advisory to Silicon Variant / Revision Map

Advisory Number	Advisory Title	IWR1443		
		ES1.0	ES2.0	ES3.0
Master Subsystem				
MSS#01	Available MSS Memory (RAM) for Customer Application is Smaller by 128 KB	X	X	
MSS#02	"System Reset" Applied Over JTAG Debugger (Emulation Channel) Could Lead to a Disconnection From the Device	X	X	
MSS#03	Incorrect Handling of "Saturation" in FFT Hardware Accelerator's Input / Output Formatter and Statistics Block	X	X	X
MSS#04	Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator	X	X	X
MSS#05	Incorrect FFT Intermediate Stage Clip Status Indication	X	X	X
MSS#06	Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader	X	X	
MSS#07	MSS interrupt Number 106 Seen as Pending by the User Application	X	X	X
MSS#08	ESM Group2 Interrupt (VIM Compare Error), Which is Mapped to FIQ Line, is Active When Control is Passed to Application	X	X	
MSS#09	ESM Group1 Interrupt (NERROR_IN_SYNC) Seen as Pending by User Application – Can Lead to Interrupt if Unmasked	X	X	
MSS#13	Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation	X	X	X
MSS#14	Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock	X	X	
MSS#15	The IWR14xx ES1.0 and ES2.0 Devices Only Work With Spansion and Macronix Devices	X	X	See[1]
MSS#19	DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario	X	X	X
MSS#21	Issue with HWA Input Formatter 16 bit real Signed Format	X	X	X
Analog / Millimeter Wave				
ANA#01	Noise Figure Degradation	X		
ANA#02	VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target	X		
ANA#03	Spurs from LVDS Output Coupling into Synthesizer	X		
ANA#04	Receiver Gain Range Availability	X		
ANA#06	Return Loss Measurement on TX: S11 < –9dB, RX S11 < –6.5dB (Accepted Value of < –10dB)	X		
ANA#07	CSI2 Activity Coupling to Clock	X	X	
ANA#08	Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz			X
ANA#11	TX, RX Gain Calibrations Sensitive to Large External Interference			X

[1] For IWR1443 ES3.0 follow QSPI recommendations in Flash Variants Supported by the mmWave Sensor.

6 Known Design Exceptions to Functional Specifications

Table 3. Advisory List

MSS#01	***Available MSS Memory (RAM) for Customer Application is Smaller by 128 KB***
Revision(s) Affected:	IWR1443 ES1.0, and IWR1443 ES2.0
Description:	Due to available RAM being used for Radar block development, RAM available for user application is limited to 448 KB instead of 576 KB.
Workaround(s):	None. Silicon update will be provided by TI.

MSS#02	***"System Reset" Applied Over JTAG Debugger (Emulation Channel) Could Lead to a Disconnection From the Device***
Revision(s) Affected:	IWR1443 ES1.0 and IWR1443 ES2.0
Description:	Debug logic in the device gets reset when Reset is applied through debugger. This results in status registers in debug registers getting cleared, and can potentially result in the device getting disconnected from the debugger.
Workaround(s):	A workaround is provided by TI's XDS110 debugger (available on TI EVMs).

MSS#03	***Incorrect Handling of "Saturation" in FFT Hardware Accelerator's Input / Output Formatter and Statistics Block***
Revision(s) Affected:	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
Description:	- Input formatter block performs saturation based on signed or unsigned samples. However, the compute engine module always saturates the input as a 24 bit signed number. - Output formatter block saturates the 16 bits unsigned number as signed number. This causes magnitude outputs to have a smaller max range. - Statistics block always assumes that input is signed when checking for saturation, but the input can be unsigned in some cases.
Workaround(s):	None, there is no planned update. The max output range must be 16 bit signed. The statistics block input should be a signed input.

MSS#04	***Number of Samples (SRCACNT) Should be >3 for Correct Operation of FFT Hardware Accelerator***
Revision(s) Affected:	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
Description:	Logic which subtracts the compute engine pipelined delay from FFT counter wraps around incorrectly when the number of samples is less (specifically, when it is 3).
Workaround(s):	None, there is no planned update. FFT engine should not be used with FFT counter value < 4.

MSS#05	***Incorrect FFT Intermediate Stage Clip Status Indication***
Revision(s) Affected:	IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0
Description:	FFT clip status register incorrectly uses all butterfly stages, even if only a few of the stages are enabled.
Workaround(s):	None, there is no planned update. HWA FFT Intermediate Stage Clip Status Indication is incorrect, do not use this feature, mask off.

MSS#06   *Internal Pulls on QSPI Data Lines not Enabled by the Device Bootloader*

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: Internal Pulls on the Data lines (D2 and D3) are not enabled by the device bootloader.

Workaround(s):   Pulls on target board required (refer to reference schematics of TI EVM).

MSS#07   *MSS interrupt Number 106 Seen as Pending by the User Application*

Revision(s) Affected: IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

Description: Due to an anomalous connection in one of the Analog blocks (which is otherwise not a concern) MSS Interrupt number 106 will always be seen as pending by the application.

Workaround(s):   For ES1.0 version of silicon, it is recommended that this interrupt is always kept as masked by the user application.

MSS#08   *ESM Group2 Interrupt (VIM Compare Error), Which is Mapped to FIQ Line, is Active When Control is Passed to Application*

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: Compare Error is always present when the control is passed to the application due to a missing configuration in device bootloader.

Workaround(s):   Since this error is connected to the FIQ line, for ES1.0 version of silicon, it is imperative that the application clears this error immediately on start up.

MSS#09   *ESM Group1 Interrupt (NERROR_IN_SYNC) Seen as Pending by User Application – Can Lead to Interrupt if Unmasked*

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: ESM Group1 interrupt will be seen as pending when the control is passed to the application due to a missing configuration in device bootloader.

Workaround(s):   User application should keep the error masked.

MSS#13   *Incorrect Read from FFT Hardware Accelerator After Complex Multiplication Operation*

Revision(s) Affected: IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

Description: Read-back from FFT hardware accelerator slave, static configuration registers, Window RAM, Param RAM, and First stage RAM gives incorrect data if the last operation performed by the accelerator was a complex multiplication.

Workaround(s):   None.

MSS#14	***Asynchronous Assertion of SoC Warm Reset may not Work Reliably When Device Operating on PLL Clock***

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: Asynchronous assertion of SoC warm reset through WARM_RESET pin, SW reset, watchdog reset, or Debug reset may not reliably work and may also result in a system hang scenario.

Workaround(s): MSS VCLK must be switched from PLL clock to REFCLK by following the prescribed software sequence before a warm reset is issued.

MSS#15	***The IWR14xx ES1.0 and ES2.0 Devices Only Work With Spansion and Macronix Devices***

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: The IWR1443 ES1.0 and IWR1443 ES2.0 devices work only with Spansion and Macronix devices. In particular, the Flash variants that have been tested to work with the ROM bootloader are:

- Spansion S25FL256S, S25FL132K0XNFB010
- Macronix MX25L3233F, MX25R1635FZNIH0 (Wide voltage part variant)

Workaround(s): In the next version of the Silicon ROM, the boot loader is expected to support a wide variety of flashes, with the prerequisite that Serial FLASH supports the SFDP command and responds with JEDEC compliant information regarding the capabilities and command set of the flash.

MSS#19	***DMA Read from Unimplemented Address Space may Result in DMA Hang Scenario***

Revision(s) Affected: IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

Description: The MSS DMA generates a BER (Bus Error) interrupt when the DMA detects a bus error due to a read from unimplemented address space. This interrupt is available on VIM Interrupt Channel-70. This read from unimplemented address space results in a hang condition in the DMA infrastructure bridge that connects it to the main interconnect.

Implication: A DMA read from an unimplemented address can result in a DMA hang condition. In the resulting state the DMA will not respond to any further DMA requests.

Workaround(s): The anomalous nERROR toggle would need to be ignored by the external monitoring circuit (if deployed).

MSS#21	***Issue with HWA Input Formatter 16 bit real Signed Format***

Revision(s) Affected: IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

Description: Wrong sign extension is implemented for 16 bit signed format in real only mode operation. Hence, signed 16-bit real format cannot be supported for input formatter.

Workaround(s): None, there is no planned update. The 16 bit signed format in real only mode can't be used with HWA.

ANA#01	***Noise Figure Degradation***
Revision(s) Affected:	IWR1443 ES1.0
Description:	Due to board limitation current typical Noise figure number is 18dB.
Workaround(s):	None. Silicon update will be provided by TI.

ANA#02	***VCO#1 [76-77GHz] Minimum Frequency Falls Short of Target***
Revision(s) Affected:	IWR1443 ES1.0
Description:	The supported frequency range is 77 GHz to 81 GHz (using VCO2).
Workaround(s):	None. Silicon update will be provided by TI.

ANA#03	***Spurs from LVDS Output Coupling into Synthesizer***
Revision(s) Affected:	IWR1443 ES1.0
Description:	For the characterization, the LVDS interface is used. In this mode, there is a package coupling to crystal oscillator pins causing spurs in LO (hence it comes out in IF spectrum).
Workaround(s):	None.

ANA#04	***Receiver Gain Range Availability***
Revision(s) Affected:	IWR1443 ES1.0
Description:	The supported receiver gain range is 18dB (versus a specification target of 24dB).
Workaround(s):	None.

ANA#06	***Return Loss Measurement on TX: S11 < −9dB, RX S11 < −6.5dB (Accepted Value of < −10dB)***
Revision(s) Affected:	IWR1443 ES1.0
Description:	The return loss measurement on TX S11 is < −9dB and the return loss measurement on RX S11 is < −6.5dB. The accepted value is < −10dB.
Workaround(s):	None. TI expects to provide an update along with the next silicon revision.

ANA#07   *CSI2 Activity Coupling to Clock*

Revision(s) Affected: IWR1443 ES1.0 and IWR1443 ES2.0

Description: The activity on the CSI lines during the state transitions at the start and at the end of CSI transfer couples into the clock leading to glitches in the TX output.

Workaround(s):   Increase the idle time between chirps such that the "start of transfer" and "end of transfer" occur during the idle time between two chirps.

1. The IWR1443 eDMA sends data from ADCBuffer to High Speed Peripheral. At the start of each chirp, CSI-2 changes from Low Power Mode to Standard Mode output. At the completion of the chirp, CSI-2 goes back from Standard mode to Low Power Mode output. When CSI-2 changes mode, there is a clock contamination of the ADC subsystem. In order to not contaminate the measurement, the CSI-2 data Output must be finished before the end of the idle time chirp parameter.

   Bitrate_perChirp_perLane = (numRxch * DFEoutrate * (numDFEsamples/chirp) * (complexmode+1) *(numbits/sample[12,14,16]) / (numLanes)

   perChirp_Outperiod = Bitrate_perChirp_perLane / (DDC_Clkrate * 2)

   IdleTime = MAX(Synthesizer_IdleTime, perChirp_Outperiod)

   Note: Synthesizer_IdleTime can be calculated in the mmWave Sensing Estimator.

2. If the customer uses the LVDS High Speed output format, this ADC clock disturbance is not seen.

ANA#08   *Doppler Spur Observed for Narrow Chirps Spanning 79.2 GHz*

Revision(s) Affected: IWR1443 ES3.0

Description: There is a nonlinearity of the synthesizer when crossing 79.2 GHz due to coupling from its reference to the VCO.

Implication: There is a spur in non-zero Doppler bin if the synthesizer crosses 79.2 GHz during a chirp. The exact Doppler bin depends on the slope of the ramp. This is not observed for wide bandwidth or higher ramp slopes.

Workaround(s):   Avoid narrow, slow ramps near 79.2 GHz.

ANA#11   *TX, RX Gain Calibrations Sensitive to Large External Interference*

Revision(s) Affected: IWR1443 ES1.0, IWR1443 ES2.0, and IWR1443 ES3.0

Description: External interference present on the RX or TX pins with level >-10dBm can lead to degraded accuracy or errors in the peak detector, TX, and RX gain calibrations. If the interference changes its level while these calibrations are actively running, the calibration algorithm may interpret this as a change in signal power, leading to incorrect convergence. This applies to boot-time PD, TX, and RX calibrations, as well as run-time TX output power calibration.

Workaround(s):   The incident power detector in the TX output power detector, along with the absolute level of the PA loopback used during the PA loopback monitors, are insensitive to this, and they can be used to check that the calibrations converged correctly. Calibration can be re-run if large interference was observed.

Trademarks

All trademarks are the property of their respective owners.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE AND DISCLAIMER