

## DESCRIPTION

The MP8869S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I<sup>2</sup>C control interface. The MP8869S offers a fully integrated solution that achieves 12A of continuous current and 15A of peak output current with excellent load and line regulation over a wide input supply range.

The output voltage level can be controlled on-the-fly through an I<sup>2</sup>C serial interface. The reference voltage range can be adjusted from 0.6V to 1.108V in 4mV steps. The voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-saving mode are also selectable through the I<sup>2</sup>C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates when the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8869S is available in a QFN-14 (3mmx4mm) package.

## FEATURES

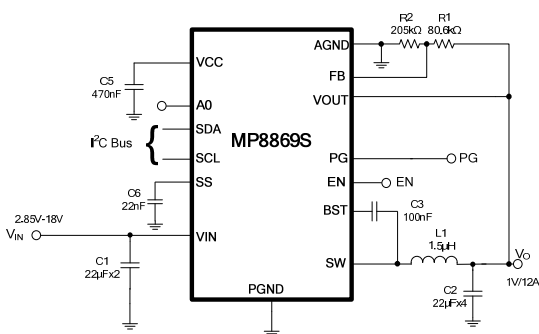
- Vout Adjustable up to 5.5V using FB pin
- Wide 2.85V to 18V Operating Input Range
- 12A Continuous/15A Peak Output Current
- 1% Internal Reference Accuracy
- I<sup>2</sup>C-Programmable Reference Range from 0.6V to 1.108V in 4mV Steps with Slew Rate Control
- 5% Accuracy Output Voltage and Output Current Monitoring via I<sup>2</sup>C
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit through I<sup>2</sup>C
- Four Different Selectable I<sup>2</sup>C Addresses
- External Soft Start (SS)
- Open-Drain Power Good (PG) Indication
- Output Over-Voltage Protection (OVP)
- Hiccup/Latch-Off Over-Current Protection (OCP)
- Available in a QFN-14 (3mmx4mm) Package

## APPLICATIONS

- Solid-State Drives (SSD)
- Flat-Panel Televisions and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Servers

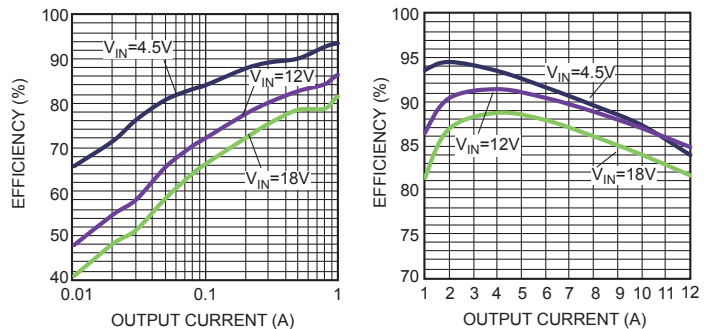
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## TYPICAL APPLICATION



## Efficiency vs. Output Current

V<sub>OUT</sub> = 1V, L = 1.5µH, DCR = 2.1mΩ



### ORDERING INFORMATION

Part Number	Package	Top Marking
MP8869SGL*	QFN-14 (3mmx4mm)	See Below
EVKT-8869S	Evaluation Kit	

\* For Tape & Reel, add suffix -Z (e.g. MP8869SGL-Z)

### TOP MARKING

**MPYW**

**8869**

**SLLL**

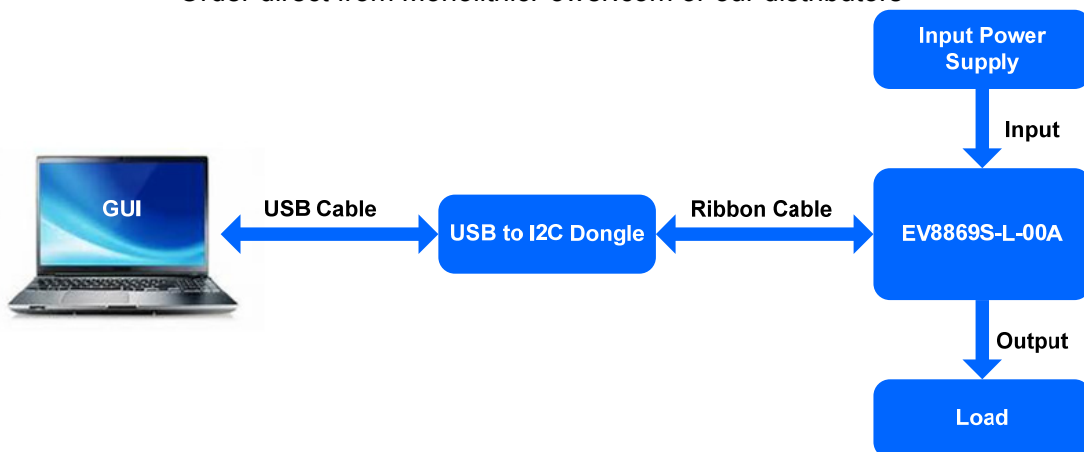
MP: Product code of MP8869SGL  
 Y: Year code  
 W: Lot number  
 8869S: First five digits of the part number  
 LLL: Lot number

### EVALUATION KIT EVKT-8869S

EVKT-8869S Kit contents: (Items can be ordered separately).

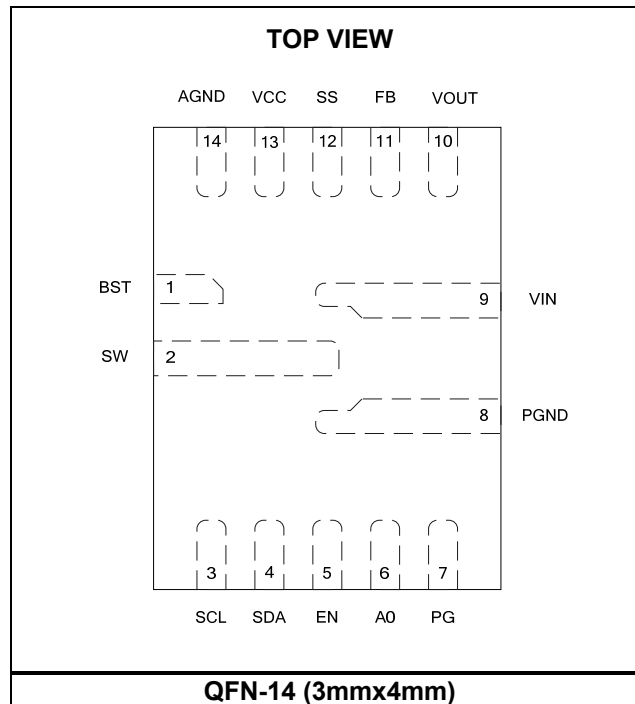
#	Part Number	Item	Quantity
1	EV8869S-L-00A	MP8869SGL Evaluation Board	1
2	EVKT-USBI2C-02	Includes one USB to I2C Dongle, one USB Cable, and one Ribbon Cable	1
3	Tdrive-8869S	USB Flash drive that stores the GUI installation file and supplemental documents	1

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**Figure 1. EVKT-8869S Evaluation Kit Setup**

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

VIN .....	-0.3V to 19V
V <sub>SW</sub> .....	-0.6V (-7V for <10ns) to VIN + 0.7V (25V for <25ns)
V <sub>BST</sub> .....	V <sub>SW</sub> + 4V
V <sub>EN</sub> .....	18V
VOUT .....	7V
All other pins .....	-0.3V to 4V
Continuous power dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	
QFN-14 (3mmx4mm).....	2.5W
Junction temperature .....	150°C
Lead temperature.....	260°C
Storage temperature.....	-65°C to 150°C

#### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage (VIN).....	2.85V to 18V
Output voltage (VOUT).....	0.6V to 5.5V
Operating junction temp. (T <sub>J</sub> ).....	-40°C to +125°C

<b>Thermal Resistance <sup>(4)</sup></b>	<b>θ<sub>JA</sub></b>	<b>θ<sub>JC</sub></b>
QFN-14 (3mmx4mm).....	48	11 ... °C/W

#### NOTES:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX) = (T<sub>J</sub>(MAX)-T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS**
**VIN = 12V, T<sub>J</sub> = -40°C to +125°C <sup>(5)</sup>, typical value is tested at T<sub>J</sub> = +25°C, unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I <sub>IN</sub>	V <sub>EN</sub> = 0V		2.1	4	μA
Supply current (quiescent)	I <sub>q</sub>	No switching, FB = 105% V <sub>REF</sub> , PFM mode		420	600	μA
HS switch on resistance	HS <sub>RDS(ON)</sub>	V <sub>BST - SW</sub> = 3.3V		15		mΩ
LS switch on resistance	LS <sub>RDS(ON)</sub>	V <sub>CC</sub> = 3.3V		4.5		mΩ
Switch leakage	SW <sub>LKG</sub>	V <sub>EN</sub> = 0V, V <sub>SW</sub> = 12V, T <sub>J</sub> = +25°C			1	μA
Low-side valley current limit	I <sub>LIMIT_L</sub>	Adjustable by I <sup>2</sup> C		14		A
Low-side negative current limit	I <sub>LIMIT_LN</sub>	In forced PWM mode or OVP state		-3		A
Low-side ZCD threshold	I <sub>ZCD</sub>	T <sub>J</sub> = +25°C		200		mA
Switching frequency	f <sub>SW1</sub>	VIN = 12V, VOUT = 1V	400	500	600	kHz
	f <sub>SW2</sub>	VIN = 12V, VOUT = 5V	400	500	600	
Minimum off time <sup>(6)</sup>	TOFF_MIN			185		ns
Minimum on time <sup>(6)</sup>	TON_MIN	VOUT = 0.6V		50		ns
Reference voltage	V <sub>ref</sub>	T <sub>J</sub> = 25°C	-1%	720	+1%	mV
		-40°C < T <sub>J</sub> < 125°C <sup>(5)</sup>	-1.5%	720	+1.5%	
FB current	I <sub>FB</sub>	V <sub>FB</sub> = 740mV		10	50	nA
A0 voltage threshold 1	V <sub>ADD_1</sub>	Set I <sup>2</sup> C address 61H			0.24	VCC
A0 voltage threshold 2	V <sub>ADD_2</sub>	Set I <sup>2</sup> C address 63H	0.28		0.49	VCC
A0 voltage threshold 3	V <sub>ADD_3</sub>	Set I <sup>2</sup> C address 65H	0.53		0.72	VCC
A0 voltage threshold 4	V <sub>ADD_4</sub>	Set I <sup>2</sup> C address 67H	0.77			VCC
A0 to GND pull-down resistor	R <sub>A0_PD</sub>			2		MΩ
EN rising threshold	V <sub>EN_RISING</sub>		1.1	1.2	1.3	V
EN threshold hysteresis	V <sub>EN_HYS</sub>			110		mV
EN to GND pull-down resistor	R <sub>EN</sub>			1.5		MΩ
VIN under-voltage lockout threshold rising	INUV <sub>Vth_r</sub>		2.45	2.65	2.85	V
VIN under-voltage lockout threshold Falling	INUV <sub>Vth_f</sub>		2.3	2.5	2.7	V
Power good UV threshold rising	PGV <sub>th-Hi</sub>	Good	0.86	0.9	0.94	VOUT
Power good UV threshold falling	PGV <sub>th-Lo</sub>	Fault	0.81	0.85	0.89	VOUT
Power good OV threshold rising	PGV <sub>th-Hi</sub>	Fault	1.11	1.15	1.19	VOUT
Power good OV threshold falling	PGV <sub>th-Lo</sub>	Good	1.01	1.05	1.09	VOUT
Power good deglitch time	PGTd	I <sup>2</sup> C programmable		30		μs
Power good sink current capability	V <sub>PG</sub>	Sink 4mA			0.4	V

**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 12V, T<sub>J</sub> = -40°C to +125°C <sup>(5)</sup>, typical value is tested at T<sub>J</sub> = +25°C, unless otherwise noted.**

Parameter	Symbol	Condition	Min	Typ	Max	Units
OVP rising threshold	V <sub>OVP_Rise</sub>	FB	121%	125%	129%	V <sub>REF</sub>
OVP falling threshold	V <sub>OVP_Falling</sub>	FB	106%	110%	114%	V <sub>REF</sub>
OVP delay	T <sub>OVP</sub>			3.7		μs
Output pin absolute OV	V <sub>OVP2</sub>		6	6.5	7	V
UVP threshold	V <sub>FB_UV_th</sub>	Hiccup entry	55%	60%	65%	V <sub>REF</sub>
UVP delay <sup>(6)</sup>	T <sub>UVP</sub>			10		μs
Soft-start current	I <sub>SS</sub>		5	7	9	μA
VCC voltage	V <sub>CC</sub>			3.5		V
VCC load regulation	V <sub>CC_reg</sub>	I <sub>CC</sub> = 20mA			3	%
Thermal shutdown <sup>(6)</sup>	T <sub>TSD</sub>			160		°C
Thermal hysteresis <sup>(6)</sup>	T <sub>TSD_HYS</sub>			20		°C

**NOTES:**

5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by design and characterization test.

**I/O LEVEL CHARACTERISTICS**

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	$V_{IL}$		-0.5	$0.3V_{CC}$	-0.5	$0.3V_{CC}$	V
High-level input voltage	$V_{IH}$		$0.7V_{CC}$	$V_{CC} + 0.5$	$0.7V_{CC}$	$V_{CC} + 0.5$	V
Hysteresis of Schmitt trigger inputs	$V_{HYS}$	$V_{CC} > 2V$	$0.05V_{CC}$	-	$0.05V_{CC}$	-	V
		$V_{CC} < 2V$	$0.1V_{CC}$	-	$0.1V_{CC}$	-	
Low-level output voltage (open drain) at 3mA sink current	$V_{OL}$	$V_{CC} > 2V$	0	0.4	0	0.4	V
		$V_{CC} < 2V$	0	$0.2V_{CC}$	0	$0.2V_{CC}$	
Low-level output current	$I_{OL}$		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	$R_{onL}$	VOL level, $I_{OL} = 3mA$	-	50	-	50	$\Omega$
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	$R_{onH}$	Both signals (SDA and SDAH, or SCL and SCLH) at $V_{CC}$ level	50	-	50	-	k $\Omega$
Pull-up current of the SCLH current source	$I_{cs}$	SCLH output levels between $0.3V_{CC}$ and $0.7V_{CC}$	2	6	2	6	mA
Rise time of the SCLH or SCL signal	$T_{rCL}$	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	$T_{fCL}$	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	$T_{rDA}$	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	$T_{fDA}$	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns

**I/O LEVEL CHARACTERISTICS (continued)**

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	$t_{SP}$		0	10	0	50	ns
Input current each I/O pin	$I_i$	Input voltage between $0.1V_{CC}$ and $0.9V_{CC}$	-	10	-10	+10	$\mu A$
Capacitance for each I/O pin	$C_i$		-	10	-	10	pF

**I<sup>2</sup>C PORT SIGNAL CHARACTERISTICS**

Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f <sub>SCLH</sub>		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	T <sub>SU;STA</sub>		160	-	600	-	ns
Hold time (repeated) start condition	T <sub>HD;STA</sub>		160	-	600	-	ns
Low period of the SCL clock	T <sub>LOW</sub>		160	-	1300	-	ns
High period of the SCL clock	T <sub>HIGH</sub>		60	-	600	-	ns
Data set-up time	T <sub>SU;DAT</sub>		10	-	100	-	ns
Data hold time	T <sub>HD;DAT</sub>		0	70	0	-	ns
Rise time of SCLH signal	T <sub>rCL</sub>		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated start condition and after an acknowledge bit	T <sub>rCL1</sub>		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T <sub>rCL</sub>		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	T <sub>rDA</sub>		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T <sub>rDA</sub>		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	T <sub>SU;STO</sub>		160	-	600	-	ns
Bus free time between a stop and start condition	T <sub>BUF</sub>		160	-	1300	-	ns
Data valid time	T <sub>VD;DAT</sub>		-	16	-	90	ns
Data valid acknowledge time	T <sub>VD;ACK</sub>		-	160	-	900	ns
Capacitive load for each bus line	C <sub>b</sub>	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Noise margin at the low level	C <sub>i</sub>	For each connected device	-	0.1V <sub>CC</sub>	0.1V <sub>CC</sub>	-	V
Noise margin at the high level	V <sub>nH</sub>	For each connected device	-	0.2V <sub>CC</sub>	0.2V <sub>CC</sub>	-	V

**NOTE:** VCC is the I<sup>2</sup>C bus voltage, 1.8V to 3.6V range, and used for 1.8V, 2.5V, and 3.3V bus voltages.

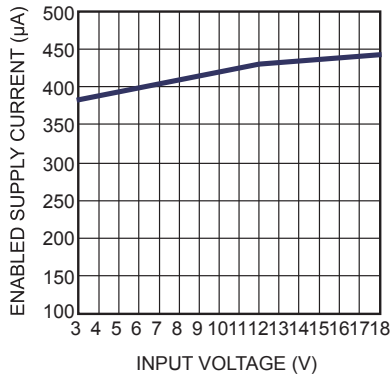


## TYPICAL PERFORMANCE CHARACTERISTICS

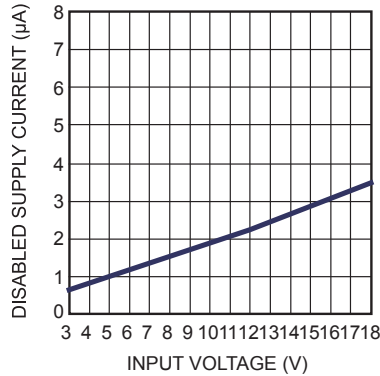
Performance waveforms are tested on the evaluation board.

$V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $L = 1.5\mu H$ ,  $F_s = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

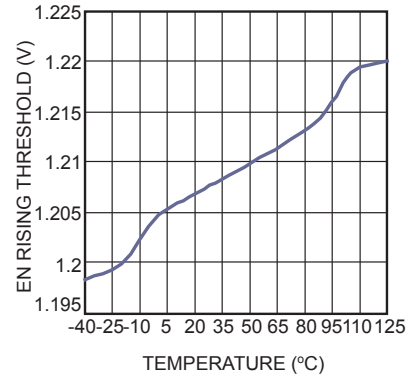
**Enabled Supply Current vs. Input Voltage**



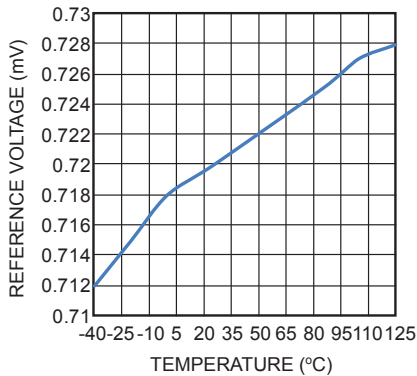
**Disabled Supply Current vs. Input Voltage**



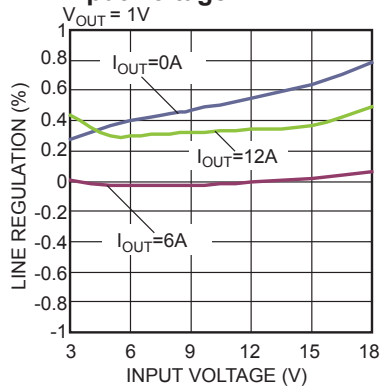
**EN Rising Threshold vs. Temperature**



**Reference Voltage vs. Temperature**

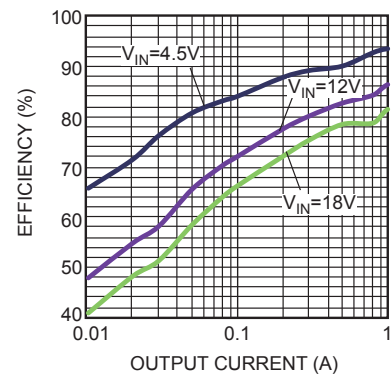


**Line Regulation vs. Input Voltage**



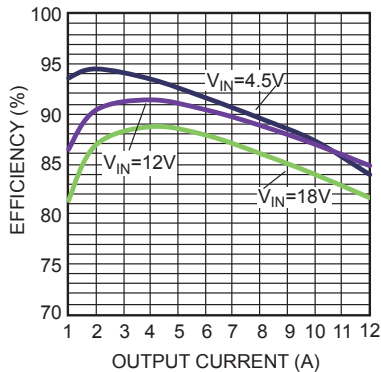
**Efficiency vs. Output Current**

$V_{OUT} = 1V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$



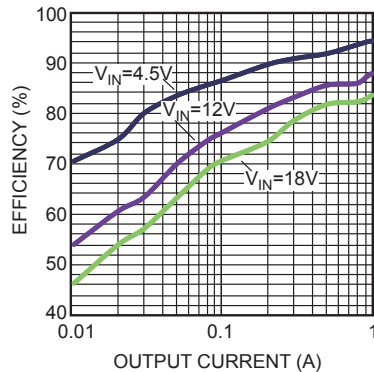
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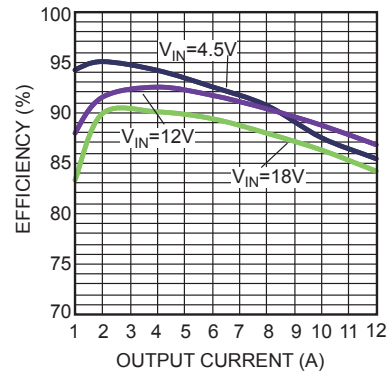
**Efficiency vs. Output Current**

$V_{OUT} = 1.2V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$



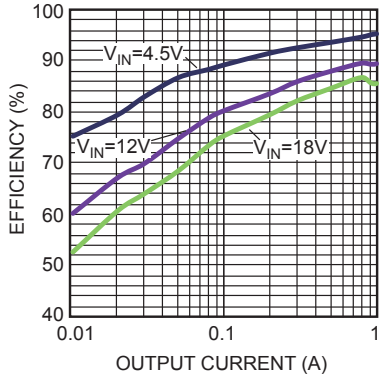
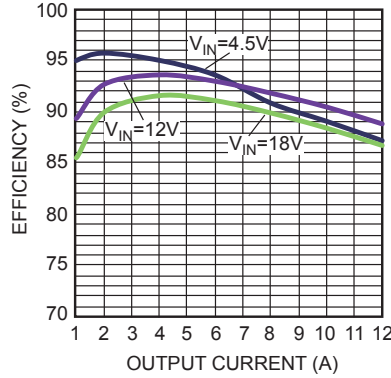
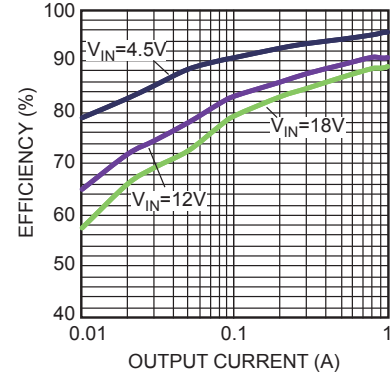
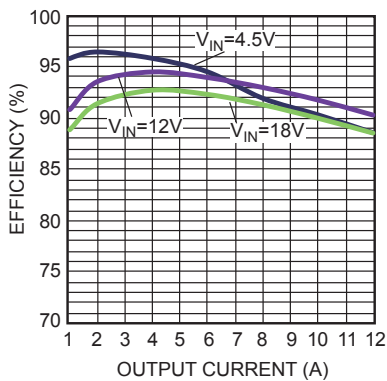
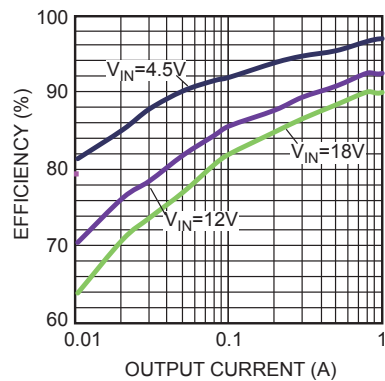
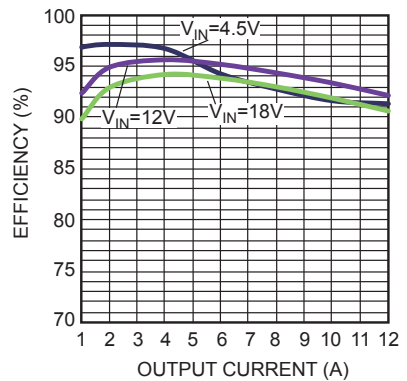
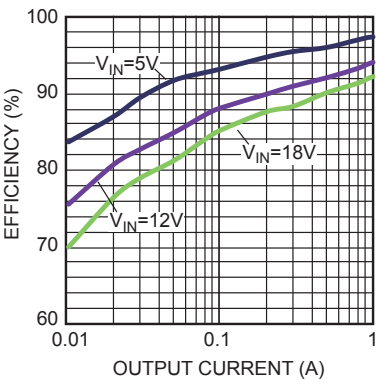
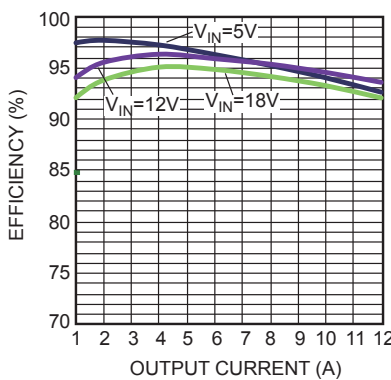
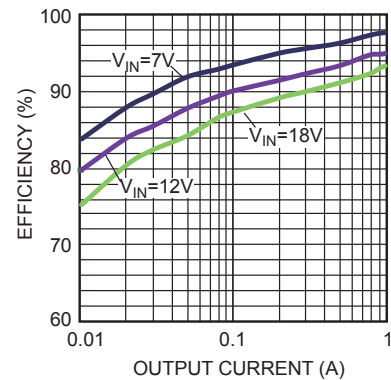
**Efficiency vs. Output Current**

$V_{OUT} = 1.2V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$



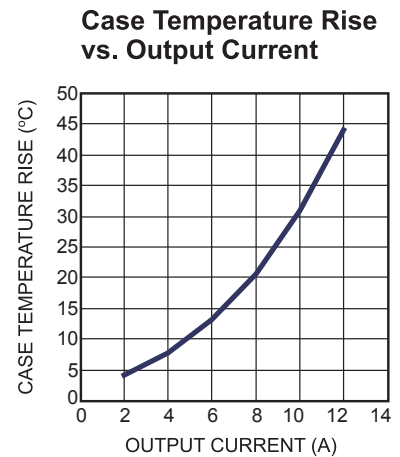
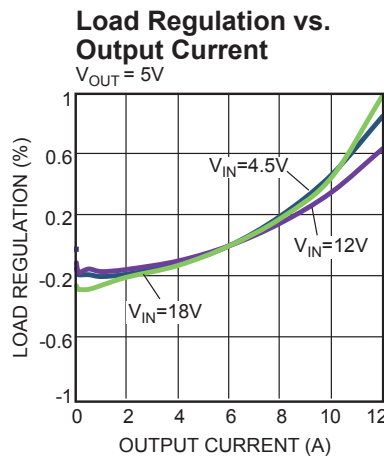
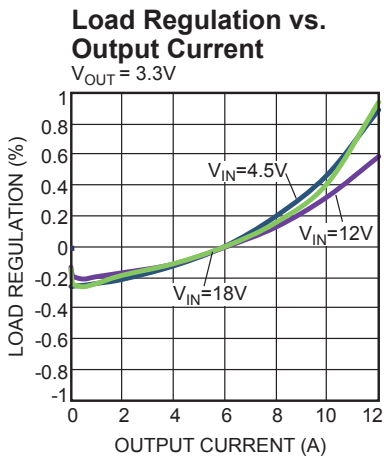
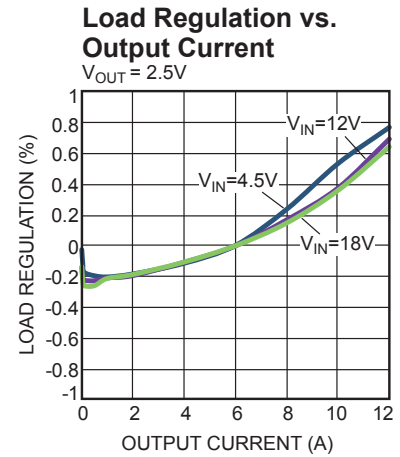
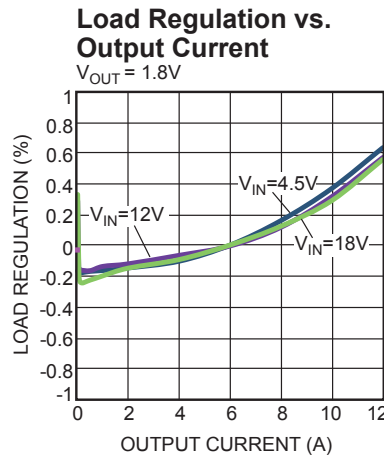
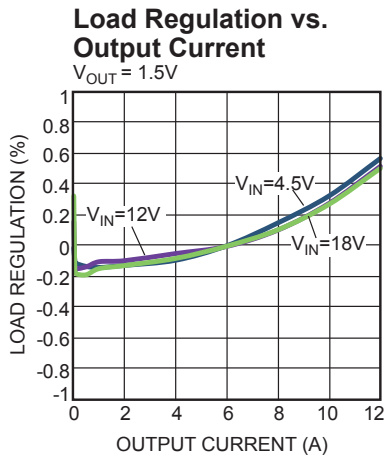
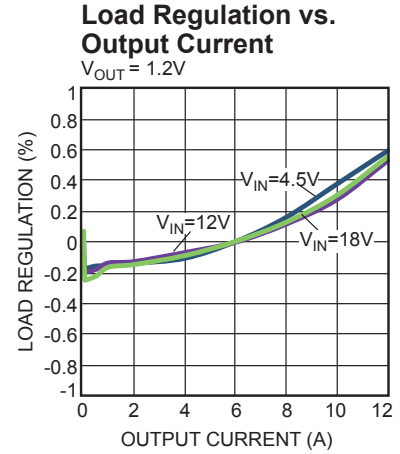
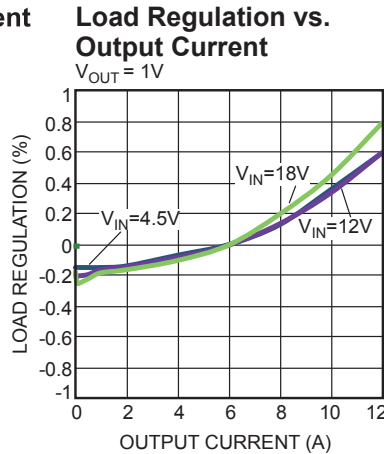
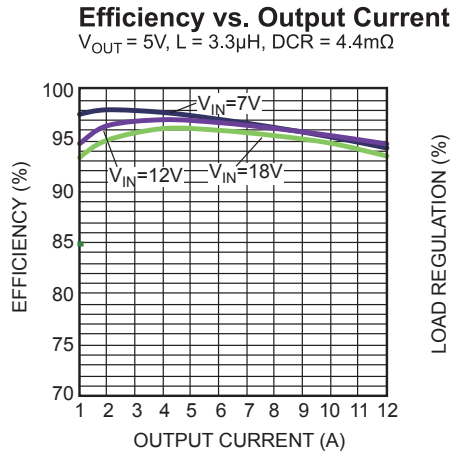
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

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 **$V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $L = 1.5\mu H$ ,  $F_S = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.**
**Efficiency vs. Output Current**  
 $V_{OUT} = 1.5V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 1.5V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 1.8V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 1.8V$ ,  $L = 1.5\mu H$ ,  $DCR = 2.1m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 2.5V$ ,  $L = 2.2\mu H$ ,  $DCR = 3m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 2.5V$ ,  $L = 2.2\mu H$ ,  $DCR = 3m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$ ,  $DCR = 3m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$ ,  $DCR = 3m\Omega$ 

**Efficiency vs. Output Current**  
 $V_{OUT} = 5V$ ,  $L = 3.3\mu H$ ,  $DCR = 4.4m\Omega$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board.

 **$V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $L = 1.5\mu H$ ,  $F_s = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.**


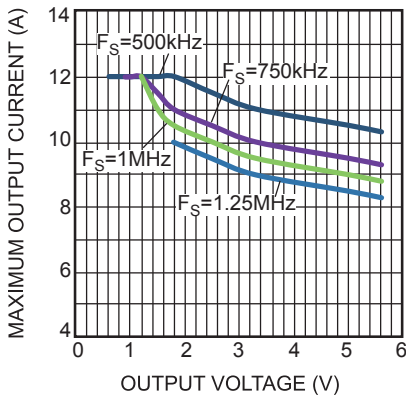
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board.

$V_{IN} = 12V$ ,  $V_{OUT} = 1V$ ,  $L = 1.5\mu H$ ,  $F_S = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.

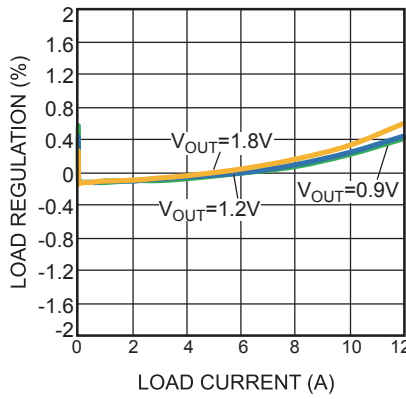
**Output Current Derating vs. Frequency and Output Voltage**

$V_{IN} = 12V$ , 4 Layer PCB Board, 8.5cmx8.5cm



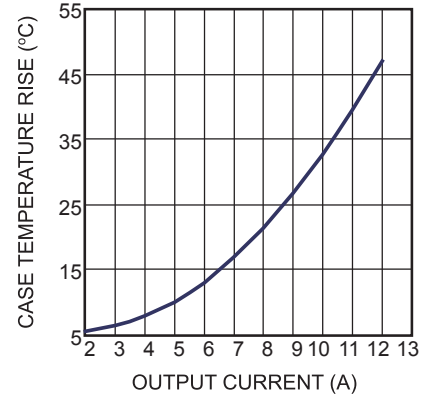
**Load Regulation**

$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$



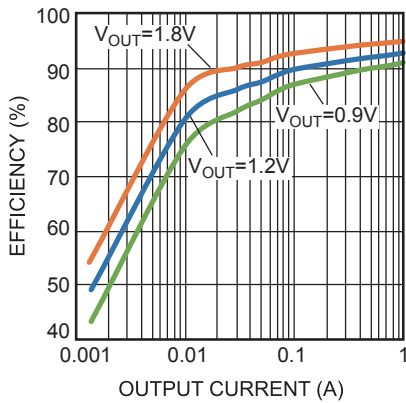
**Case Temperature Rise vs. Output Current**

$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$



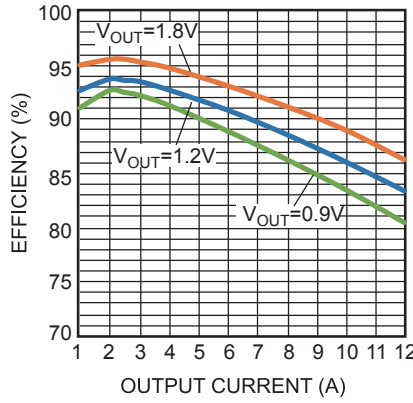
**Efficiency Curve**

$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$



**Efficiency Curve**

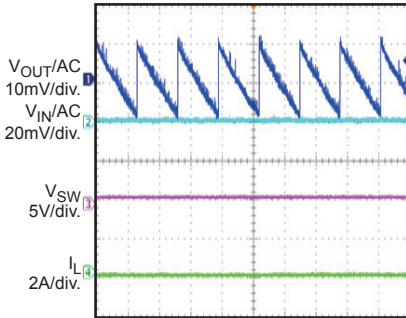
$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

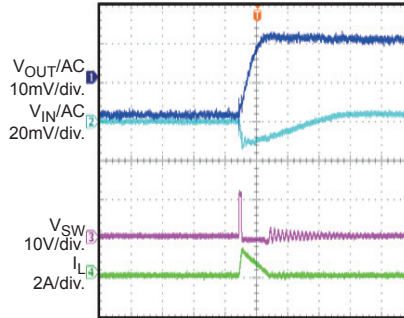
Performance waveforms are tested on the evaluation board.

**V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 1V, L = 1.5μH, F<sub>S</sub> = 500kHz, auto PFM/PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.**
**Input/Output Ripple**

 I<sub>OUT</sub> = 0A


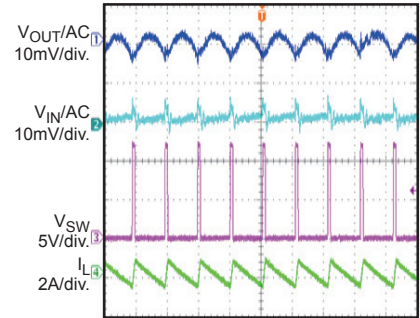
40ms/div.

**Input/Output Ripple**

 I<sub>OUT</sub> = 0A


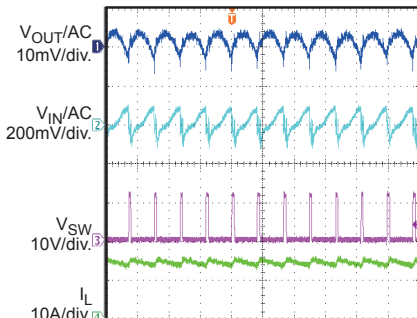
2μs/div.

**Input/Output Ripple**

 I<sub>OUT</sub> = 0A, Forced PWM Mode


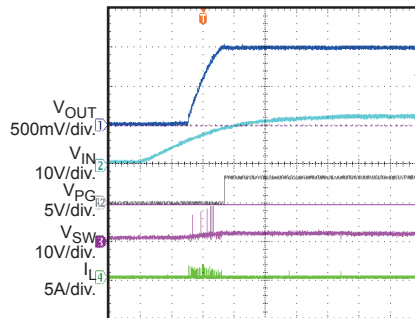
2μs/div.

**Input/Output Ripple**

 I<sub>OUT</sub> = 12A


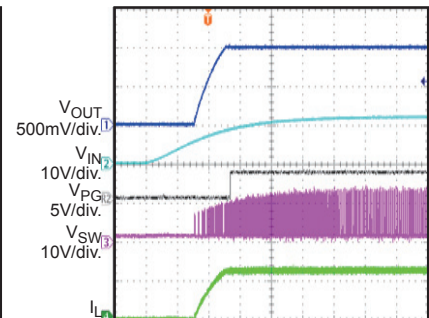
2μs/div.

**Start-Up through Input Voltage**

 I<sub>OUT</sub> = 0A


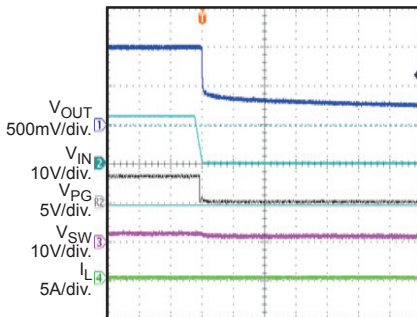
2ms/div.

**Start-Up through Input Voltage**

 I<sub>OUT</sub> = 12A


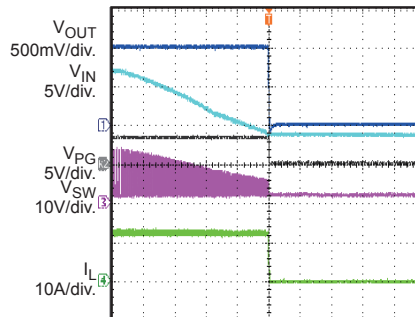
2ms/div.

**Shutdown through Input Voltage**

 I<sub>OUT</sub> = 0A


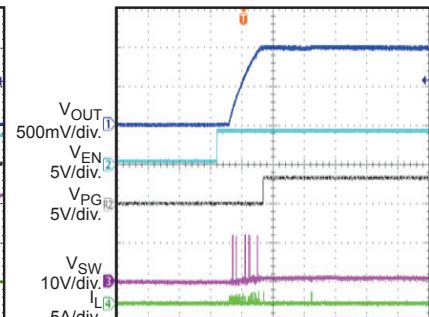
400ms/div.

**Shutdown through Input Voltage**

 I<sub>OUT</sub> = 12A


1ms/div.

**Start-Up through EN**

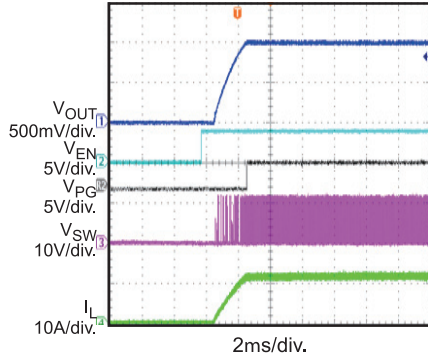
 I<sub>OUT</sub> = 0A


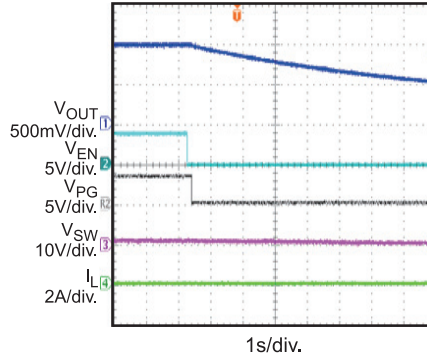
2ms/div.

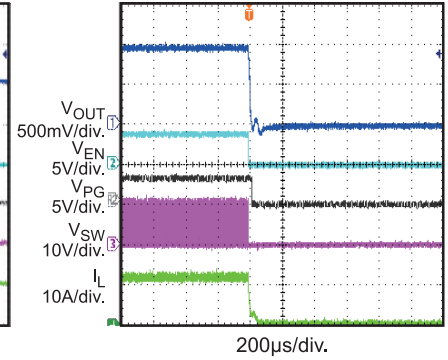
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

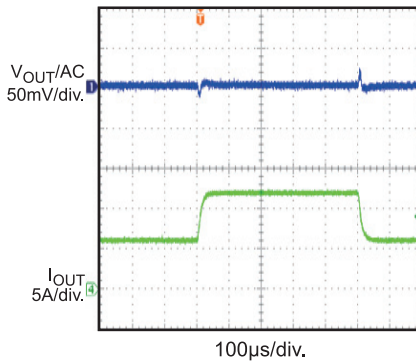
Performance waveforms are tested on the evaluation board.

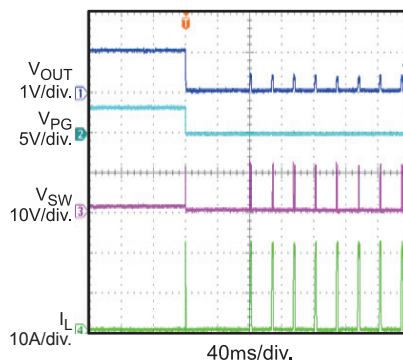
**V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 1V, L = 1.5μH, F<sub>S</sub> = 500kHz, auto PFM/PWM mode, T<sub>A</sub> = 25°C, unless otherwise noted.**
**Start-Up through EN**

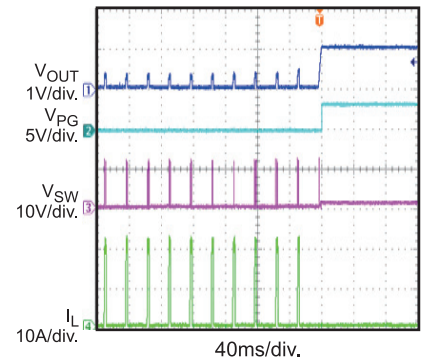
 I<sub>OUT</sub> = 12A

**Shutdown through EN**

 I<sub>OUT</sub> = 0A

**Shutdown through EN**

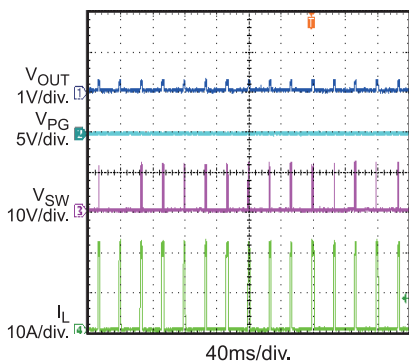
 I<sub>OUT</sub> = 12A

**Load Transient**

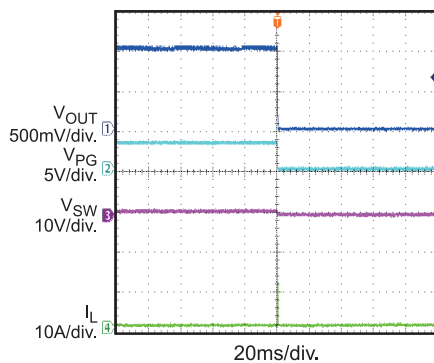
 I<sub>OUT</sub> = 6A-12A

**Short-Circuit Protection Entry**

 I<sub>OUT</sub> = 0A

**Short-Circuit Protection Recovery**

 I<sub>OUT</sub> = 0A

**Short-Circuit Protection Steady State**

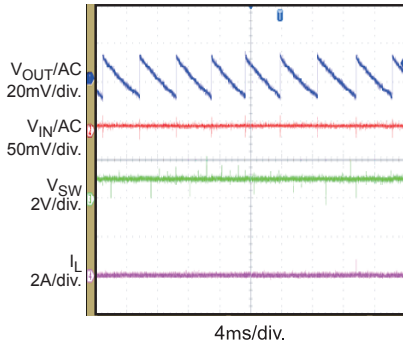
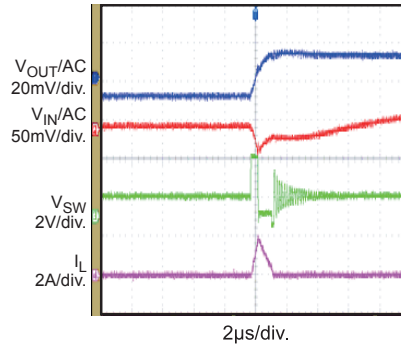
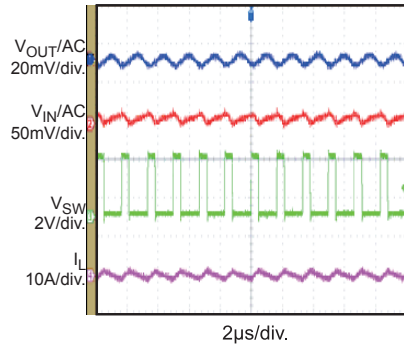
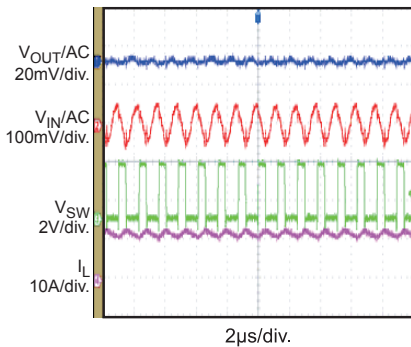
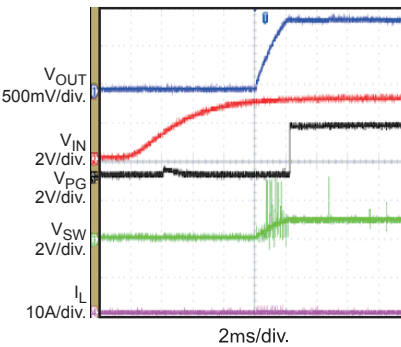
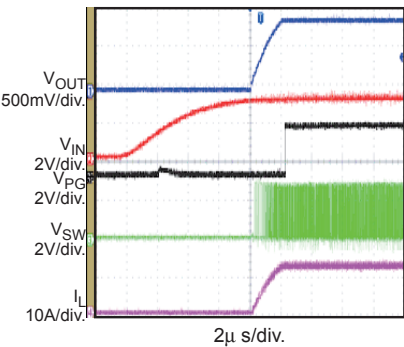
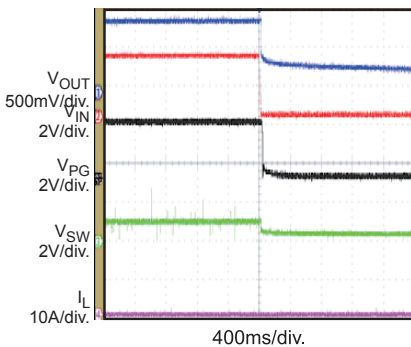
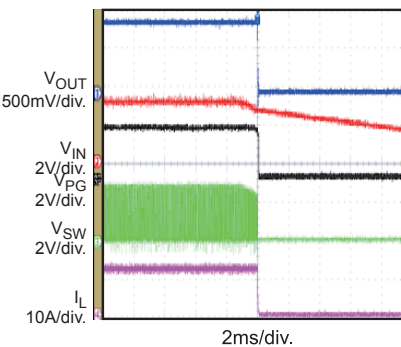
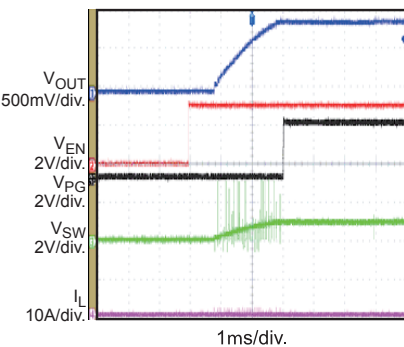
Short Output to GND


**Short-Circuit Protection Entry, Latch Off Mode**

 I<sub>OUT</sub> = 0A


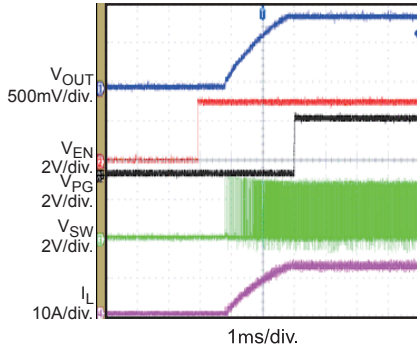
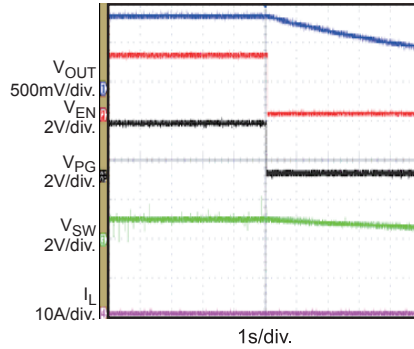
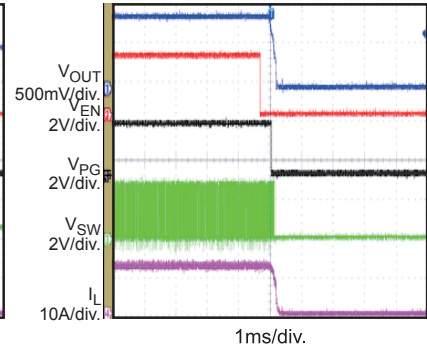
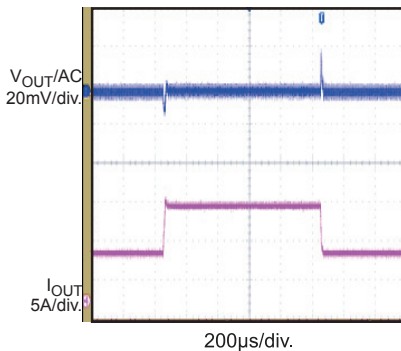
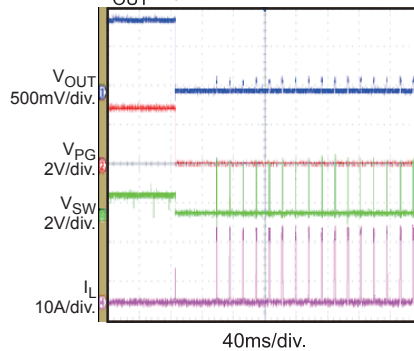
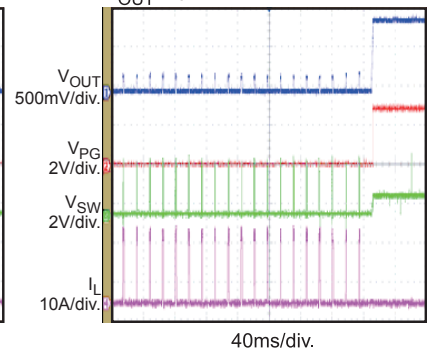
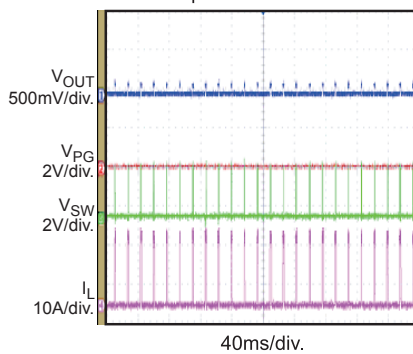
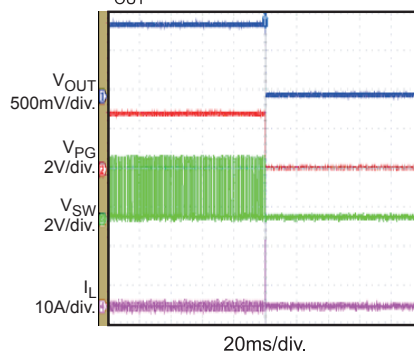
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board.

 **$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$ ,  $L = 0.47\mu H$ ,  $F_s = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.**
**Input/Output Ripple**  
 $I_{OUT} = 0A$ 

**Input/Output Ripple**  
 $I_{OUT} = 0A$ 

**Input/Output Ripple**  
 $I_{OUT} = 0A$ , Forced PWM Mode

**Input/Output Ripple**  
 $I_{OUT} = 12A$ 

**Start-Up through Input Voltage**  
 $I_{OUT} = 0A$ 

**Start-Up through Input Voltage**  
 $I_{OUT} = 12A$ 

**Shutdown through Input Voltage**  
 $I_{OUT} = 0A$ 

**Shutdown through Input Voltage**  
 $I_{OUT} = 12A$ 

**Start-Up through EN**  
 $I_{OUT} = 0A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board.

 **$V_{IN} = 3V$ ,  $V_{OUT} = 0.9V$ ,  $L = 0.47\mu H$ ,  $F_S = 500kHz$ , auto PFM/PWM mode,  $T_A = 25^\circ C$ , unless otherwise noted.**
**Start-Up through EN**  
 $I_{OUT} = 12A$ 

**Shutdown through EN**  
 $I_{OUT} = 0A$ 

**Shutdown through EN**  
 $I_{OUT} = 12A$ 

**Load Transient**  
 $I_{OUT} = 6A-12A$ 

**Short-Circuit Protection Entry**  
 $I_{OUT} = 0A$ 

**Short-Circuit Protection Recovery**  
 $I_{OUT} = 0A$ 

**Short-Circuit Protection Steady State**  
 Short Output to GND

**Short-Circuit Protection Entry, Latch Off Mode**  
 $I_{OUT} = 0A$ 




**PIN FUNCTIONS**

QFN-14 Pin#	Name	Description
1	BST	<b>Bootstrap.</b> A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	<b>Switch output.</b> Connect SW using a wide PCB trace.
3	SCL	<b>I<sup>2</sup>C serial clock.</b>
4	SDA	<b>I<sup>2</sup>C serial data.</b>
5	EN	<b>Enable.</b> Drive EN high to enable the MP8869S. EN has a 1.5M $\Omega$ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to VIN directly for auto start-up.
6	A0	<b>I<sup>2</sup>C address set-up.</b> Connect a resistor divider from VCC to A0 to set different I <sup>2</sup> C addresses.
7	PG	<b>Power good indication.</b> PG is an open-drain structure. PG is de-asserted if the output voltage is out of the regulation window.
8	PGND	<b>System power ground.</b> PGND is the reference ground of the regulated output voltage. PGND requires special consideration during the PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	<b>Supply voltage.</b> The MP8869S operates from a 2.85V to 18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN using a wide PCB trace.
10	VOUT	<b>Output voltage sense.</b> Connect VOUT to the positive terminal of the load.
11	FB	<b>Feedback.</b> Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.
12	SS	<b>Soft-start set-up.</b> Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	<b>Internal LDO regulator output.</b> Decouple VCC with a 0.47 $\mu$ F capacitor.
14	AGND	<b>Signal ground.</b> If AGND is not connected to PGND internally, ensure that AGND is connected to PGND during the PCB layout.

### BLOCK DIAGRAM

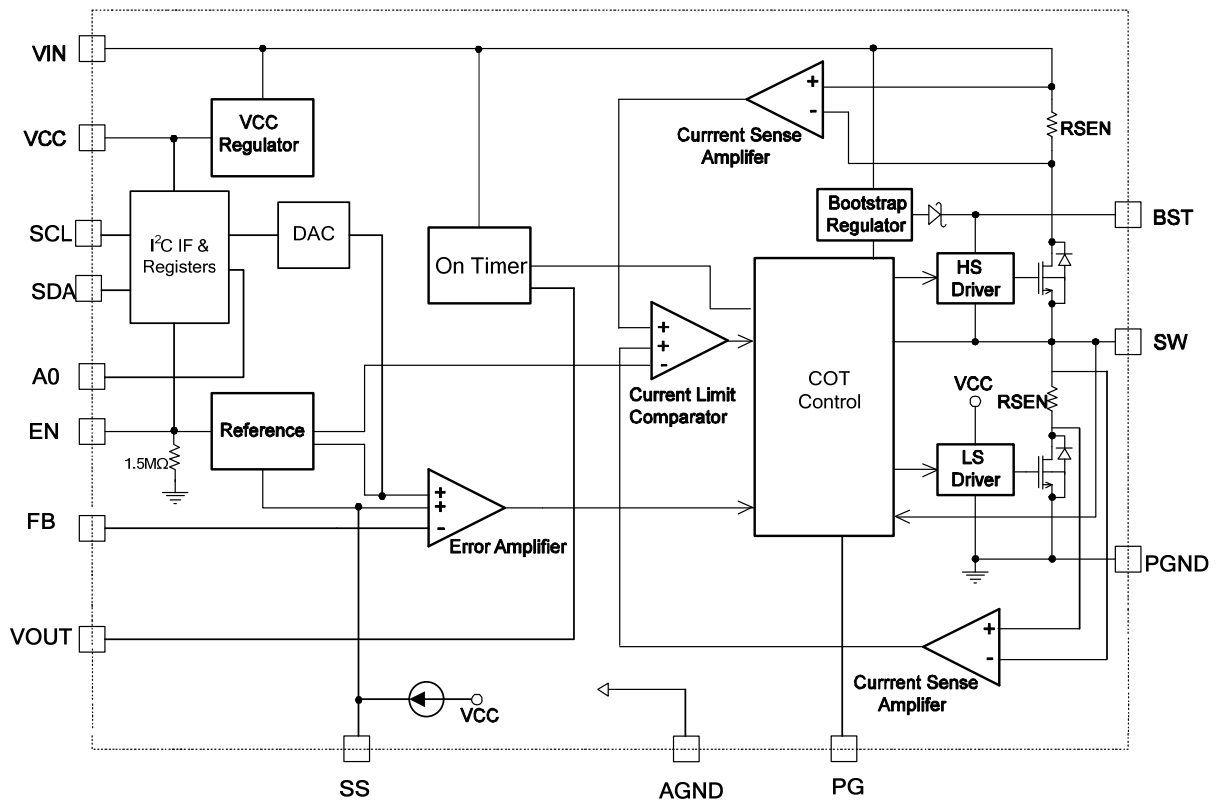


Figure 2: Functional Block Diagram

## OPERATION

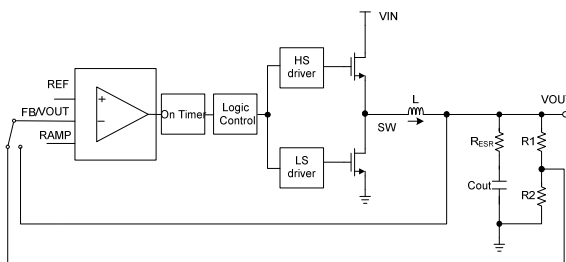
### Pulse-Width Modulation (PWM) Operation

The MP8869S is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MP8869S uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 3 shows the simplified ramp compensation block.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage ( $V_{Ramp}$ ) is below the error amplifier output voltage ( $V_{EAO}$ ), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET enters the off state. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are on at the same time, causing a dead short between input and GND, reducing efficiency dramatically. The MP8869S prevents shoot-through by generating a dead-time (DT) internally between the HS-FET off and LS-FET on period and the LS-FET off and HS-FET on period. The MP8869S enters either heavy-load operation or light-load operation depending on the amplitude of the output current.



**Figure 3: Simplified Compensation Block**

### Switching Frequency

The MP8869S uses constant-on-time (COT) control, and there is no dedicated oscillator in the IC. The input voltage is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is  $V_{OUT}/V_{IN}$ , and the switching frequency is fairly constant over the input voltage range.

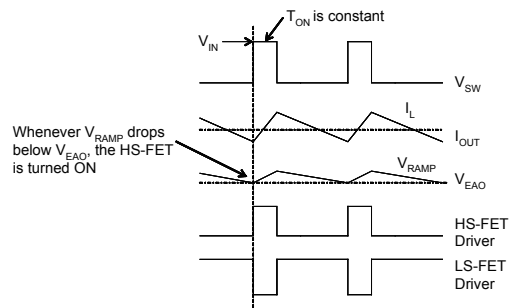
The MP8869S's switching frequency can be adjusted by setting the two bits D[5:4] in register 02 through I<sup>2</sup>C communication. When the output voltage setting is low and the input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and switching frequency decreases. Table 1 shows the maximum switching frequency vs. the output voltage when  $V_{IN} = 12V$  and  $V_{IN} = 5V$ .

**Table 1: Maximum Frequency Selecting vs. Output Voltage**

Vo (V)	Maximum Frequency Selecting	
	VIN = 12V	VIN = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

### Forced PWM Operation

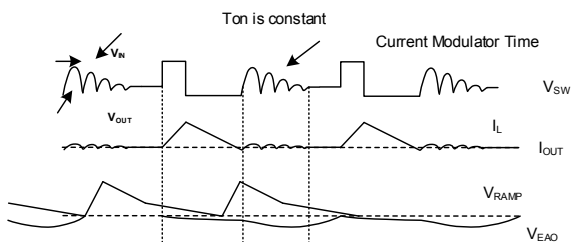
When the MP8869S works in forced pulse-width modulation (PWM) mode, the MP8869S enters continuous conduction mode (CCM), where the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is zero or a negative value. The switching frequency ( $f_{sw}$ ) is fairly constant (see Figure 4).



**Figure 4: Forced PWM Operation**

### Light-Load Operation

When the MP8869S works in auto-PWM, auto-pulse-frequency modulation (PFM) mode, or light-load operation, the MP8869S reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 5). The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when the output current is low.



**Figure 5: Light-Load Operation**

Light-load operation is also called skip mode since the HS-FET does not turn on as frequently as it does during heavy-load condition. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MP8869S reverts to PWM mode once the output current exceeds the critical level. The switching frequency then remains fairly constant over the output current range.

The MP8869S can operate in PFM mode under light load to improve efficiency (low-power mode). The MP8869S can also operate in forced PWM mode at any load condition. This mode is selectable through the I<sup>2</sup>C control. To enable low-power mode, set the mode bit to 0. To disable low-power mode, set the mode bit to 1, and the converter will work in forced PWM mode. The mode bit is set to 0 (PFM) by default.

### Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot be used as output capacitors, typically. The MP8869S has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

### VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is needed to stabilize the regulator and reduce ripple. This regulator takes the V<sub>IN</sub> input and operates in the full V<sub>IN</sub> range. After EN is pulled high and V<sub>IN</sub> is greater than 3.5V, the output of the regulator is in full regulation. When V<sub>IN</sub> is lower than 3.5V, the output voltage decreases and follows the input voltage. A 0.47μF ceramic capacitor is required for decoupling.

### Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage against the internal reference voltage and outputs a PWM signal. The reference voltage can be programmed from 0.6V to 1.108V via the I<sup>2</sup>C. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

### Enable (EN)

EN is a digital control pin that turns the regulator, including the I<sup>2</sup>C block, on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V input voltage, which allows EN to be connected to V<sub>IN</sub> directly for automatic start-up. When the external EN is high, set the EN bit to 0 in register 01 to stop the HS-FET and LS-FET from switching. The MP8869S resumes switching by setting the EN bit to 1.

### Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8869S UVLO comparator monitors the input voltage, VIN, and output voltage of the VCC regulator. The MP8869S is active when the voltages exceed the UVLO rising threshold.

### Soft-Start (SS) and Pre-Bias Start-Up

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The approximate typical soft-start time can be calculated with Equation (2):

$$t_{ss}(\text{ms}) = \frac{V_{ref}(\text{V}) \times C_{ss}(\text{nF})}{7\mu\text{A}} \quad (2)$$

Where  $V_{ref}$  is reference voltage.

If the output of the MP8869S is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed output voltage at FB.

The MP8869S also provides a selectable soft-stop function which defines the output discharge behavior after an EN shutdown. By default, the output is not controlled after EN shutdown. If setting the soft-stop control bit D[3] to 1 in register 02 via the I<sup>2</sup>C, the output is discharged linearly to zero in a quarter of the soft-start time.

### Over-Current Protection (OCP)

The MP8869S has a default, hiccup, cycle-by-cycle, over-current limiting control. The current-limit circuit employs both a high-side current limit and a low-side valley current-sensing algorithm. The MP8869S uses the  $R_{DS(ON)}$  of the LS-FET as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal is above the current-limit threshold, the PWM on pulse is terminated, and the LS-FET is turned on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the

positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. PWM is not allowed to initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current limit occurs, the output voltage drops until VOUT is below the under-voltage (UV) threshold (typically 60% below the reference). Once UV is triggered, the MP8869S enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8869S exits hiccup mode once the over-current condition is removed.

Short the output to ground first, and then power on the part. The MP8869S's I<sup>2</sup>C is disabled in this condition. The I<sup>2</sup>C resumes operation after the short circuit is removed. When the hiccup over-current protection (OCP) bit D[1] in register 01 is set to 0 by the I<sup>2</sup>C, a latch-off occurs if OCP is triggered, and FB under-voltage protection (UVP) is triggered.

### Power Good (PG)

The power good (PG) pin indicates whether the output voltage is in the normal range compared to the internal reference voltage. PG is an open-drain structure. An external pull-up supply is required. During power-up, the PG output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum. This helps reduce in-rush current at start-up.

When the output voltage is higher than 90% and lower than 115% of the internal reference voltage, and the soft start is finished, then the PG signal is pulled high. When the output voltage is lower than 85% after the soft start finishes, the PG signal remains low. When the output voltage is higher than 115% of the internal reference, PG is switched low. The PG signal rises back to high after the output voltage drops below 105% of the internal reference voltage.

PG implements an adjustable deglitch time via the I<sup>2</sup>C whenever VOUT crosses the under-voltage and over-voltage (UV, OV) rising and falling threshold. This guarantees the correct indication when the output voltage is scaled through the I<sup>2</sup>C.

The PG output is pulled low immediately when EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) are triggered.

#### Input Over-Voltage Protection (VIN OVP)

The MP8869S monitors VIN to detect an input over-voltage event. This function is active only when the output is in OV or a soft-stop condition. When the output is in the over-voltage protection (OVP) state or soft stop is enabled, output discharge is enabled to charge the input voltage high. When the input voltage exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

#### Output Over-Voltage Protection (OVP)

The MP8869S monitors both FB and VOUT to detect an over-voltage event. When the FB voltage becomes higher than 125% of the internal reference voltage, an internal comparator monitors FB, and the controller enters dynamic regulation mode. The input voltage may be charged up during this time. When input OVP is triggered, the IC stops switching. If OVP mode is set to auto retry in the I<sup>2</sup>C, the IC begins switching once the input voltage drops below the VIN OVP recover threshold. Otherwise, the MP8869S latches off. OVP auto-retry mode or latch-off mode occurs only if the soft start has finished.

Dynamic regulation mode can be operated by turning on the low side until the low-side negative current limit is triggered. Then the body diode of the HS-FET free-wheels the current.

The output power charges the input, which may trigger the VIN OVP function. In VIN OVP, neither the HS-FET or LS-FET turn on and stop charging VIN. If the output is still over-voltage and the input voltage drops below the VIN OVP threshold, repeat the operation. If the output voltage is below 110% of the internal reference voltage, then output OVP is exited.

#### Output Absolute Over-Voltage Protection (OVP\_ABS)

The MP8869S's VOUT can be adjusted by the feedback reference voltage and the external resistor dividers. But MP8869S's output voltage must be set lower than the absolute OVP threshold (typically 6.5V).

The MP8869S monitors VOUT to detect absolute OVP. When VOUT is larger than 6.5V, the controller enters dynamic regulation mode if the OVP retry bit is set to 1 in the I<sup>2</sup>C register 01. Otherwise, the MP8869S latches off when output OVP and input OVP are both triggered. Absolute OVP works once both the input voltage and EN are higher than their rising thresholds. This means that this function can work even during a soft start.

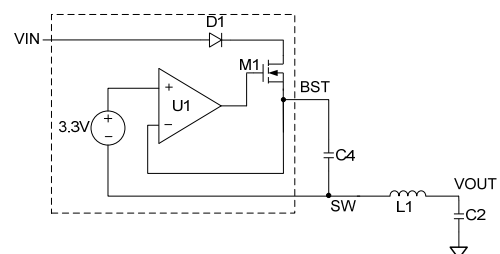
#### Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits can be monitored in register 06 for more information about the IC silicon temperature.

#### Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.4V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated by VIN internally through D1, M1, C4, L1, and C2 (see Figure 6). If V<sub>BST</sub> - V<sub>SW</sub> exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.



**Figure 6: Internal Bootstrap Charging Circuit**

### Start-Up and Shutdown

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V<sub>EAO</sub> and the internal supply rail are then pulled down.

### I<sup>2</sup>C Control and Default Output Voltage

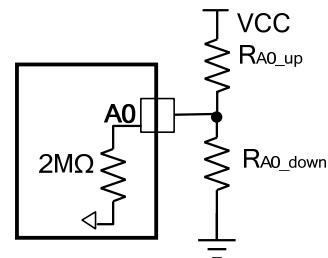
When the MP8869S is enabled, the output voltage is determined by the FB resistors with a programmed soft-start time. After that, the I<sup>2</sup>C bus can communicate with the master. If the chip does not receive an I<sup>2</sup>C communication signal continuously, it can work well through FB and perform behavior similar to a traditional non-I<sup>2</sup>C part. The output voltage is determined by the resistor dividers R1, R2, and FB reference voltage. V<sub>OUT</sub> can be calculated using Equation (3):

$$V_{OUT} = V_{REF} \times \left( \frac{R1 + R2}{R2} \right) \quad (3)$$

Note that the output voltage cannot be set higher than an absolute OVP threshold (typically 6.5V).

### I<sup>2</sup>C Slave Address

To support multiple devices used on the same I<sup>2</sup>C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect A0 to this reference voltage to set a different I<sup>2</sup>C slave address (see Figure 7). The internal circuit changes the I<sup>2</sup>C address accordingly. When the master sends an 8-bit address value, the 7-bit I<sup>2</sup>C address should be followed by 0/1 to indicate a write/read operation. Table 2 shows the recommended I<sup>2</sup>C address selection by the A0 voltage.



**Figure 7: I<sup>2</sup>C Slave Address Selection Set-Up**

**Table 2: Recommended I<sup>2</sup>C Slave Address Selection by A0 Resistor Divider**

A0 Upper Resistor R <sub>A0_up</sub> (kΩ)	A0 Lower Resistor R <sub>A0_down</sub> (kΩ)	I <sup>2</sup> C Slave Address	
		Binary	Hex
No connect	No connect	110 0001	61H
500	300	110 0011	63H
300	500	110 0101	65H
100	No connect	110 0111	67H

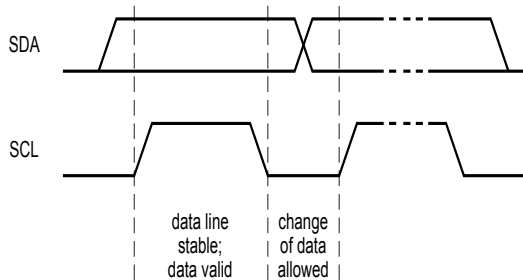
## I<sup>2</sup>C INTERFACE

### I<sup>2</sup>C Serial Interface Description

The I<sup>2</sup>C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP8869S interface is an I<sup>2</sup>C slave. The I<sup>2</sup>C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled by the I<sup>2</sup>C interface instantaneously.

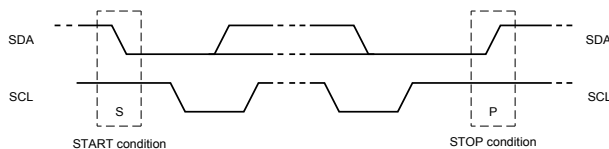
### Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).



**Figure 8: Bit Transfer on the I<sup>2</sup>C Bus**

Start and stop are signaled by the master device, which signifies the beginning and the end of the I<sup>2</sup>C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).



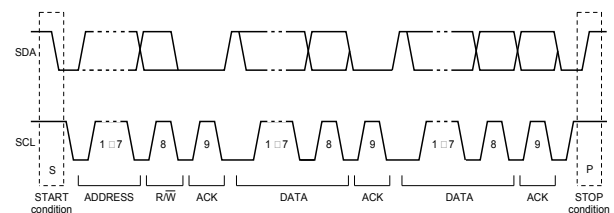
**Figure 9: Start and Stop Conditions**

Start (S) and stop (P) conditions are always generated by the master. The bus is considered to be busy after the start condition and is considered to be free again after a minimum of 4.7μs after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start and repeated start conditions are identical functionally.

### Transfer Data

Every byte put on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains at stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 10. After the start condition, a slave address is sent. This address is seven bits long followed by an eighth bit data direction bit (r/w). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.



**Figure 10: Complete Data Transfer**

The MP8869S requires a start condition, a valid I<sup>2</sup>C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8869S acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the MP8869S. The MP8869S performs an update on the falling edge of the LSB byte.

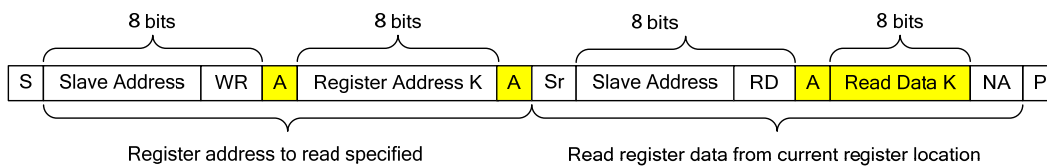


## I<sup>2</sup>C WRITE AND READ SEQUENCE EXAMPLE



<input type="checkbox"/>	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	WR Write = 0
<input checked="" type="checkbox"/>	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition	RD Read = 1

### I<sup>2</sup>C Write Example—Write Single Register



<input type="checkbox"/>	Master to Slave	A = Acknowledge (SDA = LOW)	S = Start Condition	Sr = Repeat Start Condition	WR Write = 0
<input checked="" type="checkbox"/>	Slave to Master	NA = NOT Acknowledge (SDA = HIGH)	P = Stop Condition	RD Read = 1	

### I<sup>2</sup>C Read Example—Read Single Register

## REGISTER DESCRIPTION

### Register Map

The MP8869S contains seven write or read registers. Register 00 is the feedback reference voltage selection register. Register 01 is the first system control register and can be used to set the slew rate, hiccup OCP, etc. Register 02 is the second system control register and can be used to set the switching frequency, current limit, etc.

Register 03 and register 04 are output current and output voltage indicating registers. Register 05 is the IC ID register. Register 06 is the IC status indication register and can be used to check if the IC is in over-current protection, over-temperature protection status, etc. The register map is shown below.

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	r/w	Reserved	Feedback reference						
01	SysCntlreg1	r/w	EN	GO_BIT	Slew rate			Retry OVP	Hiccup OCP	Mode
02	SysCntlreg2	r/w	PG deglitch time		Switching frequency	Soft stop	Current limit adjust			
03	Output current	r	Output current							
04	Output voltage	r	Output voltage							
05	ID1	r	Vendor ID				Die ID			
06	Status	r	Reserved				OC	OTEW	OT	PG

### 1) Reg00 VSEL

Register 00 is the feedback reference voltage selection register. The MP8869S default feedback reference voltage is 0.72V, so the MP8869S's default output voltage is determined by the FB resistor divider and 0.72V default reference after power start-up or EN start-up. The reference voltage is adjustable from 0.6V to 1.108V. Before adjusting the feedback reference voltage, the bit GO\_BIT of the first system control register 01 should be set to 1, and then the reference voltage can be adjusted by the lower seven bits of register 00.

When the feedback reference voltage setting command is finished, GO\_BIT auto-resets to 0 to prevent false operation of the VOUT scaling. GO\_BIT should be set to 1 before adjusting the feedback reference voltage via the I<sup>2</sup>C.

Table 3 shows the feedback reference voltage selection chart from 0.6V to 1.108V via the I<sup>2</sup>C.

NAME	BITS	DEFAULT	DESCRIPTION
Reserved	D[7]	0	Reserved for further use.
Feedback reference	D[6:0]	001 1110	Set the feedback reference voltage from 0.6V to 1.108V (see Table 3). The default value is 0.72V.

**Table 3: Feedback Reference Voltage Selection Chart**

D[6:0]	VREF(V)	D[6:0]	VREF (V)	D[6:0]	VREF (V)	D[6:0]	VREF(V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

## 2) Reg01 SysCntlreg1

Register 01 is the first system control register.

The highest bit, EN, can be used to turn the part on or off when the external EN is high. When the external EN is high, the MP8869S shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. The MP8869S resumes switching by setting the EN bit to 1 again. When the external EN is low, the converter is off, and the I<sup>2</sup>C shuts down.

Set GO\_BIT to 1 to enable the I<sup>2</sup>C's authority to write the feedback reference. When the command is finished, GO\_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

The IC switches to forced PWM mode when GO\_BIT is set to 1 to achieve a smooth output waveform during the output dynamic scaling. After the output scaling is complete, GO\_BIT is set to 0 automatically, and the IC operation mode switches to the original mode set by the Mode bit.

The 3-bit slew rate D[5:3] is used for slew rate selection during the output voltage dynamic scaling. A proper slew rate reduces the inrush current, as well as voltage overshoot and undershoot. Eight different slew rate levels can be selected.

The bit retry OVP defines the protection mode when OVP is triggered. When retry OVP is set to 1, the part enters auto-recovery when OVP is removed. When retry OVP is set to 0, the MP8869S latches off once output OVP occurs, and VIN OVP is triggered until VIN or EN are toggled.

The bit hiccup OCP defines the OCP mode. When hiccup OCP is set to 1, the MP8869S enters hiccup mode when OCP and UVP are both triggered. When hiccup OCP is set to 0, the MP8869S enters latch-off when OCP and UVP are both triggered.

The lowest bit, mode, is used for selecting forced PWM or auto PFM/PWM mode at light load. When mode is set to 0, auto-PFM/PWM mode is enabled at light load. When mode is set to 1, forced PWM mode is enabled at light load.

NAME	BITS	DEFAULT	DESCRIPTION			
EN	D[7]	1	I <sup>2</sup> C controlled turn-on or turn-off of the part. When the external EN is low, the converter is off, and the I <sup>2</sup> C shuts down. When EN is high, the EN bit takes over. The default EN bit is 1.			
GO_BIT	D[6]	0	Switch bit of the I <sup>2</sup> C writing authority for the feedback reference command only. Set GO_BIT = 1 to enable the I <sup>2</sup> C's authority to write the feedback reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false operation of the Vref scaling. Voltage scaling examples: 1) Set GO_BIT = 1. 2) Write register 00: set the feedback reference. 3) Read back the GO_BIT value to see if the output scaling is finished. If GO_BIT = 0, the voltage scaling is done. Otherwise, Vref is still in adjustment. 4) Set GO_BIT = 1 if the output voltage scaling is needed a second time. 5) Write register 00: set the feedback reference.			
Slew rate	D[5:3]	100	The slew rate during the I <sup>2</sup> C-controlled voltage changing is defined by three bits. The output voltage changes linearly from the previous voltage to the new set voltage with a slew rate (see below). This helps reduce inrush current, voltage overshoot, and voltage undershoot greatly.			
			D[5:3]	Slew Rate	D[5:3]	Slew Rate
			000	40mV/μs	100	5mV/μs
			001	30mV/μs	101	2.5mV/μs
			010	20mV/μs	110	1.25mV/μs
011	10mV/μs	111	0.625mV/μs			
Retry OVP	D[2]	1	FB or Vref OVP mode selection bit. 1 means the part auto-recovers when OVP is removed. 0 means the part latches off once output OVP and VIN OVP are both triggered until VIN or EN is power reset.			
Hiccup OCP	D[1]	1	Over-current protection mode selection. 1 means hiccup mode OCP. 0 means latch-off type OCP.			
Mode	D[0]	0	Set mode to 0 to enable PFM mode; set mode to 1 to disable auto-PFM/PWM mode. Default is auto-PFM/PWM mode for light load.			

### 3) Reg02 SysCntlreg2

Register 02 is the second system control register.

The highest two bits of the PG deglitch time D[7:6] defines the PG signal rising and falling edge delay times. When output OVP or UVP is triggered, the PG signal turns low or high after a delay time. There are four levels of PG delay time that can be programmed by the I<sup>2</sup>C in different conditions.

The two switching frequency bits D[5:4] are used for switching frequency selection. The MP8869S supports up to 1.25MHz of switching frequency by setting the two bits to 11. The MP8869S maximum programmable switching frequency is limited by internal minimum on-time (see Table 1).

NAME	BITS	DEFAULT	DESCRIPTION			
PG Deglitch Time	D[7:6]	11	Power good signal rising and falling edges' delay time. When FB or VOUT is out of regulation window, the PG comparator is triggered, but needs a delay time before the PG signal can turn high or low.			
			D[7:6]	PG Deglitch	D[7:6]	PG Deglitch
			00	<1μs	10	12μs
			01	6μs	11	30μs
Switching Frequency	D[5:4]	00	Switching frequency set bit. There is no dedicated frequency oscillator inside the part. The switching frequency is fairly fixed by controlling the T <sub>ON</sub> timer.			
			D[5:4]	Frequency	D[5:4]	Frequency
			00	500kHz	10	1MHz
			01	750kHz	11	1.25MHz
Soft Stop	D[3]	0	This bit defines the VOUT discharge behavior after EN shutdown. 0 means VOUT is not controlled after EN shutdown. 1 means VOUT is discharged linearly to zero with the set soft-stop time.			
Current Limit Adjust	D[2:0]	001	D[2:0]	Valley Current Limit (A)	D[2:0]	Valley Current Limit (A)
			000	16	100	8.5
			001	14	101	7
			010	12	110	6
			011	10	111	5

The bit soft stop defines the output voltage discharge behavior after EN shutdown. When soft stop is set to 0, the output voltage is not controlled after EN shutdown. When soft stop is set to 1, the output voltage is discharged linearly to zero with the set soft-stop time.

The lowest three bits, current limit adjust D[2:0], are used for peak and valley current-limit selection. There are eight levels of current limit that can be selected for different application conditions.

#### 4) Reg03 Output Current

Register 03 is an output current-indicating register. After the MP8869S starts up, the DC output current information can be read through the I<sup>2</sup>C communication.

When the inductor current is in discontinuous conduction mode (DCM), the output current sense is not very accurate. The Mode bit can be set to 1 (PWM mode) for good current sensing accuracy at light load.

When the inductor current enters CCM, the output current sense accuracy is excellent (typical accuracy is 5% when the output current is higher than 2A).

Table 4 shows the output current chart from 0A to 12.75A.

NAME	BITS	DEFAULT	DESCRIPTION
Output Current	D[7:0]	0000 0000	Output current monitor bits. Table 4 shows the output current monitor chart.

**Table 4: Output Current Chart**

D[7:0]	I <sub>out</sub> (A)	D[7:0]	I <sub>out</sub> (A)	D[7:0]	I <sub>out</sub> (A)	D[7:0]	I <sub>out</sub> (A)	D[7:0]	I <sub>out</sub> (A)	D[7:0]	I <sub>out</sub> (A)
0000 0000	0	0010 1011	2.15	0101 0110	4.3	1000 0001	6.45	1010 1100	8.6	1101 0111	10.75
0000 0001	0.05	0010 1100	2.2	0101 0111	4.35	1000 0010	6.5	1010 1101	8.65	1101 1000	10.8
0000 0010	0.1	0010 1101	2.25	0101 1000	4.4	1000 0011	6.55	1010 1110	8.7	1101 1001	10.85
0000 0011	0.15	0010 1110	2.3	0101 1001	4.45	1000 0100	6.6	1010 1111	8.75	1101 1010	10.9
0000 0100	0.2	0010 1111	2.35	0101 1010	4.5	1000 0101	6.65	1011 0000	8.8	1101 1011	10.95
0000 0101	0.25	0011 0000	2.4	0101 1011	4.55	1000 0110	6.7	1011 0001	8.85	1101 1100	11
0000 0110	0.3	0011 0001	2.45	0101 1100	4.6	1000 0111	6.75	1011 0010	8.9	1101 1101	11.05
0000 0111	0.35	0011 0010	2.5	0101 1101	4.65	1000 1000	6.8	1011 0011	8.95	1101 1110	11.1
0000 1000	0.4	0011 0011	2.55	0101 1110	4.7	1000 1001	6.85	1011 0100	9	1101 1111	11.15
0000 1001	0.45	0011 0100	2.6	0101 1111	4.75	1000 1010	6.9	1011 0101	9.05	1110 0000	11.2
0000 1010	0.5	0011 0101	2.65	0110 0000	4.8	1000 1011	6.95	1011 0110	9.1	1110 0001	11.25
0000 1011	0.55	0011 0110	2.7	0110 0001	4.85	1000 1100	7	1011 0111	9.15	1110 0010	11.3
0000 1100	0.6	0011 0111	2.75	0110 0010	4.9	1000 1101	7.05	1011 1000	9.2	1110 0011	11.35
0000 1101	0.65	0011 1000	2.8	0110 0011	4.95	1000 1110	7.1	1011 1001	9.25	1110 0100	11.4
0000 1110	0.7	0011 1001	2.85	0110 0100	5	1000 1111	7.15	1011 1010	9.3	1110 0101	11.45
0000 1111	0.75	0011 1010	2.9	0110 0101	5.05	1001 0000	7.2	1011 1011	9.35	1110 0110	11.5
0001 0000	0.8	0011 1011	2.95	0110 0110	5.1	1001 0001	7.25	1011 1100	9.4	1110 0111	11.55
0001 0001	0.85	0011 1100	3	0110 0111	5.15	1001 0010	7.3	1011 1101	9.45	1110 1000	11.6
0001 0010	0.9	0011 1101	3.05	0110 1000	5.2	1001 0011	7.35	1011 1110	9.5	1110 1001	11.65
0001 0011	0.95	0011 1110	3.1	0110 1001	5.25	1001 0100	7.4	1011 1111	9.55	1110 1010	11.7
0001 0100	1	0011 1111	3.15	0110 1010	5.3	1001 0101	7.45	1100 0000	9.6	1110 1011	11.75
0001 0101	1.05	0100 0000	3.2	0110 1011	5.35	1001 0110	7.5	1100 0001	9.65	1110 1100	11.8
0001 0110	1.1	0100 0001	3.25	0110 1100	5.4	1001 0111	7.55	1100 0010	9.7	1110 1101	11.85
0001 0111	1.15	0100 0010	3.3	0110 1101	5.45	1001 1000	7.6	1100 0011	9.75	1110 1110	11.9
0001 1000	1.2	0100 0011	3.35	0110 1110	5.5	1001 1001	7.65	1100 0100	9.8	1110 1111	11.95
0001 1001	1.25	0100 0100	3.4	0110 1111	5.55	1001 1010	7.7	1100 0101	9.85	1111 0000	12
0001 1010	1.3	0100 0101	3.45	0111 0000	5.6	1001 1011	7.75	1100 0110	9.9	1111 0001	12.05
0001 1011	1.35	0100 0110	3.5	0111 0001	5.65	1001 1100	7.8	1100 0111	9.95	1111 0010	12.1
0001 1100	1.4	0100 0111	3.55	0111 0010	5.7	1001 1101	7.85	1100 1000	10	1111 0011	12.15
0001 1101	1.45	0100 1000	3.6	0111 0011	5.75	1001 1110	7.9	1100 1001	10.05	1111 0100	12.2
0001 1110	1.5	0100 1001	3.65	0111 0100	5.8	1001 1111	7.95	1100 1010	10.1	1111 0101	12.25
0001 1111	1.55	0100 1010	3.7	0111 0101	5.85	1010 0000	8	1100 1011	10.15	1111 0110	12.3
0010 0000	1.6	0100 1011	3.75	0111 0110	5.9	1010 0001	8.05	1100 1100	10.2	1111 0111	12.35
0010 0001	1.65	0100 1100	3.8	0111 0111	5.95	1010 0010	8.1	1100 1101	10.25	1111 1000	12.4
0010 0010	1.7	0100 1101	3.85	0111 1000	6	1010 0011	8.15	1100 1110	10.3	1111 1001	12.45
0010 0011	1.75	0100 1110	3.9	0111 1001	6.05	1010 0100	8.2	1100 1111	10.35	1111 1010	12.5
0010 0100	1.8	0100 1111	3.95	0111 1010	6.1	1010 0101	8.25	1101 0000	10.4	1111 1011	12.55
0010 0101	1.85	0101 0000	4	0111 1011	6.15	1010 0110	8.3	1101 0001	10.45	1111 1100	12.6
0010 0110	1.9	0101 0001	4.05	0111 1100	6.2	1010 0111	8.35	1101 0010	10.5	1111 1101	12.65
0010 0111	1.95	0101 0010	4.1	0111 1101	6.25	1010 1000	8.4	1101 0011	10.55	1111 1110	12.7
0010 1000	2	0101 0011	4.15	0111 1110	6.3	1010 1001	8.45	1101 0100	10.6	1111 1111	12.75
0010 1001	2.05	0101 0100	4.2	0111 1111	6.35	1010 1010	8.5	1101 0101	10.65		
0010 1010	2.1	0101 0101	4.25	1000 0000	6.4	1010 1011	8.55	1101 0110	10.7		

### 5) Reg04 Output Voltage

Register 04 is an output voltage-indicating register. After part starts up, the output voltage can be read through the I<sup>2</sup>C communication. In light load, if the mode bit is set to 0, the MP8869S works in PFM mode. At extremely light-load or no-load condition, the ADC only works when the first pulse comes, and then the MP8869S refreshes the output voltage register before it enters sleep mode.

At this moment, the sensed output voltage is the maximum value, not the average output voltage. So the I<sup>2</sup>C readback voltage is slightly higher than the set point. When taking some load to the part, it will get higher sense accuracy. The mode bit can be set to 1 (PWM mode) for good voltage sensing accuracy at light load. Table 5 shows the output voltage chart from 0.5V to 5.643V.

NAME	BITS	DEFAULT	DESCRIPTION
Output voltage	D[7:0]	0000 0000	Output voltage monitor bits. Table 5 shows the output voltage monitor chart.

**Table 5: Output Voltage Chart**

D[7:0]	V <sub>OUT</sub> (V)	D[7:0]	V <sub>OUT</sub> (V)	D[7:0]	V <sub>OUT</sub> (V)	D[7:0]	V <sub>OUT</sub> (V)	D[7:0]	V <sub>OUT</sub> (V)	D[7:0]	V <sub>OUT</sub> (V)
0000 0000	0.500	0010 1011	1.367	0101 0110	2.235	1000 0001	3.102	1010 1100	3.969	1101 0111	4.837
0000 0001	0.520	0010 1100	1.387	0101 0111	2.255	1000 0010	3.122	1010 1101	3.989	1101 1000	4.857
0000 0010	0.540	0010 1101	1.408	0101 1000	2.275	1000 0011	3.142	1010 1110	4.010	1101 1001	4.877
0000 0011	0.561	0010 1110	1.428	0101 1001	2.295	1000 0100	3.162	1010 1111	4.030	1101 1010	4.897
0000 0100	0.581	0010 1111	1.448	0101 1010	2.315	1000 0101	3.183	1011 0000	4.050	1101 1011	4.917
0000 0101	0.601	0011 0000	1.468	0101 1011	2.335	1000 0110	3.203	1011 0001	4.070	1101 1100	4.937
0000 0110	0.621	0011 0001	1.488	0101 1100	2.356	1000 0111	3.223	1011 0010	4.090	1101 1101	4.958
0000 0111	0.641	0011 0010	1.509	0101 1101	2.376	1000 1000	3.243	1011 0011	4.110	1101 1110	4.978
0000 1000	0.661	0011 0011	1.529	0101 1110	2.396	1000 1001	3.263	1011 0100	4.131	1101 1111	4.998
0000 1001	0.682	0011 0100	1.549	0101 1111	2.416	1000 1010	3.283	1011 0101	4.151	1110 0000	5.018
0000 1010	0.702	0011 0101	1.569	0110 0000	2.436	1000 1011	3.304	1011 0110	4.171	1110 0001	5.038
0000 1011	0.722	0011 0110	1.589	0110 0001	2.456	1000 1100	3.324	1011 0111	4.191	1110 0010	5.058
0000 1100	0.742	0011 0111	1.609	0110 0010	2.477	1000 1101	3.344	1011 1000	4.211	1110 0011	5.079
0000 1101	0.762	0011 1000	1.630	0110 0011	2.497	1000 1110	3.364	1011 1001	4.231	1110 0100	5.099
0000 1110	0.782	0011 1001	1.650	0110 0100	2.517	1000 1111	3.384	1011 1010	4.252	1110 0101	5.119
0000 1111	0.803	0011 1010	1.670	0110 0101	2.537	1001 0000	3.404	1011 1011	4.272	1110 0110	5.139
0001 0000	0.823	0011 1011	1.690	0110 0110	2.557	1001 0001	3.425	1011 1100	4.292	1110 0111	5.159
0001 0001	0.843	0011 1100	1.710	0110 0111	2.578	1001 0010	3.445	1011 1101	4.312	1110 1000	5.179
0001 0010	0.863	0011 1101	1.730	0110 1000	2.598	1001 0011	3.465	1011 1110	4.332	1110 1001	5.200
0001 0011	0.883	0011 1110	1.751	0110 1001	2.618	1001 0100	3.485	1011 1111	4.352	1110 1010	5.220
0001 0100	0.903	0011 1111	1.771	0110 1010	2.638	1001 0101	3.505	1100 0000	4.373	1110 1011	5.240
0001 0101	0.924	0100 0000	1.791	0110 1011	2.658	1001 0110	3.526	1100 0001	4.393	1110 1100	5.260
0001 0110	0.944	0100 0001	1.811	0110 1100	2.678	1001 0111	3.546	1100 0010	4.413	1110 1101	5.280
0001 0111	0.964	0100 0010	1.831	0110 1101	2.699	1001 1000	3.566	1100 0011	4.433	1110 1110	5.300
0001 1000	0.984	0100 0011	1.851	0110 1110	2.719	1001 1001	3.586	1100 0100	4.453	1110 1111	5.321
0001 1001	1.004	0100 0100	1.872	0110 1111	2.739	1001 1010	3.606	1100 0101	4.473	1111 0000	5.341
0001 1010	1.024	0100 0101	1.892	0111 0000	2.759	1001 1011	3.626	1100 0110	4.494	1111 0001	5.361
0001 1011	1.045	0100 0110	1.912	0111 0001	2.779	1001 1100	3.647	1100 0111	4.514	1111 0010	5.381
0001 1100	1.065	0100 0111	1.932	0111 0010	2.799	1001 1101	3.667	1100 1000	4.534	1111 0011	5.401
0001 1101	1.085	0100 1000	1.952	0111 0011	2.820	1001 1110	3.687	1100 1001	4.554	1111 0100	5.421
0001 1110	1.105	0100 1001	1.972	0111 0100	2.840	1001 1111	3.707	1100 1010	4.574	1111 0101	5.442
0001 1111	1.125	0100 1010	1.993	0111 0101	2.860	1010 0000	3.727	1100 1011	4.595	1111 0110	5.462
0010 0000	1.145	0100 1011	2.013	0111 0110	2.880	1010 0001	3.747	1100 1100	4.615	1111 0111	5.482
0010 0001	1.166	0100 1100	2.033	0111 0111	2.900	1010 0010	3.768	1100 1101	4.635	1111 1000	5.502
0010 0010	1.186	0100 1101	2.053	0111 1000	2.920	1010 0011	3.788	1100 1110	4.655	1111 1001	5.522
0010 0011	1.206	0100 1110	2.073	0111 1001	2.941	1010 0100	3.808	1100 1111	4.675	1111 1010	5.543
0010 0100	1.226	0100 1111	2.093	0111 1010	2.961	1010 0101	3.828	1101 0000	4.695	1111 1011	5.563
0010 0101	1.246	0101 0000	2.114	0111 1011	2.981	1010 0110	3.848	1101 0001	4.716	1111 1100	5.583
0010 0110	1.266	0101 0001	2.134	0111 1100	3.001	1010 0111	3.868	1101 0010	4.736	1111 1101	5.603
0010 0111	1.287	0101 0010	2.154	0111 1101	3.021	1010 1000	3.889	1101 0011	4.756	1111 1110	5.623
0010 1000	1.307	0101 0011	2.174	0111 1110	3.041	1010 1001	3.909	1101 0100	4.776	1111 1111	5.643
0010 1001	1.327	0101 0100	2.194	0111 1111	3.062	1010 1010	3.929	1101 0101	4.796		
0010 1010	1.347	0101 0101	2.214	1000 0000	3.082	1010 1011	3.949	1101 0110	4.816		

**5) Reg06 ID1**

Register 05 is the IC information indicating register. The highest four bits, vendor ID D[7:4], are set to 1000 internally.

The lowest four bits, IC Revision ID D[3:0], indicates IC revision information.

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000.
IC Revision ID	D[3:0]	IC revision.

**7) Reg06 Status**

Register 06 is a fault condition indicating register. The highest four bits, D[7:4], are reserved for future use.

The bit OTEW is the die temperature early warning indication. When the bit is set to 1, the IC die temperature is higher than 120°C.

The bit OC is the output over-current indication. When the bit is set to 1, the IC is in hiccup mode or OC latch-off.

The bit PG is output power good indication. When the bit is set to 1, the output power is normal.

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	Reserved for future use.
OC	D[3]	Output over-current indication. When this bit is high, the IC is in hiccup mode or trips OC latch off.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120°C.
OT	D[1]	Over-temperature indication. When the bit is high the IC is in thermal shutdown
PG	D[0]	Output power good indication. When the bit is high the VOUT power is normal. This means VOUT is higher than 95% and lower than 115% of the designed regulation voltage. PG compares FB/VOUT with REF.

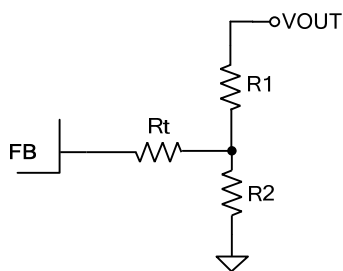


## APPLICATION INFORMATION

### Setting the Output Voltage in a FB Control Loop

The MP8869S can be controlled by the FB loop. The output voltage can be set by the external resistor dividers. The FB loop reference voltage is a default value (0.72V) and can be programmed by the I<sup>2</sup>C. The MP8869S's output voltage must be below the absolute OVP threshold (typically 6.5V).

The FB loop network is shown in Figure 11.



**Figure 11: FB Loop Network**

Calculate R1 and R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (4)$$

Table 6 lists the recommended feedback resistors value for common output voltages.

**Table 6: Resistor Selection for Common Output Voltages<sup>(8)</sup>**

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)	Rt(kΩ)	L(μH)
1.0	80.6	205	10	1.5
1.2	80.6	121	10	1.5
1.5	80.6	74.4	10	1.5
1.8	80.6	53.6	10	1.5
2.5	80.6	32.4	10	2.2
3.3	80.6	22.6	10	2.2
5	80.6	13.7	10	3.3

**NOTE:**

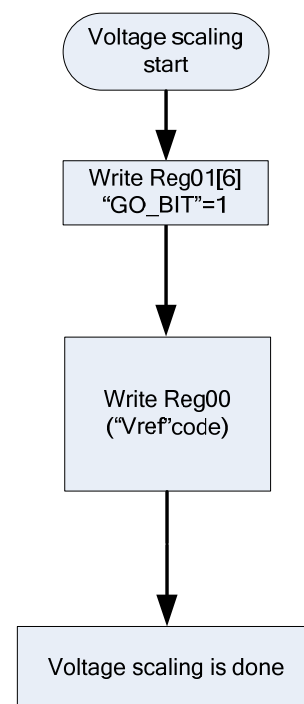
8) The recommended parameters are based on a 12V input voltage and 22μFx4 output capacitor. Different input voltage and output capacitor values may affect the selection of R1 and R2. For other components' parameters, please refer to the Typical Application Circuits on page 37 to page 39.

### Output Voltage Dynamic Scale

The output voltage dynamic scaling can be done only via the I<sup>2</sup>C. Refer to Figure 11 and follow the steps below.

- 1) Write GO\_BIT (Reg01[6]) to 1.
- 2) Write Reg00 to set the reference voltage by feedback reference (Reg00 [6:0]) simultaneously. When the command is finished, GO\_BIT auto-resets to 0 to prevent false operation of the VOUT scaling.

Repeat the above two steps if the output voltage must be changed to a different voltage.



**Figure 12: Output Voltage Dynamic Scale Flow Chart**

### Selecting the Inductor

Use a 0.47μH to 5μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance less than 5mΩ. For most designs, the inductance value can be derived from Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI<sub>L</sub> is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , shown in Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple caused by the capacitance can be estimated with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

### Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (10)$$

Where  $L_1$  is the inductor value, and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8869S can be optimized for a wide range of capacitance and ESR values.

### Selecting the Bootstrap Capacitor and Resistor

The bootstrap capacitor powers the floating power MOSFET driver. It is recommended to use 0.1µF ceramic capacitor.

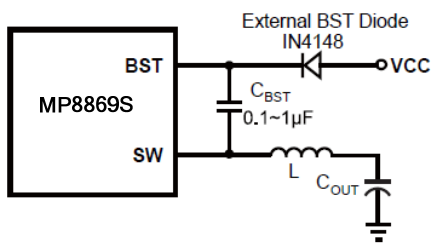
The value of Bootstrap resistor generally is recommended to be in the range from 0 to 10Ω. BST resistor determines the turning on speed of the high side MOSFET. For the design where the VCC decoupling capacitor layout could not be optimized and follow the recommended layout, the 10Ω BST resistor is recommended to be used to in series with the BST capacitor.

### External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- VOUT is 5V or 3.3V
- Duty cycle is high:  $D > 50\%$

In these cases, add an external BST diode from VCC to BST (see Figure 13).



**Figure 13: Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

### Connect VCC to VIN at a Low Input Voltage

VCC can be connected to VIN directly when VIN is lower than 3.5V. This helps improve the MP8869S's low input voltage efficiency performance. To use this application set-up, the VIN spike voltage must be limited below 4V, otherwise VCC may be damaged.

### PCB Layout Guidelines <sup>(9)</sup>

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 14 and follow the guidelines below.

1. Place the high-current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least two layers for the VIN and PGND trace to achieve better thermal performance.
4. Add several vias close to the VIN and PGND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node SW short and away from the feedback network.
10. Keep the BST voltage path (BST, C<sub>3</sub>, and SW) as short as possible.

**NOTE:**

9) The recommended layout is based on the Typical Application circuit on page 37 to page 39.

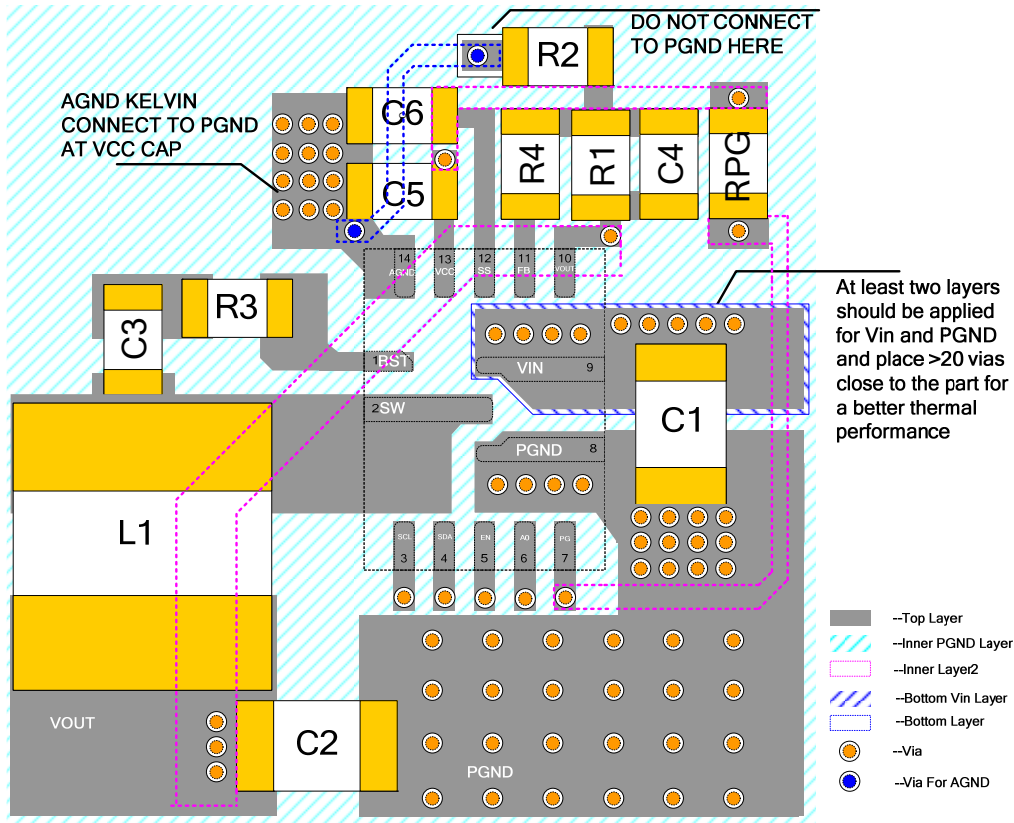


Figure 14: Recommended Layout

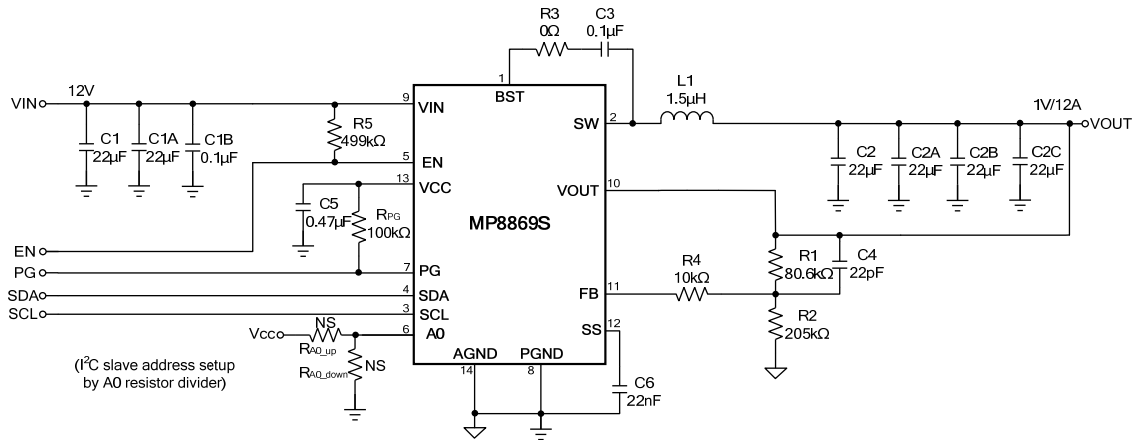
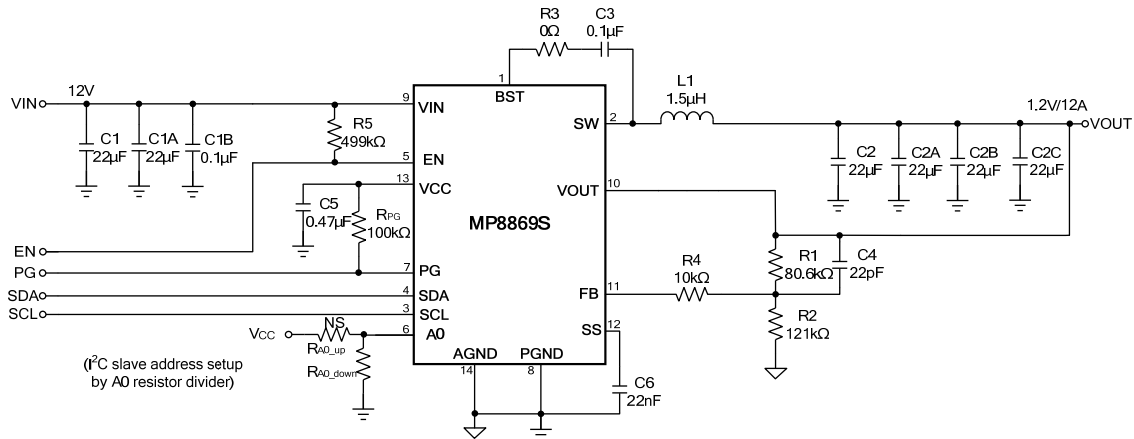
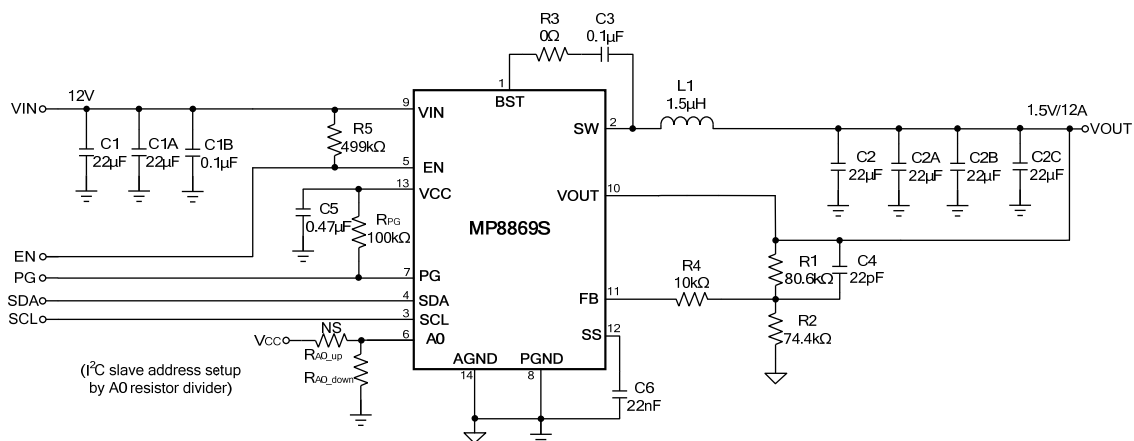
**Design Example**

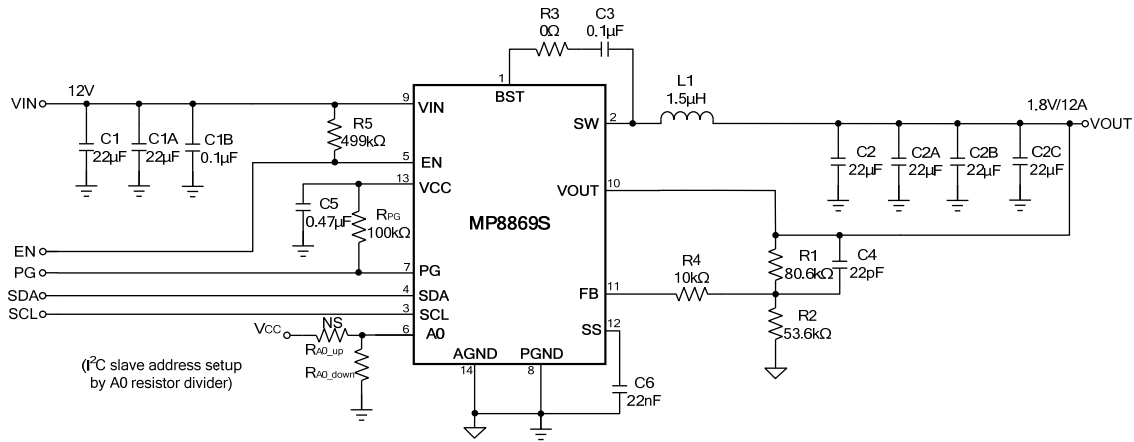
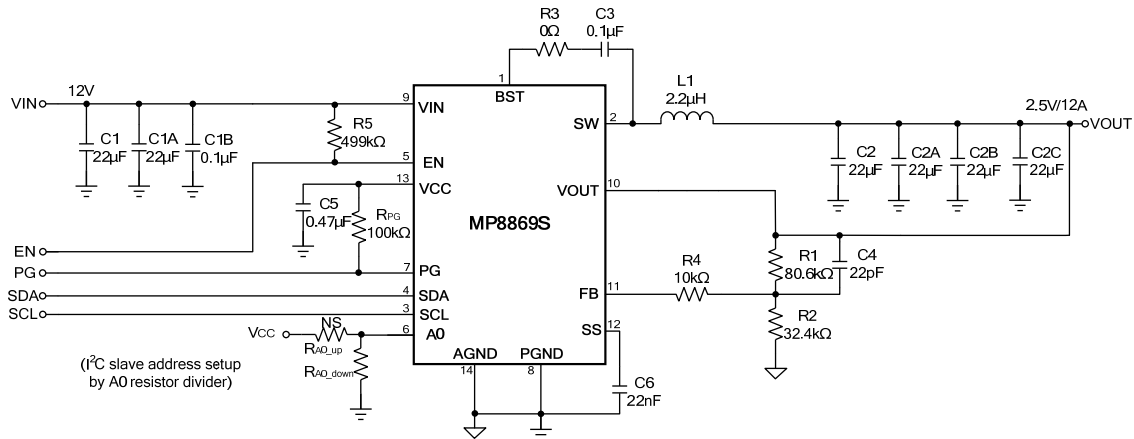
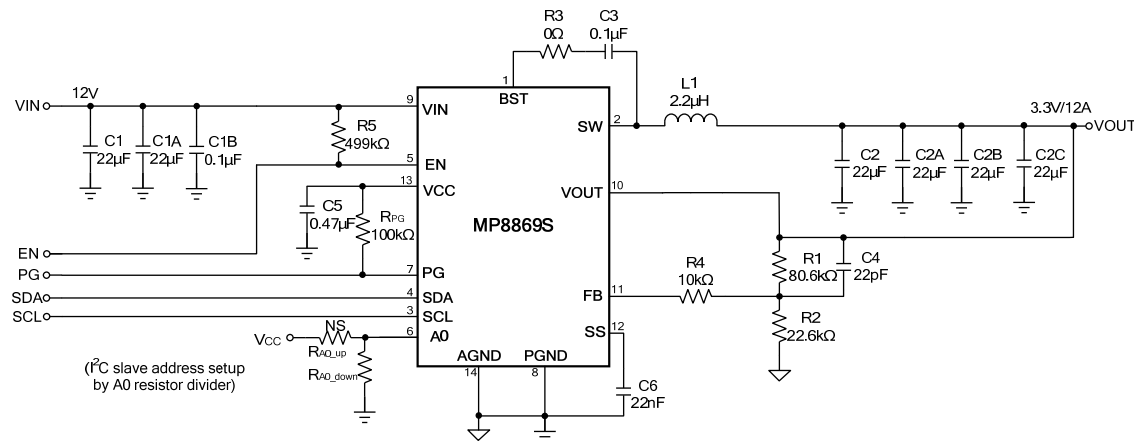
Table 7 is a design example following the application guidelines for the specifications below.

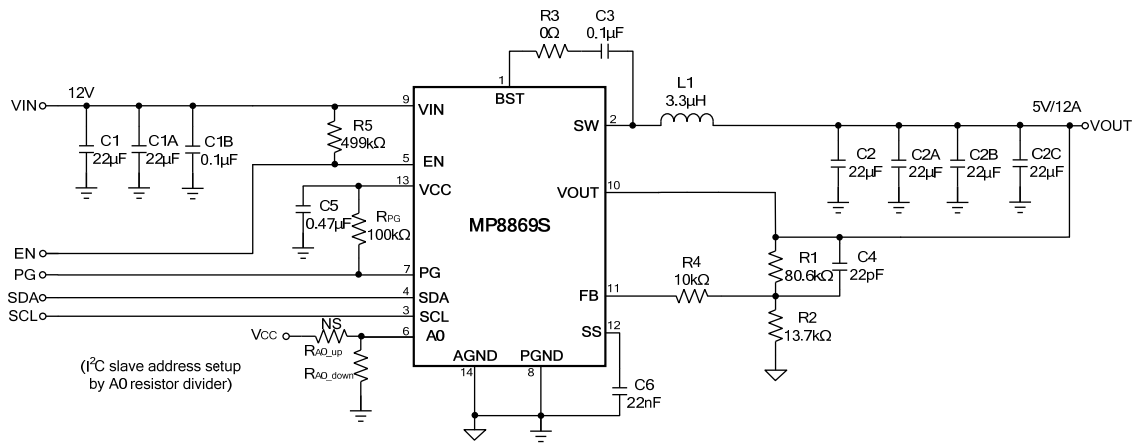
**Table 7: Design Example**

$V_{IN}$	5V
$V_{OUT}$	1.8V
$I_o$	12A

The detailed application schematics are shown in Figure 15 through Figure 21. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

**TYPICAL APPLICATION CIRCUITS (10)**

**Figure 15: VIN = 12V, VOUT = 1V, IOUT = 12A**

**Figure 16: VIN = 12V, VOUT = 1.2V, IOUT = 12A**

**Figure 17: VIN = 12V, VOUT = 1.5V, IOUT = 12A**

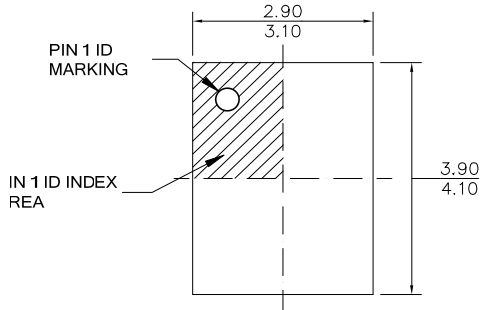
**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 18: VIN = 12V, VOUT = 1.8V, IOUT = 12A**

**Figure 19: VIN = 12V, VOUT = 2.5V, IOUT = 12A**

**Figure 20: VIN = 12V, VOUT = 3.3V, IOUT = 12A**

**TYPICAL APPLICATION CIRCUITS (continued)**

**Figure 21: VIN = 12V, VOUT = 5V, IOUT = 12A**
**NOTE:**

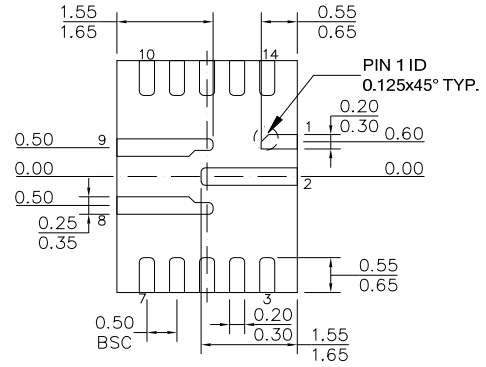
- 10) All circuits are based on a 0.72V default reference voltage. The MP8869S's output voltage can be adjusted by the feedback reference voltage and external resistor dividers. However, the MP8869S's output voltage must be set lower than the absolute over-voltage protection threshold (typically 6.5V).

PACKAGE INFORMATION

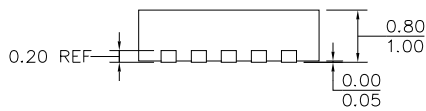
QFN-14 (3mmx4mm)



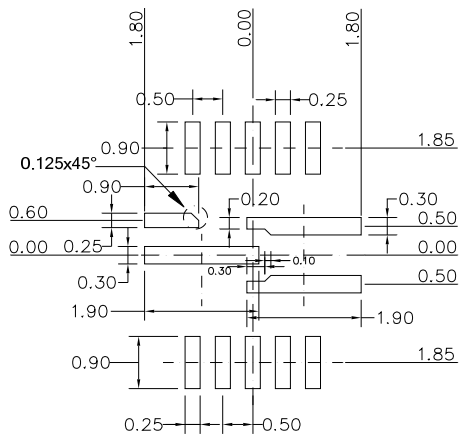
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



## Revision History

Revision #	Revision Date	Description	Pages Updated
1.05	08/04/2020	Update the page4 for EC table, add 2.3 to $INUV_{V_{th\_f}}$ min.	Page 4

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