SLUS485A – JULY 2001 – REVISED NOVEMBER 2001

DUAL COLD CATHODE FLUORESCENT LAMP CONTROLLER

FEATURES

- **Synchronous or Nonsynchronous Operation**
- **Dual Output and Control Stages**
- **BiCMOS Technology**
- **Accurate Current Control with 2-mA Typical Supply Current**
- **Analog or Digital Low-Frequency Dimming Capability**
- **Open Lamp Protection with Voltage Clamp**
- **4.5-V to 25-V Operation**
- **PWM Frequencies Synchronized to External Resonant Tanks**
- **TSSOP-16 (PW) Package**

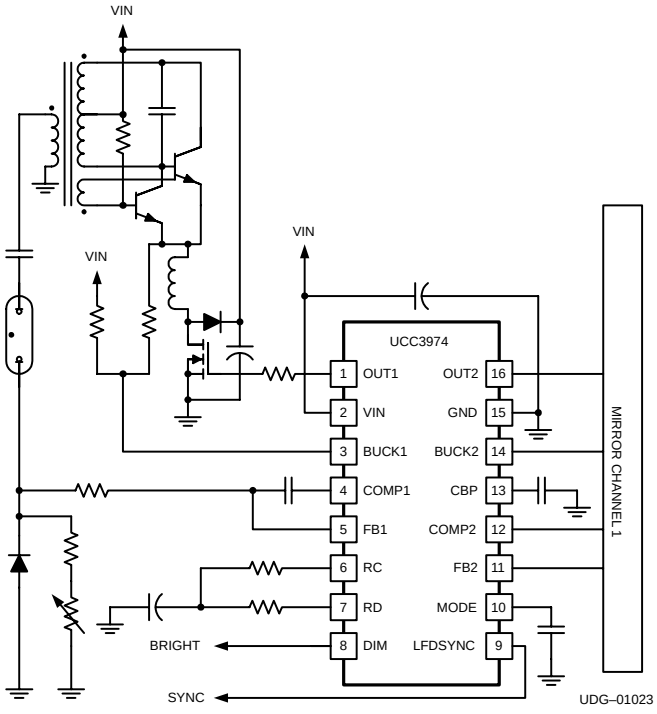
APPLICATIONS

- **Portable PCs**
- **Desktop LCD Monitors**
- **Internet Appliances**

DESCRIPTION

Design goals for a cold cathode fluorescent lamp (CCFL) converter used for a liquid crystal display (LCD) monitor application include small size, high efficiency, and low cost. The UCC2974/UCC3974 CCFL controllers provide the necessary circuit blocks to implement a highly efficient LCD monitor backlight supply in a small 16-pin TSSOP package. The device features two control stages for operating independent resonant tanks for multi-lamp designs. The BiCMOS controller typically consumes less than 2-mA of operating current, improving overall system efficiency. External parts count is minimized and system cost is reduced by integrating such features as dual PWM driver stages, open lamp protection, overvoltage clamp, and synchronization circuitry between the buck and push-pull stages. The device operates in both analog and low-frequency dimming modes.

TYPICAL APPLICATION



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, VBAT . . . . . 27 V
Input voltage range, BUCK . . . . . –5 V to VBAT
MODE . . . . . –0.3 V to 4.3 V
Mode maximum forced current . . . . . 300 µA
Operating virtual junction temperature range, T_J . . . . . –55°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Unless otherwise specified, all voltages are with respect to GND.

AVAILABLE OPTIONS

T_J	PACKAGE
	PW§ (SSOP)
–40°C to 85°C	UCC2974PW
0°C to 70°C	UCC3974PW

§ This package is available taped and reeled. To order this packaging option, add an R suffix to the part number. (e.g. UCC2974PWR)

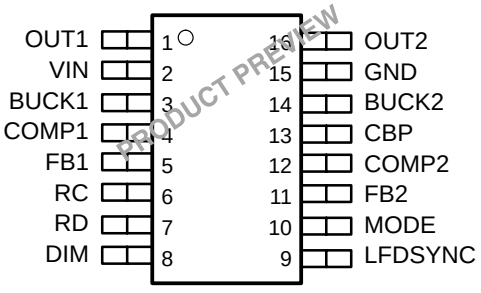
DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
16-pin PW with solder	775 mW	6.2 mW/°C	495 mW	402 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{IN}	4.5		25	V
Mode voltage	0		4.3	V
DIM voltage	0		3.5	V
LFDSYNC amplitude	0		4.5	V

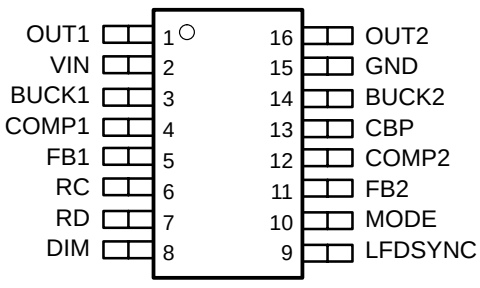
UCC2974
PW PACKAGE
(TOP VIEW)





ACTUAL SIZE
(5,10mm x 6,60mm)

UCC3974
PW PACKAGE
(TOP VIEW)



electrical characteristics over recommended operating virtual junction temperature range, T_A = 0°C to 70°C for the UCC3974, T_A = –40°C to 85°C, for the UCC2974, $T_A = T_J$. $V_{IN} = V_{BUCK}$ = 12 V, MODE = OPEN (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IN}	V_{IN} supply current	12 V ≤ V_{IN} ≤ 25 V			1.7	3	mA
		V_{IN} = 12 V,	MODE < 0.425 V		300	500	µA
	UVLO threshold voltage	LOW to HIGH		3.6	4	4.4	V
	UVLO hysteresis voltage			35	120	200	mV

output

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level output voltage	12 V ≤ V_{IN} ≤ 25 V		8	10.5	13	V
Low-level output voltage	MODE = 0.5 V,	I_{SINK} = 1 mA		50	200	mV
Rise time	C_L = 1 nF			170	350	ns
Fall time	C_L = 1 nF			140	300	

oscillator

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Free-running oscillator frequency	12 V ≤ V_{IN} ≤ 25 V,	BUCK = V_{IN}	30	45	60	kHz
Free-running synchronizable oscillator frequency	12 V ≤ V_{IN} ≤ 25 V,	BUCK = V_{IN}–3	62		220	
Maximum duty cycle	FB = 1 V		100%			
Minimum duty cycle	FB = 2 V				0%	
BUCK input bias current	BUCK = VIN = 12 V			3	10	µA
	BUCK = VIN = 25 V			3	10	
Zero detect threshold voltage	Measured at BUCK with respect to V_{IN}, 12 V ≤ V_{IN} ≤ 25 V		–2.4	–1.7	–1.1	V

error amplifier

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage	COMP = FB,	0°C ≤ T_A ≤ 70°C	1.465	1.5	1.535	V
	COMP = FB,	–40°C ≤ T_A ≤ 85°C	1.455	1.5	1.545	
Line regulation voltage	12 V ≤ V_{IN} ≤ 25 V			1	5	mV
Input bias current				100	250	nA
Open loop gain			60	80		dB
High-level output voltage	FB = 1 V,	I_{SOURCE} = 50 µA	3.5	3.7	4.2	V
Low-level output voltage	FB = 2 V,	I_{SINK} = 50 µA		0.15	0.35	
Output source current	FB = 1 V,	COMP = 2 V		–1.2	–0.3	mA
Output sink current	FB = 2 V,	COMP = 2 V	45	90		µA
Unity gain bandwidth	T_J = 25C,	See Note 1	2	5		MHz

NOTE 1: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, T_A = 0°C to 70°C for the UCC3974, T_A = –40°C to 85°C, for the UCC2974, $T_A = T_J$. $V_{IN} = V_{BUCK}$ = 12 V, MODE = OPEN (unless otherwise noted)

mode select

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Enable threshold voltage		0.425	0.500	0.575	V
Output enable threshold voltage		0.85	1.00	1.15	
Open lamp detect enable voltage threshold		2.75	3	3.25	
Low-frequency dimming (LFD) voltage threshold		3.8	4.0	4.1	
MODE output current	MODE = 0.5 V	3.3	5.0	6.8	µA
MODE clamp voltage	MODE = OPEN	4.0	4.2	4.4	V

low-frequency dimming

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle	R_C = 400 kΩ, R_D = 20 kΩ, C_{LFD} = 10 nF, DIM < 0.5 V	6%	10%	12%	
Maximum duty cycle	R_C = 400 kΩ, R_D = 20 kΩ, C_{LFD} = 10 nF, DIM > 3.1 V	100%			
Free-running oscillator frequency	R_C = 400 kΩ, R_D = 20 kΩ, C_{LFD} = 10 nF		200		Hz
Synchronized oscillator frequency	R_C = 400 kΩ, R_D = 20 kΩ, C_{LFD} = 10 nF, $F_{LFDSYNC}$ = 400 Hz at $V_{LFDSYNC}$ = 2.25 V		400		

open lamp

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Open lamp detect threshold voltage	V_{IN} = 12 V, Measured at VBUCK wrt V_{IN}	–8.5	–7.8	–7.0	V
	V_{IN} = 25 V, Measured at VBUCK wrt V_{IN}	–8.6	–7.8	–6.9	
Voltage clamp detect threshold voltage	Measured at VBUCK	–9.6	–8.75	–8.0	

NOTES: 1: Ensured by design, not production tested.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BUCK1	3	I	Voltage sense for the resonant tank.
BUCK2	14	I	
CBP	13	O	Internally generated low-voltage supply. Bypass to GND with 0.1-μF bypass coordinator.
COMP1	4	O	Outputs of the error amplifiers for the two channels.
COMP2	12	O	
DIM	8	I	Reference signal applied to the LFD PWM that determines the LFD duty cycle.
FB1	5	I	Inverting inputs of the error amplifiers.
FB2	11	I	
GND	15	–	Power supply return.
LFDSYNC	9	I	2.5-V logic-compatible pin used to synchronize the LFD oscillator.
MODE	10	I	Start-up timing control.
OUT1	1	O	FET drive outputs for the two channels. The pin is driven between GND and internal voltage (typically 12 V).
OUT2	16	O	
RC	6	O	Connection for the low-frequency dimming (LFD) charge resistor. The other terminal of the resistor is connected to the LFD capacitor, C_{LFD}.
RD	7	O	Connection for low-frequency dimming (LFD) discharge resistor, R_D. The other terminal of the resistor is connected to the LFD capacitor, C_{LFD}. LFD frequency us user programmable by varying R_C, R_D and C_{FLD}.
VIN	2	I	Power supply input. 4.5 V to 25 V.

detailed pin descriptions

DIM – The range is approximately 0.5 V to 3 V for the programmed minimum 100% duty cycle. If the LFDSYNC pin is pulled above 2.25 V before MODE crosses the LFD enable threshold and is held high, the function of DIM changes from an analog voltage, which determines the LFD duty cycle, to a digital signal (2.5-V logic compatible) which turns the lamps on or off directly. This allows users to implement their own LFD solution and easily interface it to the UCC3974. Pulling this pin above 3.0 V (weak internal pull-up device is provided) causes the LFD section of the device to provide 100% LFD duty cycle.

LFDSYNC – This 2.5-V logic compatible pin is used to synchronize the LFD oscillator. A positive pulse restarts the LFD ramp. Weak internal pull-down device provided. This pin must be set high when digital LFD mode control is required.

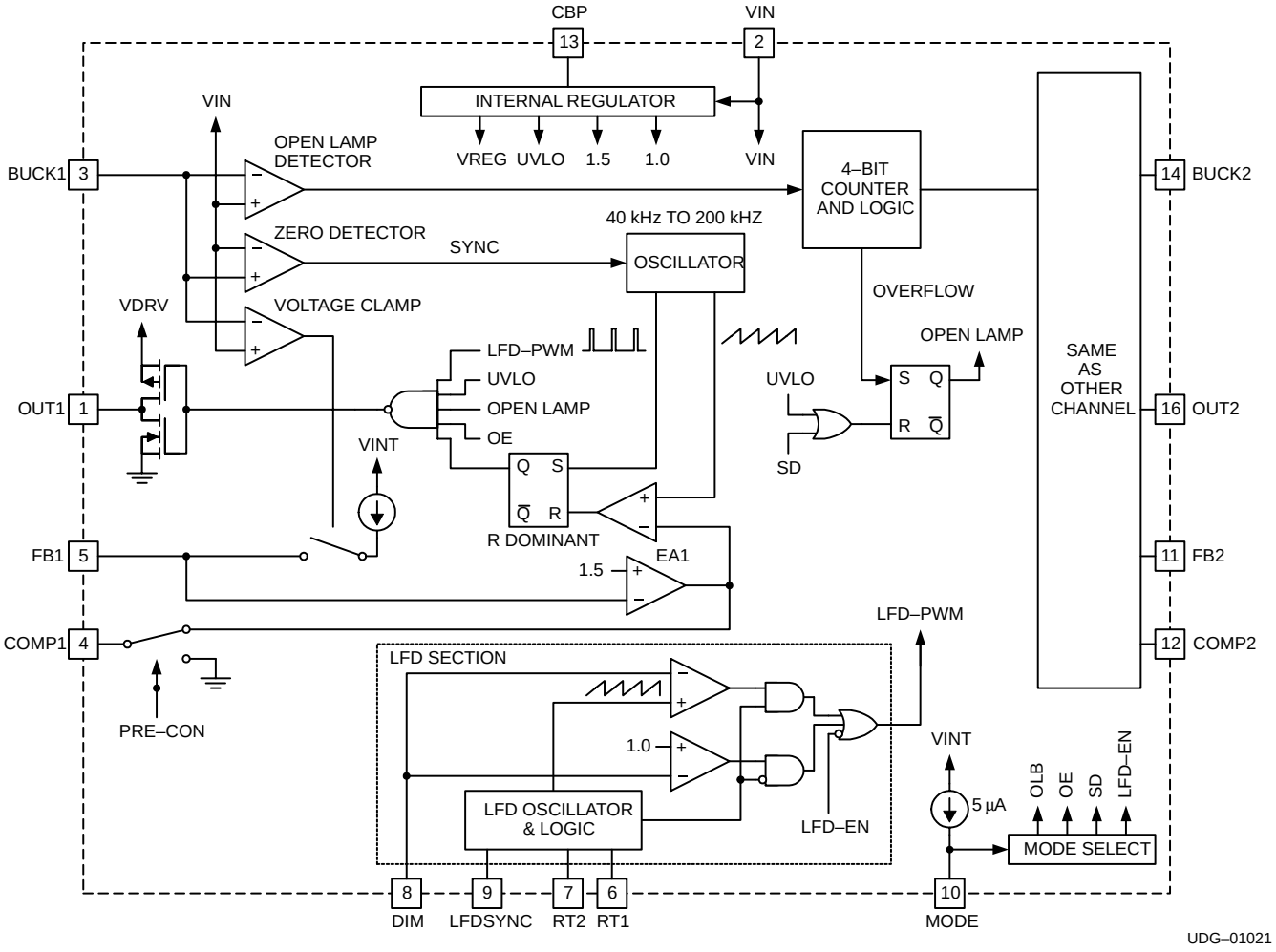
MODE – This pin controls the start-up timing for the device. A capacitor is connected from this pin to ground and has a constant current forced into it. The pin voltage controls the state of the device. When the system has a power cycle, the pin is discharged to ground..

MODE PIN VOLTAGE	FUNCTION
V_{MODE} < 0.5 V	All circuitry is disabled.
V_{MODE} > 0.5 V	Internal circuitry is enabled.
V_{MODE} > 1.0 V	Output driver is enabled.
V_{MODE} > 3.0 V	Enable open lamp detection circuitry.
V_{MODE} > 4.0 V	Enable low-frequency dimming (LFD).

BUCK1/BUCK2 – These pins are used to sense the voltage on the resonant tank. This voltage is used for synchronizing the internal high-frequency oscillators with the resonant tanks. This voltage is also used to detect an open lamp condition when MODE is above 3 V.

APPLICATION INFORMATION

functional block diagram



general description

The UCC3974 extends the capabilities of the UCC3972 and UCC3973 backlight controllers. The basic functionality is the same as that for the UCC3972; a buck controlled current source feeding a royer oscillator CCFL circuit. As such the application information for the UCC3972 that pertains to the royer oscillator, buck controller and CCFL circuit in general apply to the UCC3974. Also, this device implements a voltage clamping scheme, similar to that of the UCC3973, using an internal current source to bias up the FB pin and thereby limiting the current available to the royer stage. This limits the voltage to which the secondary side of the transformer is exposed.

The extensions this device provides are two separately controlled channels to be used with two separate royer stages, and integrated low-frequency dimming (LFD) control .

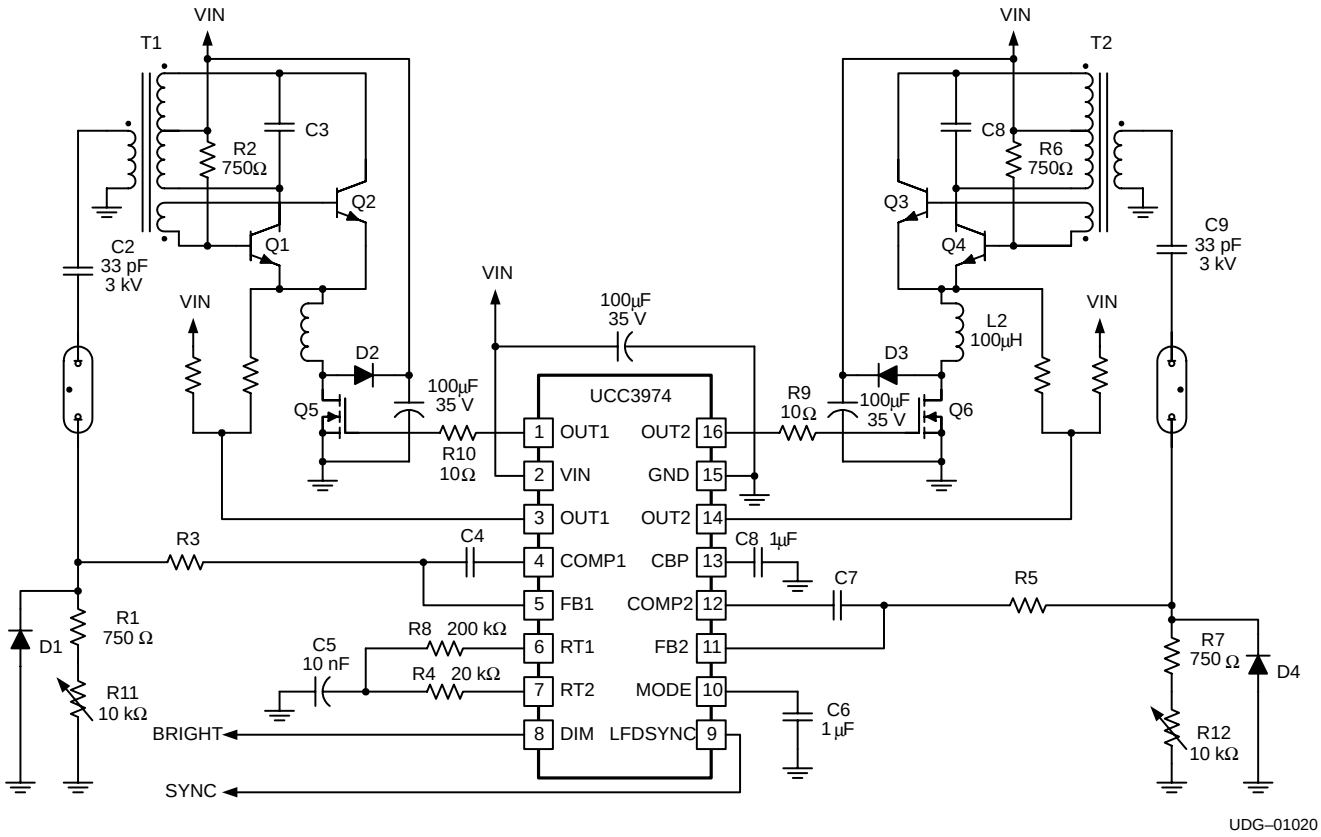


Figure 1. Typical Dual-Channel Application

low-frequency dimming (LFD)

The low-frequency dimming section of the device is implemented as either a low frequency pulse width modulator (PWM) or as a direct digital input. In either case, the DIM pin is the controlling input. The type of DIM input is determined at startup. As the MODE pin transitions through the LFD_ENABLE threshold, the LFDSYNC pin is observed. When this pin is high, the DIM pin is a 2.5-V compatible logic input. When the DIM pin is high, the output is enabled. When it is low the output is disabled. The user is required to provide the correct frequency and duty ratio to the DIM pin in this mode. To change the mode of operation without power cycling the device, the MODE pin must be brought below the LFD_ENABLE threshold and then brought above it with the LFDSYNC pin held in the desired state.

To use DIM as an analog input, the LFDSYNC pin must be low when mode crosses the LFD_ENABLE threshold. In this mode, DIM becomes an analog input that varies the amount of time that the lamp is on during the period of the LFD oscillator. From 0.5 V to 3 V applied to the DIM pin varies the lamp on duty cycle from the programmed minimum to 100%.

> **NOTE:** The analog dimming signal is senitive to coupled noise from the lamps. Noise on this line will be seen as lamp flicker. It is highly reccommended that precautions be taken to prevent noise coupling to this signal for optimum results.

Applying a pulse train to the LFDSYNC pin will synchronize the LFD oscillator to that pulse train. The frequency of the applied pulse train must be higher than the free running frequency of the oscillator.

APPLICATION INFORMATION

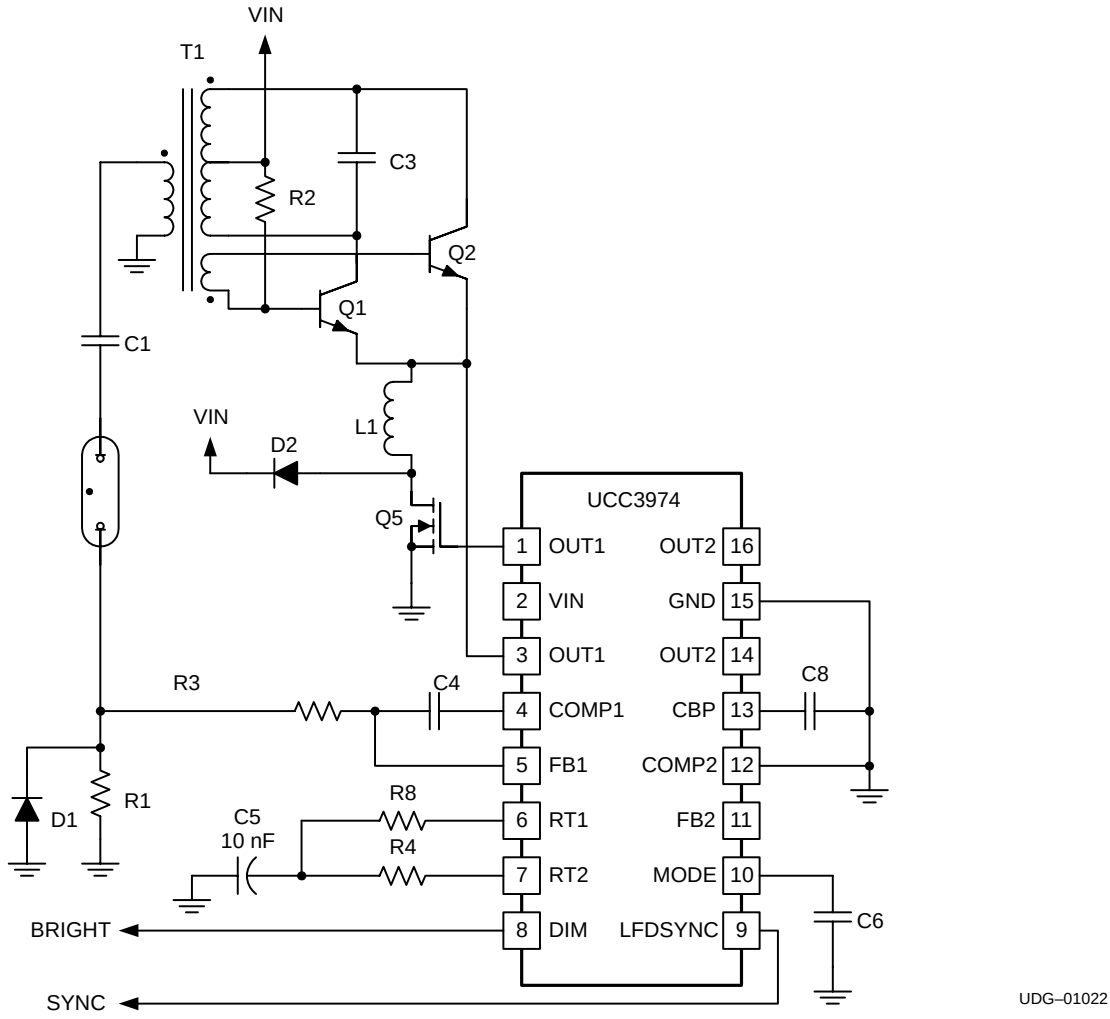


Figure 2. Typical Single-Channel Application

APPLICATION INFORMATION

low-frequency dimming oscillator

The oscillator for the LFD section of the device is an R-C relaxation oscillator with programmable upslope and downslope on its timing ramp. Figure 3 shows a simplified LFD oscillator diagram that illustrates the principle. The charge time for the timing capacitor, C_T is the time it takes to charge that capacitor from 0.5 V to 3 V from a 4.2-V source through RC. This time is:

$$t_c = 1.126 \times R_C \times C_T \tag{1}$$

The discharge time is the time it takes to discharge the C_T capacitor from 3 V to 0.5 V through R_D connected to GND. This time is:

$$t_d = 1.792 \times R_D \times C_T \tag{2}$$

The period of the LFD oscillator is simply the sum of the charge and discharge times, or

$$T = C_T \left(1.126 \times R_C + 1.792 \times R_D\right) \tag{3}$$

The minimum duty cycle of the LFD PWM when operating in this mode is:

$$d_{min} = \frac{t_d}{T} \tag{4}$$

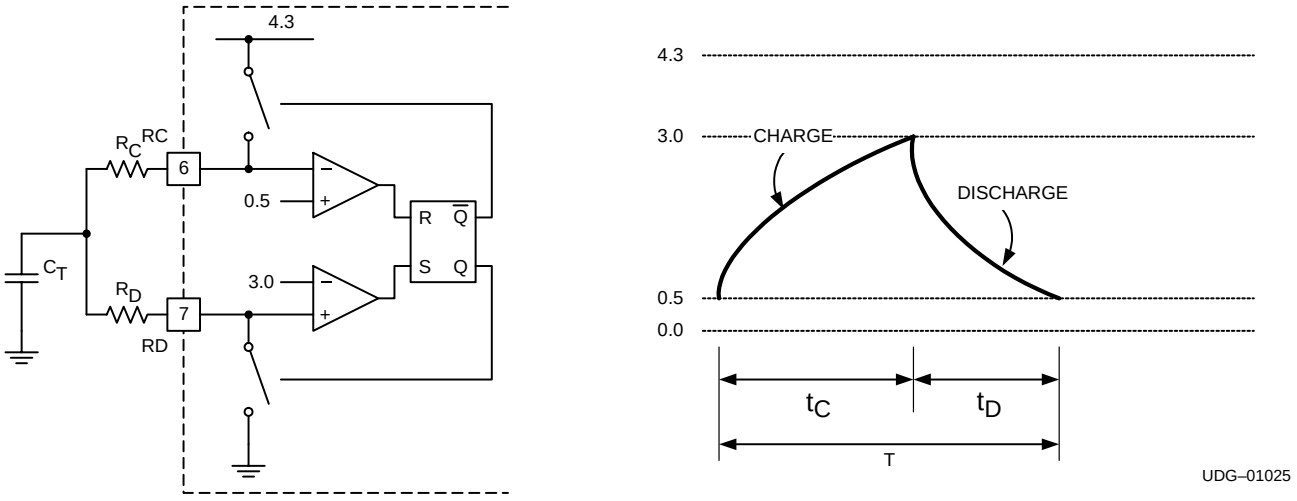


Figure 3. LFD Oscillator

APPLICATION INFORMATION

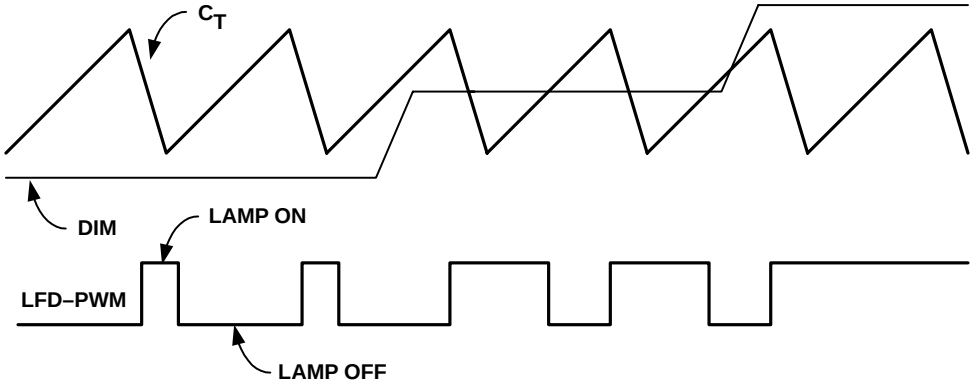


Figure 4. LFD Waveforms

Note from the Figure 4 that the LFD-PWM output is turned on at the start of the discharge cycle and is turned off when C_T crosses the DIM signal or at the start of the charge cycle if DIM is less than the valley voltage of 0.5 V.

The LFD oscillator runs free at some frequency determined by the external timing components. The LFD oscillator can be synchronized to a system clock signal. by applying this clock signal to the LFDSYNC pin. The signal must not be applied during power up since the MODE pin's crossing of the LFD_ENABLE threshold determines the function DIM takes on. If the synchronization signal is applied during power up, unpredictable results may occur. The synchronization frequency should be fairly close to (but higher than) the free run frequency of the oscillator. The operating range for the DIM signal is reduced when synchronizing the LFD oscillator just as with any other PWM. A synchronization pulse causes termination of the current charge cycle and starts a discharge. The ratio of free run to synchronization frequencies is the reduction factor for DIM's operating range.

For instance if the free-run frequency is 90% of the synchronization frequency, DIM is active over the 0.5-V to 2.75-V range instead of the 0.5-V to 3-V range. As a general recommendation, the free-run frequency should be kept within the 100-Hz to 1-kHz range, and synchronization should be limited to 120% of the free-run frequency to preserve control range on DIM.

output driver

The OUT1 and OUT2 pins are designed to directly drive small power MOSFETs. Output drive capability is limited by the 50-Ω maximum resistance of the driver. For large FETs where this drive level is insufficient, a separate driver is required. Note also that the output drive level is limited to approximately 12 V if the input voltage exceeds that level. For input voltages below 12 V, the driver drives to slightly below the input voltage.

startup sequence

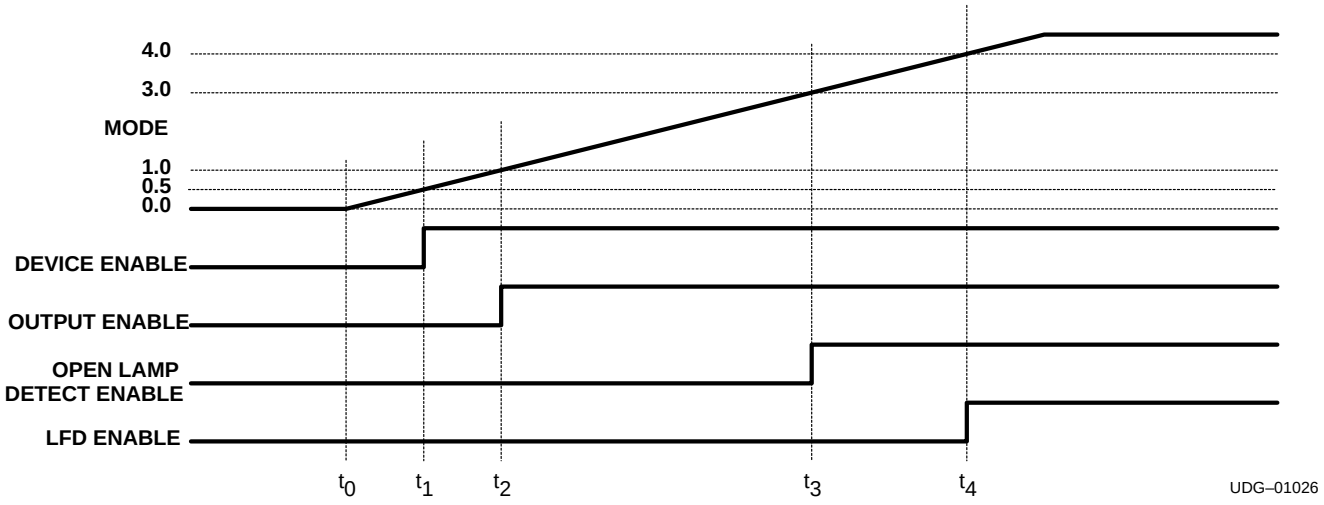


Figure 5. Start-Up Sequence

Figure 5 describes what happens during a typical startup sequence. At t0, power is applied to the system. A constant current source begins charging the external capacitor connected to the MODE pin. Until the voltage on the MODE pin reaches 0.5 V (t1), the internal circuitry on the device is disabled and nothing happens at the outputs. As the voltage crosses 0.5 V, the internal circuitry is powered up. When the voltage crosses 1 V at t2, the outputs are enabled, allowing the buck stages to begin to charge up and to supply current to the royer stages.

During the period from t2 to t3, the open lamp detection circuitry is disabled, preventing a false trip of the open lamp detector circuit when the lamp is trying to ignite for the first time. As a precaution against severe overvoltage on the high-voltage secondary of the transformer, a clamp circuit is included in the UCC3974. The function of the clamp circuit is to monitor the voltage on the BUCK pins and prevent that voltage to drop more than 8.7-V below the input rail. This is accomplished by sourcing a current from the FB pin when the BUCK voltage drops more than 8.7 V.

The magnitude of the current sourced from this pin is proportional to the excess drop of the BUCK voltage beyond 8.7 V. The maximum current sourced from this pin is approximately 200 μA. Consequently, the impedance at the FB pin affects the speed at which this clamp becomes effective. A small capacitor and large resistors in the feedback network increases the effectiveness of this feature. From t3 onward, the open lamp detector circuit is enabled. Each time the BUCK pin drops more than 7.8-V below VIN, a 4-bit counter is clocked. If the counter reaches a count of 16 (4 bits) it declares an open lamp fault and shuts down the device. Resetting the device requires a power cycle. The counter in the open lamp detector is an up/down counter. If the BUCK pin only occasionally dips below the 7.8-V threshold, an open lamp condition is not declared since the counter is clocked down on each cycle in which BUCK does not cross the 7.8-V threshold. At time t4, LFD is enabled. Depending on the state of LFDSYNC when this threshold is crossed, DIM is either an analog input or a digital one.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3974PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3974	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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