UM11099

PCAL6534 demonstration board OM13541

Rev. 1.0 — 1 August 2019 User manual

Document information

Information	Content
Keywords	OM13320 Fm+ development kit, OM13260 Fm+ I2C bus development board, OM13303 GPIO target board
Abstract	Installation guide and User Manual for the OM13541 34-bit GPIO Daughter Card that connects to OM13260 Fm+ I2C bus development board. This daughter board makes it easy to test and design with the PCAL6534, an ultra-low voltage translating 34-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I2C-bus interface. This daughter board, along with the Fm+ Development board, provides an easy to use evaluation platform.

Revision history

Rev	Date	Description
v.1	20190801	Initial version

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1 Introduction

The PCAL6534 34-bit GPIO evaluation board allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V on SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V on I/O ports with active low reset input control and open-drain active low interrupt output indicator (red LED) plus one hardware address input setting to select one of four different slave addresses. A graphical interface allows the user to easily explore the different functions of the I/O expander.

The IC communicates to the host via the industry standard I^2C-bus/SMBus port. The evaluation software runs under Microsoft Windows PC platform.

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2 Features of the OM13541 34-bit GPIO daughter board

- Direct connection to OM13260 Fm+ I^2C-bus Development board
- Easy to use GUI-based software demonstrates the capabilities of the PCAL6534
- Jumper configuration for most features of PCAL6534
- Flexible power supply configuration: 3.3 V, 5 V or external supply
- Direct connection to OM13303 GPIO Target board for I/O visualization
- Convenient test points for easy scope measurements and signal access
- Jumper configuration of device I^2C address
- LED indicators for power and $\overline{INT}$
- No external power supply required and obtains +5 V power from PC USB port

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3 Hardware description

3.1 Power supply jumpers

The power supply selection for the OM13541 is very flexible and allows for detailed analysis and evaluation of 34-bit GPIO device. J13 selects +5V_PWR supply from either the tester connector J1 (pins 4 and 6, +5V_TSTR) or the Fm+ board connector J11 (pins 7 and 12, +5V). J7 selects VDDP (U1 pin A6) supply from either +5V_PWR or +3V3 (J11 pins 8 and 11) and J2 selects VDDI (U1 pin A1) supply from either +3V3 (J11 pins 8 and 11) or +5V_PWR. If external power operation is desired from TP2 (VDDP-IN) and TP3 (VDDI), no jumper is required on J7 and J2. The D2 green LED is lit when VDDP is available.

3.2 SCL and SDA jumpers

The I^2C -bus signals SDA and SCL supplied to the device under test can be sourced from either the Fm+ board via J11 or the tester via J1. Jumpers J10 and J9 select the I^2C bus 1 or bus 2 signals from the Fm+ board, shorting pins 1 to 2 to select I^2C bus 1 while shorting pins 2 to 3 to select I^2C bus 2.

3.3 Device reset, interrupt and address pin selection

- **Reset** (U1, pin A5), the device is resetting when shorting pin 1 to 2 on jumper J5
- **Interrupt** (U1, pin B1), open-drain interrupt ($\overline{INT}$) output is activated and D1 red LED is lit when any input state differs from its corresponding Input Port register state, TP4 can be used to monitor the $\overline{INT}$ pin 32.
- **Address input** (U1, pin A4), jumper J8 is used to select device address as shorting pins 1 to 2 (VDD, address is 46h), shorting pins 3 to 4 (VSS, address is 44h), shorting pins 5 to 6 (SDA, address is 42h), shorting pins 7 to 8 (SCL, address is 40h).

3.4 Board layout viewer

Figure 1 shows all jumper locations and labels on PCB.

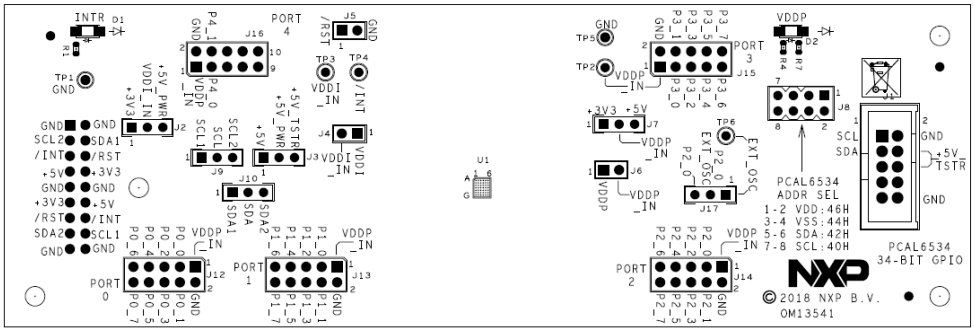


Figure 1. PCAL6534 demo board layout and Labels

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3.5 Connector pinouts

- **J1** (10-pin male tester connector) is connected to master which is driving either I^2C-bus for PCAL6534. This is easily achieved with third party development tools from Total Phase (http://www.totalphase.com). There are two tools called Aardvark and Beagle that direct connect to this board through J1.

Table 1. J1 10-pin tester connector

J1 Pin #	Function	Board connection
1	SCL	U1 pin A3 (PCAL6534)
2,10	GND	Ground
3	SDA	U1 pin A2 (PCAL6544)
4, 6	+5V_TSTR	J13 pin 3
5	SDOUT (MISO)	NC
7	SCLK	NC
8	SDIN (MOSI)	NC
9	/CS (SS)	NC

Note: Since SDA and SCL are both connected to the device (U1) under test, the Aardvark and the Fm+ Development board cannot be used simultaneously. The Beagle, a bus sniffer, does not have any issues.

- **J11** (18-pin female connector) can connect directly to the OM13260 Fm+ Development board. This connector provides power, I^2C signals and other ancillary signals.

Table 2. J11 18-pin Fm+ board connector

J11 Pin #	Function	Board connection
1, 2, 9, 10, 17, 18	GND	Ground
3	SCL2	SCL Bus 2 to J9 pin 3
4	SDA1	SDA Bus 1 to J10 pin 1
5, 14	$\overline{\text{INT}}$	Interrupt to U1 pin B1, LED (D1) and TP4 (test point 4)
6, 13	RESET	U1 pin A5 and J5 pin 1
7, 12	+5V	J3 pin 1
8, 11	+3V3	J2 pin 1 and J7 pin 1
15	SDA2	SDA Bus 2 to J10 pin 3
16	SCL1	SCL Bus 1 to J9 pin 1

Note: The connector on the Fm+ board is a male, shrouded 14 pin types, while the connector on this 34-bit GPIO board is an 18-pin female. The reason lies with the shroud around the 14-pin connector. To ensure correct mating of the female with the male, two pin positions on both female sides are grounded.

- **J12, J13, J14, J15, J16** (10-pin male connector) is connected to GPIO target board (OM13303) which consists of eight LEDs and eight switches and connects directly to this 34-bit GPIO board through J12 (I/O of port 0), J13 (I/O of port 1), J14 (I/O of port 2), J15 (I/O of port 3), J16 (I/O of port 4). These switches and LEDs on GPIO target board permit easy exercise of the I/O functionality of the device under test. The LEDs light red when the voltage on that channel is below VDDP x 0.3V and LEDs light green

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when the voltage is above VDDP x 0.7V. The LEDs remain off when the voltage is between those two levels.

Table 3. J12, J13, J14, J15, J16 10-pin GPIO target board connector

J[12:16] pin #	Function	Board connection
1	VDDP_IN	J7 pin 2 and TP2 (test point 2) and by J6 to VDDP (U1 pin A6)
2	GND	Ground
3	P[0:4]_0 (I/O 0)	U1 pin C1, D3, E3, E6, B5
4	P[0:4]_1 (I/O 1)	U1 pin B2, F1, F4, E4, B4
5	P[0:4]_2 (I/O 2)	U1 pin B3, E2, G5, D5
6	P[0:4]_3 (I/O 3)	U1 pin D1, G1, G5, D6
7	P[0:4]_4 (I/O 4)	U1 pin C2, G2, G6, D4
8	P[0:4]_5 (I/O 5)	U1 pin C3, F2, F6, C5
9	P[0:4]_6 (I/O 6)	U1 pin E1, G3, F5, C6
10	P[0:4]_7 (I/O 7)	U1 pin D2, F3, E5, C4

3.6 All jumpers default setting and test points

Figure 2 shows the PCAL6534 demo board.

- D1 (red LED) is connected to interrupt output (U1 pin B1), it is ON when $\overline{INT}$ is asserted
- TP4 ($\overline{INT}$) is connected to interrupt output (U1 pin B1) for probing use.
- TP1 and TP5 are GND test points for probing use.
- TP6 (EXT_OSC) is external clock input through J17 (1-2) to P2_0 (pin E3) for debouncer circuit use
- TP2 (VDDP_IN) and TP3 (VDDI) are connected to external power inputs.
- All jumpers default settings and functions are shown in Table 4.

Table 4. All jumpers setting for test and evaluation

Jumper	Default setting	Comment
J7 (3-pin)	2-3 (VDDP_IN = +5V_PWR)	This jumper is used to select VDDP for U1 device (pin A6) 1-2: select +3V3 2-3: select +5V_PWR
J2 (3-pin)	1-2 (VDDI_IN = +3V3)	This jumper is used to select VDDI for U1device VDDI (pin A1) 1-2: select +3V3 (from Fm+ development board) 2-3: select +5V_PWR
J3 (3-pin)	1-2 (+5V = +5V_PWR)	This jumper is used to select +5V_PWR source 1-2: select +5V from Fm+ development board 2-3: select +5V_TSTR from tester (beagle) board
J4 (2-pin)	Short	Short: connect VDDI to U1 device VDDI (pin A1) Open: connect current meter to measure the IDDI on U1 device
J5 (2-pin)	Open	Short: force /RESET (U1 pin A5) to GND Open: 10K pull-up /RESET (U1 pin A5) to VDDI
J6 (2-pin)	Short	Short: connect VDDP_IN to U1 device VDDP (pin A6) Open: connect current meter to measure the IDDP on U1 device

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Jumper	Default setting	Comment
J8 (4x2-pin)	1-2 (VDDI)*note1	This 4x2 jumper is used to select input value for ADDR (U1 pin A4) 1-2: select VDDI (address is 0x46 for PCAL6534) 3-4: select VSS (address is 0x44 for PCAL6534) 5-6: select SDA (address is 0x42 for PCAL6534) 7-8: select SCL (address is 0x40 for PCAL6534)
J9 (3-pin)	1-2 (SCL = SCL1)	This jumper is used to select SCL source for U1 device (pin A3) 1-2: select SCL1 (bus 1 from Fm+ development board) 2-3: select SCL2 (bus 2 from Fm+ development board)
J10 (3-pin)	1-2 (SDA = SDA1)	This jumper is used to select SDA source for U1 device (pin A2) 1-2: select SDA1 (bus 1 from Fm+ development board) 2-3: select SDA2 (bus 2 from Fm+ development board)
J11 (18-pin)	Connect Fm+ development board	This 18-pin female connect to PORT A/B/C/D (14-pin male) on Fm+ development board (OM13260) for power supply, I2C-bus and control signals to test
J12-J16 (10-pin)	Connect to GPIO Target board	This 10-pin male connect to GPIO target board (OM13303) for input/ output pins test
J17 (3-pin)	2-3 (P2_0)	This jumper is used to select function either P2_0 or EXT_OSC for U1 device (pin E3) 1-2: select external oscillator (EXT_OSC) input for debounce circuit use 2-3: select P2_0 input as normal operation
1. Default PCAL6534 slave address is set to 0x46 (ADDR = VDD)		

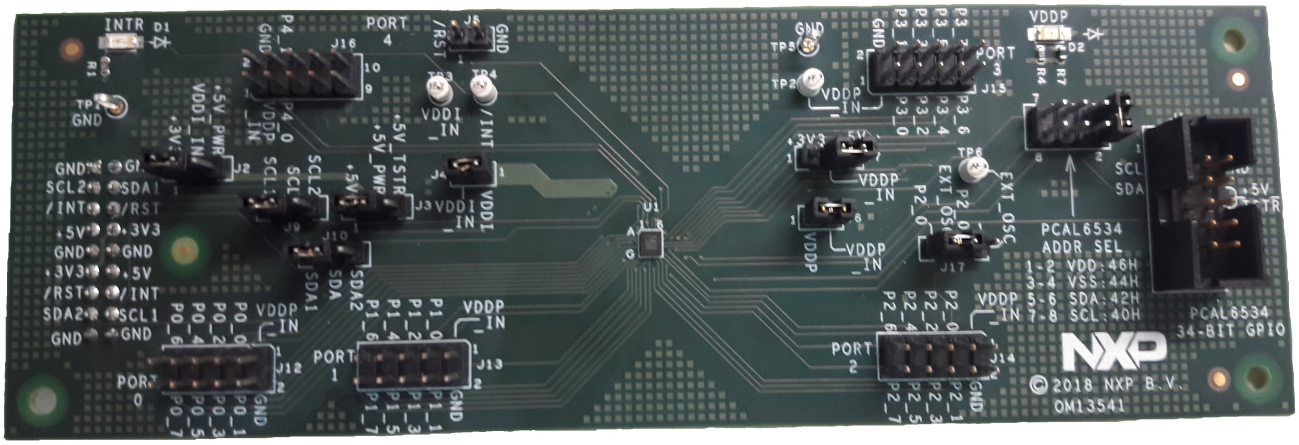


Figure 2. PCAL6534 demo board (OM13541)

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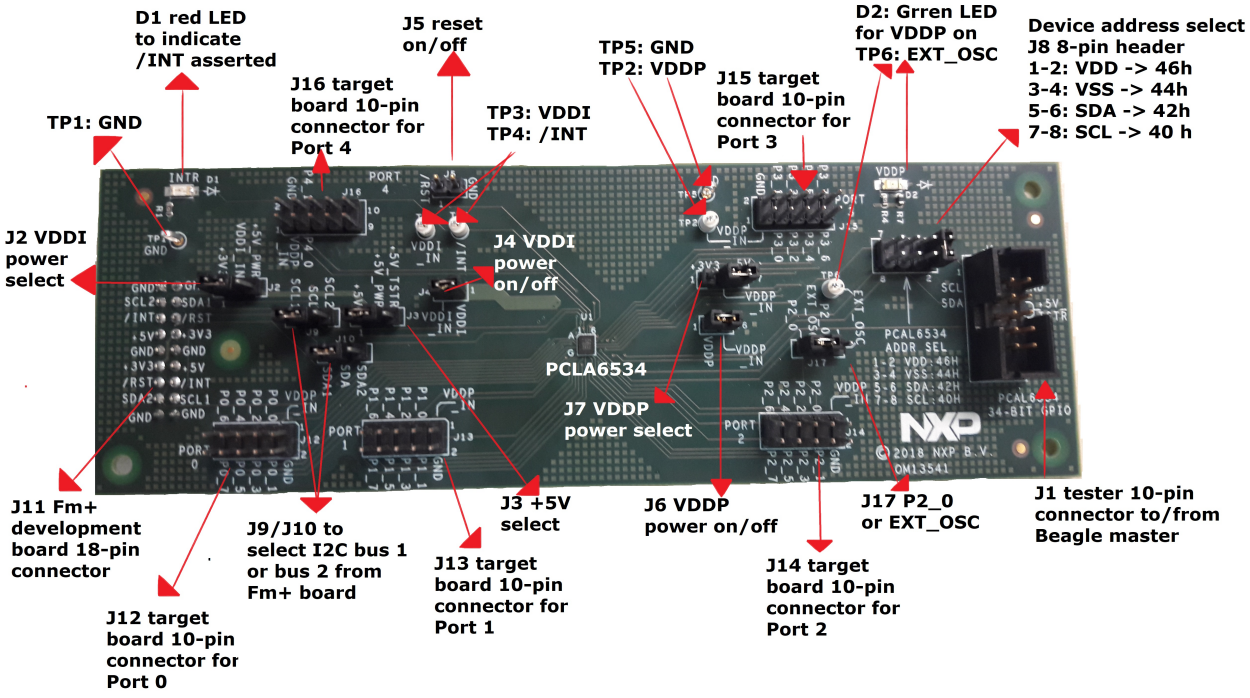


Figure 3. PCAL6534 demo board (OM13541) detailed

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4 Schematic

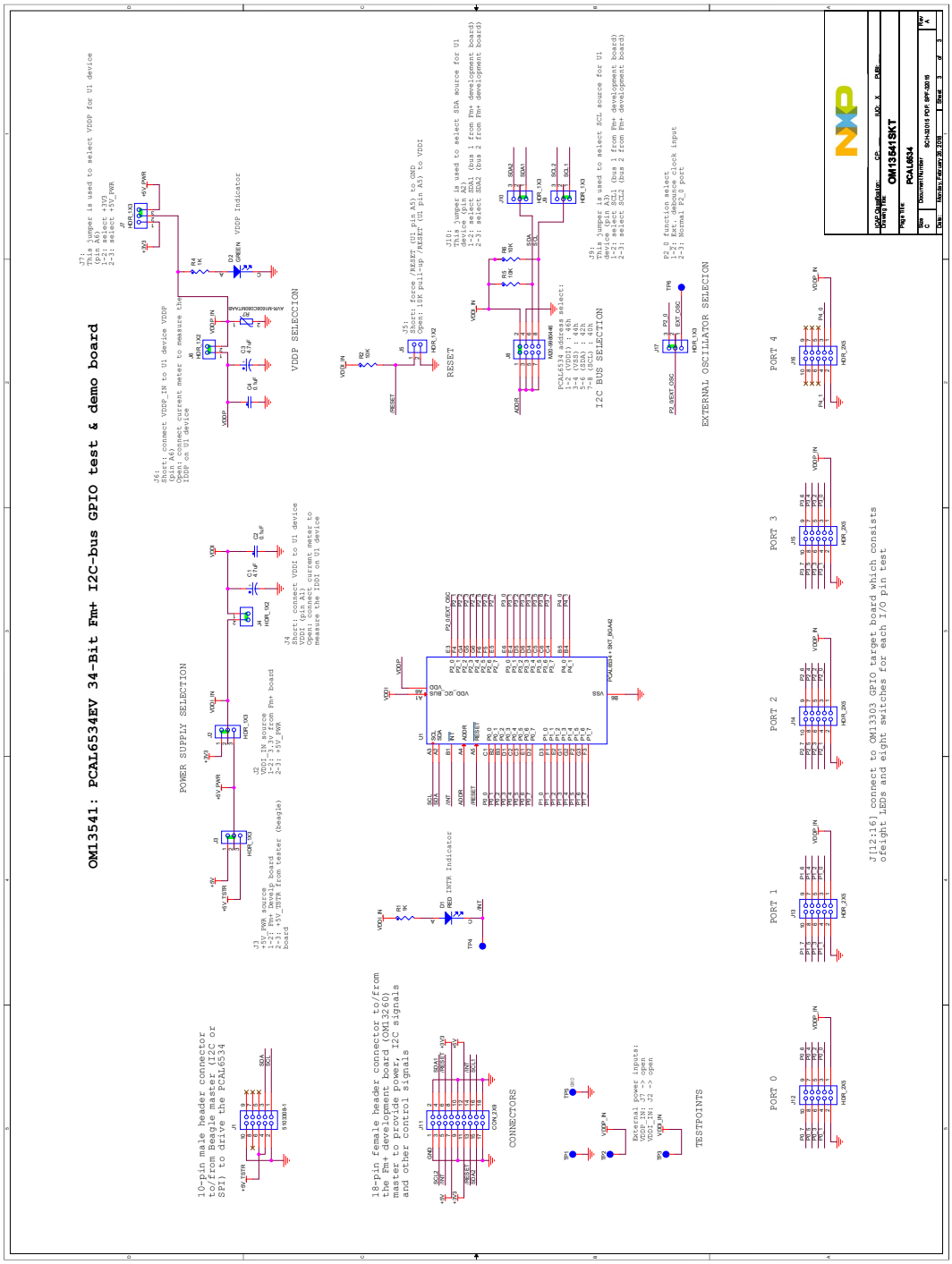


Figure 4. PCAL6534 demo board schematic

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5 Installation

5.1 PCAL6534 demo board, Fm+ development board, GPIO target board

The OM13541 PCAL6534 34-bit GPIO demo board is a daughter card to the OM13260 Fm+ I2C bus development board, which is part of the Fm+ development board kit (OM13320); three I/O ports (8-bit × 3) on PCAL6534 are connected to the GPIO target board for I/O visualization. You may download the software, user manual, and find ordering information at the NXP web site:

https://www.nxp.com/products/analog/interfaces/ic-bus/ic-led-controllers/ic-fm-plus-development-board:OM13320

5.2 OM13541 connection to Fm+ I^2C-bus development board

The OM13260 Fm+ I^2C-bus development board should be disconnected from your PC before mounting the OM13541 board with GPIO target board on to it. The OM13541 board has an 18-pin female connector (J11) that connects to CN4 14-pin male connector on the Fm+ development board (OM13260) as shown in Figure 5. Five GPIO Target boards (OM13303) through ribbon cables connect to 10-pin male connectors (J12, J13, J14, J15, J16) on OM13541 PCAL6534 34-bit GPIO demo board for 8-bit I/O port0, port1, port2, port3 and port4.

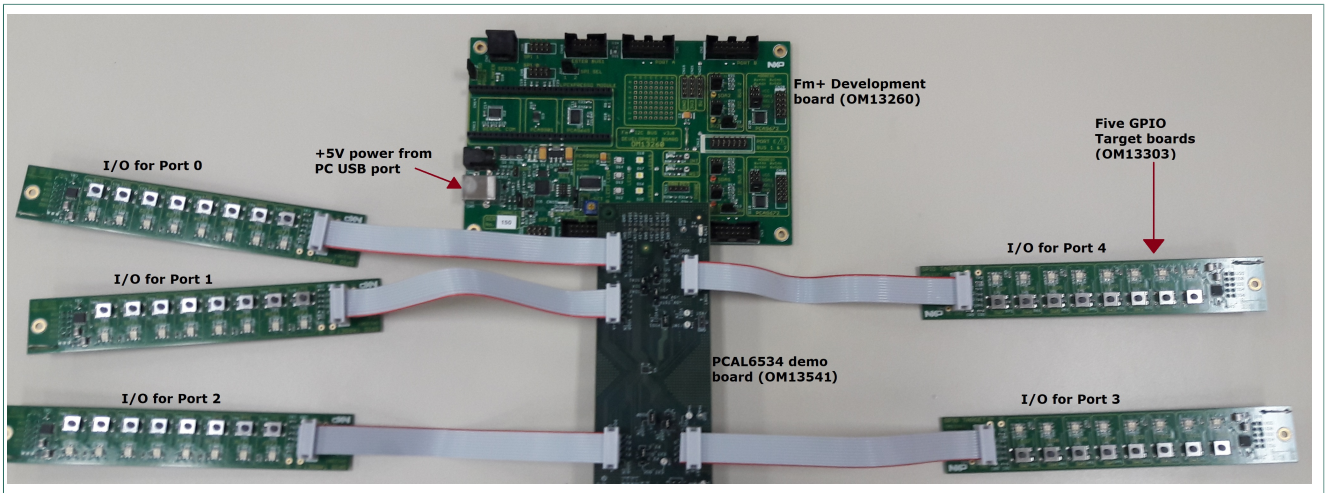


Figure 5. PCAL6534 demo board (OM13541) mounting to the Fm+ development board (OM13260) and connecting to five GPIO target boards (OM13303)

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6 PCAL6534 evaluation steps with Fm+ development board

The PCAL6534 is controlled by the Fm+ development board GUI in Expert mode as shown in Figure 6 and Figure 7.

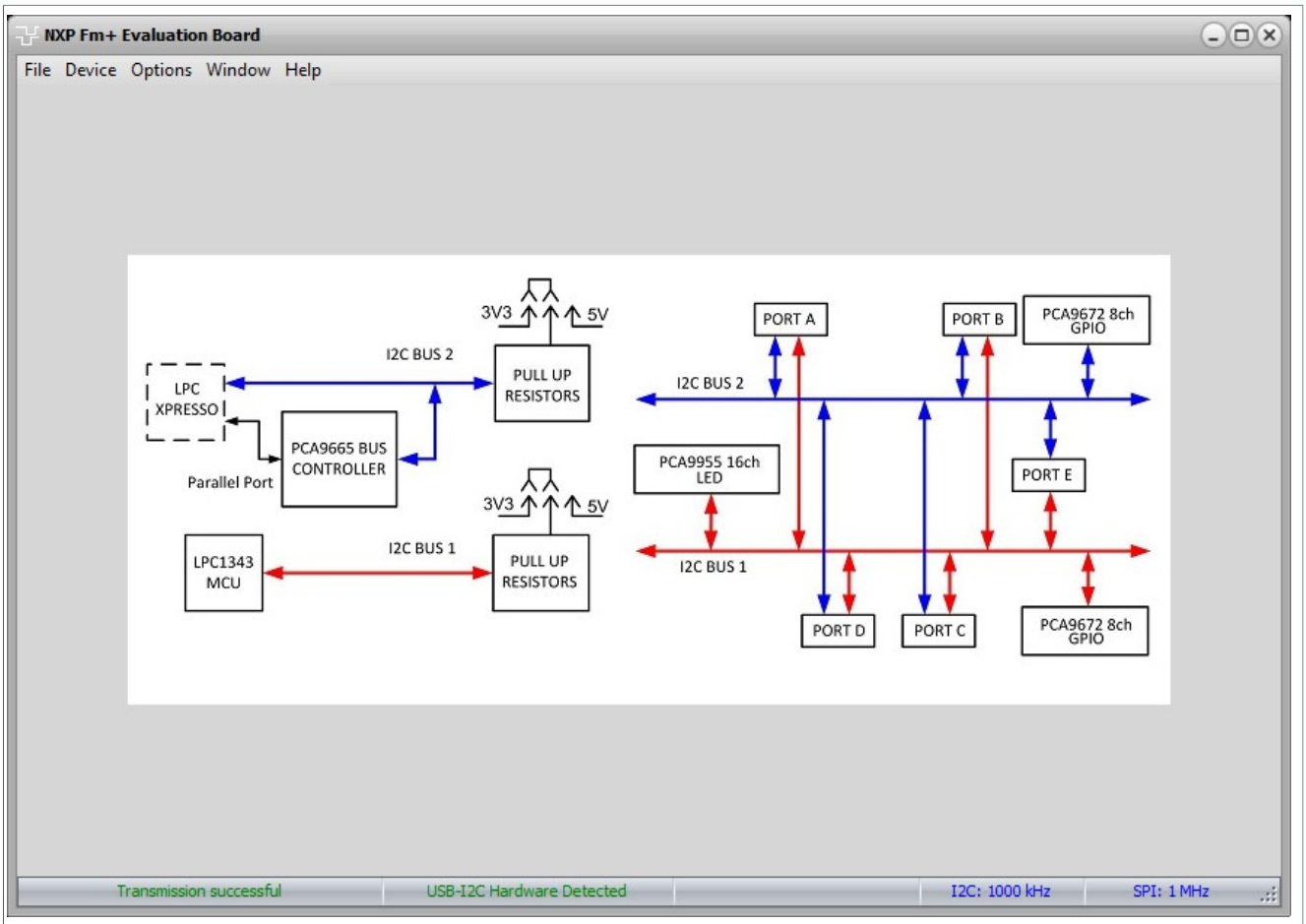


Figure 6. Select the Expert Mode from Fm+ development board GUI (1 of 2)

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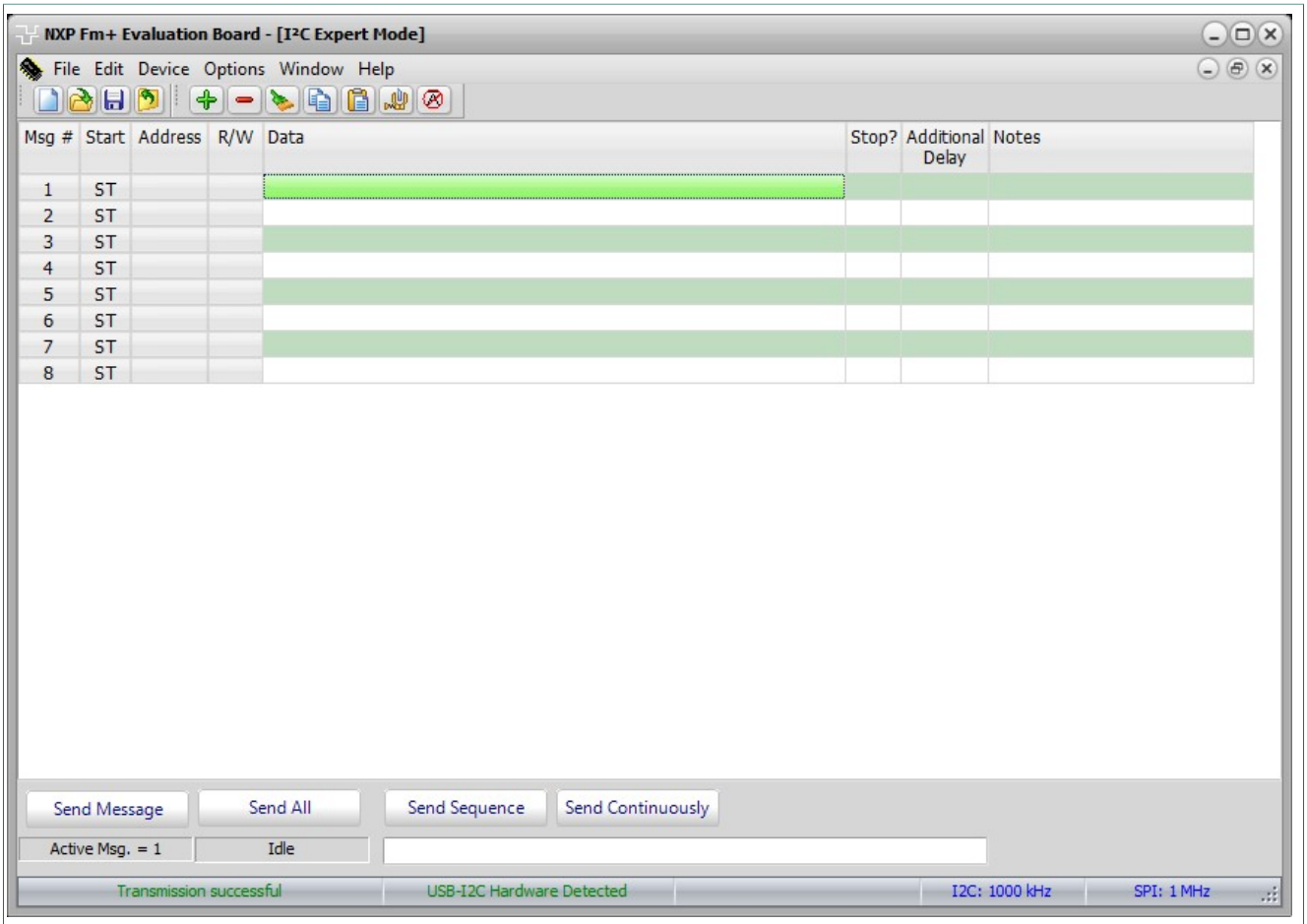


Figure 7. Select the Expert Mode from Fm+ development board GUI (2 of 2)

Connect the hardware as described in Section 5.2. All jumpers are in default setting and device address is set to 0x46h on J8 (set ADDR = VDDI) for PCAL6534 demo board. When you have correctly installed the software and the demonstration board hardware is connected and recognized by the computer, start the Fm+ development board software. As shown in Figure 7, when the demonstration board hardware is correctly connected to the USB port and the computer recognizes it, the message “USB-I2C Hardware Detected” is displayed on the bottom of the window.

6.1 PCAL6534 output shifting pattern demo for all five ports

1. From the ‘Device’ drop-down menus select ‘Expert Mode’ as shown in Figure 7.
2. Copy the “output shifting pattern on all five ports” text file as shown below. From the ‘File’ drop-down menus select ‘Open’, and from the “open data file” window to select the “output shifting pattern on all five ports” text file.

```
==========================================================================
Expert Mode Data File
46,Write,Yes,200,0F,00,00,00,00,00,Comments: set all GPIOs as output ports
46,Write,Yes,200,05,FF,FF,FF,FF,FF,Comments: write registers 04,05,06 to set all
output ports to 1s
46,Write,Yes,200,05,FE,FE,FE,FE,FE,Comments: set bit0 to 0 in all five ports
46,Write,Yes,200,05,FD,FD,FD,FD,FD,Comments: set bit1 to 0 in all five ports
```


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46,Write,Yes,200,05,FB,FB,FB,FB,Comments: set bit2 to 0 in Ports 0 to 3
46,Write,Yes,200,05,F7,F7,F7,F7,Comments: set bit3 to 0 in Ports 0 to 3
46,Write,Yes,200,05,EF,EF,EF,EF,Comments: set bit4 to 0 in Ports 0 to 3
46,Write,Yes,200,05,DF,DF,DF,DF,Comments: set bit5 to 0 in Ports 0 to 3
46,Write,Yes,200,05,BF,BF,BF,BF,Comments: set bit6 to 0 in Ports 0 to 3
46,Write,Yes,200,05,7F,7F,7F,7F,Comments: set bit7 to 0 in Ports 0 to 3
Sequence:01,02,03,04,05,06,07,08,09,10
==========

3. After opening the “output shifting pattern on all five ports” text file, the “NXP Fm+ Board GUI” in Expert mode screen is displayed as shown in Figure 8.
4. Click the ‘Send All’ button; all the valid messages on the screen are sent in the order of the row number (Msg #). This action is performed once.

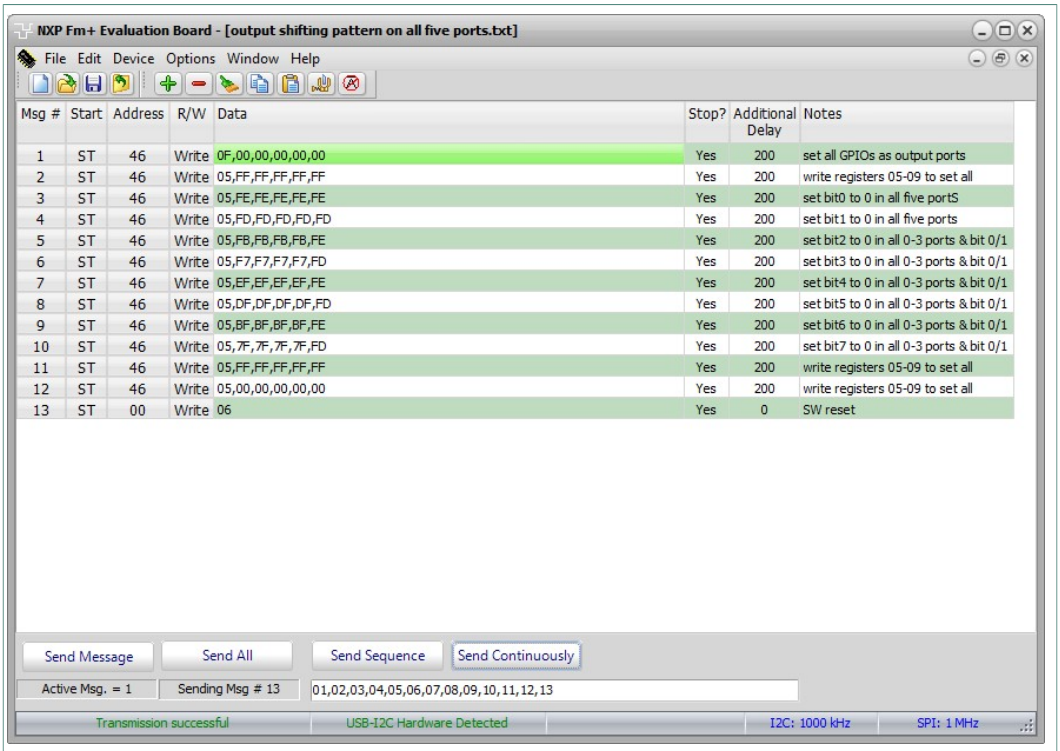


Figure 8. Message data in Expert mode to demo “output shifting pattern on all five ports”

6.2 PCAL6534 registers are controlled by Fm+ board GUI

1. Select 34-bit PCAL6534 from I/O Expanders as shown in Figure 9.

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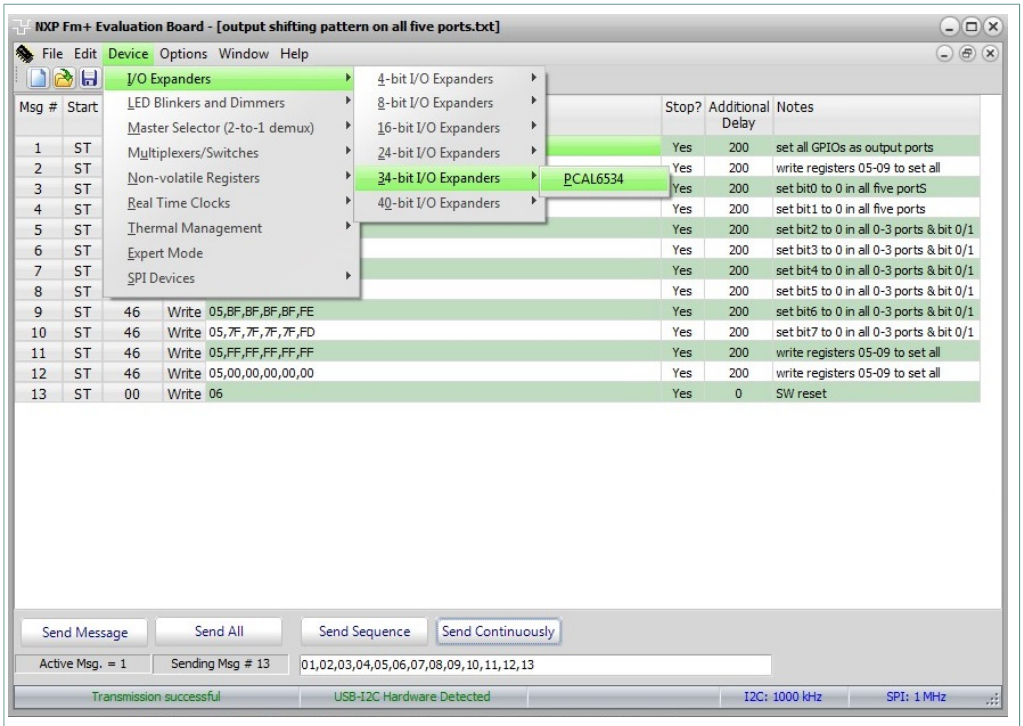


Figure 9. Device selection screen for PCAL6534

2. Input registers read are shown in Figure 10.

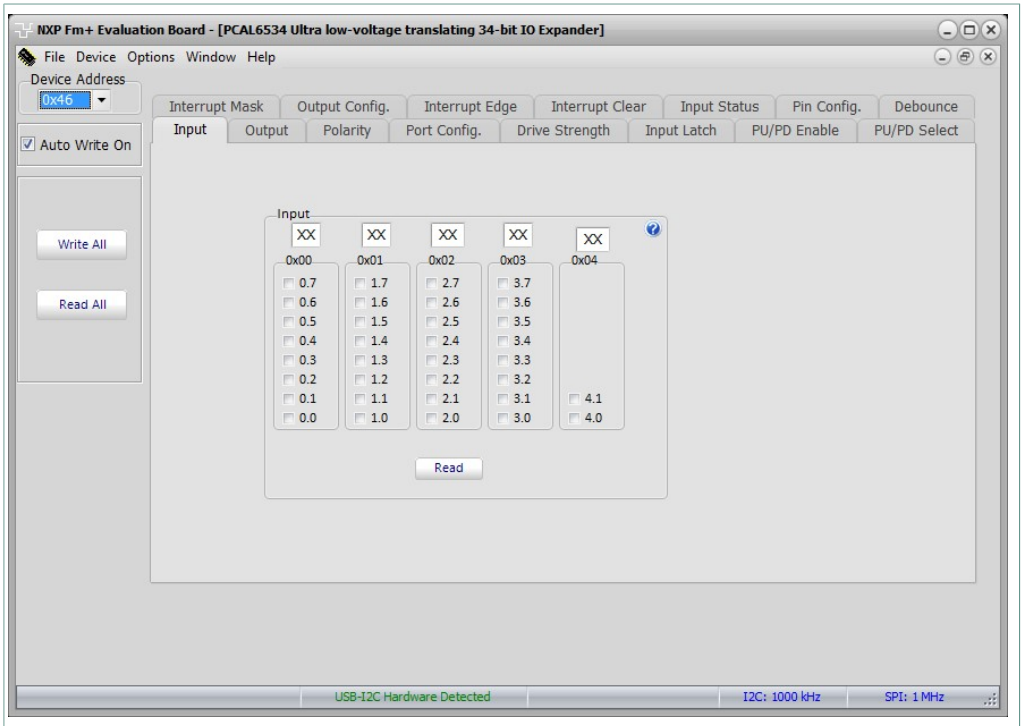


Figure 10. Device configuration screen for registers 00-04 hex

3. Output registers read or write are shown in Figure 11.

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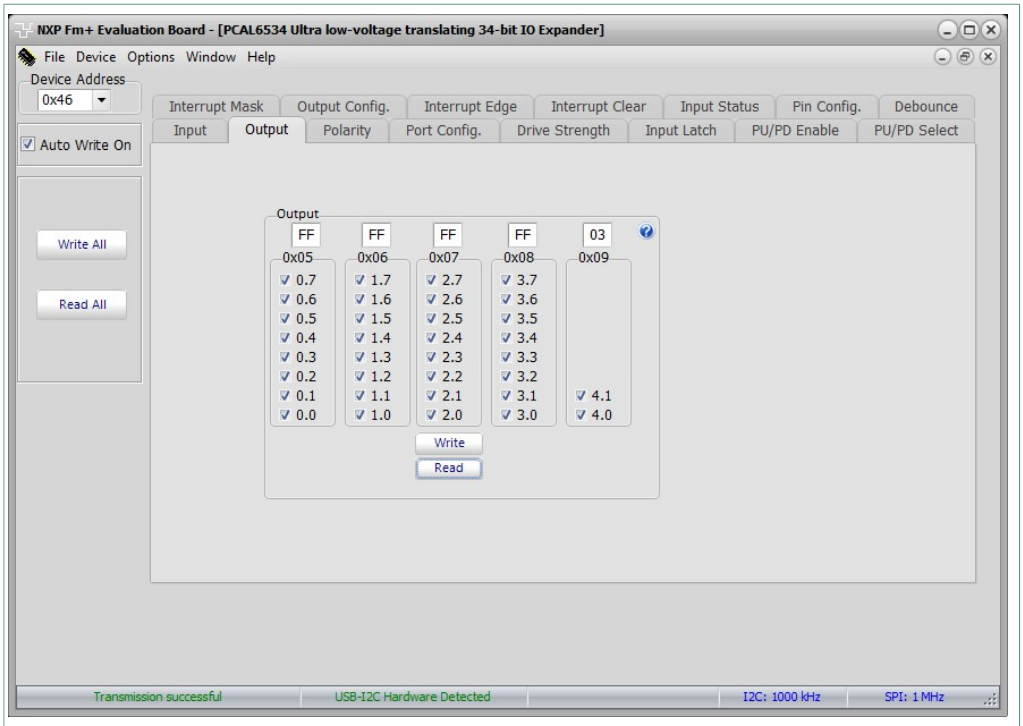


Figure 11. Device configuration screen for registers 05-09 hex

4. Polarity registers read or write are shown in Figure 12.

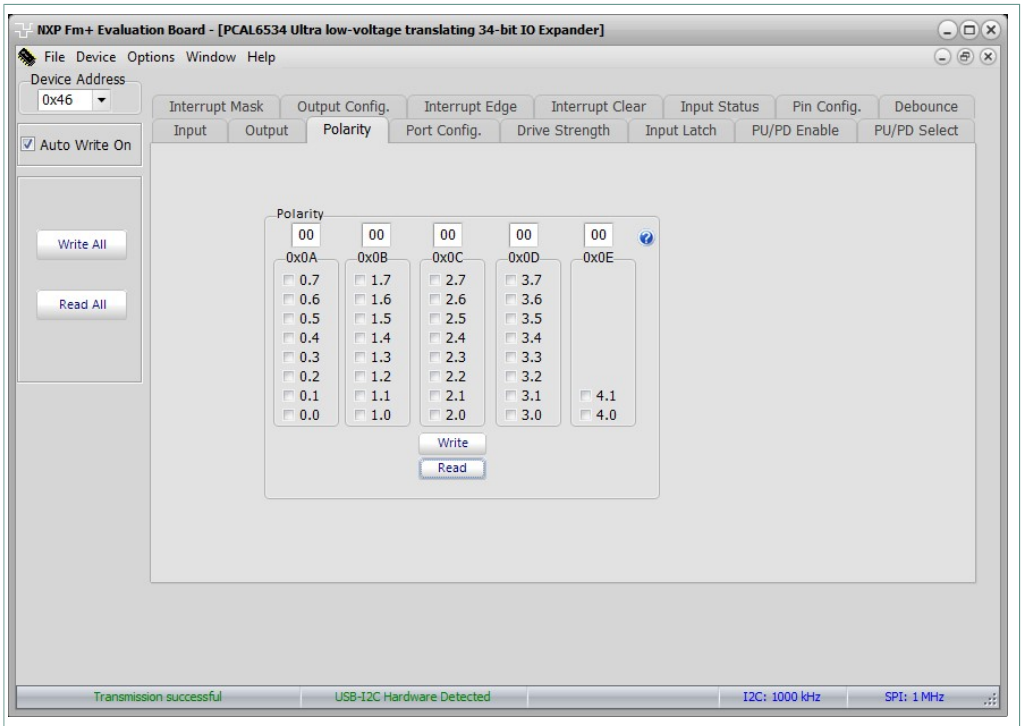


Figure 12. Device configuration screen for registers 0A-0E hex

5. Port Configuration registers read or write are shown in Figure 13.

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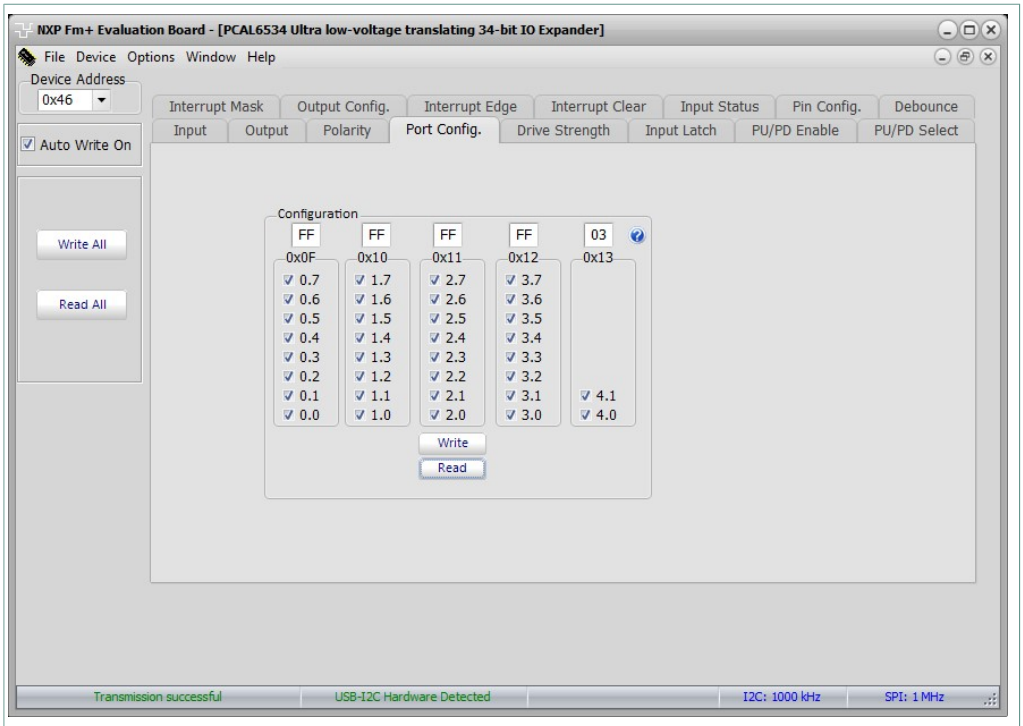


Figure 13. Device configuration screen for registers 0F-13 hex

6. Drive strength registers read or write are shown in Figure 14.

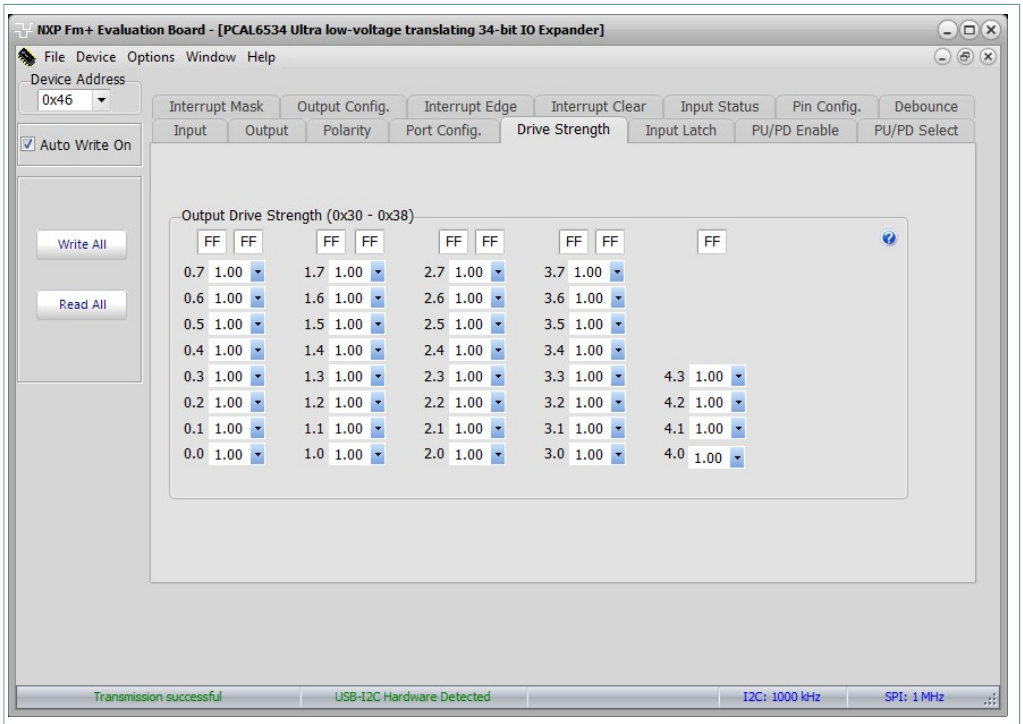


Figure 14. Device configuration screen for registers 30-38 hex

7. Input latch registers read or write are shown in Figure 15.

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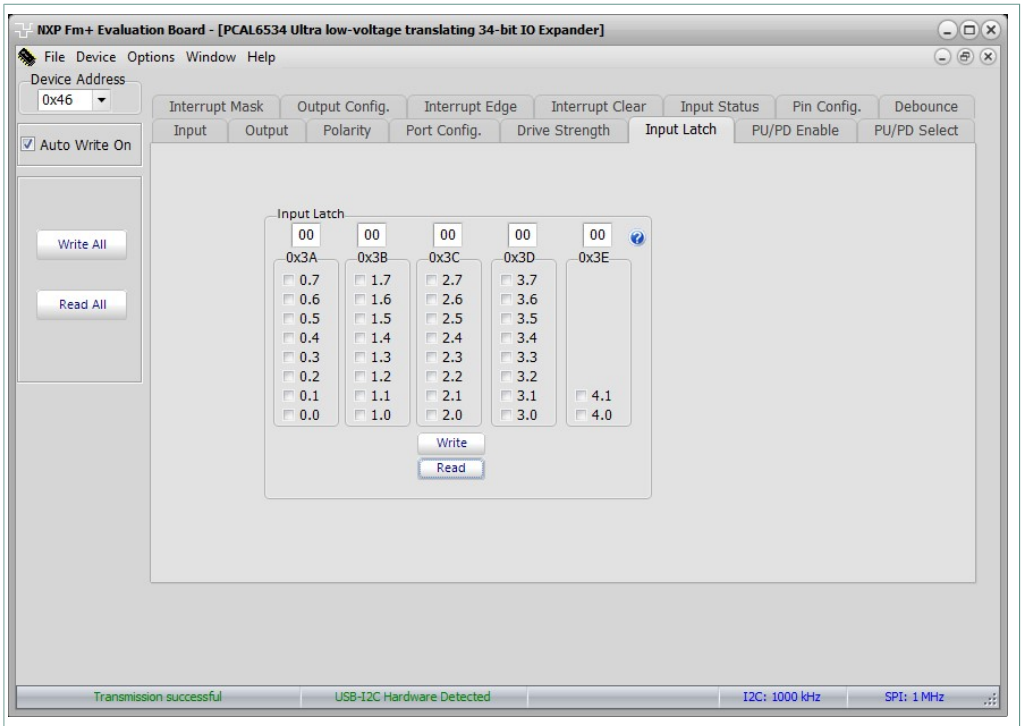


Figure 15. Device configuration screen for registers 3A-3E hex

8. PU/PD Enable registers read or write are shown in Figure 16.

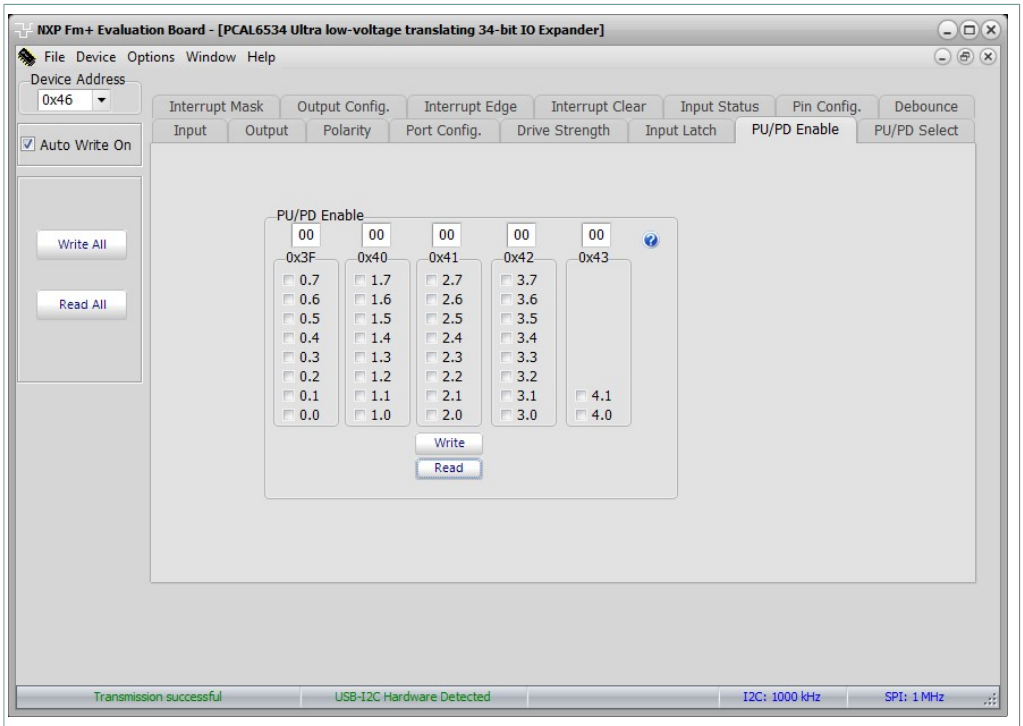


Figure 16. Device configuration screen for registers 3F-43 hex

9. PU/PD select registers read or write are shown in Figure 17.

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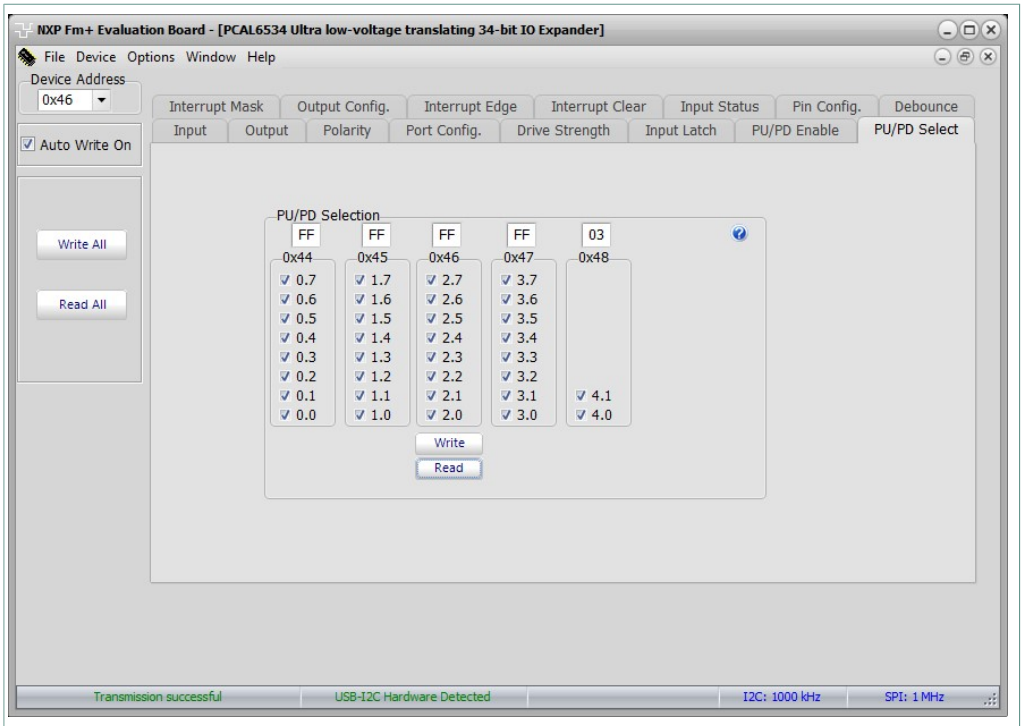


Figure 17. Device configuration screen for registers 44-48 hex

10. Interrupt mask registers read or write are shown in Figure 18.

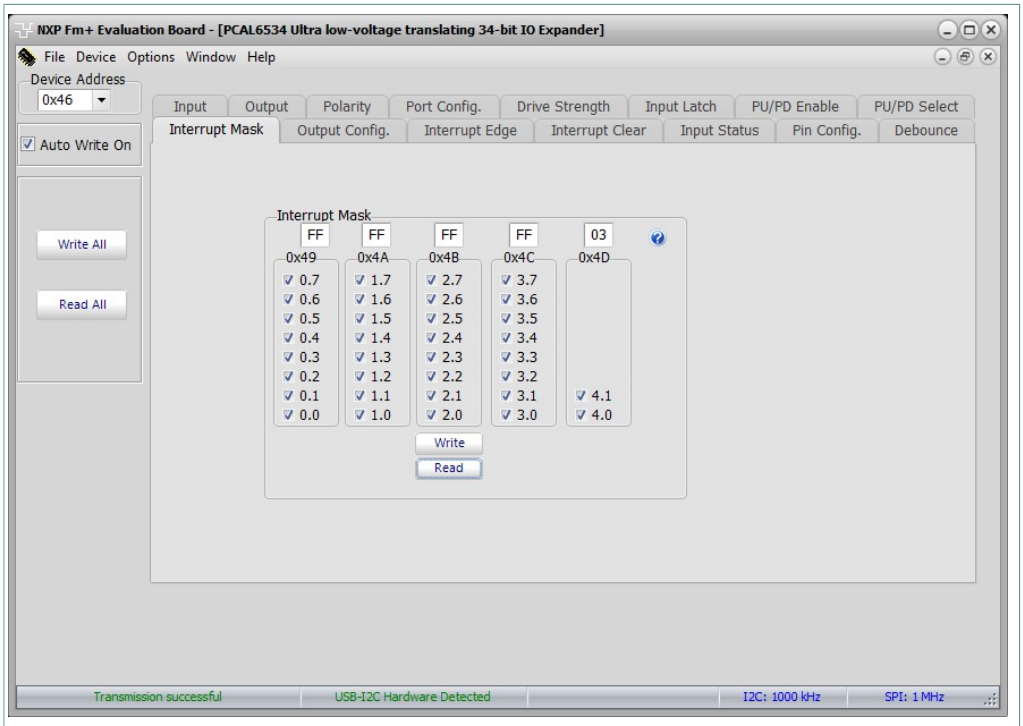


Figure 18. Device configuration screen for registers 49-4D hex

11. Output port configuration register read or write is shown in Figure 19.

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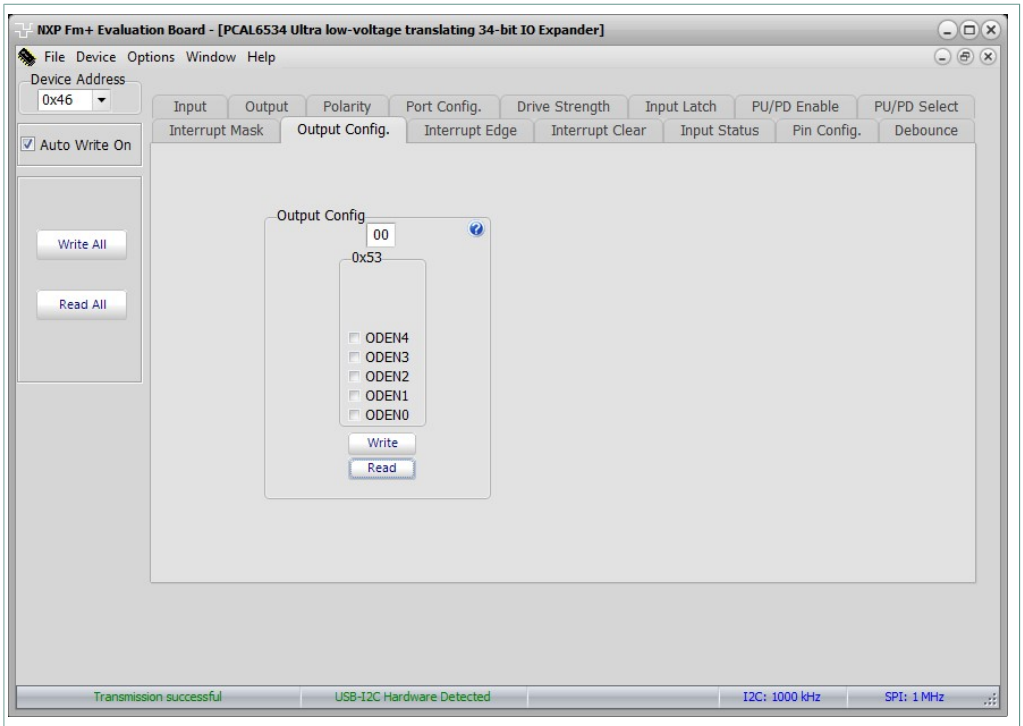


Figure 19. Device configuration screen for registers 53 hex

12. Interrupt edge registers read or write are shown in Figure 20.

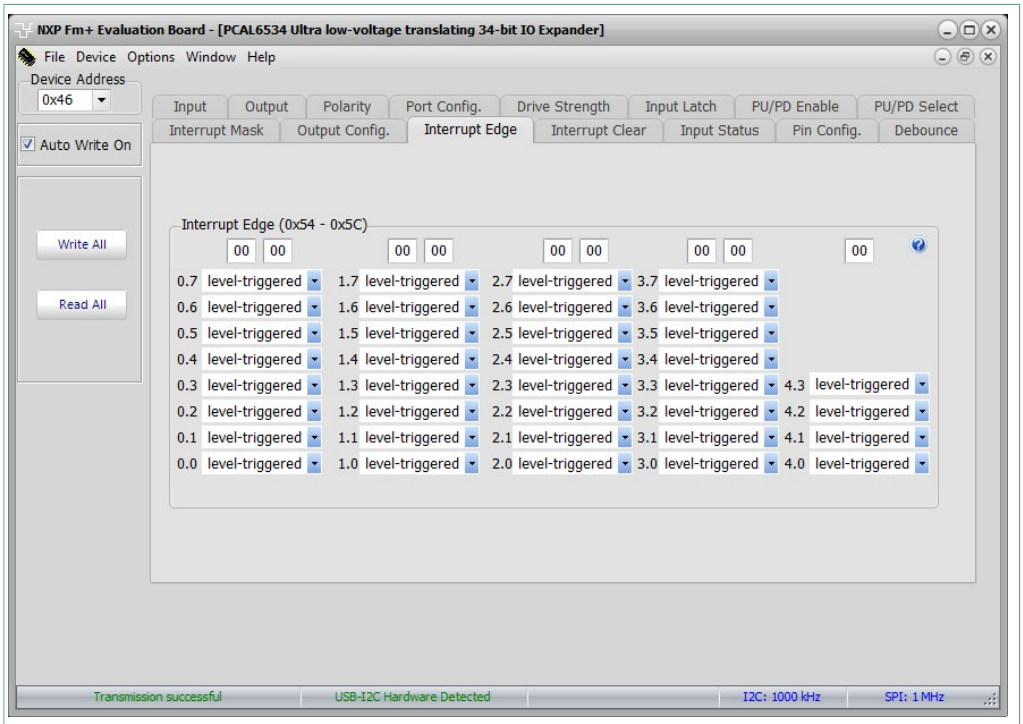


Figure 20. Device configuration screen for registers 54-5C hex

13. Interrupt Clear registers write are shown in Figure 21.

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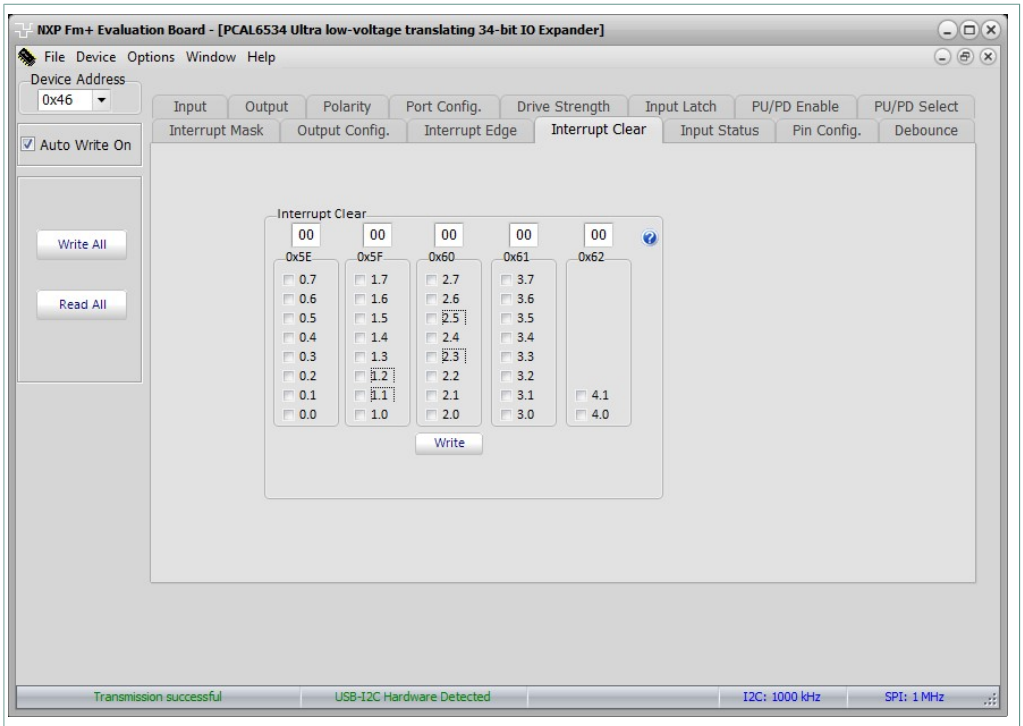


Figure 21. Device configuration screen for registers 5E-62 hex

14. Input status registers read are shown in Figure 22.

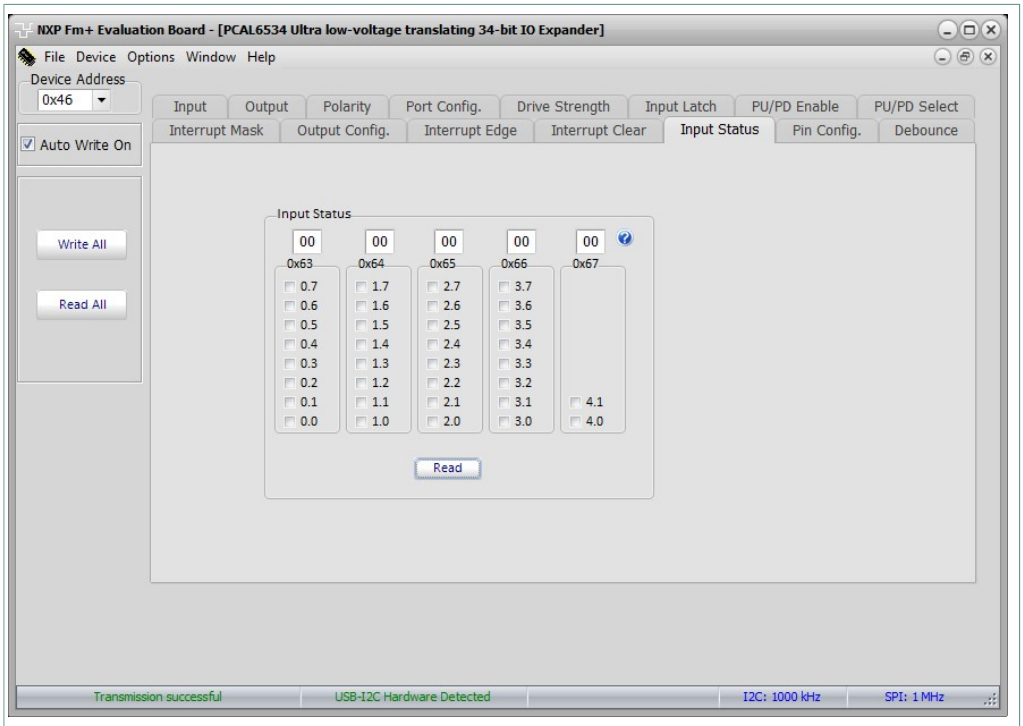


Figure 22. Device configuration screen for registers 63-67 hex

15. Pin Configuration registers read or write are shown in Figure 23.

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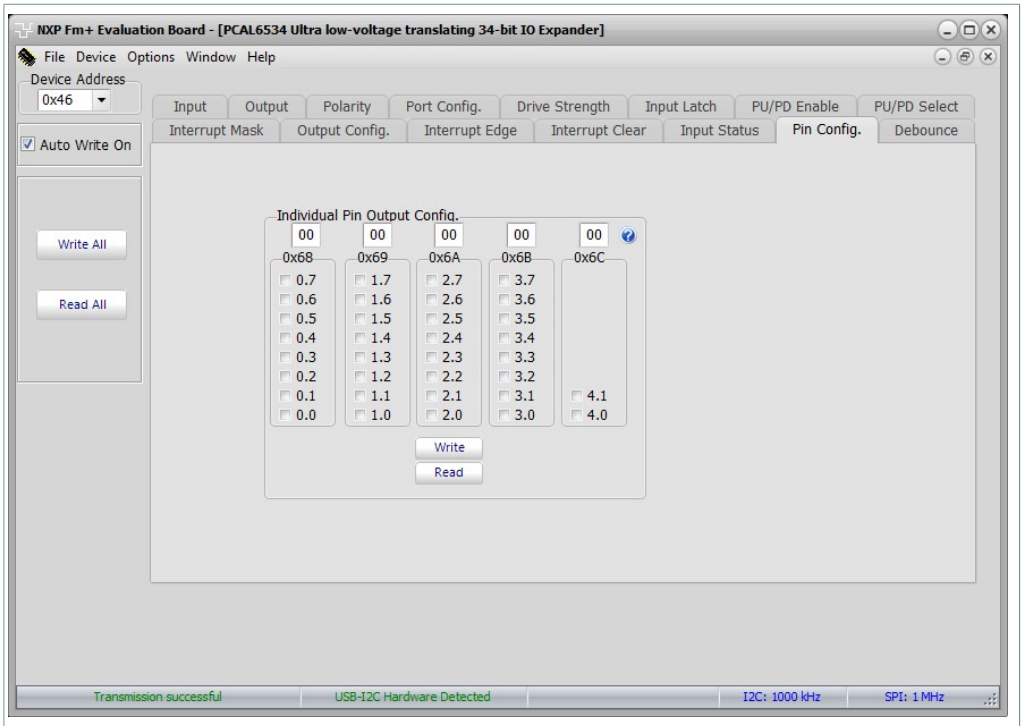


Figure 23. Device configuration screen for registers 68-6C hex

16. Debounce registers read or write are shown in Figure 24.

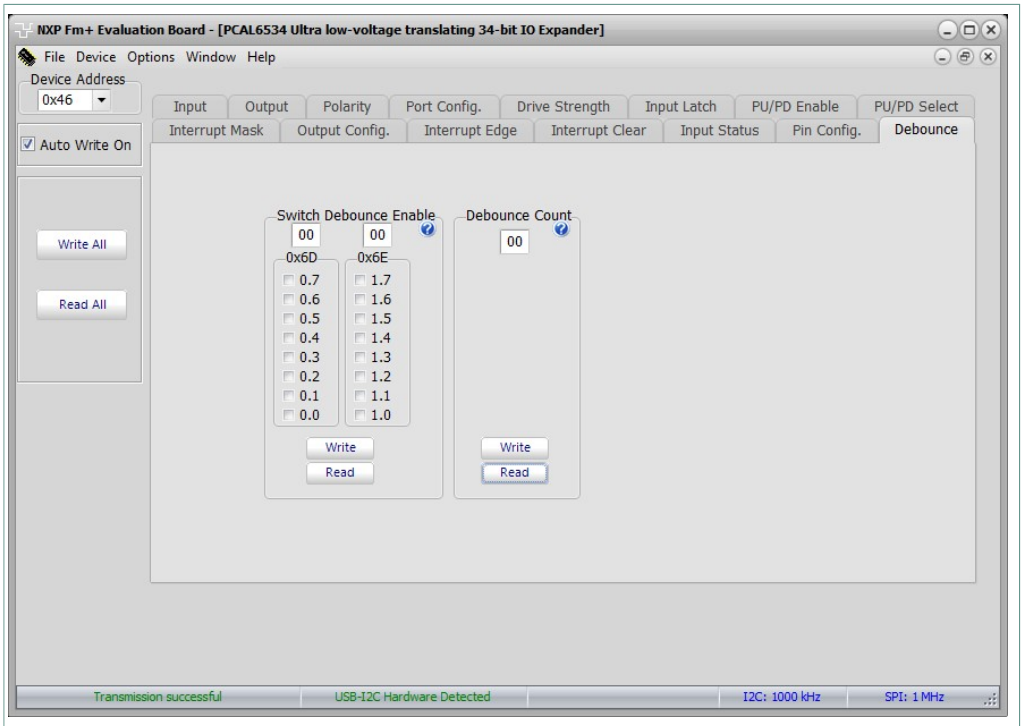


Figure 24. Device configuration screen for registers 6D-6F hex

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7 Support

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8 Abbreviations

Table 5. Abbreviations

Acronym	Description
ESD	Electro Static Discharge
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
I^2C-bus	Inter-integrated Circuit bus
LED	Light Emitting Diode
PC	Personal Computer
PCB	Printed-Circuit Board
SMBus	System Management Bus
USB	Universal Serial Bus

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9 References

1. PCAL6534, Ultra low-voltage translating 34-bit Fm+ I^2C-bus/SMBus I/O expander; Product data sheet; NXP Semiconductors
2. UM10741, Fm+ Development Kit OM13320 User manual; NXP Semiconductors

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