EVALUATION KIT AVAILABLE

MAX8989

Multimode PA Step-Down Converter with Linear Bypass Mode

General Description

The MAX8989 step-down converter is optimized for powering the power amplifier (PA) in multistandard handsets such as LTE, WCDMA, GSM, and EDGE. The device integrates a high-efficiency PWM step-down converter for medium- and low-power transmission with an 85mΩ (typ) low dropout (LDO) bypass regulator, in parallel with the step-down converter, enabling high-power transmission.

The IC uses an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The bypass LDO powers the PA directly from the battery during high-power transmission or in case of insufficient headroom between the input and programmed output. The bypass LDO is enabled when the output voltage is greater than 1.0V. In the case where the output current exceeds the step-down converter current limit, the bypass LDO provides supplementary current to the output, ensuring a stable output voltage. The bypass LDO also provides a smooth transition between step-down regulation and operation in dropout.

The IC is available in a 9-bump, 1.6mm x 1.6mm WLP package (0.69mm max height).

Applications

LTE, WCDMA, GSM, and EDGE Cell Phones/ Smartphones

Features

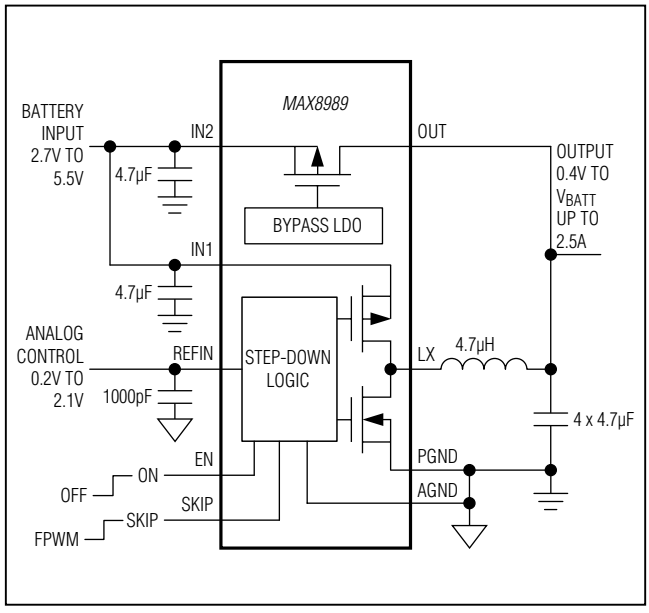
- **PA Step-Down Converter**
  - **25µs (typ) Settling Time for 0.4V to 3.2V Output Voltage Change**
  - **Dynamic Output Voltage Setting from 0.4V to V_{IN}**
  - **85mΩ pFET and 100% Duty Cycle for Low Dropout**
  - **2MHz Switching Frequency**
  - **Low Output Voltage Ripple**
  - **2% Output Voltage Accuracy Over Load, Line, and Temperature**
  - **Tiny External Components**
- **2.5A Output Current Capability**
- **Simple Logic On/Off Control**
- **Low 0.1µA Shutdown Current**
- **2.7V to 5.5V Supply Voltage Range**
- **Thermal Overload Protection**
- **1.6mm x 1.6mm WLP Package (0.69mm max Height)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8989EWL+T	-40°C to +85°C	9 WLP 0.5mm pitch

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel. This device has a minimum order increment of 2500 pieces.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5489; Rev 1; 1/11

ABSOLUTE MAXIMUM RATINGS

IN1, IN2, SKIP, EN, REFIN to AGND ..... -0.3V to +6.0V
OUT to AGND ..... -0.3V to (V_{IN2} + 0.3V)
IN1 to IN2 ..... -0.3V to +0.3V
PGND to AGND ..... -0.3V to +0.3V
IN1, IN2, OUT, LX Current (Note 1) ..... $1A_{RMS}$
OUT Short Circuit to AGND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
9-Bump WLP 0.5mm Pitch
(derate 14.1mW/°C above +70°C) 1.1W
Operating Temperature Range ..... -40°C to +85°C
Junction to Ambient
Thermal Resistance (θ_{JA}) (Note 2) ..... 71°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature (T_{JMAX}) ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LX has internal clamp diodes to PGND and IN1. Applications that forward bias this diode should take care not to exceed the power dissipation limits of the device.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN2} = V_{SKIP} = V_{EN} = 3.6V, V_{REFIN} = 0.9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range (V_{IN})	V_{IN1} = V_{IN2}		2.7		5.5	V
Input Undervoltage Threshold	V_{IN2} rising, 180mV typical hysteresis		2.52	2.63	2.70	V
No-Load Supply Current	V_{EN} = $V_{IN_}$, I_{OUT} = 0A, SKIP = AGND, switching			3		mA
	V_{EN} = $V_{IN_}$, I_{OUT} = 0A, V_{SKIP} = $V_{IN_}$, V_{REFIN} = 0.35V, no switching			0.115		
Shutdown Supply Current	V_{EN} = 0V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.1		
THERMAL PROTECTION						
Thermal Shutdown	T_J rising, 20°C typical hysteresis			+160		°C
LOGIC CONTROL						
EN and SKIP Logic-Input High Voltage			1.3			V
EN and SKIP Logic-Input Low Voltage					0.4	V
EN Internal Pulldown Resistor				800		kΩ
SKIP Logic-Input Current	V_{IL} = 0V, V_{IH} = 5.5V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
POWER-UP TIMING (Figure 2)						
Time Delay from EN Until LX Starts Switching (t_{EN_BUCK})				62	130	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{SKIP} = V_{EN} = 3.6V, V_{REFIN} = 0.9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 3)

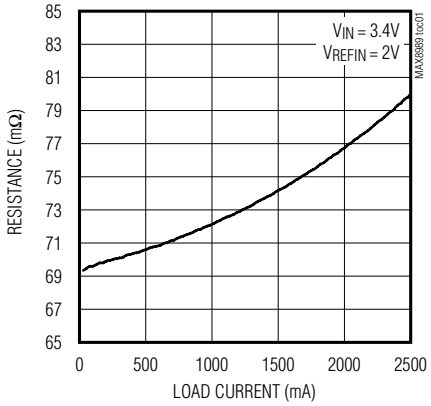
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFIN						
Common-Mode Range			0.2		1.7	V
REFIN to OUT Gain	V_{REFIN} = 0.32V, I_{LX} = 0A		1.89	2	2.11	V/V
	V_{REFIN} = 1.32V, I_{LX} = 0A		1.96	2.0	2.04	
Input Resistance				800		kΩ
REFIN Source Current				30		µA
Forced Dropout Mode Threshold	Above this threshold, the MAX8989 is forced into dropout mode, no hysteresis is implemented		1.80	1.95	2.10	V
LINEAR BYPASS						
On-Resistance	p-channel MOSFET bypass, I_{OUT} = 400mA			77		mΩ
Bypass LDO Current Limit	V_{REFIN} = 0.6V		1.2	1.8		A
Step-Down Converter Current Limit in Bypass Mode			1.3	1.6	1.8	A
Total Current Limit in Bypass Mode			2.5	3.4		A
Bypass LDO Off-Leakage Current	V_{IN2} = 5.5V, V_{OUT} = 0V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		1		
Linear Bypass Regulation Threshold	Below nominal output voltage, I_{OUT} = 0mA, V_{REFIN} = 0.5V or 1.2V			50		mV
Linear Bypass Regulation Enable Threshold	Linear bypass is enabled when V_{OUT} rises above this threshold			1.0		V
Linear Bypass Enable Threshold Hysteresis				25		mV
STEP-DOWN CONVERTER						
LX On-Resistance	p-channel MOSFET, I_{LX} = 100mA			0.175	0.300	Ω
	n-channel MOSFET, I_{LX} = 100mA			0.260	0.425	
LX Leakage Current	V_{EN} = 0V, V_{LX} = 0V	T_A = +25°C		0.1	5	µA
		T_A = +85°C		1		
p-Channel MOSFET Peak Current Limit			1.3	1.6	1.8	A
n-Channel MOSFET Valley Current Limit			1.0	1.3	1.5	A
n-Channel MOSFET Negative Current Limit			1.2	1.5	1.8	A
Automatic Skip Mode Enable Threshold	Skip mode is disabled when V_{OUT} rises above this threshold			1.0		V
Automatic Skip Mode Enable Threshold Hysteresis				25		mV
Static Zero-Crossing Threshold				20		mA
Minimum On- and Off-Times				70		ns
No Load Switching Frequency	T_A = +25°C		1.74	2	2.35	MHz
	T_A = -40°C to +85°C		1.6	2	2.4	

Note 3: The device is 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

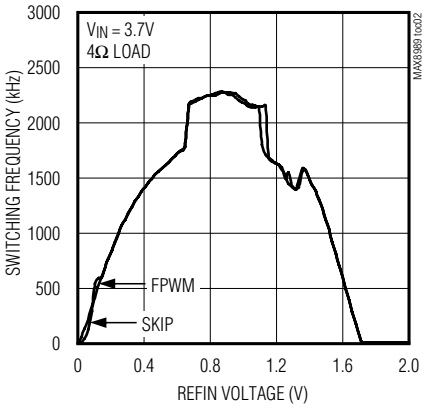
Typical Operating Characteristics

(*Typical Operating Circuit*, V_{IN1} = V_{IN2} = 3.7V, **V_{REFIN} = 0.9V, L1 = 4.7µH (TOKO DFE252012C)**, T_A = +25°C, unless otherwise noted.)

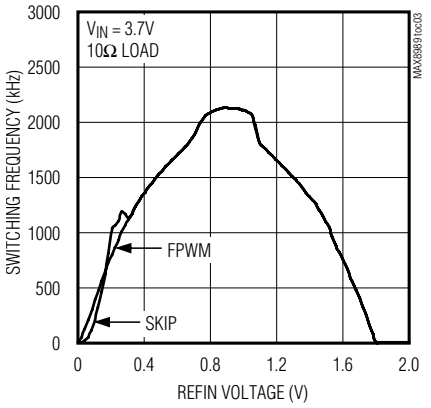
DROPOUT RESISTANCE vs. LOAD CURRENT



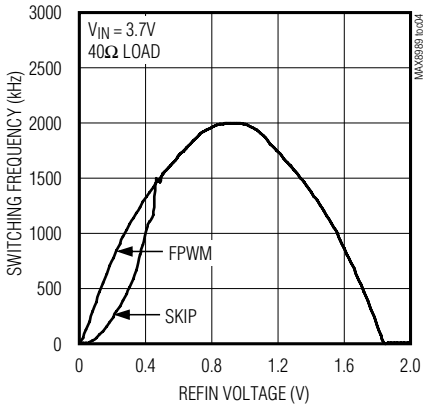
SWITCHING FREQUENCY vs. REFIN VOLTAGE



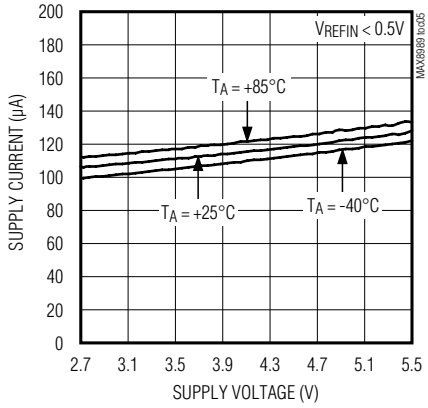
SWITCHING FREQUENCY vs. REFIN VOLTAGE



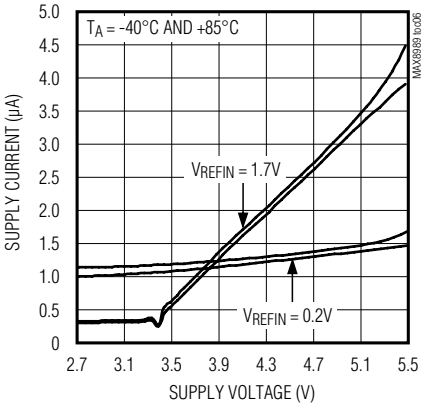
SWITCHING FREQUENCY vs. REFIN VOLTAGE



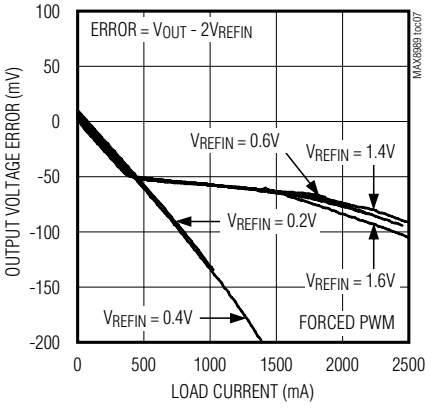
NO LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (SKIP MODE)



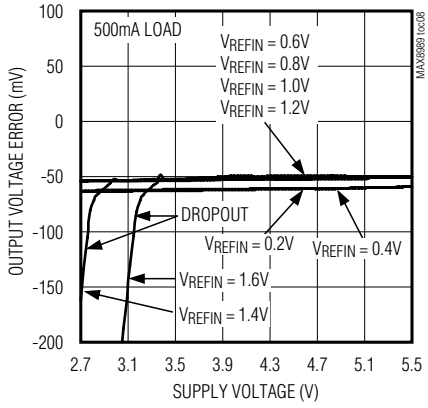
NO LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (FPWM MODE)



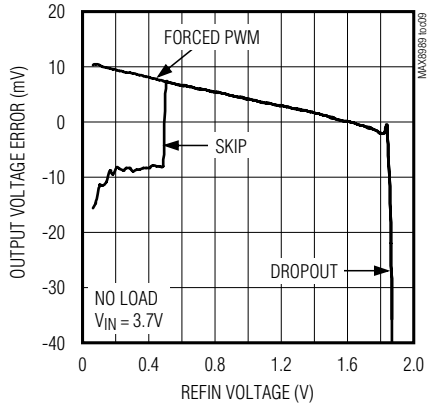
LOAD REGULATION ERROR vs. LOAD CURRENT



LINE REGULATION ERROR vs. SUPPLY VOLTAGE



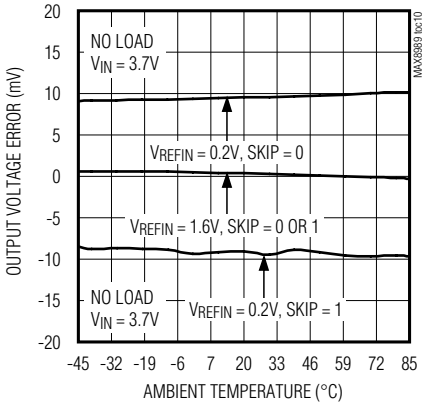
OUTPUT VOLTAGE ERROR vs. REFIN VOLTAGE



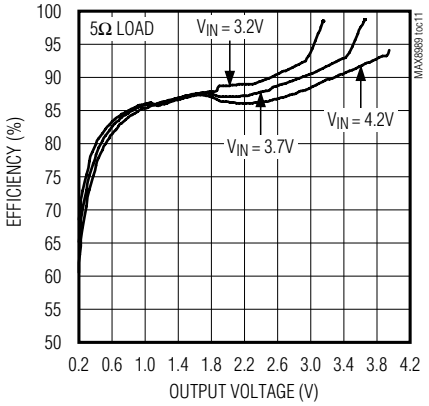
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN1} = V_{IN2} = 3.7V, **V_{REFIN} = 0.9V, L1 = 4.7µH (TOKO DFE252012C)**, T_A = +25°C, unless otherwise noted.)

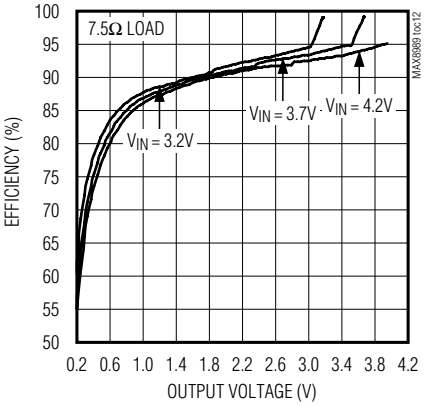
OUTPUT VOLTAGE ERROR vs. TEMPERATURE



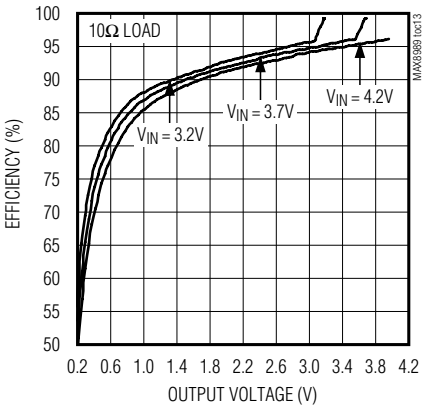
EFFICIENCY vs. OUTPUT VOLTAGE



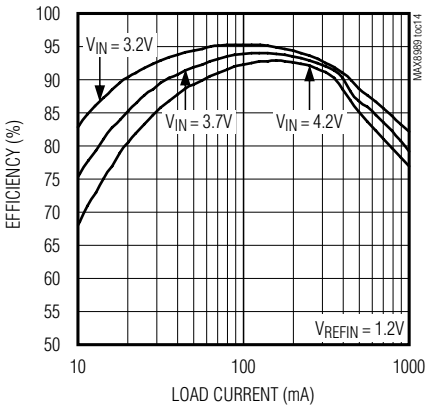
EFFICIENCY vs. OUTPUT VOLTAGE



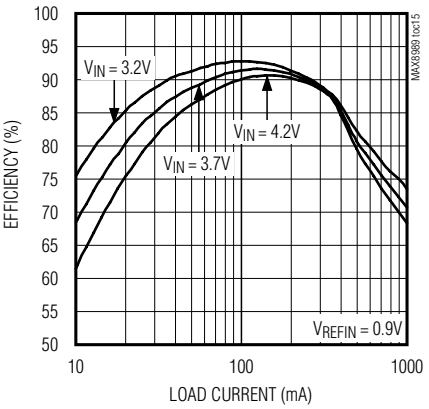
EFFICIENCY vs. OUTPUT VOLTAGE



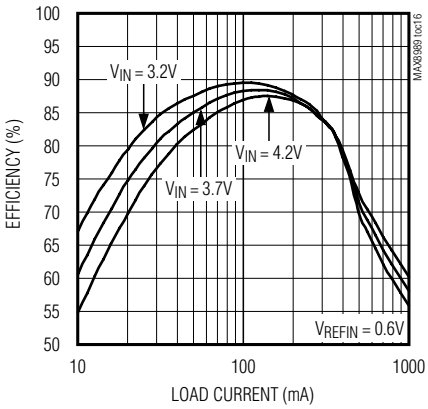
EFFICIENCY vs. LOAD CURRENT



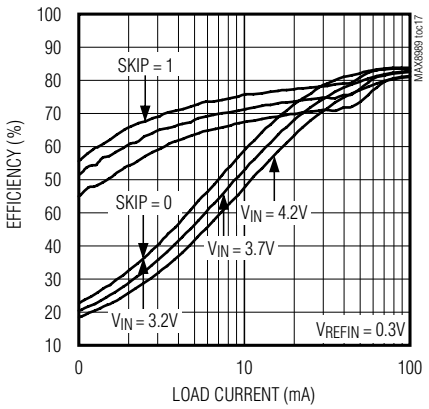
EFFICIENCY vs. LOAD CURRENT



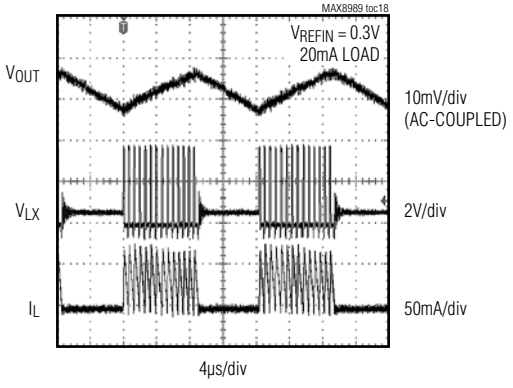
EFFICIENCY vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT



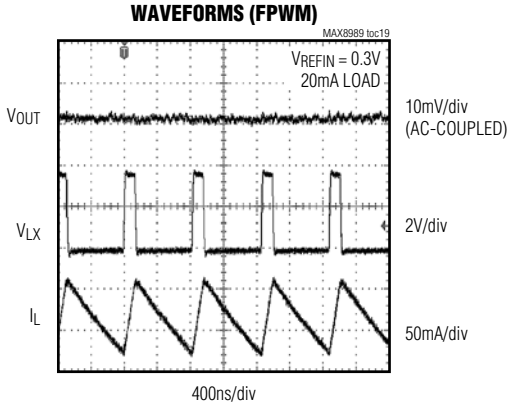
LIGHT-LOAD SWITCHING WAVEFORMS (SKIP)



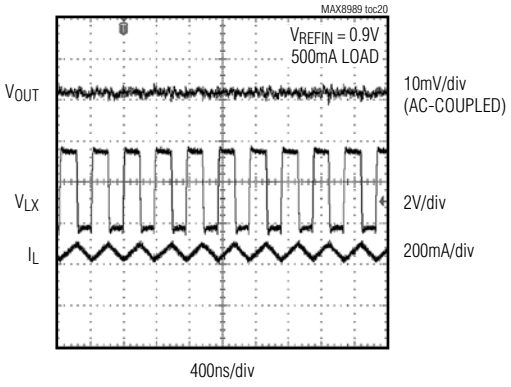
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN1} = V_{IN2} = 3.7V, **V_{REFIN} = 0.9V, L1 = 4.7µH (TOKO DFE252012C)**, T_A = +25°C, unless otherwise noted.)

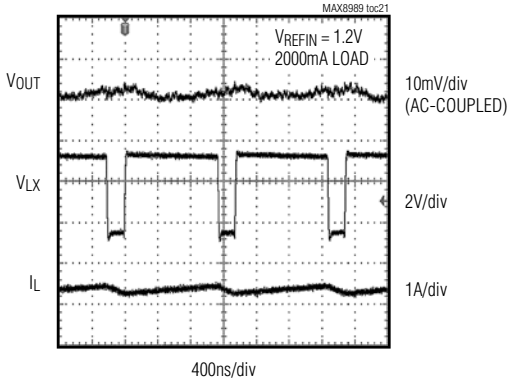
LIGHT-LOAD SWITCHING WAVEFORMS (FPWM)



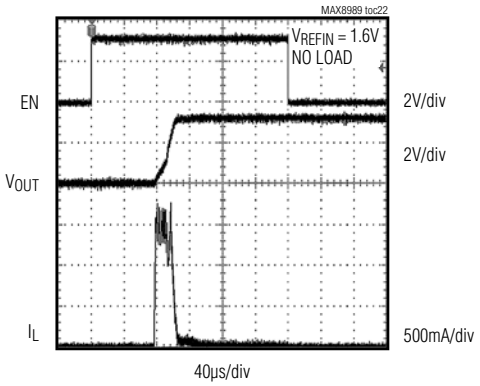
MEDIUM-LOAD SWITCHING WAVEFORMS



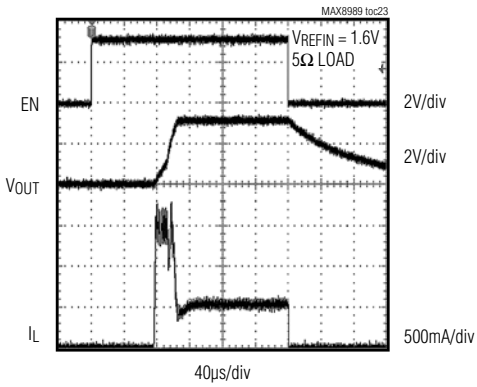
HEAVY-LOAD SWITCHING WAVEFORMS



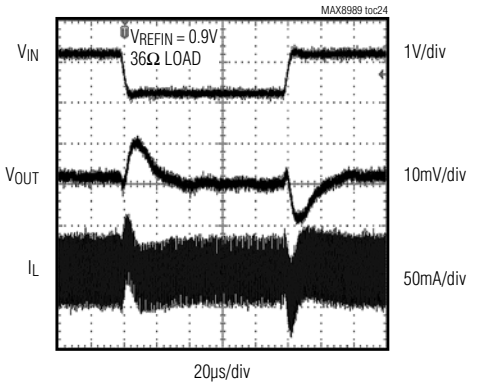
ENABLE WAVEFORMS



ENABLE WAVEFORMS



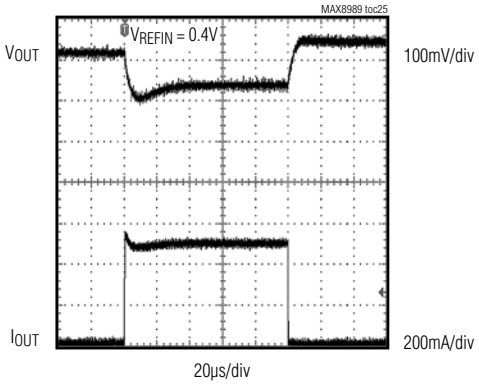
LINE TRANSIENT 4.2V TO 3.2V TO 4.2V



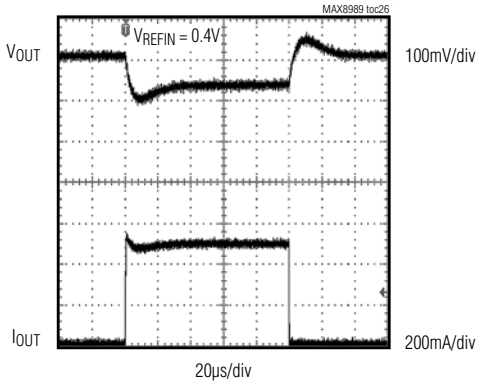
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN1} = V_{IN2} = 3.7V, **V_{REFIN} = 0.9V, L1 = 4.7µH (TOKO DFE252012C)**, T_A = +25°C, unless otherwise noted.)

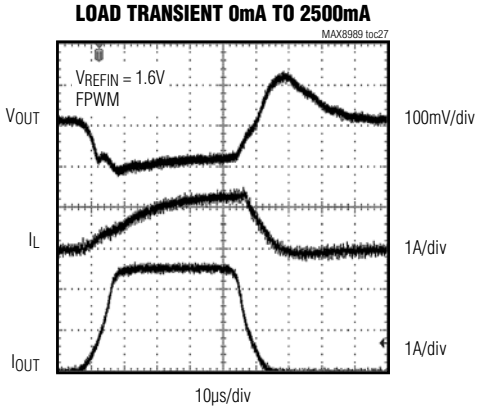
LOAD TRANSIENT 0mA TO 500mA (SKIP)



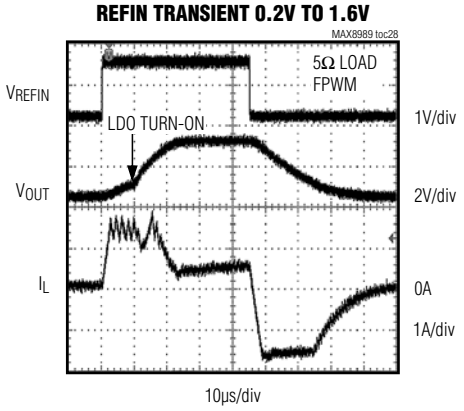
LOAD TRANSIENT 0mA TO 500mA (FPWM)



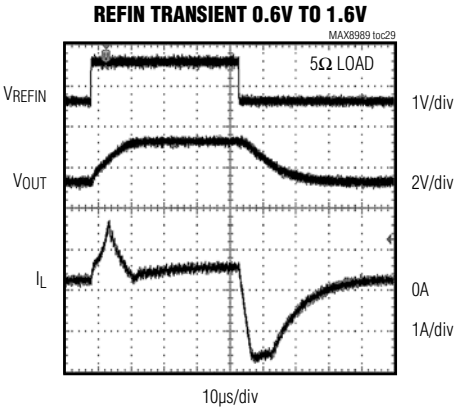
LOAD TRANSIENT 0mA TO 2500mA



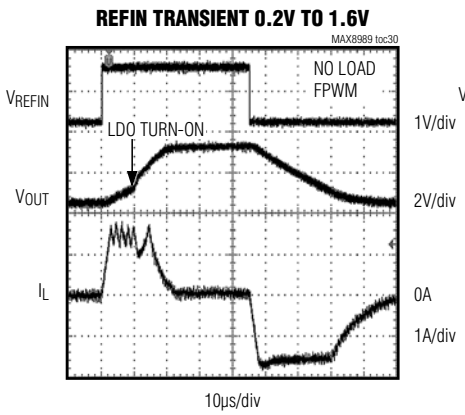
REFIN TRANSIENT 0.2V TO 1.6V



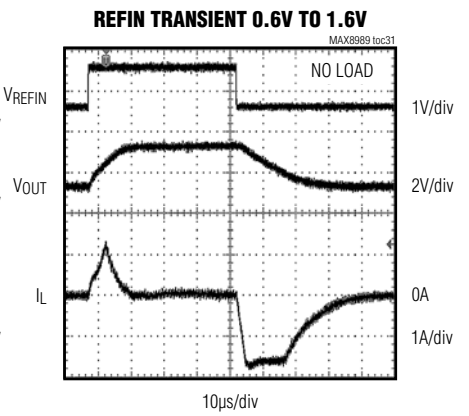
REFIN TRANSIENT 0.6V TO 1.6V



REFIN TRANSIENT 0.2V TO 1.6V



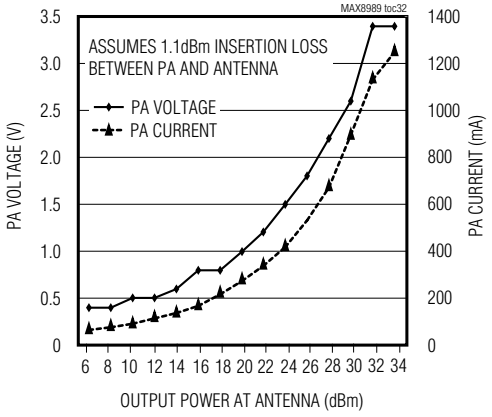
REFIN TRANSIENT 0.6V TO 1.6V



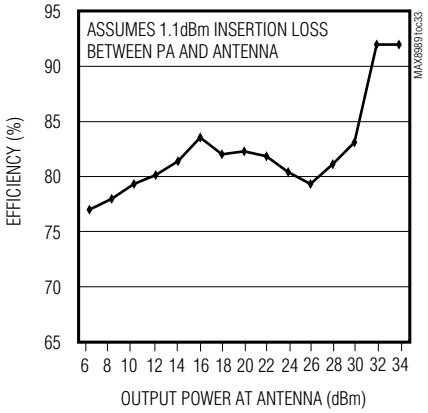
Typical Operating Characteristics

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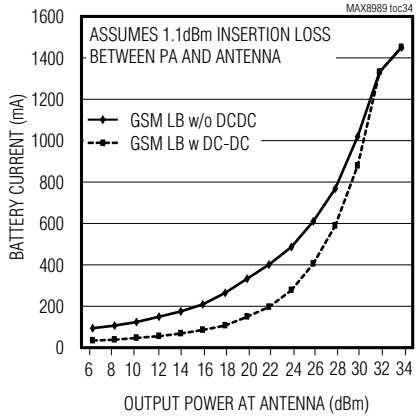
GSM LOW-BAND PA VOLTAGE/CURRENT vs. OUTPUT POWER



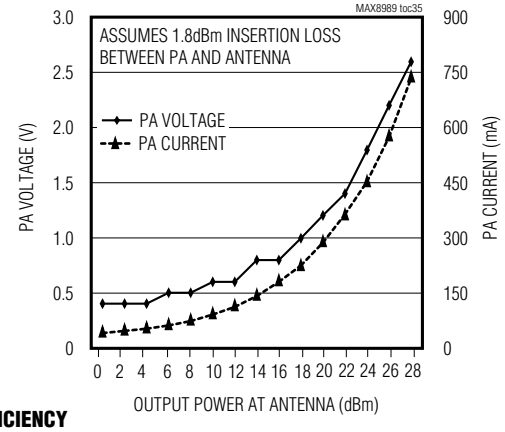
GSM LOW-BAND CONVERTER EFFICIENCY vs. OUTPUT POWER



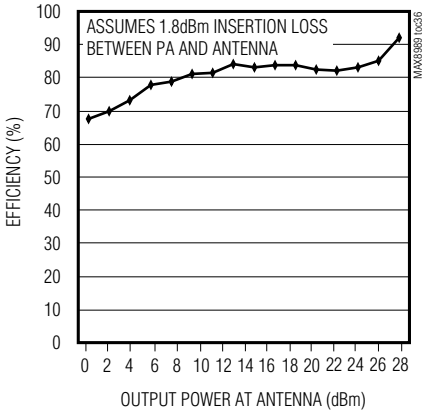
GSM LOW-BAND BATTERY CURRENT vs. OUTPUT POWER



GSM HIGH-BAND PA VOLTAGE/CURRENT vs. OUTPUT POWER



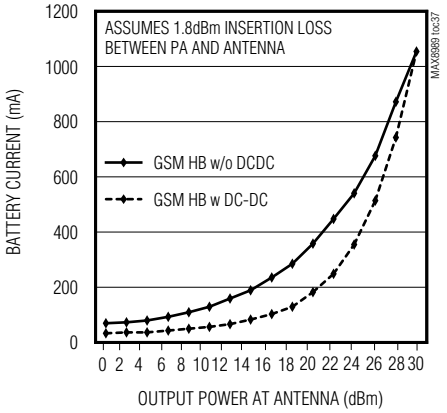
GSM HIGH-BAND CONVERTER EFFICIENCY vs. OUTPUT POWER



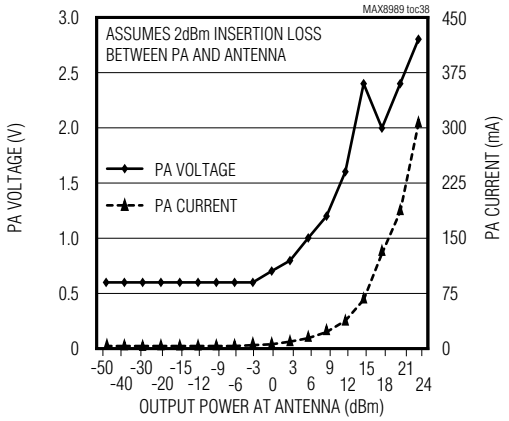
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN1} = V_{IN2} = 3.7V, T_A = +25°C, unless otherwise noted. **PA operating characteristics based on SKY77604 PA Module.**)

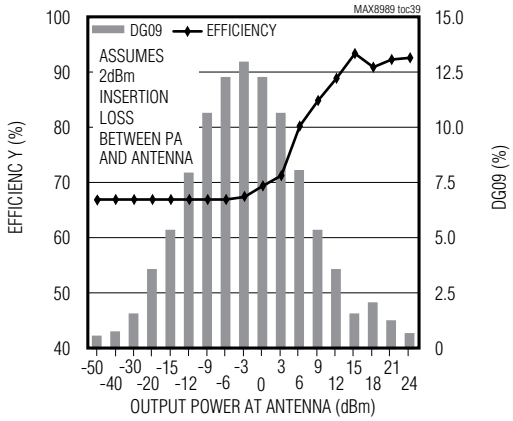
GSM HIGH-BAND BATTERY CURRENT vs. OUTPUT POWER



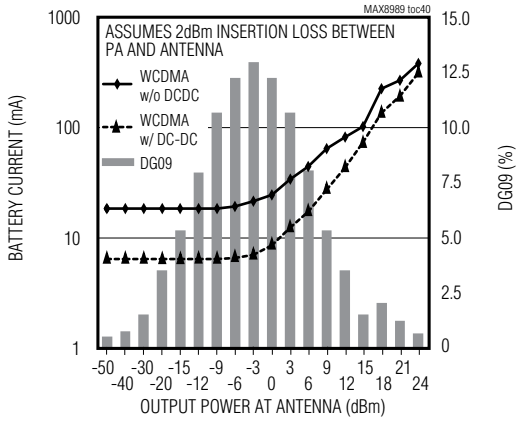
WCDMA BAND 5 PA VOLTAGE/CURRENT vs. OUTPUT POWER



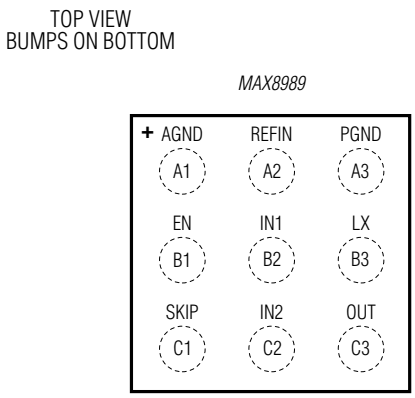
WCDMA BAND 5 PA CONVERTER EFFICIENCY vs. OUTPUT POWER



WCDMA BAND 5 BATTERY CURRENT vs. OUTPUT POWER



Bump Configuration



WLP

Bump Description

PIN	NAME	FUNCTION
A1	AGND	Low-Noise Analog Ground. Connect AGND to the ground plane at a single point away from high switching currents. See the *PCB Layout* section.
A2	REFIN	Reference Input. REFIN typically connects to the output of an external DAC used to control the IC's output voltage for continuous PA power adjustment. To improve noise immunity, bypass REFIN with a 1000pF capacitor to AGND. The output voltage regulates to 2.0 x V_{REFIN}. REFIN is pulled down to ground through an internal 800kΩ resistor.
A3	PGND	Power Ground. Connect PGND to the ground plane near the input and output capacitor grounds. See the *PCB Layout* section.
B1	EN	Enable Input. Connect EN to IN_ or logic-high for normal operation. Connect EN to ground or logic-low to shut down the output. EN is internally pulled down to ground through an 800kΩ resistor.
B2	IN1	Supply Voltage Input for the Step-Down Converter. Connect IN1 and IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN1 with a 4.7µF ceramic capacitor as close as possible between IN1 and PGND.
B3	LX	Inductor Connection
C1	SKIP	Skip Mode Enable Input. Connect SKIP to IN_ or logic-high to enable low-power skip mode during light-load operation when the output voltage is less than 1.0V. Connect SKIP to ground or logic-low for forced PWM operation.
C2	IN2	Supply Voltage Input for the Bypass LDO. Connect IN1 and IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 4.7µF ceramic capacitor as close as possible between IN2 and PGND.
C3	OUT	Output of the Linear Bypass LDO. Connect OUT to the output of the step-down converter. Bypass OUT with four 4.7µF ceramic capacitors as close as possible to OUT and PGND.

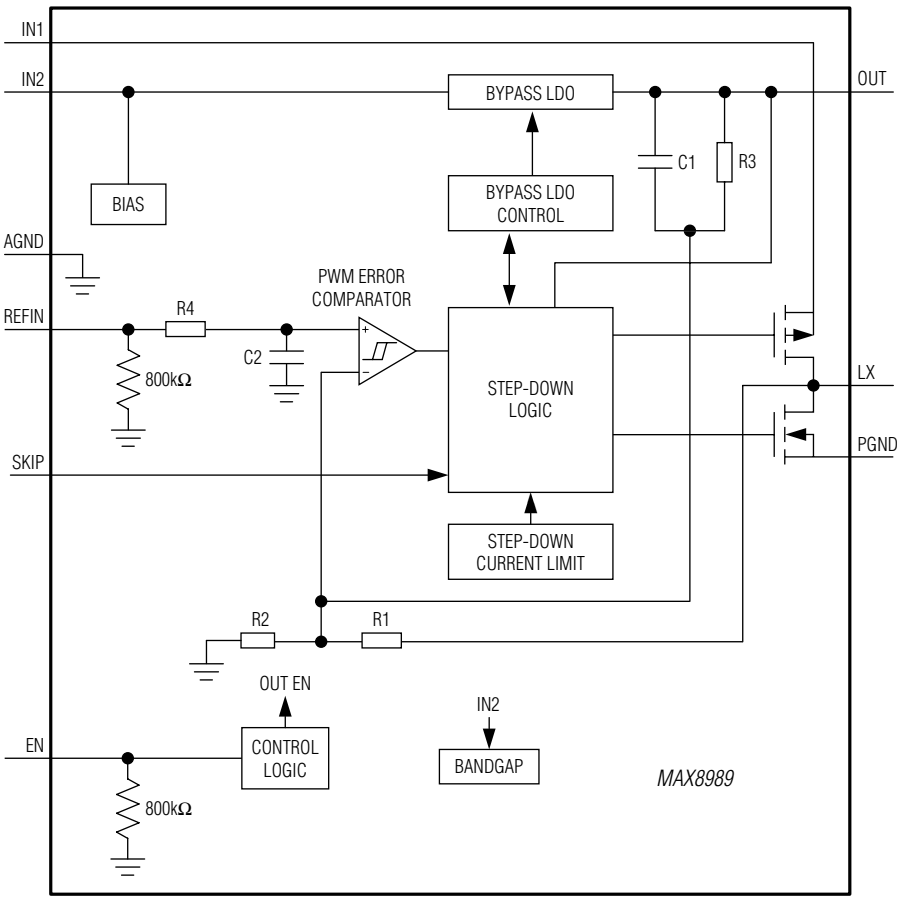


Figure 1. Functional Diagram

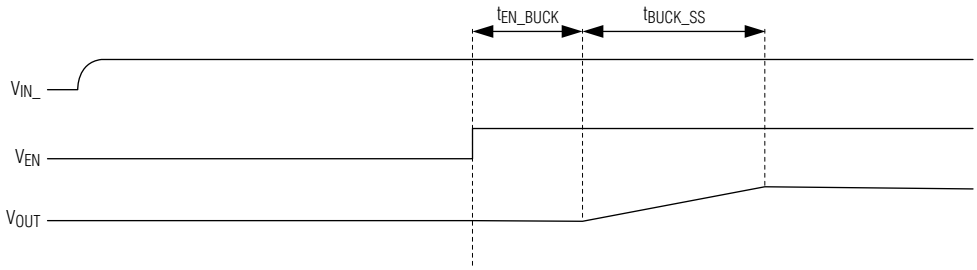


Figure 2. Power-Up Timing

Detailed Description

The MAX8989 step-down converter is optimized for powering the power amplifier (PA) in multistandard cellular handsets such as LTE, WCDMA, GSM, and EDGE. The IC integrates a high-efficiency PWM step-down converter for medium and low-power transmission with an 85mΩ (typ) bypass regulator, in parallel with the step-down converter, to power the PA during high-power transmission.

Step-Down Converter

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low output ripple, and physically tiny external components. The control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This high-side switch remains on until the minimum on-time expires and the output voltage is within regulation, or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Hysteretic control is sometimes referred to as ripple control, since voltage ripple is used to control when the high-side and low-side switches are turned on and off. To ensure stability with low ESR ceramic output capacitors, the IC combines ripple from the output with the ramp signal generated by the switching node (LX). This is seen in Figure 1 with resistor R1 and capacitor C1 providing the combined ripple signal. Injecting ramp voltage from the switching node also improves line regulation because the slope of the ramp adjusts with changes in input voltage.

Hysteretic control has a significant advantage over fixed-frequency control schemes: fast transient response. Hysteretic control uses an error comparator, instead of an error amplifier with compensation, and there is no fixed-frequency clock. Therefore, a hysteretic converter reacts virtually immediately to any load transient on the output without having to wait for a new clock pulse or for the output of the error amplifier to move as with a fixed-frequency converter.

With a fixed-frequency step-down converter, the magnitude of output voltage ripple is a function of the switching frequency, inductor value, output capacitor and ESR, and input and output voltage. Since the inductance value and switching frequency are fixed, the output ripple varies with changes in line voltage. With a hysteretic step-down converter, since the ripple voltage is essentially fixed, the switching frequency varies with changes in line voltage. Some variation with load current can also be seen, however, this is part of what gives the hysteretic converter its great transient response.

The IC is trimmed to provide a 2MHz switching frequency during 50% duty cycle condition (3.6V input and 1.8V output). See the *Typical Operating Characteristics* section for more information on how switching frequency can vary with respect to load current and supply voltage.

Voltage-Positioning Load Regulation

The IC step-down converter utilizes a unique feedback network. By taking DC feedback from the LX node through R1 of Figure 1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. To improve the load regulation, resistor R3 is included in the feedback. This configuration yields load regulation equal to half of the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients and when changing the output voltage from one level to another. However, when calculating the required REFIN voltage, the load regulation should be considered. Because inductor resistance (R_L) is typically well specified and the typical PA is a resistive load, the V_{REFIN} to V_{OUT} gain is slightly less than 2.0V/V. The output voltage is approximately:

$$V_{OUT} = 2 \times V_{REFIN} - \frac{1}{2} \times R_L \times I_{LOAD}$$

When the output voltage drops by more than 60mV (typ) due to load regulation ($0.5 \times R_L \times I_{LOAD} > 60mV$) and the output voltage is above the linear bypass threshold (1V typ), the linear bypass regulator starts to supplement current to the output ensuring that the output is kept in regulation. While the linear bypass regulator is sourcing current, the step-down converter continues to supply most of the load to maximize efficiency.

Skip Mode

The IC has an optional skip mode that provides the highest possible efficiency during light load conditions. Skip mode is active when SKIP is logic-high and V_{OUT} is less than 1V.

In addition, when the bypass LDO is sourcing current, skip mode is automatically enabled to prevent the step-down converter from sinking current in an overvoltage condition.

During skip mode, the hysteretic comparator turns on the high-side switch based on the output voltage value. Once the output voltage is high enough, the high-side switch is turned off and the low-side switch is turned on to return the inductor current to zero. A zero-crossing comparator is enabled in this mode to minimize power consumption by turning off the low-side switch as close as possible to the true inductor-current zero-crossing. In skip mode, the output ripple remains low at all loads, and the switching frequency decreases with lighter loads.

Linear Bypass and Dropout

A low-dropout linear regulator is connected in parallel with the step-down converter. The output voltage of the linear regulator is set slightly lower than the nominal regulation voltage of the step-down converter (60mV typ). This allows the output to maintain regulation when the output is slewed at a rate faster than the bandwidth of the step-down converter and when the load current exceeds the current limit of the step-down converter. Linear bypass operation is disabled when the output voltage is below the linear bypass regulation enable threshold (1V typ).

The IC enters full dropout under two conditions:

- The IC is commanded to regulate to a setting higher than V_{IN}.
- REFIN is set to more than 2.1V (min).

Under either condition, the step-down converter goes to 100% duty cycle by turning on its p-channel MOSFET, and the linear regulator enters dropout by turning on fully. Note that forced dropout mode (the second condition) does not implement hysteresis on REFIN.

Shutdown

Connect EN to ground or logic-low to place the IC in shutdown mode, reducing the input current to 0.1µA (typ). In shutdown, the control circuitry, bypass linear regulator, internal switching MOSFET, and synchronous rectifier turn off, and LX becomes high impedance. Connect EN to IN_ or logic-high for normal operation.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the IC. If the junction temperature exceeds +160°C, the IC turns off, allowing it to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Inductor Selection

The step-down converter operates with a typical switching frequency of 2MHz. A 4.7µH is recommended for best performance. The inductor's DC current rating only needs to match the maximum load of the application because the IC features zero-current overshoot during startup and load transients. See Table 1 for suggested inductors and manufacturers.

Output Capacitor Selection

The output capacitor keeps the output voltage ripple small and ensures regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided. Tantalum capacitors are not recommended.

Four 4.7µF output capacitors are recommended for most applications. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased, however, care should be taken with regards to output voltage slew rate requirements.

Input Capacitor Selection

The input capacitors reduce the current peaks drawn from the battery or input power source and reduce switching noise in the IC. The impedance of C_{IN1} and C_{IN2} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided.

For most applications, connect a 4.7µF capacitor from IN1 to PGND and a 4.7µF capacitor from IN2 to PGND. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

Table 1. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	R_L (mΩ typ)	CURRENT RATING (mA)	DIMENSIONS (mm max)
TOKO	DEM2810C	4.7	170	1000	3.0 x 3.2 x 1.0
	DFE252010C	4.7	320	1600	2.7 x 2.2 x 1.0
	DFE252012C	4.7	210	1600	2.7 x 2.2 x 1.2
TDK	VLF302510	4.7	140	950	3.0 x 2.5 x 1.0
	VLS252010T	4.7	367	980	2.6 x 2.1 x 1.0
Samsung	CIG22H4R7MNE	4.7	233	1000	2.7 x 2.2 x 1.2

Thermal Considerations

In applications where the IC runs at high ambient temperatures or with heavy loads, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately +160°C, the thermal overload protection is activated.

The IC maximum power dissipation depends on the thermal resistance of the package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

where T_A is the ambient temperature, T_{JMAX} is the maximum junction temperature, and θ_{JA} is the junction to ambient thermal resistance. See the *Absolute Maximum Ratings* section.

The power dissipated in the device is approximately:

$$P_D = V_{OUT} \times I_{LOAD} \times \left(\frac{1}{\eta} - 1\right) - \left(I_L^2 \times R_L\right)$$

where η is the efficiency of the MAX8989 (see the *Typical Operating Characteristics* section), I_{LOAD} is the RMS load current, I_L is the RMS inductor current, and R_L is the inductor resistance.

PCB Layout

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, resulting in a stable and well-regulated output.

For the input supplies, it is critical to route them as separate lines from the power source with separate decoupling capacitors on IN1 and IN2. This is necessary to prevent switching noise on IN1 from coupling into IN2.

Grounding of the IC is also critical. The AGND and PGND must be routed as separate nets, and connected together as close as possible to the PGND bump of the IC. AGND can be used to shield REFIN along its routing. AGND must be connected to the ground of the source generating REFIN. To avoid noise coupling into AGND, care must be taken in the layout to ensure isolation from AGND to PGND, having cuts in the ground plane wherever necessary.

The input decoupling capacitor on IN1 filters the input supply of the step-down converter. The layout needs to ensure as short a path as possible from IN1, through C_{IN1}, to PGND for optimal decoupling. The point in the layout where this input capacitor connects to PGND serves as the star-connection ground point for all three critical capacitors (C_{IN1}, C_{IN2}, and C_{OUT}).

The input decoupling capacitor on IN2 filters the input supply for the linear regulator. Its bottom plate should be routed to the star-ground point in the layout.

The OUT trace needs to be short and wide because it carries the current from the linear regulator.

The trace between the inductor and LX should also be low impedance as this trace has a noisy, switching waveform. Keep LX away from noise-sensitive traces such as REFIN and AGND.

The capacitor from REFIN to AGND is optional. The REFIN capacitor can be used when needed to prevent high-frequency noise from coupling into REFIN.

The ground connection among CIN, COUT, and the PA ground is also extremely critical. Parasitic impedance in this ground connection results in degraded RF performance. Contact your Maxim representative for more detailed information and assistance.

For a PCB layout example, refer to the MAX8989 Evaluation Kit data sheet.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91B1+1	21-0067	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/10	Initial release	—
1	1/11	Updated IN1, IN2, OUT, LX current absolute maximum rating	2

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