

N-channel 950 V, 0.120 Ω typ., 38 A, MDmesh™ DK5
Power MOSFETs in TO-247 and TO-247 long leads packages

Datasheet - production data

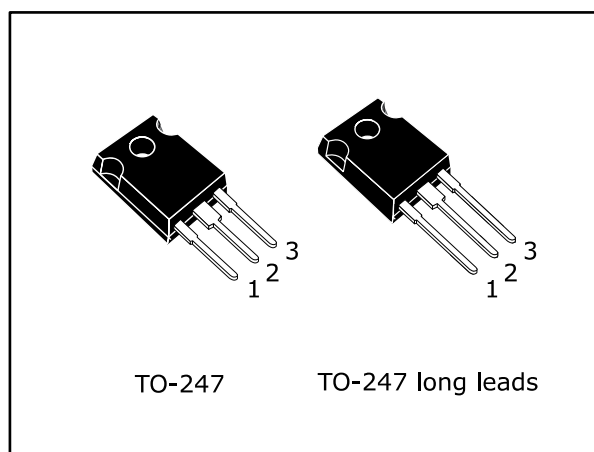
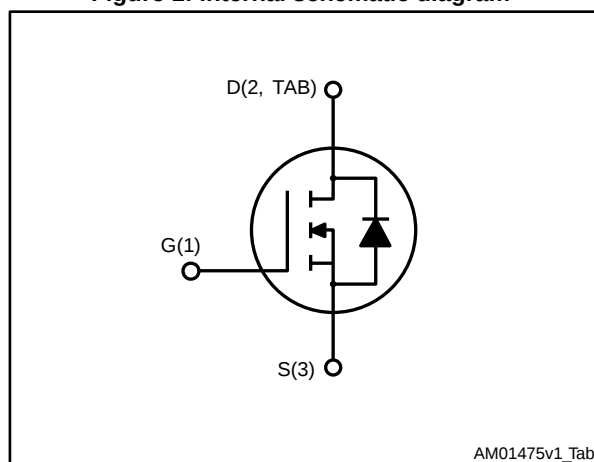


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STW40N95DK5	950 V	0.130 Ω	38 A
STWA40N95DK5			

- Fast-recovery body diode
- Best R_{DS(on)} x area
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are part of the MDmesh™ DK5 fast recovery diode series. The MDmesh™ DK5 combines very low recovery charge (Q_{rr}) and recovery time (t_{rr}) with an excellent improvement in R_{DS(on)} * area and one of the most effective switching behaviors, ideal for half bridge and full bridge converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW40N95DK5	40N95DK5	TO-247	Tube
STWA40N95DK5		TO-247 long leads	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	38	V
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	24	A
$I_{DM}^{(1)}$	Drain current (pulsed)	152	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

(1) Pulse width limited by safe operating area

(2) $I_{SD} \leq 19\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 475\text{ V}$ (3) $V_{DS} \leq 760\text{ V}$

Table 3: Avalanche characteristics

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.28	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^{\circ}\text{C}/\text{W}$

Table 4: Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche	13	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 13\text{ A}$, $V_{DD} = 50\text{ V}$)	730	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	950			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 950 V			1	μA
		V _{GS} = 0 V, V _{DS} = 950 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate source leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DD} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 19 A		0.120	0.130	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	3480	-	pF
C _{oss}	Output capacitance		-	235	-	pF
C _{rss}	Reverse transfer capacitance		-	2.3	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0 V, V _{DS} = 0 to 760 V	-	371	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	134	-	pF
R _g	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	2	-	Ω
Q _g	Total gate charge	V _{DD} = 760 V, I _D = 38 A, V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	100	-	nC
Q _{gs}	Gate source charge		-	19.5	-	nC
Q _{gd}	Gate drain charge		-	67.6	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 475 \text{ V}$, $I_D = 19 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 14: "Test circuit for resistive load switching times")	-	30	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	82	-	ns
t_f	Fall time		-	11	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 19 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	170		ns
Q_{rr}	Reverse recovery charge		-	1.4		μC
I_{RRM}	Reverse recovery current		-	15		A
t_{rr}	Reverse recovery time	$I_{SD} = 19 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ } ^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	340		ns
Q_{rr}	Reverse recovery charge		-	5		μC
I_{RRM}	Reverse recovery current		-	30		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Forward bias safe operating area

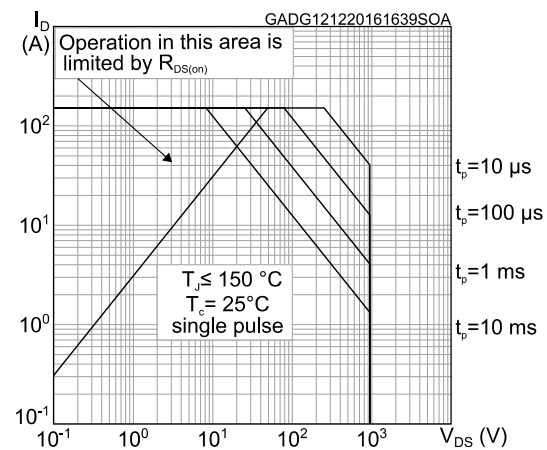


Figure 3: Thermal impedance

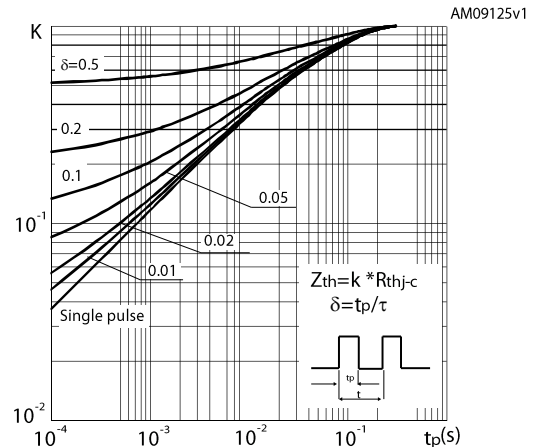


Figure 4: Output characteristics

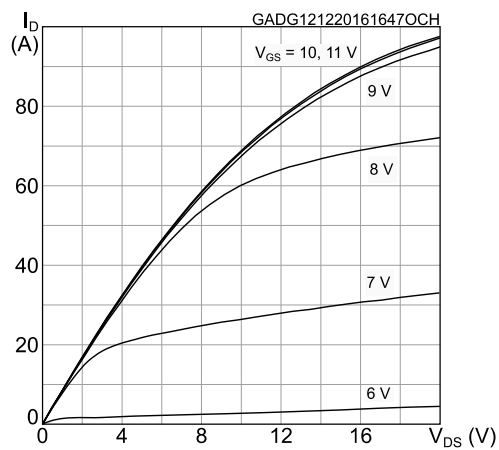


Figure 5: Transfer characteristics

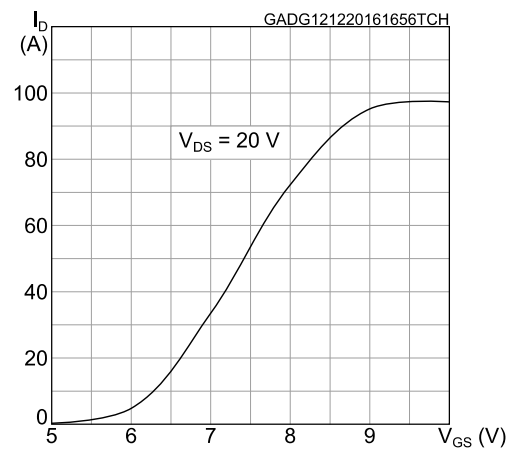


Figure 6: Gate charge vs gate-source voltage

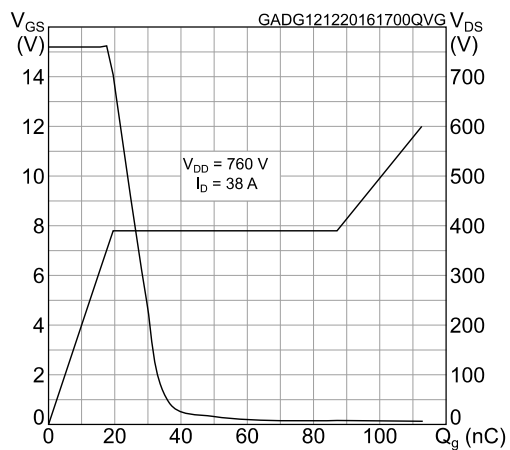


Figure 7: Static drain-source on-resistance

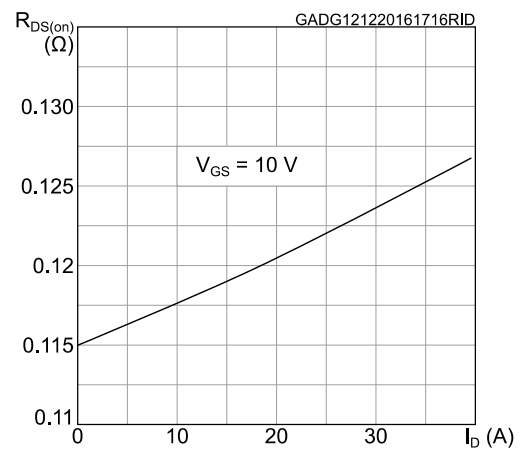


Figure 8: Capacitance variations

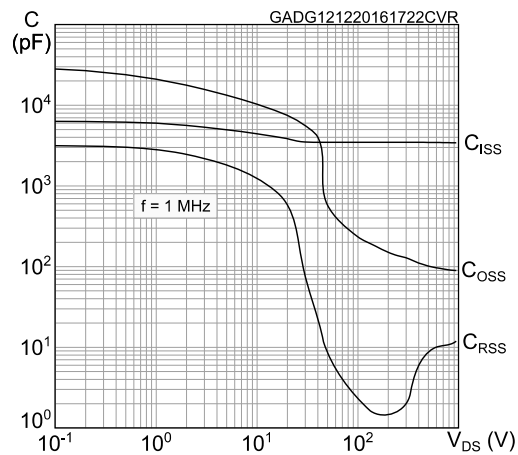


Figure 9: Normalized gate threshold voltage vs temperature

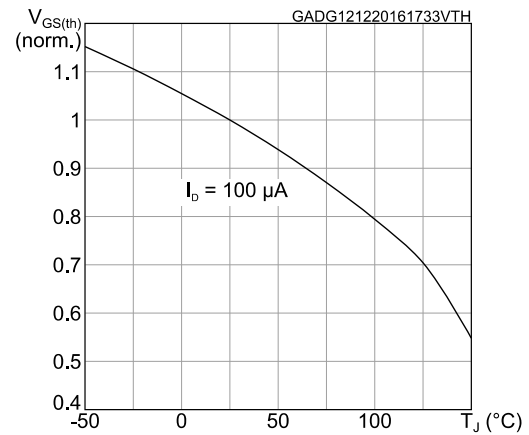


Figure 10: Normalized on-resistance vs temperature

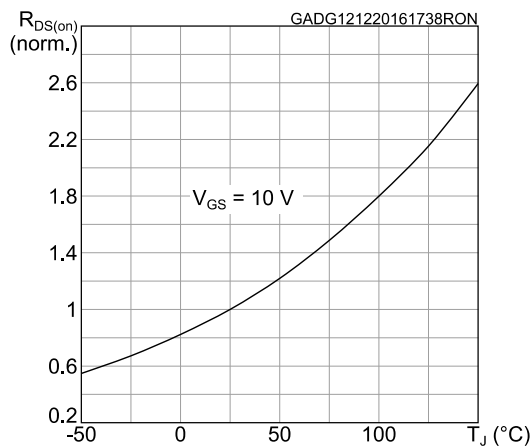
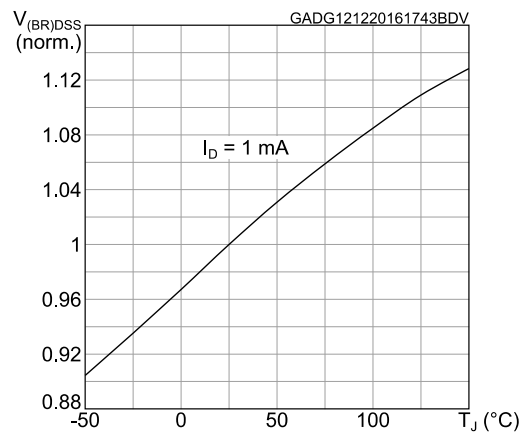
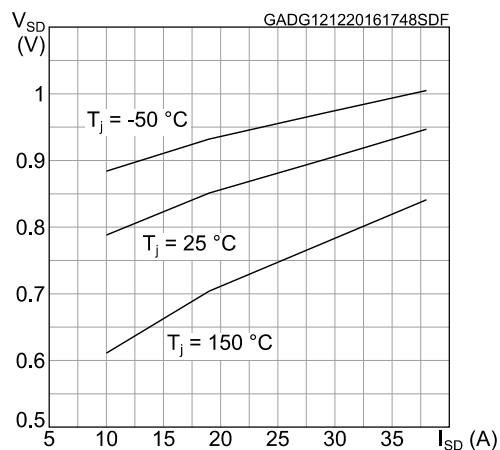
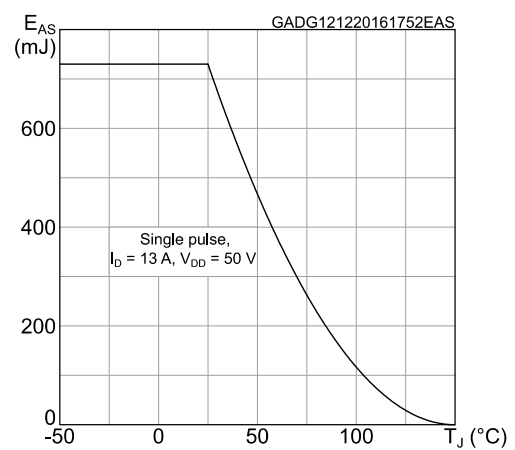
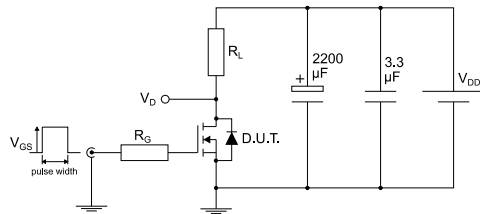
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics

Figure 13: Maximum avalanche energy vs starting T_J 

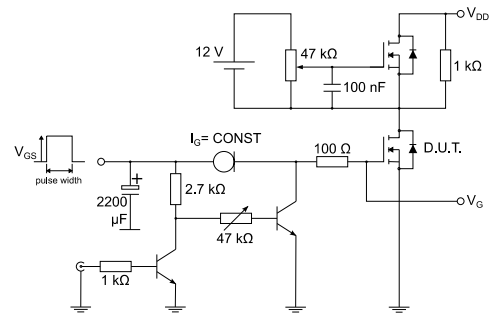
3 Test circuits

Figure 14: Test circuit for resistive load switching times



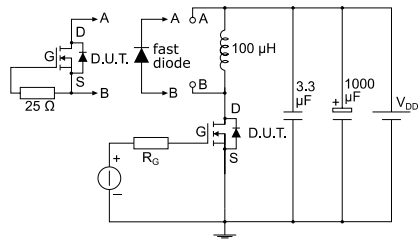
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Figure 15: Test circuit for gate charge behavior



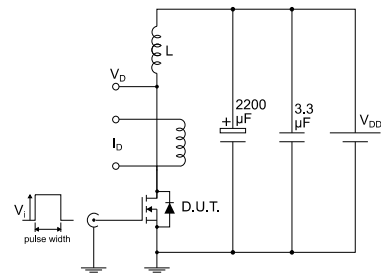
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Figure 16: Test circuit for inductive load switching and diode recovery times



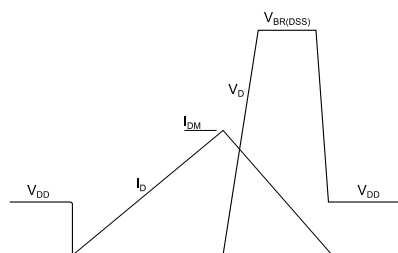
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Figure 17: Unclamped inductive load test circuit



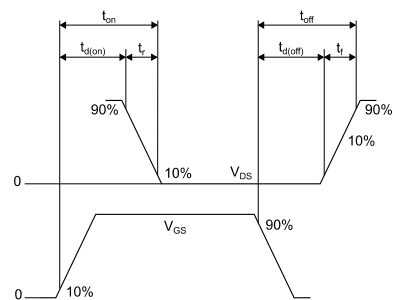
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



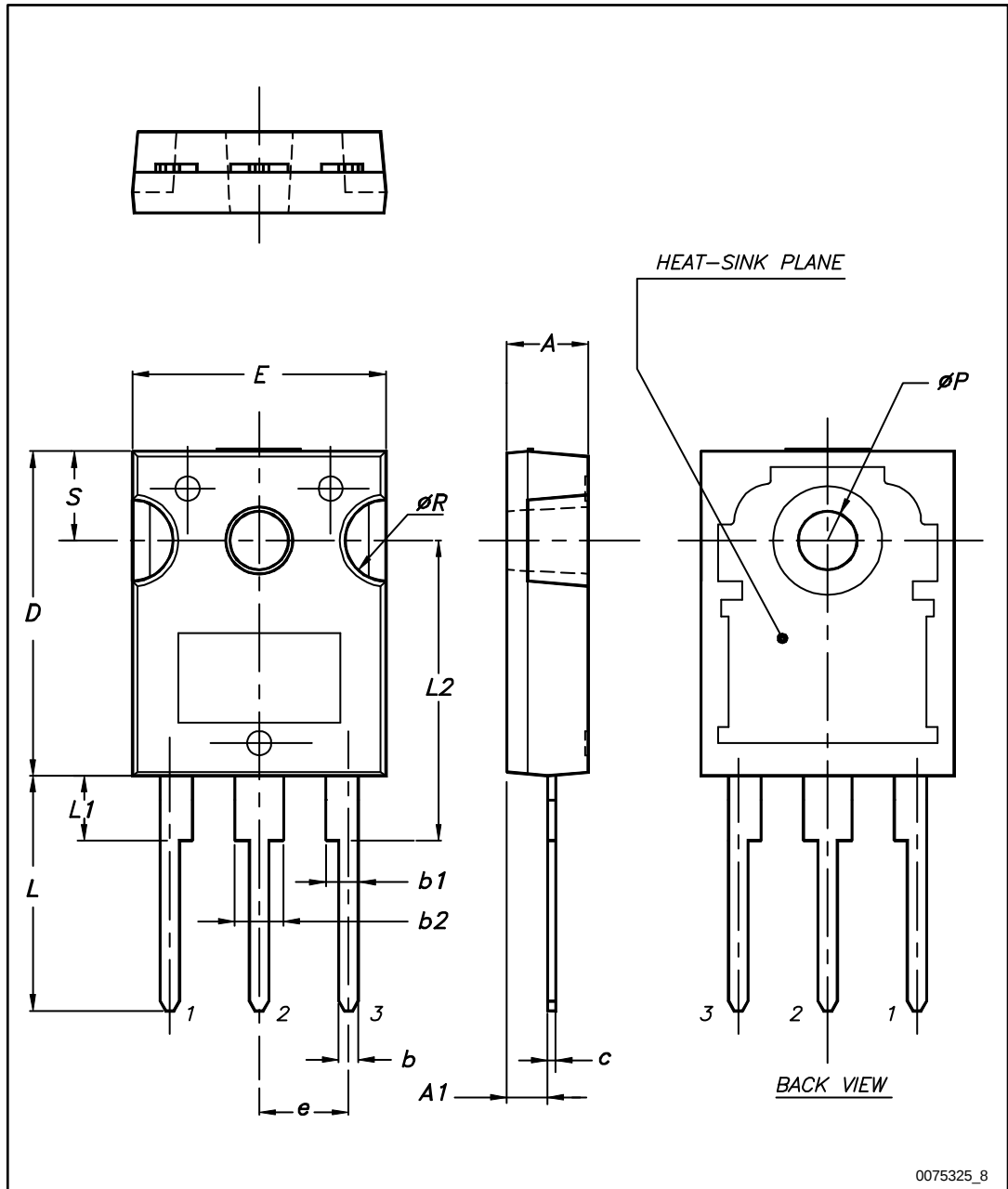
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline



0075325_8

Table 9: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.2 TO-247 long leads package information

Figure 21: TO-247 long lead package outline

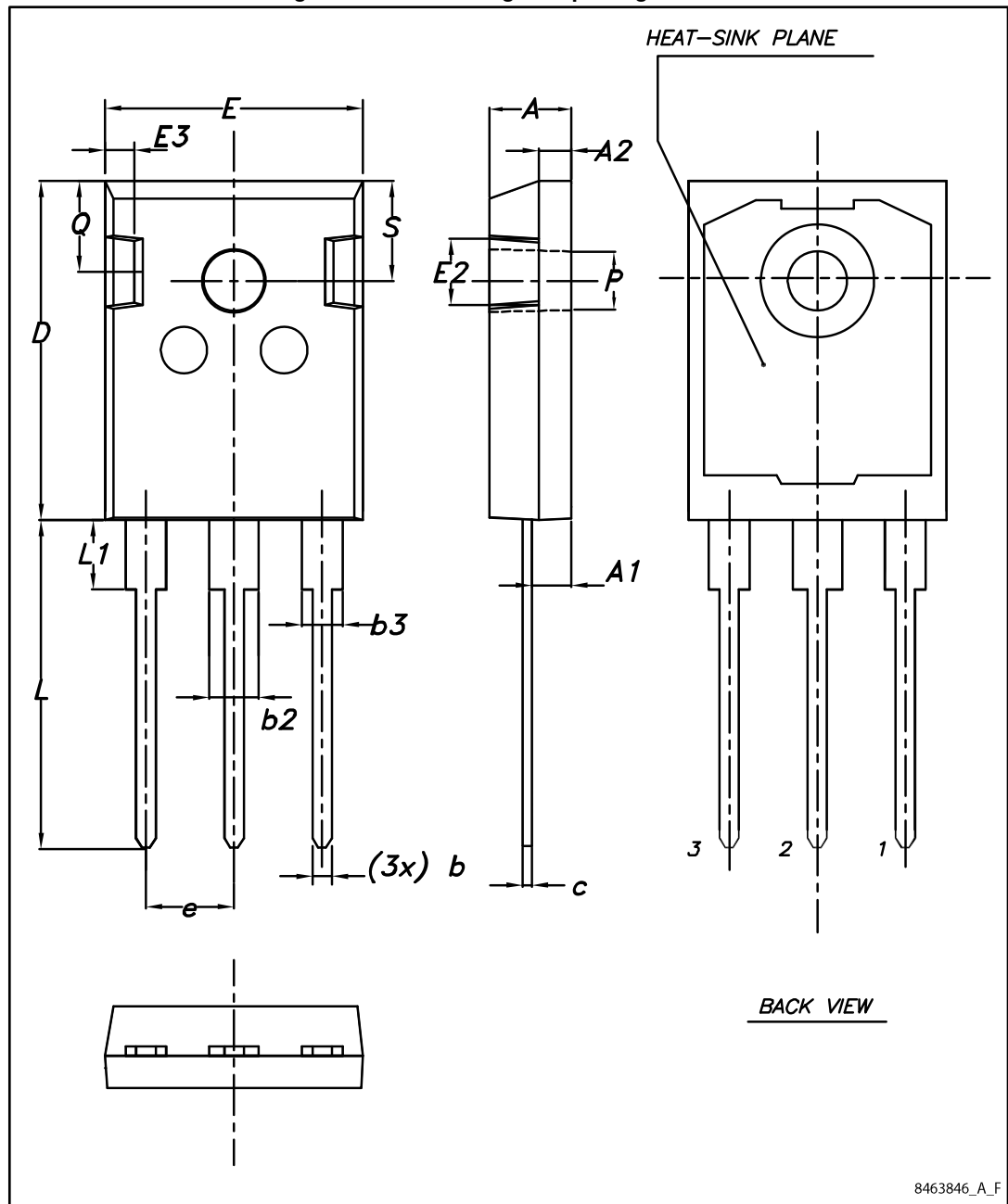


Table 10: TO-247 long lead package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
19-Sep-2013	1	First release.
13-Nov-2015	2	Updated title, features and description in cover page. Updated Section 10 : "Electrical characteristics" and Section 12.1:"TO-247 package information" Minor text changes.
12-Apr-2016	3	Updated title,silhouette and description in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> . Updated <i>Section 10: "Electrical characteristics"</i> . Added <i>Figure 21: "TO-247 long lead package outline"</i> . Minor text changes
15-Dec-2016	4	Datasheet status promoted from preliminary to production data. Updated document title on cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "Thermal data"</i> , <i>Table 5: "On/off states"</i> , <i>Table 6: "Dynamic"</i> and <i>Table 8: "Source-drain diode"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes

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