# PIC32MX5XX/6XX/7XX

## 32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet

### Operating Conditions

- 2.3V to 3.6V, -40ºC to +105ºC, DC to 80 MHz

### Core: 80 MHz/105 DMIPS MIPS32® M4K®

- MIPS16e® mode for up to 40% smaller code size
- Code-efficient (C and Assembly) architecture
- Single-cycle (MAC) 32x16 and two-cycle 32x32 multiply

### Clock Management

- 0.9% internal oscillator (on some variants)
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer
- Fast wake-up and start-up

### Power Management

- Low-power management modes (Sleep and Idle)
- Integrated Power-on Reset, Brown-out Reset
- 0.5 mA/MHz dynamic current (typical)
- 41 µA IPD current (typical)

### Graphics Features

- External graphics interface with up to 34 Parallel Master Port (PMP) pins:
  - Interface to external graphics controller
  - Capable of driving LCD directly with DMA and internal or external memory

### Analog Features

- ADC Module:
  - 10-bit 1 Msps rate with one Sample and Hold (S&H)
  - 16 analog inputs
  - Can operate during Sleep mode
- Flexible and independent ADC trigger sources
- Comparators:
  - Two dual-input Comparator modules
  - Programmable references with 32 voltage points

### Timers/Output Compare/Input Capture

- Five General Purpose Timers:
  - Five 16-bit and up to two 32-bit Timers/Counters
- Five Output Compare (OC) modules
- Five Input Capture (IC) modules
- Real-Time Clock and Calendar (RTCC) module

### Communication Interfaces

- USB 2.0-compliant Full-Speed OTG controller
- 10/100 Mbps Ethernet MAC with MII and RMII interface
- CAN module:
  - 2.0B Active with DeviceNet™ addressing support
- Six UART modules (20 Mbps):
  - Supports LIN 2.1 protocols and IrDA® support
- Up to four 4-wire SPI modules (25 Mbps)
- Up to five $I^2C$ modules (up to 1 Mbaud) with SMBus support
- Parallel Master Port (PMP)

### Direct Memory Access (DMA)

- Up to eight channels of hardware DMA with automatic data size detection
- 32-bit Programmable Cyclic Redundancy Check (CRC)
- Six additional channels dedicated to USB, Ethernet and CAN modules

### Input/Output

- 15 mA or 10 mA source/sink for standard $V_{OH}/V_{OL}$ and up to 22 mA for non-standard $V_{OH1}$
- 5V-tolerant pins
- Selectable open drain and pull-ups
- External interrupts

### Class B Support

- Class B Safety Library, IEC 60730

### Debugger Development Support

- In-circuit and in-application programming
- 4-wire MIPS® Enhanced JTAG interface
- Unlimited program and six complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan

### Packages

| Type | QFN | TQFP | | | TFBGA | VTLA |
|---|---|---|---|---|---|---|
| Pin Count | 64 | 64 | 100 | 100 | 121 | 124 |
| I/O Pins (up to) | 51 | 51 | 83 | 83 | 83 | 83 |
| Contact/Lead Pitch | 0.50 | 0.50 | 0.40 | 0.50 | 0.80 | 0.50 |
| Dimensions | 9x9x0.9 | 10x10x1 | 12x12x1 | 14x14x1 | 10x10x1.1 | 9x9x0.9 |

**Note:** All dimensions are in millimeters (mm) unless specified.

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**TABLE 1: PIC32MX5XX USB AND CAN FEATURES**

| USB and CAN | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Pins | Program Memory (KB) | Data Memory (KB) | USB | CAN | Timers/Capture/Compare | DMA Channels (Programmable/Dedicated) | UART(2,3) | SPI(3) | $I^2C$(3) | 10-bit 1 Msps ADC (Channels) | Comparators | PMP/PSP | JTAG | Trace | Packages(4) |
| PIC32MX534F064H | 64 | 64 + 12(1) | 16 | 1 | 1 | 5/5/5 | 4/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX564F064H | 64 | 64 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX564F128H | 64 | 128 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX575F256H | 64 | 256 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX575F512H | 64 | 512 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX534F064L | 100 | 64 + 12(1) | 16 | 1 | 1 | 5/5/5 | 4/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX564F064L | 100 | 64 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX564F128L | 100 | 128 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX575F256L | 100 | 256 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX575F512L | 100 | 512 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |

**Legend:** PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA(5)

**Note 1:** This device features 12 KB boot Flash memory.

**2:** CTS and RTS pins may not be available for all UART modules. Refer to the **"Device Pin Tables"** section for more information.

**3:** Some pins between the UART, SPI and $I^2C$ modules may be shared. Refer to the **"Device Pin Tables"** section for more information.

**4:** Refer to **34.0 "Packaging Information"** for more information.

**5:** 100-pin devices in the VTLA package are available upon request. Please contact your local Microchip Sales Office for details.


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**TABLE 2: PIC32MX6XX USB AND ETHERNET FEATURES**

| USB and Ethernet | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Pins | Program Memory (KB) | Data Memory (KB) | USB | Ethernet | Timers/Capture/Compare | DMA Channels (Programmable/Dedicated) | UART(2,3) | SPI(3) | I2C(3) | 10-bit 1 Msps ADC (Channels) | Comparators | PMP/PSP | JTAG | Trace | Packages(4) |
| PIC32MX664F064H | 64 | 64 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX664F128H | 64 | 128 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX675F256H | 64 | 256 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX675F512H | 64 | 512 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX695F512H | 64 | 512 + 12(1) | 128 | 1 | 1 | 5/5/5 | 8/4 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX664F064L | 100 | 64 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX664F128L | 100 | 128 + 12(1) | 32 | 1 | 1 | 5/5/5 | 4/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX675F256L | 100 | 256 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX675F512L | 100 | 512 + 12(1) | 64 | 1 | 1 | 5/5/5 | 8/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG, TL |
| PIC32MX695F512L | 100 | 512 + 12(1) | 128 | 1 | 1 | 5/5/5 | 8/4 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG, TL |

**Legend:** PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA(5)

**Note 1:** This device features 12 KB boot Flash memory.

**2:** CTS and RTS pins may not be available for all UART modules. Refer to the **"Device Pin Tables"** section for more information.

**3:** Some pins between the UART, SPI and $I^2C$ modules may be shared. Refer to the **"Device Pin Tables"** section for more information.

**4:** Refer to **34.0 "Packaging Information"** for more information.

**5:** 100-pin devices other than those listed here are available in the VTLA package upon request. Please contact your local Microchip Sales Office for details.

**TABLE 3: PIC32MX7XX USB, ETHERNET, AND CAN FEATURES**

| USB, Ethernet, and CAN | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Pins | Program Memory (KB) | Data Memory (KB) | USB | Ethernet | CAN | Timers/Capture/Compare | DMA Channels (Programmable/Dedicated) | UART(2,3) | SPI(3) | I²C(3) | 10-bit 1 Msps ADC (Channels) | Comparators | PMP/PSP | JTAG | Trace | Packages(4) |
| PIC32MX764F128H | 64 | 128 + 12(1) | 32 | 1 | 1 | 1 | 5/5/5 | 4/8 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX775F256H | 64 | 256 + 12(1) | 64 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX775F512H | 64 | 512 + 12(1) | 64 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX795F512H | 64 | 512 + 12(1) | 128 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 3 | 4 | 16 | 2 | Yes | Yes | No | PT, MR |
| PIC32MX764F128L | 100 | 128 + 12(1) | 32 | 1 | 1 | 1 | 5/5/5 | 4/6 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX775F256L | 100 | 256 + 12(1) | 64 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX775F512L | 100 | 512 + 12(1) | 64 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG |
| PIC32MX795F512L | 100 | 512 + 12(1) | 128 | 1 | 1 | 2 | 5/5/5 | 8/8 | 6 | 4 | 5 | 16 | 2 | Yes | Yes | Yes | PT, PF, BG, TL |

**Legend:** PF, PT = TQFP MR = QFN BG = TFBGA TL = VTLA(5)

**Note 1:** This device features 12 KB boot Flash memory.

**2:** CTS and RTS pins may not be available for all UART modules. Refer to the **"Device Pin Tables"** section for more information.

**3:** Some pins between the UART, SPI and I²C modules may be shared. Refer to the **"Device Pin Tables"** section for more information.

**4:** Refer to **Section 34.0 "Packaging Information"** for more information.

**5:** 100-pin devices other than those listed here are available in the VTLA package upon request. Please contact your local Microchip Sales Office for details.


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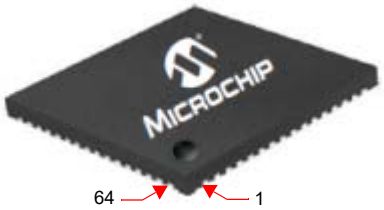
## Device Pin Tables

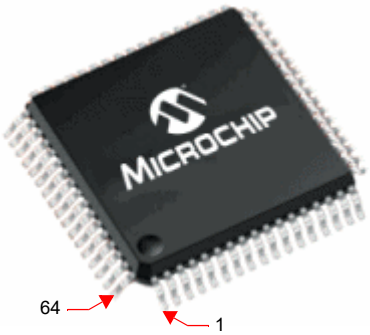
### TABLE 4: PIN NAMES FOR 64-PIN USB AND CAN DEVICES

**64-PIN QFN(2) AND TQFP (TOP VIEW)**

**PIC32MX534F064H**
**PIC32MX564F064H**
**PIC32MX564F128H**
**PIC32MX575F256H**
**PIC32MX575F512H**




QFN(2)




TQFP

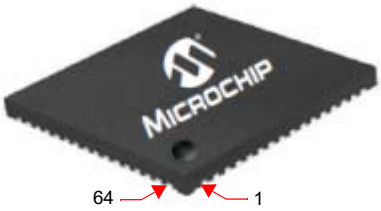
| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PMD5/RE5 | 33 | USBID/RF3 |
| 2 | PMD6/RE6 | 34 | VBUS |
| 3 | PMD7/RE7 | 35 | VUSB3V3 |
| 4 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 36 | D-/RG3 |
| 5 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 37 | D+/RG2 |
| 6 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 38 | VDD |
| 7 | MCLR | 39 | OSC1/CLKI/RC12 |
| 8 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | Vss |
| 10 | VDD | 42 | RTCC/IC1/INT1/RD8 |
| 11 | AN5/C1IN+/VBUSON/CN7/RB5 | 43 | SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 |
| 12 | AN4/C1IN-/CN6/RB4 | 44 | SCL1/IC3/PMCS2/PMA15/INT3/RD10 |
| 13 | AN3/C2IN+/CN5/RB3 | 45 | IC4/PMCS1/PMA14/INT4/RD11 |
| 14 | AN2/C2IN-/CN4/RB2 | 46 | OC1/INT0/RD0 |
| 15 | PGEC1/AN1/VREF-/CVREF-/CN3/RB1 | 47 | SOSCI/CN1/RC13 |
| 16 | PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0 | 48 | SOSCO/T1CK/CN0/RC14 |
| 17 | PGEC2/AN6/OCFA/RB6 | 49 | SCK3/U4TX/U1RTS/OC2/RD1 |
| 18 | PGED2/AN7/RB7 | 50 | SDA3/SDI3/U1RX/OC3/RD2 |
| 19 | AVDD | 51 | SCL3/SDO3/U1TX/OC4/RD3 |
| 20 | AVSS | 52 | OC5/IC5/PMWR/CN13/RD4 |
| 21 | AN8/SS4/U5RX/U2CTS/C1OUT/RB8 | 53 | PMRD/CN14/RD5 |
| 22 | AN9/C2OUT/PMA7/RB9 | 54 | CN15/RD6 |
| 23 | TMS/AN10/CVREFOUT/PMA13/RB10 | 55 | CN16/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C1RX/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | C1TX/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | PMD0/RE0 |
| 29 | AN14/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14 | 61 | PMD1/RE1 |
| 30 | AN15/OCFB/PMALL/PMA0/CN12/RB15 | 62 | PMD2/RE2 |
| 31 | AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4 | 63 | PMD3/RE3 |
| 32 | AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5 | 64 | PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.
**2:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

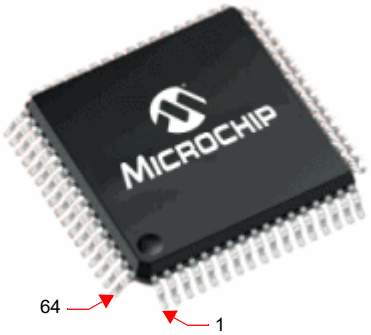
**TABLE 5: PIN NAMES FOR 64-PIN USB AND ETHERNET DEVICES**

**64-PIN QFN(2) AND TQFP (TOP VIEW)**

**PIC32MX664F064H**
**PIC32MX664F128H**
**PIC32MX675F256H**
**PIC32MX675F512H**
**PIC32MX695F512H**




**QFN(2)**




**TQFP**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | ETXEN/PMD5/RE5 | 33 | USBID/RF3 |
| 2 | ETXD0/PMD6/RE6 | 34 | VBUS |
| 3 | ETXD1/PMD7/RE7 | 35 | VUSB3V3 |
| 4 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 36 | D-/RG3 |
| 5 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 37 | D+/RG2 |
| 6 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 38 | VDD |
| 7 | MCLR | 39 | OSC1/CLKI/RC12 |
| 8 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | Vss |
| 10 | VDD | 42 | RTCC/AERXD1/ETXD3/IC1/INT1/RD8 |
| 11 | AN5/C1IN+/VBUSON/CN7/RB5 | 43 | AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 |
| 12 | AN4/C1IN-/CN6/RB4 | 44 | ECOL/AECRSDV/SCL1/IC3/PMCS2/PMA15/INT3/RD10 |
| 13 | AN3/C2IN+/CN5/RB3 | 45 | ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11 |
| 14 | AN2/C2IN-/CN4/RB2 | 46 | OC1/INT0/RD0 |
| 15 | PGEC1/AN1/VREF-/CVREF-/CN3/RB1 | 47 | SOSCI/CN1/RC13 |
| 16 | PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0 | 48 | SOSCO/T1CK/CN0/RC14 |
| 17 | PGEC2/AN6/OCFA/RB6 | 49 | EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1 |
| 18 | PGED2/AN7/RB7 | 50 | SDA3/SDI3/U1RX/OC3/RD2 |
| 19 | AVDD | 51 | SCL3/SDO3/U1TX/OC4/RD3 |
| 20 | AVSS | 52 | OC5/IC5/PMWR/CN13/RD4 |
| 21 | AN8/SS4/U5RX/U2CTS/C1OUT/RB8 | 53 | PMRD/CN14/RD5 |
| 22 | AN9/C2OUT/PMA7/RB9 | 54 | AETXEN/ETXERR/CN15/RD6 |
| 23 | TMS/AN10/CVREFOUT/PMA13/RB10 | 55 | ETXCLK/AERXERR/CN16/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | AETXD1/ERXD3/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | AETXD0/ERXD2/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | ERXD1/PMD0/RE0 |
| 29 | AN14/SCK4/U5TX/U2RTSU2RTS/PMALH/PMA1/RB14 | 61 | ERXD0/PMD1/RE1 |
| 30 | AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15 | 62 | ERXDV/ECRSDV/PMD2/RE2 |
| 31 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 | 63 | ERXCLK/EREFCLK/PMD3/RE3 |
| 32 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 | 64 | ERXERR/PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.
**2:** The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.


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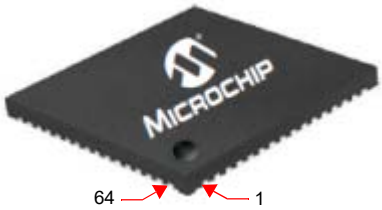
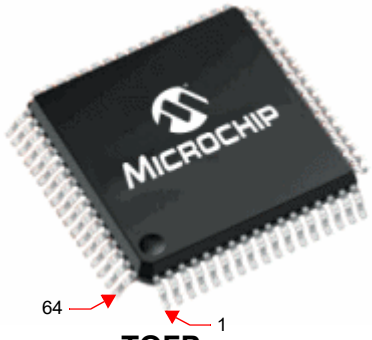
**TABLE 6: PIN NAMES FOR 64-PIN USB, ETHERNET, AND CAN DEVICES**

**64-PIN QFN(3) AND TQFP (TOP VIEW)**

**PIC32MX764F128H**
**PIC32MX775F256H**
**PIC32MX775F512H**
**PIC32MX795F512H**




**QFN(3)**




**TQFP**

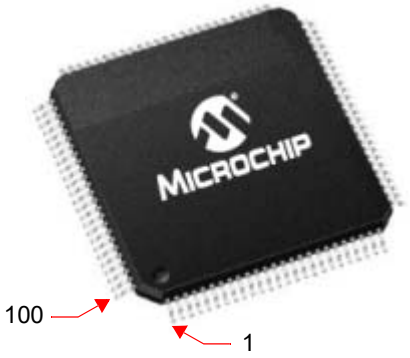
| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | ETXEN/PMD5/RE5 | 33 | USBID/RF3 |
| 2 | ETXD0/PMD6/RE6 | 34 | VBUS |
| 3 | ETXD1/PMD7/RE7 | 35 | VUSB3V3 |
| 4 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 36 | D-/RG3 |
| 5 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 37 | D+/RG2 |
| 6 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 38 | VDD |
| 7 | MCLR | 39 | OSC1/CLKI/RC12 |
| 8 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 40 | OSC2/CLKO/RC15 |
| 9 | VSS | 41 | Vss |
| 10 | VDD | 42 | RTCC/AERXD1/ETXD3/IC1/INT1/RD8 |
| 11 | AN5/C1IN+/VBUSON/CN7/RB5 | 43 | AERXD0/ETXD2/SS3/U4RX/U1CTS/SDA1/IC2/INT2/RD9 |
| 12 | AN4/C1IN-/CN6/RB4 | 44 | ECOL/AECRSDV/SCL1/IC3/PMCS2/PMA15/INT3/RD10 |
| 13 | AN3/C2IN+/CN5/RB3 | 45 | ECRS/AEREFCLK/IC4/PMCS1/PMA14/INT4/RD11 |
| 14 | AN2/C2IN-/CN4/RB2 | 46 | OC1/INT0/RD0 |
| 15 | PGEC1/AN1/VREF-/CVREF-/CN3/RB1 | 47 | SOSCI/CN1/RC13 |
| 16 | PGED1/AN0/VREF+/CVREF+/PMA6/CN2/RB0 | 48 | SOSCO/T1CK/CN0/RC14 |
| 17 | PGEC2/AN6/OCFA/RB6 | 49 | EMDIO/AEMDIO/SCK3/U4TX/U1RTS/OC2/RD1 |
| 18 | PGED2/AN7/RB7 | 50 | SDA3/SDI3/U1RX/OC3/RD2 |
| 19 | AVDD | 51 | SCL3/SDO3/U1TX/OC4/RD3 |
| 20 | AVSS | 52 | OC5/IC5/PMWR/CN13/RD4 |
| 21 | AN8/C2TX(2)/SS4/U5RX/U2CTS/C1OUT/RB8 | 53 | PMRD/CN14/RD5 |
| 22 | AN9/C2OUT/PMA7/RB9 | 54 | AETXEN/ETXERR/CN15/RD6 |
| 23 | TMS/AN10/CVREFOUT/PMA13/RB10 | 55 | ETXCLK/AERXERR/CN16/RD7 |
| 24 | TDO/AN11/PMA12/RB11 | 56 | VCAP |
| 25 | VSS | 57 | VDD |
| 26 | VDD | 58 | C1RX/AETXD1/ERXD3/RF0 |
| 27 | TCK/AN12/PMA11/RB12 | 59 | C1TX/AETXD0/ERXD2/RF1 |
| 28 | TDI/AN13/PMA10/RB13 | 60 | ERXD1/PMD0/RE0 |
| 29 | AN14/C2RX(2)/SCK4/U5TX/U2RTS/PMALH/PMA1/RB14 | 61 | ERXD0/PMD1/RE1 |
| 30 | AN15/EMDC/AEMDC/OCFB/PMALL/PMA0/CN12/RB15 | 62 | ERXDV/ECRSDV/PMD2/RE2 |
| 31 | AC1TX/SDA5/SDI4/U2RX/PMA9/CN17/RF4 | 63 | ERXCLK/EREFCLKPMD3/RE3 |
| 32 | AC1RX/SCL5/SDO4/U2TX/PMA8/CN18/RF5 | 64 | ERXERR/PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.
**2:** This pin is not available on PIC32MX765F128H devices.
**3:** The metal plane at the bottom of the QFN device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX534F064L**
**PIC32MX564F064L**
**PIC32MX564F128L**
**PIC32MX575F512L**
**PIC32MX575F256L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | PMD5/RE5 | 38 | TCK/RA1 |
| 4 | PMD6/RE6 | 39 | AC1TX/SCK4/U5TX/U2RTS/RF13 |
| 5 | PMD7/RE7 | 40 | AC1RX/SS4/U5RX/U2CTS/RF12 |
| 6 | T2CK/RC1 | 41 | AN12/PMA11/RB12 |
| 7 | T3CK/RC2 | 42 | AN13/PMA10/RB13 |
| 8 | T4CK/RC3 | 43 | AN14/PMALH/PMA1/RB14 |
| 9 | T5CK/SDI1/RC4 | 44 | AN15/OCFB/PMALL/PMA0/CN12/RB15 |
| 10 | SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 45 | VSS |
| 11 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 46 | VDD |
| 12 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 47 | SS3/U4RX/U1CTS/CN20/RD14 |
| 13 | MCLR | 48 | SCK3/U4TX/U1RTS/CN21/RD15 |
| 14 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 49 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| 15 | VSS | 50 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |
| 16 | VDD | 51 | USBID/RF3 |
| 17 | TMS/RA0 | 52 | SDA3/SDI3/U1RX/RF2 |
| 18 | INT1/RE8 | 53 | SCL3/SDO3/U1TX/RF8 |
| 19 | INT2/RE9 | 54 | VBUS |
| 20 | AN5/C1IN+/VBUSON/CN7/RB5 | 55 | VUSB3V3 |
| 21 | AN4/C1IN-/CN6/RB4 | 56 | D-/RG3 |
| 22 | AN3/C2IN+/CN5/RB3 | 57 | D+/RG2 |
| 23 | AN2/C2IN-/CN4/RB2 | 58 | SCL2/RA2 |
| 24 | PGEC1/AN1/CN3/RB1 | 59 | SDA2/RA3 |
| 25 | PGED1/AN0/CN2/RB0 | 60 | TDI/RA4 |
| 26 | PGEC2/AN6/OCFA/RB6 | 61 | TDO/RA5 |
| 27 | PGED2/AN7/RB7 | 62 | VDD |
| 28 | VREF-/CVREF-/PMA7/RA9 | 63 | OSC1/CLKI/RC12 |
| 29 | VREF+/CVREF+/PMA6/RA10 | 64 | OSC2/CLKO/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVSS | 66 | SCL1/INT3/RA14 |
| 32 | AN8/C1OUT/RB8 | 67 | SDA1/INT4/RA15 |
| 33 | AN9/C2OUT/RB9 | 68 | RTCC/IC1/RD8 |
| 34 | AN10/CVREFOUT/PMA13/RB10 | 69 | SS1/IC2/RD9 |
| 35 | AN11/PMA12/RB11 | 70 | SCK1/IC3/PMCS2/PMA15/RD10 |

**Note 1:** Shaded pins are 5V tolerant.


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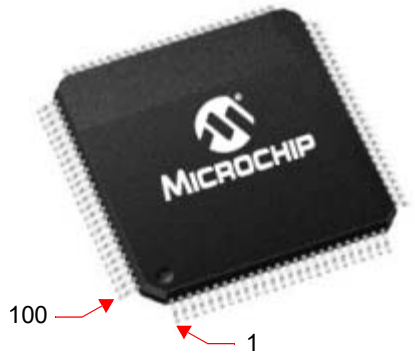
**TABLE 7: PIN NAMES FOR 100-PIN USB AND CAN DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX534F064L**
**PIC32MX564F064L**
**PIC32MX564F128L**
**PIC32MX575F512L**
**PIC32MX575F256L**



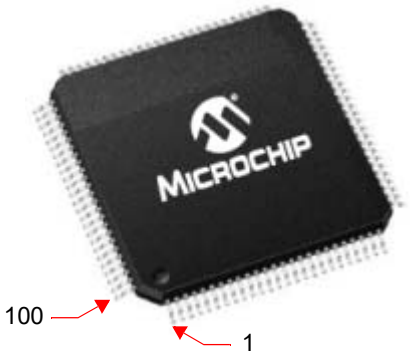

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | IC4/PMCS1/PMA14/RD11 | 86 | VDD |
| 72 | SDO1/OC1/INT0/RD0 | 87 | C1RX/PMD11/RF0 |
| 73 | SOSCI/CN1/RC13 | 88 | C1TX/PMD10/RF1 |
| 74 | SOSCO/T1CK/CN0/RC14 | 89 | PMD9/RG1 |
| 75 | VSS | 90 | PMD8/RG0 |
| 76 | OC2/RD1 | 91 | TRCLK/RA6 |
| 77 | OC3/RD2 | 92 | TRD3/RA7 |
| 78 | OC4/RD3 | 93 | PMD0/RE0 |
| 79 | IC5/PMD12/RD12 | 94 | PMD1/RE1 |
| 80 | PMD13/CN19/RD13 | 95 | TRD2/RG14 |
| 81 | OC5/PMWR/CN13/RD4 | 96 | TRD1/RG12 |
| 82 | PMRD/CN14/RD5 | 97 | TRD0/RG13 |
| 83 | PMD14/CN15/RD6 | 98 | PMD2/RE2 |
| 84 | PMD15/CN16/RD7 | 99 | PMD3/RE3 |
| 85 | VCAP | 100 | PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.

**TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX664F064L**
**PIC32MX664F128L**
**PIC32MX675F256L**
**PIC32MX675F512L**
**PIC32MX695F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AERXERR/RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | PMD5/RE5 | 38 | TCK/RA1 |
| 4 | PMD6/RE6 | 39 | SCK4/U5TX/U2RTS/RF13 |
| 5 | PMD7/RE7 | 40 | SS4/U5RX/U2CTS/RF12 |
| 6 | T2CK/RC1 | 41 | AN12/ERXD0/AECRS/PMA11/RB12 |
| 7 | T3CK/RC2 | 42 | AN13/ERXD1/AECOL/PMA10/RB13 |
| 8 | T4CK/RC3 | 43 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| 9 | T5CK/SDI1/RC4 | 44 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| 10 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 45 | VSS |
| 11 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 46 | VDD |
| 12 | ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 47 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| 13 | MCLR | 48 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 |
| 14 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 49 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| 15 | VSS | 50 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |
| 16 | VDD | 51 | USBID/RF3 |
| 17 | TMS/RA0 | 52 | SDA3/SDI3/U1RX/RF2 |
| 18 | AERXD0/INT1/RE8 | 53 | SCL3/SDO3/U1TX/RF8 |
| 19 | AERXD1/INT2/RE9 | 54 | VBUS |
| 20 | AN5/C1IN+/VBUSON/CN7/RB5 | 55 | VUSB3V3 |
| 21 | AN4/C1IN-/CN6/RB4 | 56 | D-/RG3 |
| 22 | AN3/C2IN+/CN5/RB3 | 57 | D+/RG2 |
| 23 | AN2/C2IN-/CN4/RB2 | 58 | SCL2/RA2 |
| 24 | PGEC1/AN1/CN3/RB1 | 59 | SDA2/RA3 |
| 25 | PGED1/AN0/CN2/RB0 | 60 | TDI/RA4 |
| 26 | PGEC2/AN6/OCFA/RB6 | 61 | TDO/RA5 |
| 27 | PGED2/AN7/RB7 | 62 | VDD |
| 28 | VREF-/CVREF-/AERXD2/PMA7/RA9 | 63 | OSC1/CLKI/RC12 |
| 29 | VREF+/CVREF+/AERXD3/PMA6/RA10 | 64 | OSC2/CLKO/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVSS | 66 | AETXCLK/SCL1/INT3/RA14 |
| 32 | AN8/C1OUT/RB8 | 67 | AETXEN/SDA1/INT4/RA15 |
| 33 | AN9/C2OUT/RB9 | 68 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| 34 | AN10/CVREFOUT/PMA13/RB10 | 69 | SS1/IC2/RD9 |
| 35 | AN11/ERXERR/AETXERR/PMA12/RB11 | 70 | SCK1/IC3/PMCS2/PMA15/RD10 |

**Note 1:** Shaded pins are 5V tolerant.


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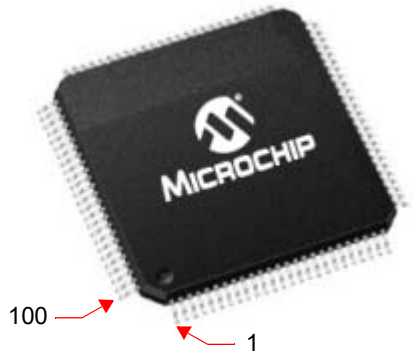
**TABLE 8: PIN NAMES FOR 100-PIN USB AND ETHERNET DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX664F064L**
**PIC32MX664F128L**
**PIC32MX675F256L**
**PIC32MX675F512L**
**PIC32MX695F512L**



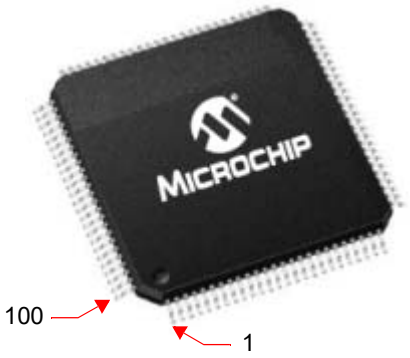

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 | 86 | VDD |
| 72 | SDO1/OC1/INT0/RD0 | 87 | ETXD1/PMD11/RF0 |
| 73 | SOSCI/CN1/RC13 | 88 | ETXD0/PMD10/RF1 |
| 74 | SOSCO/T1CK/CN0/RC14 | 89 | ETXERR/PMD9/RG1 |
| 75 | VSS | 90 | PMD8/RG0 |
| 76 | OC2/RD1 | 91 | TRCLK/RA6 |
| 77 | OC3/RD2 | 92 | TRD3/RA7 |
| 78 | OC4/RD3 | 93 | PMD0/RE0 |
| 79 | ETXD2/IC5/PMD12/RD12 | 94 | PMD1/RE1 |
| 80 | ETXD3/PMD13/CN19/RD13 | 95 | TRD2/RG14 |
| 81 | OC5/PMWR/CN13/RD4 | 96 | TRD1/RG12 |
| 82 | PMRD/CN14/RD5 | 97 | TRD0/RG13 |
| 83 | ETXEN/PMD14/CN15/RD6 | 98 | PMD2/RE2 |
| 84 | ETXCLK/PMD15/CN16/RD7 | 99 | PMD3/RE3 |
| 85 | VCAP/VDDCORE | 100 | PMD4/RE4 |

**Note 1:** Shaded pins are 5V tolerant.

**TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AERXERR/RG15 | 36 | VSS |
| 2 | VDD | 37 | VDD |
| 3 | PMD5/RE5 | 38 | TCK/RA1 |
| 4 | PMD6/RE6 | 39 | AC1TX/SCK4/U5TX/U2RTS/RF13 |
| 5 | PMD7/RE7 | 40 | AC1RX/SS4/U5RX/U2CTS/RF12 |
| 6 | T2CK/RC1 | 41 | AN12/ERXD0/AECRS/PMA11/RB12 |
| 7 | T3CK/AC2TX(1)/RC2 | 42 | AN13/ERXD1/AECOL/PMA10/RB13 |
| 8 | T4CK/AC2RX(1)/RC3 | 43 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| 9 | T5CK/SDI1/RC4 | 44 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| 10 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | 45 | VSS |
| 11 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 | 46 | VDD |
| 12 | ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8 | 47 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| 13 | MCLR | 48 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 |
| 14 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 | 49 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| 15 | VSS | 50 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |
| 16 | VDD | 51 | USBID/RF3 |
| 17 | TMS/RA0 | 52 | SDA3/SDI3/U1RX/RF2 |
| 18 | AERXD0/INT1/RE8 | 53 | SCL3/SDO3/U1TX/RF8 |
| 19 | AERXD1/INT2/RE9 | 54 | VBUS |
| 20 | AN5/C1IN+/VBUSON/CN7/RB5 | 55 | VUSB3V3 |
| 21 | AN4/C1IN-/CN6/RB4 | 56 | D-/RG3 |
| 22 | AN3/C2IN+/CN5/RB3 | 57 | D+/RG2 |
| 23 | AN2/C2IN-/CN4/RB2 | 58 | SCL2/RA2 |
| 24 | PGEC1/AN1/CN3/RB1 | 59 | SDA2/RA3 |
| 25 | PGED1/AN0/CN2/RB0 | 60 | TDI/RA4 |
| 26 | PGEC2/AN6/OCFA/RB6 | 61 | TDO/RA5 |
| 27 | PGED2/AN7/RB7 | 62 | VDD |
| 28 | VREF-/CVREF-/AERXD2/PMA7/RA9 | 63 | OSC1/CLKI/RC12 |
| 29 | VREF+/CVREF+/AERXD3/PMA6/RA10 | 64 | OSC2/CLKO/RC15 |
| 30 | AVDD | 65 | VSS |
| 31 | AVSS | 66 | AETXCLK/SCL1/INT3/RA14 |
| 32 | AN8/C1OUT/RB8 | 67 | AETXEN/SDA1/INT4/RA15 |
| 33 | AN9/C2OUT/RB9 | 68 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| 34 | AN10/CVREFOUT/PMA13/RB10 | 69 | SS1/IC2/RD9 |
| 35 | AN11/ERXERR/AETXERR/PMA12/RB11 | 70 | SCK1/IC3/PMCS2/PMA15/RD10 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.


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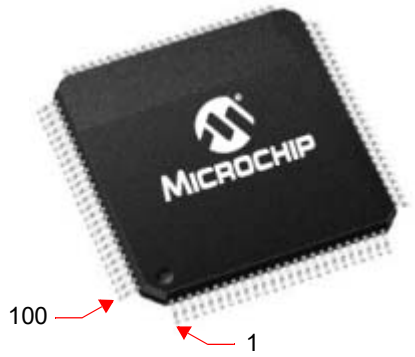
**TABLE 9: PIN NAMES FOR 100-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)**

**100-PIN TQFP (TOP VIEW)**

**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**



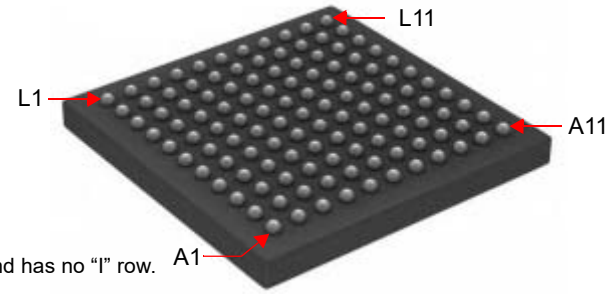

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 71 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 | 86 | VDD |
| 72 | SDO1/OC1/INT0/RD0 | 87 | C1RX/ETXD1/PMD11/RF0 |
| 73 | SOSCI/CN1/RC13 | 88 | C1TX/ETXD0/PMD10/RF1 |
| 74 | SOSCO/T1CK/CN0/RC14 | 89 | C2TX(1)/ETXERR/PMD9/RG1 |
| 75 | VSS | 90 | C2RX(1)/PMD8/RG0 |
| 76 | OC2/RD1 | 91 | TRCLK/RA6 |
| 77 | OC3/RD2 | 92 | TRD3/RA7 |
| 78 | OC4/RD3 | 93 | PMD0/RE0 |
| 79 | ETXD2/IC5/PMD12/RD12 | 94 | PMD1/RE1 |
| 80 | ETXD3/PMD13/CN19/RD13 | 95 | TRD2/RG14 |
| 81 | OC5/PMWR/CN13/RD4 | 96 | TRD1/RG12 |
| 82 | PMRD/CN14/RD5 | 97 | TRD0/RG13 |
| 83 | ETXEN/PMD14/CN15/RD6 | 98 | PMD2/RE2 |
| 84 | ETXCLK/PMD15/CN16/RD7 | 99 | PMD3/RE3 |
| 85 | VCAP/VDDCORE | 100 | PMD4/RE4 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.

**TABLE 10: PIN NAMES FOR USB AND CAN DEVICES**

**121-PIN TFBGA (BOTTOM VIEW)**

**PIC32MX534F064L**
**PIC32MX564F064L**
**PIC32MX564F128L**
**PIC32MX575F256L**
**PIC32MX575F512L**




**Note:** The TFBGA package skips from row "H" to row "J" and has no "I" row.

| Pin # | Full Pin Name |
|---|---|
| A1 | PMD4/RE4 |
| A2 | PMD3/RE3 |
| A3 | TRD0/RG13 |
| A4 | PMD0/RE0 |
| A5 | PMD8/RG0 |
| A6 | C1TX/PMD10/RF1 |
| A7 | VDD |
| A8 | VSS |
| A9 | IC5/PMD12/RD12 |
| A10 | OC3/RD2 |
| A11 | OC2/RD1 |
| B1 | No Connect (NC) |
| B2 | RG15 |
| B3 | PMD2/RE2 |
| B4 | PMD1/RE1 |
| B5 | TRD3/RA7 |
| B6 | C1RX/PMD11/RF0 |
| B7 | VCAP |
| B8 | PMRD/CN14/RD5 |
| B9 | OC4/RD3 |
| B10 | VSS |
| B11 | SOSCO/T1CK/CN0/RC14 |
| C1 | PMD6/RE6 |
| C2 | VDD |
| C3 | TRD1/RG12 |
| C4 | TRD2/RG14 |
| C5 | TRCLK/RA6 |
| C6 | No Connect (NC) |
| C7 | PMD15/CN16/RD7 |
| C8 | OC5/PMWR/CN13/RD4 |
| C9 | VDD |
| C10 | SOSCI/CN1/RC13 |
| C11 | IC4/PMCS1/PMA14/RD11 |
| D1 | T2CK/RC1 |
| D2 | PMD7/RE7 |
| D3 | PMD5/RE5 |
| D4 | VSS |
| D5 | VSS |
| D6 | No Connect (NC) |
| D7 | PMD14/CN15/RD6 |
| D8 | PMD13/CN19/RD13 |
| D9 | SDO1/OC1/INT0/RD0 |
| D10 | No Connect (NC) |
| D11 | SCK1/IC3/PMCS2/PMA15/RD10 |
| E1 | T5CK/SDI1/RC4 |

| Pin # | Full Pin Name |
|---|---|
| E2 | T4CK/RC3 |
| E3 | SCK2/U6TXU6TX/U3RTS/PMA5/CN8/RG6 |
| E4 | T3CK/RC2 |
| E5 | VDD |
| E6 | PMD9/RG1 |
| E7 | VSS |
| E8 | SDA1/INT4/RA15 |
| E9 | RTCC/IC1/RD8 |
| E10 | SS1/IC2/RD9 |
| E11 | SCL1/INT3/RA14 |
| F1 | MCLR |
| F2 | SCL4/SDO2/U3TX/PMA3/CN10/RG8 |
| F3 | SS2/U6RX/U3CTS/PMA2/CN11/RG9 |
| F4 | SDA4/SDI2/U3RX/PMA4/CN9/RG7 |
| F5 | VSS |
| F6 | No Connect (NC) |
| F7 | No Connect (NC) |
| F8 | VDD |
| F9 | OSC1/CLKI/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | INT1/RE8 |
| G2 | INT2/RE9 |
| G3 | TMS/RA0 |
| G4 | No Connect (NC) |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect (NC) |
| G9 | TDO/RA5 |
| G10 | SDA2/RA3 |
| G11 | TDI/RA4 |
| H1 | AN5/C1IN+/VBUSON/CN7/RB5 |
| H2 | AN4/C1IN-/CN6/RB4 |
| H3 | VSS |
| H4 | VDD |
| H5 | No Connect (NC) |
| H6 | VDD |
| H7 | No Connect (NC) |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2 |
| H11 | SCL2/RA2 |
| J1 | AN3/C2IN+/CN5/RB3 |
| J2 | AN2/C2IN-/CN4/RB2 |

**Note 1:** Shaded pins are 5V tolerant.


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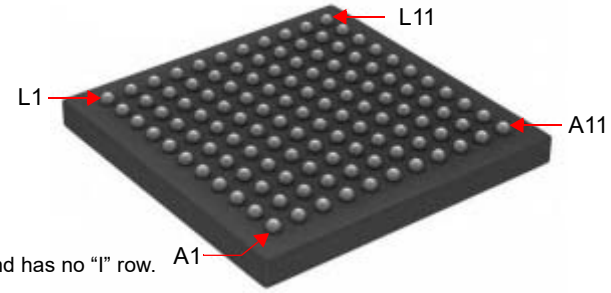
**TABLE 10: PIN NAMES (CONTINUED)FOR USB AND CAN DEVICES**

**121-PIN TFBGA (BOTTOM VIEW)**

**PIC32MX534F064L**
**PIC32MX564F064L**
**PIC32MX564F128L**
**PIC32MX575F256L**
**PIC32MX575F512L**




**Note:** The TFBGA package skips from row “H” to row “J” and has no “I” row.

| Pin # | Full Pin Name |
|---|---|
| J3 | PGED2/AN7/RB7 |
| J4 | AVDD |
| J5 | AN11/PMA12/RB11 |
| J6 | TCK/RA1 |
| J7 | AN12/PMA11/RB12 |
| J8 | No Connect (NC) |
| J9 | No Connect (NC) |
| J10 | SCL3/SDO3/U1TX/RF8 |
| J11 | D-/RG3 |
| K1 | PGEC1/AN1/CN3/RB1 |
| K2 | PGED1/AN0/CN2/RB0 |
| K3 | VREF+/CVREF+/PMA6/RA10 |
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | AC1RX/$\overline{SS4}$/U5RX/$\overline{U2CTS}$/RF12 |
| K7 | AN14/PMALH/PMA1/RB14 |

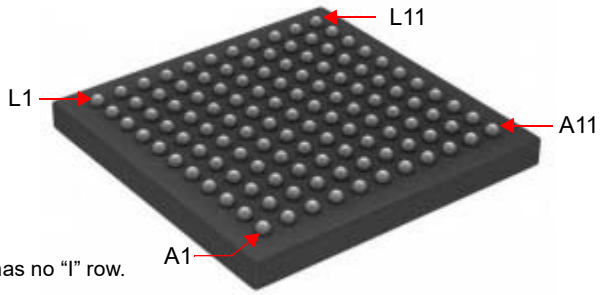
| Pin # | Full Pin Name |
|---|---|
| K8 | VDD |
| K9 | SCK3/U4TX/$\overline{U1RTS}$/CN21/RD15 |
| K10 | USBID/RF3 |
| K11 | SDA3/SDI3/U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/PMA7/RA9 |
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | AC1TX/SCK4/U5TX/$\overline{U2RTS}$/RF13 |
| L7 | AN13/PMA10/RB13 |
| L8 | AN15/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | $\overline{SS3}$/U4RX/$\overline{U1CTS}$/CN20/RD14 |
| L10 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| L11 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |

**Note 1:** Shaded pins are 5V tolerant.

**TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES**

**121-PIN TFBGA (BOTTOM VIEW)**

**PIC32MX664F064L**
**PIC32MX664F128L**
**PIC32MX675F256L**
**PIC32MX675F512L**
**PIC32MX695F512L**




**Note:** The TFBGA package skips from row “H” to row “J” and has no “I” row.

| Pin # | Full Pin Name |
|---|---|
| A1 | PMD4/RE4 |
| A2 | PMD3/RE3 |
| A3 | TRD0/RG13 |
| A4 | PMD0/RE0 |
| A5 | PMD8/RG0 |
| A6 | ETXD0/PMD10/RF1 |
| A7 | VDD |
| A8 | VSS |
| A9 | ETXD2/IC5/PMD12/RD12 |
| A10 | OC3/RD2 |
| A11 | OC2/RD1 |
| B1 | No Connect (NC) |
| B2 | AERXERR/RG15 |
| B3 | PMD2/RE2 |
| B4 | PMD1/RE1 |
| B5 | TRD3/RA7 |
| B6 | ETXD1/PMD11/RF0 |
| B7 | VCAP |
| B8 | PMRD/CN14/RD5 |
| B9 | OC4/RD3 |
| B10 | VSS |
| B11 | SOSCO/T1CK/CN0/RC14 |
| C1 | PMD6/RE6 |
| C2 | VDD |
| C3 | TRD1/RG12 |
| C4 | TRD2/RG14 |
| C5 | TRCLK/RA6 |
| C6 | No Connect (NC) |
| C7 | ETXCLK/PMD15/CN16/RD7 |
| C8 | OC5/PMWR/CN13/RD4 |
| C9 | VDD |
| C10 | SOSCI/CN1/RC13 |
| C11 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 |
| D1 | T2CK/RC1 |
| D2 | PMD7/RE7 |
| D3 | PMD5/RE5 |
| D4 | VSS |
| D5 | VSS |
| D6 | No Connect (NC) |
| D7 | ETXEN/PMD14/CN15/RD6 |
| D8 | ETXD3/PMD13/CN19/RD13 |
| D9 | SDO1/OC1/INT0/RD0 |
| D10 | No Connect (NC) |
| D11 | SCK1/IC3/PMCS2/PMA15/RD10 |
| E1 | T5CK/SDI1/RC4 |

| Pin # | Full Pin Name |
|---|---|
| E2 | T4CK/RC3 |
| E3 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 |
| E4 | T3CK/RC2 |
| E5 | VDD |
| E6 | ETXERR/PMD9/RG1 |
| E7 | VSS |
| E8 | AETXEN/SDA1/INT4/RA15 |
| E9 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| E10 | SS1/IC2/RD9 |
| E11 | AETXCLK/SCL1/INT3/RA14 |
| F1 | MCLR |
| F2 | ERXDV/AERXDV/ECRSDV/AECRSDV//SCL4/SDO2/U3TX/PMA3/CN10/RG8 |
| F3 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 |
| F4 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 |
| F5 | VSS |
| F6 | No Connect (NC) |
| F7 | No Connect (NC) |
| F8 | VDD |
| F9 | OSC1/CLKI/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | AERXD0/INT1/RE8 |
| G2 | AERXD1/INT2/RE9 |
| G3 | TMS/RA0 |
| G4 | No Connect (NC) |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect (NC) |
| G9 | TDO/RA5 |
| G10 | SDA2/RA3 |
| G11 | TDI/RA4 |
| H1 | AN5/C1IN+/VBUSON/CN7/RB5 |
| H2 | AN4/C1IN-/CN6/RB4 |
| H3 | VSS |
| H4 | VDD |
| H5 | No Connect (NC) |
| H6 | VDD |
| H7 | No Connect (NC) |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2 |
| H11 | SCL2/RA2 |
| J1 | AN3/C2IN+/CN5/RB3 |
| J2 | AN2/C2IN-/CN4/RB2 |

**Note 1:** Shaded pins are 5V tolerant.


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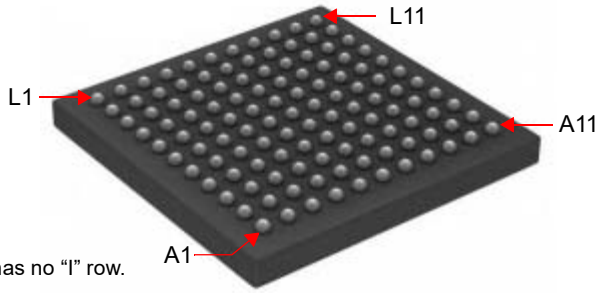
**TABLE 11: PIN NAMES FOR USB AND ETHERNET DEVICES (CONTINUED)**

**121-PIN TFBGA (BOTTOM VIEW)**

**PIC32MX664F064L**
**PIC32MX664F128L**
**PIC32MX675F256L**
**PIC32MX675F512L**
**PIC32MX695F512L**



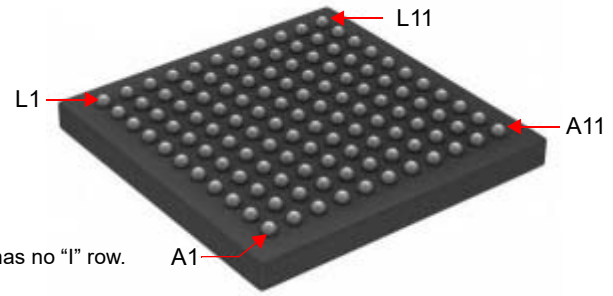

**Note:** The TFBGA package skips from row “H” to row “J” and has no “I” row.

| Pin # | Full Pin Name |
|---|---|
| J3 | PGED2/AN7/RB7 |
| J4 | AVDD |
| J5 | AN11/ERXERR/AETXERR/PMA12/RB11 |
| J6 | TCK/RA1 |
| J7 | AN12/ERXD0/AECRS/PMA11/RB12 |
| J8 | No Connect (NC) |
| J9 | No Connect (NC) |
| J10 | SCL3/SDO3/U1TX/RF8 |
| J11 | D-/RG3 |
| K1 | PGEC1/AN1/CN3/RB1 |
| K2 | PGED1/AN0/CN2/RB0 |
| K3 | VREF+/CVREF+/AERXD3/PMA6/RA10 |
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | $\overline{SS4}$/U5RX/$\overline{U2CTS}$/RF12 |
| K7 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| K8 | VDD |
| K9 | AETXD1/SCK3/U4TX/$\overline{U1RTS}$/CN21/RD15 |
| K10 | USBID/RF3 |
| K11 | SDA3/SDI3/U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/AERXD2/PMA7/RA9 |
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | SCK4/U5TX/$\overline{U2RTS}$/RF13 |
| L7 | AN13/ERXD1/AECOL/PMA10/RB13 |
| L8 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | AETXD0/$\overline{SS3}$/U4RX/$\overline{U1CTS}$/CN20/RD14 |
| L10 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| L11 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |

**Note 1:** Shaded pins are 5V tolerant.

**TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES**

**121-PIN TFBGA (BOTTOM VIEW)**




**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**

**Note:** The TFBGA package skips from row "H" to row "J" and has no "I" row.

| Pin # | Full Pin Name |
|---|---|
| A1 | PMD4/RE4 |
| A2 | PMD3/RE3 |
| A3 | TRD0/RG13 |
| A4 | PMD0/RE0 |
| A5 | C2RX(1)/PMD8/RG0 |
| A6 | C1TX/ETXD0/PMD10/RF1 |
| A7 | VDD |
| A8 | VSS |
| A9 | ETXD2/IC5/PMD12/RD12 |
| A10 | OC3/RD2 |
| A11 | OC2/RD1 |
| B1 | No Connect (NC) |
| B2 | AERXERR/RG15 |
| B3 | PMD2/RE2 |
| B4 | PMD1/RE1 |
| B5 | TRD3/RA7 |
| B6 | C1RX/ETXD1/PMD11/RF0 |
| B7 | VCAP |
| B8 | PMRD/CN14/RD5 |
| B9 | OC4/RD3 |
| B10 | VSS |
| B11 | SOSCO/T1CK/CN0/RC14 |
| C1 | PMD6/RE6 |
| C2 | VDD |
| C3 | TRD1/RG12 |
| C4 | TRD2/RG14 |
| C5 | TRCLK/RA6 |
| C6 | No Connect (NC) |
| C7 | ETXCLK/PMD15/CN16/RD7 |
| C8 | OC5/PMWR/CN13/RD4 |
| C9 | VDD |
| C10 | SOSCI/CN1/RC13 |
| C11 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 |
| D1 | T2CK/RC1 |
| D2 | PMD7/RE7 |
| D3 | PMD5/RE5 |
| D4 | VSS |
| D5 | VSS |
| D6 | No Connect (NC) |
| D7 | ETXEN/PMD14/CN15/RD6 |
| D8 | ETXD3/PMD13/CN19/RD13 |
| D9 | SDO1/OC1/INT0/RD0 |
| D10 | No Connect (NC) |
| D11 | SCK1/IC3/PMCS2/PMA15/RD10 |
| E1 | T5CK/SDI1/RC4 |

| Pin # | Full Pin Name |
|---|---|
| E2 | T4CK/AC2RX(1)/RC3 |
| E3 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 |
| E4 | T3CK/AC2TX(1)/RC2 |
| E5 | VDD |
| E6 | C2TX(1)/ETXERR/PMD9/RG1 |
| E7 | VSS |
| E8 | AETXEN/SDA1/INT4/RA15 |
| E9 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| E10 | SS1/IC2/RD9 |
| E11 | AETXCLK/SCL1/INT3/RA14 |
| F1 | MCLR |
| F2 | ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8 |
| F3 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 |
| F4 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 |
| F5 | VSS |
| F6 | No Connect (NC) |
| F7 | No Connect (NC) |
| F8 | VDD |
| F9 | OSC1/CLKI/RC12 |
| F10 | VSS |
| F11 | OSC2/CLKO/RC15 |
| G1 | AERXD0/INT1/RE8 |
| G2 | AERXD1/INT2/RE9 |
| G3 | TMS/RA0 |
| G4 | No Connect (NC) |
| G5 | VDD |
| G6 | VSS |
| G7 | VSS |
| G8 | No Connect (NC) |
| G9 | TDO/RA5 |
| G10 | SDA2/RA3 |
| G11 | TDI/RA4 |
| H1 | AN5/C1IN+/VBUSON/CN7/RB5 |
| H2 | AN4/C1IN-/CN6/RB4 |
| H3 | VSS |
| H4 | VDD |
| H5 | No Connect (NC) |
| H6 | VDD |
| H7 | No Connect (NC) |
| H8 | VBUS |
| H9 | VUSB3V3 |
| H10 | D+/RG2 |
| H11 | SCL2/RA2 |
| J1 | AN3/C2IN+/CN5/RB3 |
| J2 | AN2/C2IN-/CN4/RB2 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.


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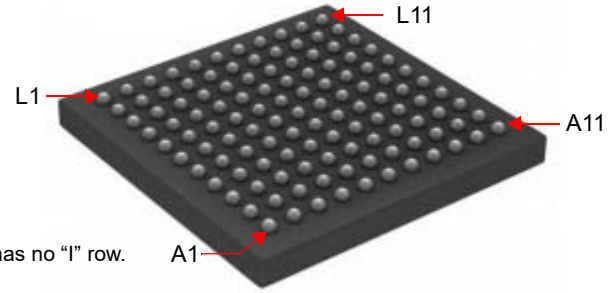
**TABLE 12: PIN NAMES FOR USB, ETHERNET, AND CAN DEVICES (CONTINUED)**

**121-PIN TFBGA (BOTTOM VIEW)**

**PIC32MX764F128L**
**PIC32MX775F256L**
**PIC32MX775F512L**
**PIC32MX795F512L**




**Note:** The TFBGA package skips from row "H" to row "J" and has no "I" row.

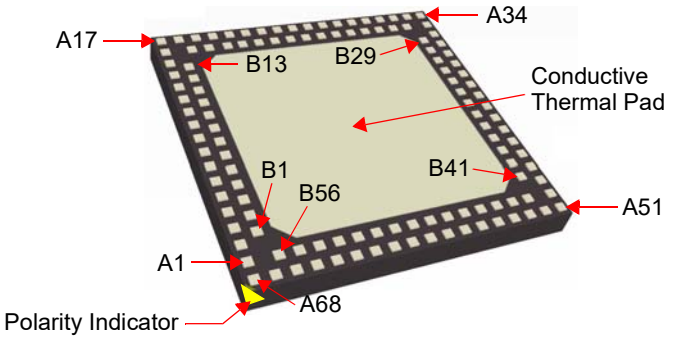
| Pin # | Full Pin Name |
|---|---|
| J3 | PGED2/AN7/RB7 |
| J4 | AVDD |
| J5 | AN11/ERXERR/AETXERR/PMA12/RB11 |
| J6 | TCK/RA1 |
| J7 | AN12/ERXD0/AECRS/PMA11/RB12 |
| J8 | No Connect (NC) |
| J9 | No Connect (NC) |
| J10 | SCL3/SDO3/U1TX/RF8 |
| J11 | D-/RG3 |
| K1 | PGEC1/AN1/CN3/RB1 |
| K2 | PGED1/AN0/CN2/RB0 |
| K3 | VREF+/CVREF+/AERXD3/PMA6/RA10 |
| K4 | AN8/C1OUT/RB8 |
| K5 | No Connect (NC) |
| K6 | AC1RX/SS4/U5RX/U2CTS/RF12 |
| K7 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| K8 | VDD |
| K9 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 |
| K10 | USBID/RF3 |
| K11 | SDA3/SDI3/U1RX/RF2 |
| L1 | PGEC2/AN6/OCFA/RB6 |
| L2 | VREF-/CVREF-/AERXD2/PMA7/RA9 |
| L3 | AVSS |
| L4 | AN9/C2OUT/RB9 |
| L5 | AN10/CVREFOUT/PMA13/RB10 |
| L6 | AC1TX/SCK4/U5TX/U2RTS/RF13 |
| L7 | AN13/ERXD1/AECOL/PMA10/RB13 |
| L8 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 |
| L9 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| L10 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| L11 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 |

**Note 1:** This pin is not available on PIC32MX764F128L devices.
**2:** Shaded pins are 5V tolerant.

**TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES**

**124-PIN VTLA (BOTTOM VIEW)[2,3]**

**PIC32MX675F512L**
**PIC32MX695F512L**
**PIC32MX795F512L**




| Package Bump # | Full Pin Name | Package Bump # | Full Pin Name |
|---|---|---|---|
| A1 | No Connect (NC) | A38 | D-/RG3 |
| A2 | AERXERR/RG15 | A39 | SCL2/RA2 |
| A3 | VSS | A40 | TDI/RA4 |
| A4 | PMD6/RE6 | A41 | VDD |
| A5 | T2CK/RC1 | A42 | OSC2/CLKO/RC15 |
| A6 | T4CK/AC2RX(1)/RC3 | A43 | VSS |
| A7 | ECOL/SCK2/U6TX/U3RTS/PMA5/CN8/RG6 | A44 | AETXEN/SDA1/INT4/RA15 |
| A8 | ERXDV/AERXDV/ECRSDV/AECRSDV/SCL4/SDO2/U3TX/PMA3/CN10/RG8 | A45 | SS1/IC2/RD9 |
| A9 | ERXCLK/AERXCLK/EREFCLK/AEREFCLK/SS2/U6RX/U3CTS/PMA2/CN11/RG9 | A46 | EMDC/AEMDC/IC4/PMCS1/PMA14/RD11 |
| A10 | VDD | A47 | SOSCI/CN1/RC13 |
| A11 | AERXD0/INT1/RE8 | A48 | VDD |
| A12 | AN5/C1IN+/VBUSON/CN7/RB5 | A49 | No Connect (NC) |
| A13 | AN3/C2IN+/CN5/RB3 | A50 | No Connect (NC) |
| A14 | VDD | A51 | No Connect (NC) |
| A15 | PGEC1/AN1/CN3/RB1 | A52 | OC2/RD1 |
| A16 | No Connect (NC) | A53 | OC4/RD3 |
| A17 | No Connect (NC) | A54 | ETXD3/PMD13/CN19/RD13 |
| A18 | No Connect (NC) | A55 | PMRD/CN14/RD5 |
| A19 | No Connect (NC) | A56 | ETXCLK/PMD15/CN16/RD7 |
| A20 | PGEC2/AN6/OCFA/RB6 | A57 | No Connect (NC) |
| A21 | VREF-/CVREF-/AERXD2/PMA7/RA9 | A58 | No Connect (NC) |
| A22 | AVDD | A59 | VDD |
| A23 | AN8/C1OUT/RB8 | A60 | C1TX/ETXD0/PMD10/RF1 |
| A24 | AN10/CVREFOUT/PMA13/RB10 | A61 | C2RX(1)/PMD8/RG0 |
| A25 | VSS | A62 | TRD3/RA7 |
| A26 | TCK/RA1 | A63 | VSS |
| A27 | AC1RX(1)/SS4/U5RX/U2CTS/RF12 | A64 | PMD1/RE1 |
| A28 | AN13/ERXD1/AECOL/PMA10/RB13 | A65 | TRD1/RG12 |
| A29 | AN15/ERXD3/AETXD2/OCFB/PMALL/PMA0/CN12/RB15 | A66 | PMD2/RE2 |
| A30 | VDD | A67 | PMD4/RE4 |
| A31 | AETXD1/SCK3/U4TX/U1RTS/CN21/RD15 | A68 | No Connect (NC) |
| A32 | SCL5/SDO4/U2TX/PMA8/CN18/RF5 | B1 | VDD |
| A33 | No Connect (NC) | B2 | PMD5/RE5 |
| A34 | No Connect (NC) | B3 | PMD7/RE7 |
| A35 | USBID/RF3 | B4 | T3CK/AC2TX(1)/RC2 |
| A36 | SDA3/SDI3/U1RX/RF2 | B5 | T5CK/SDI1/RC4 |
| A37 | VBUS | B6 | ECRS/SDA4/SDI2/U3RX/PMA4/CN9/RG7 |
| B7 | MCLR | B32 | SDA2/RA3 |

**Note 1:** This pin is only available on PIC32MX795F512L devices.
**2:** Shaded package bumps are 5V tolerant.
**3:** It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.


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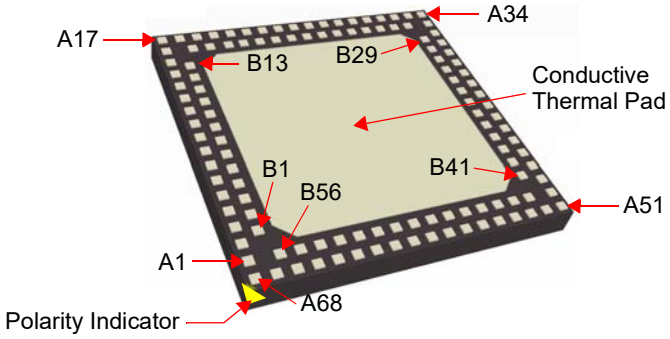
**TABLE 13: PIN NAMES FOR 124-PIN USB, ETHERNET, AND CAN DEVICES (CONTINUED)**

**124-PIN VTLA (BOTTOM VIEW)(2,3)**

**PIC32MX675F512L**
**PIC32MX695F512L**
**PIC32MX795F512L**




| Package Bump # | Full Pin Name |
|---|---|
| B8 | VSS |
| B9 | TMS/RA0 |
| B10 | AERXD1/INT2/RE9 |
| B11 | AN4/C1IN-/CN6/RB4 |
| B12 | VSS |
| B13 | AN2/C2IN-/CN4/RB2 |
| B14 | PGED1/AN0/CN2/RB0 |
| B15 | No Connect (NC) |
| B16 | PGED2/AN7/RB7 |
| B17 | VREF+/CVREF+/AERXD3/PMA6/RA10 |
| B18 | AVSS |
| B19 | AN9/C2OUT/RB9 |
| B20 | AN11/ERXERR/AETXERR/PMA12/RB11 |
| B21 | VDD |
| B22 | AC1TX/SCK4/U5TX/U2RTS/RF13 |
| B23 | AN12/ERXD0/AECRS/PMA11/RB12 |
| B24 | AN14/ERXD2/AETXD3/PMALH/PMA1/RB14 |
| B25 | VSS |
| B26 | AETXD0/SS3/U4RX/U1CTS/CN20/RD14 |
| B27 | SDA5/SDI4/U2RX/PMA9/CN17/RF4 |
| B28 | No Connect (NC) |
| B29 | SCL3/SDO3/U1TX/RF8 |
| B30 | VUSB3V3 |
| B31 | D+/RG2 |

| Package Bump # | Full Pin Name |
|---|---|
| B33 | TDO/RA5 |
| B34 | OSC1/CLKI/RC12 |
| B35 | No Connect (NC) |
| B36 | AETXCLK/SCL1/INT3/RA14 |
| B37 | RTCC/EMDIO/AEMDIO/IC1/RD8 |
| B38 | SCK1/IC3/PMCS2/PMA15/RD10 |
| B39 | SDO1/OC1/INT0/RD0 |
| B40 | SOSCO/T1CK/CN0/RC14 |
| B41 | VSS |
| B42 | OC3/RD2 |
| B43 | ETXD2/IC5/PMD12/RD12 |
| B44 | OC5/PMWR/CN13/RD4 |
| B45 | ETXEN/PMD14/CN15/RD6 |
| B46 | VSS |
| B47 | No Connect (NC) |
| B48 | VCAP |
| B49 | C1RX(1)/ETXD1/PMD11/RF0 |
| B50 | C2TX(1)/ETXERR/PMD9/RG1 |
| B51 | TRCLK/RA6 |
| B52 | PMD0/RE0 |
| B53 | VDD |
| B54 | TRD2/RG14 |
| B55 | TRD0/RG13 |
| B56 | PMD3/RE3 |

**Note 1:** This pin is only available on PIC32MX795F512L devices.
**2:** Shaded package bumps are 5V tolerant.
**3:** It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

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### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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## Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note 1:** To access the documents listed below, browse to the documentation section of the PIC32MX795F512L product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 4. "Prefetch Cache"** (DS60001119)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Capture"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I2C)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)


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## 1.0 DEVICE OVERVIEW

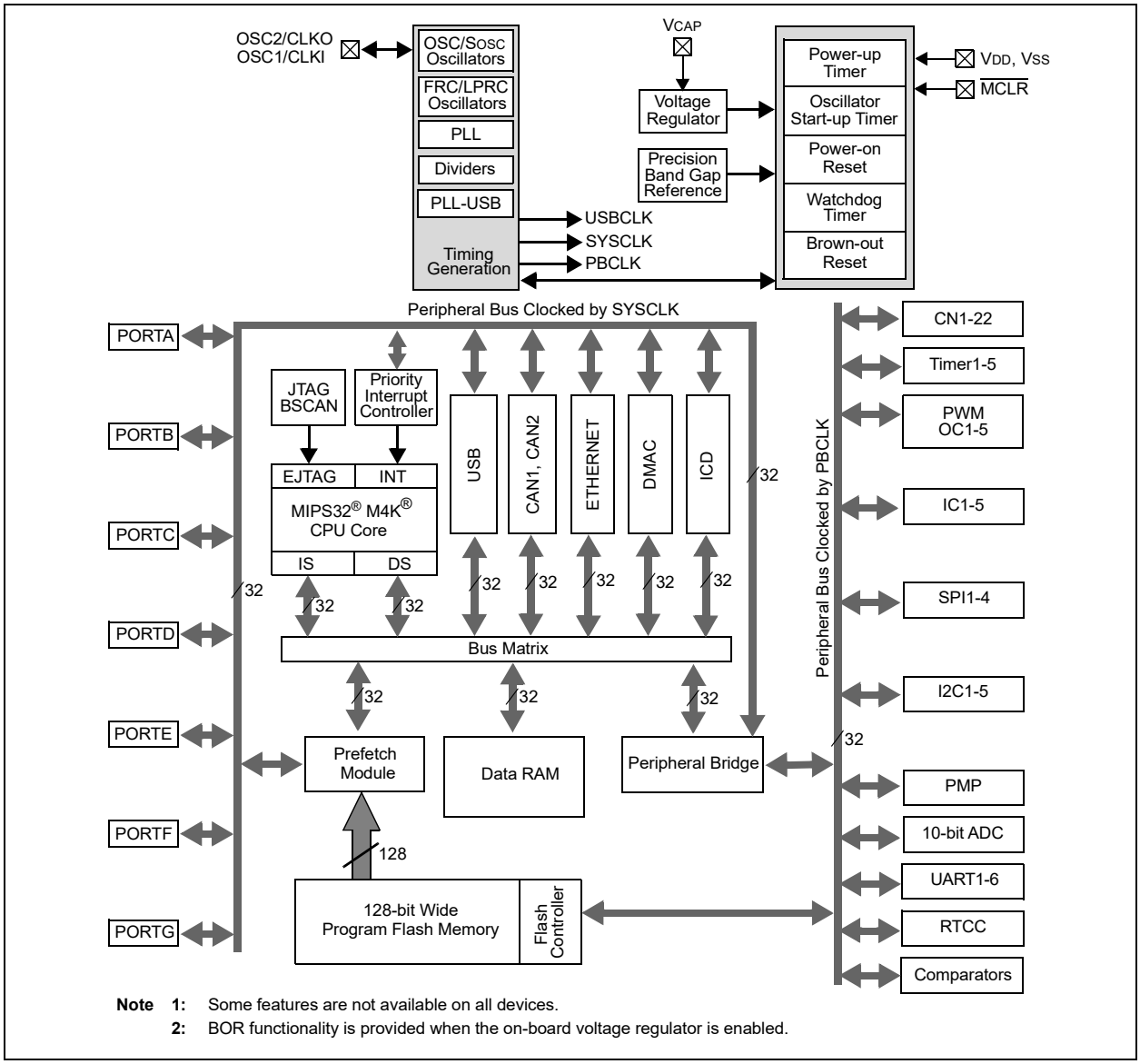
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX5XX/6XX/7XX devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX5XX/6XX/7XX family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: BLOCK DIAGRAM(1,2)**




**Note 1:** Some features are not available on all devices.
**2:** BOR functionality is provided when the on-board voltage regulator is enabled.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| AN0 | 16 | 25 | K2 | B14 | I | Analog | Analog input channels |
| AN1 | 15 | 24 | K1 | A15 | I | Analog | |
| AN2 | 14 | 23 | J2 | B13 | I | Analog | |
| AN3 | 13 | 22 | J1 | A13 | I | Analog | |
| AN4 | 12 | 21 | H2 | B11 | I | Analog | |
| AN5 | 11 | 20 | H1 | A12 | I | Analog | |
| AN6 | 17 | 26 | L1 | A20 | I | Analog | |
| AN7 | 18 | 27 | J3 | B16 | I | Analog | |
| AN8 | 21 | 32 | K4 | A23 | I | Analog | |
| AN9 | 22 | 33 | L4 | B19 | I | Analog | |
| AN10 | 23 | 34 | L5 | A24 | I | Analog | |
| AN11 | 24 | 35 | J5 | B20 | I | Analog | |
| AN12 | 27 | 41 | J7 | B23 | I | Analog | |
| AN13 | 28 | 42 | L7 | A28 | I | Analog | |
| AN14 | 29 | 43 | K7 | B24 | I | Analog | |
| AN15 | 30 | 44 | L8 | A29 | I | Analog | |
| CLKI | 39 | 63 | F9 | B34 | I | ST/ CMOS | External clock source input. Always associated with OSC1 pin function. |
| CLKO | 40 | 64 | F11 | A42 | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | 39 | 63 | F9 | B34 | I | ST/ CMOS | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | 40 | 64 | F11 | A42 | I/O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| SOSCI | 47 | 73 | C10 | A47 | I | ST/ CMOS | 32.768 kHz low-power oscillator crystal input; CMOS otherwise |
| SOSCO | 48 | 74 | B11 | B40 | O | — | 32.768 kHz low-power oscillator crystal output |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input; TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| CN0 | 48 | 74 | B11 | B40 | I | ST | Change notification inputs. Can be software programmed for internal weak pull-ups on all inputs. |
| CN1 | 47 | 73 | C10 | A47 | I | ST | |
| CN2 | 16 | 25 | K2 | B14 | I | ST | |
| CN3 | 15 | 24 | K1 | A15 | I | ST | |
| CN4 | 14 | 23 | J2 | B13 | I | ST | |
| CN5 | 13 | 22 | J1 | A13 | I | ST | |
| CN6 | 12 | 21 | H2 | B11 | I | ST | |
| CN7 | 11 | 20 | H1 | A12 | I | ST | |
| CN8 | 4 | 10 | E3 | A7 | I | ST | |
| CN9 | 5 | 11 | F4 | B6 | I | ST | |
| CN10 | 6 | 12 | F2 | A8 | I | ST | |
| CN11 | 8 | 14 | F3 | A9 | I | ST | |
| CN12 | 30 | 44 | L8 | A29 | I | ST | |
| CN13 | 52 | 81 | C8 | B44 | I | ST | |
| CN14 | 53 | 82 | B8 | A55 | I | ST | |
| CN15 | 54 | 83 | D7 | B45 | I | ST | |
| CN16 | 55 | 84 | C7 | A56 | I | ST | |
| CN17 | 31 | 49 | L10 | B27 | I | ST | |
| CN18 | 32 | 50 | L11 | A32 | I | ST | |
| CN19 | — | 80 | D8 | A54 | I | ST | |
| CN20 | — | 47 | L9 | B26 | I | ST | |
| CN21 | — | 48 | K9 | A31 | I | ST | |
| IC1 | 42 | 68 | E9 | B37 | I | ST | Capture Inputs 1-5 |
| IC2 | 43 | 69 | E10 | A45 | I | ST | |
| IC3 | 44 | 70 | D11 | B38 | I | ST | |
| IC4 | 45 | 71 | C11 | A46 | I | ST | |
| IC5 | 52 | 79 | A9 | A60 | I | ST | |
| OCFA | 17 | 26 | L1 | A20 | I | ST | Output Compare Fault A Input |
| OC1 | 46 | 72 | D9 | B39 | O | — | Output Compare Output 1 |
| OC2 | 49 | 76 | A11 | A52 | O | — | Output Compare Output 2 |
| OC3 | 50 | 77 | A10 | B42 | O | — | Output Compare Output 3 |
| OC4 | 51 | 78 | B9 | A53 | O | — | Output Compare Output 4 |
| OC5 | 52 | 81 | C8 | B44 | O | — | Output Compare Output 5 |
| OCFB | 30 | 44 | L8 | A29 | I | ST | Output Compare Fault B Input |
| INT0 | 46 | 72 | D9 | B39 | I | ST | External Interrupt 0 |
| INT1 | 42 | 18 | G1 | A11 | I | ST | External Interrupt 1 |
| INT2 | 43 | 19 | G2 | B10 | I | ST | External Interrupt 2 |
| INT3 | 44 | 66 | E11 | B36 | I | ST | External Interrupt 3 |
| INT4 | 45 | 67 | E8 | A44 | I | ST | External Interrupt 4 |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| RA0 | — | 17 | G3 | B9 | I/O | ST | PORTA is a bidirectional I/O port |
| RA1 | — | 38 | J6 | A26 | I/O | ST | |
| RA2 | — | 58 | H11 | A39 | I/O | ST | |
| RA3 | — | 59 | G10 | B32 | I/O | ST | |
| RA4 | — | 60 | G11 | A40 | I/O | ST | |
| RA5 | — | 61 | G9 | B33 | I/O | ST | |
| RA6 | — | 91 | C5 | B51 | I/O | ST | |
| RA7 | — | 92 | B5 | A62 | I/O | ST | |
| RA9 | — | 28 | L2 | A21 | I/O | ST | |
| RA10 | — | 29 | K3 | B17 | I/O | ST | |
| RA14 | — | 66 | E11 | B36 | I/O | ST | |
| RA15 | — | 67 | E8 | A44 | I/O | ST | |
| RB0 | 16 | 25 | K2 | B14 | I/O | ST | PORTB is a bidirectional I/O port |
| RB1 | 15 | 24 | K1 | A15 | I/O | ST | |
| RB2 | 14 | 23 | J2 | B13 | I/O | ST | |
| RB3 | 13 | 22 | J1 | A13 | I/O | ST | |
| RB4 | 12 | 21 | H2 | B11 | I/O | ST | |
| RB5 | 11 | 20 | H1 | A12 | I/O | ST | |
| RB6 | 17 | 26 | L1 | A20 | I/O | ST | |
| RB7 | 18 | 27 | J3 | B16 | I/O | ST | |
| RB8 | 21 | 32 | K4 | A23 | I/O | ST | |
| RB9 | 22 | 33 | L4 | B19 | I/O | ST | |
| RB10 | 23 | 34 | L5 | A24 | I/O | ST | |
| RB11 | 24 | 35 | J5 | B20 | I/O | ST | |
| RB12 | 27 | 41 | J7 | B23 | I/O | ST | |
| RB13 | 28 | 42 | L7 | A28 | I/O | ST | |
| RB14 | 29 | 43 | K7 | B24 | I/O | ST | |
| RB15 | 30 | 44 | L8 | A29 | I/O | ST | |
| RC1 | — | 6 | D1 | A5 | I/O | ST | PORTC is a bidirectional I/O port |
| RC2 | — | 7 | E4 | B4 | I/O | ST | |
| RC3 | — | 8 | E2 | A6 | I/O | ST | |
| RC4 | — | 9 | E1 | B5 | I/O | ST | |
| RC12 | 39 | 63 | F9 | B34 | I/O | ST | |
| RC13 | 47 | 73 | C10 | A47 | I/O | ST | |
| RC14 | 48 | 74 | B11 | B40 | I/O | ST | |
| RC15 | 40 | 64 | F11 | A42 | I/O | ST | |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| RD0 | 46 | 72 | D9 | B39 | I/O | ST | PORTD is a bidirectional I/O port |
| RD1 | 49 | 76 | A11 | A52 | I/O | ST | |
| RD2 | 50 | 77 | A10 | B42 | I/O | ST | |
| RD3 | 51 | 78 | B9 | A53 | I/O | ST | |
| RD4 | 52 | 81 | C8 | B44 | I/O | ST | |
| RD5 | 53 | 82 | B8 | A55 | I/O | ST | |
| RD6 | 54 | 83 | D7 | B45 | I/O | ST | |
| RD7 | 55 | 84 | C7 | A56 | I/O | ST | |
| RD8 | 42 | 68 | E9 | B37 | I/O | ST | |
| RD9 | 43 | 69 | E10 | A45 | I/O | ST | |
| RD10 | 44 | 70 | D11 | B38 | I/O | ST | |
| RD11 | 45 | 71 | C11 | A46 | I/O | ST | |
| RD12 | — | 79 | A9 | B43 | I/O | ST | |
| RD13 | — | 80 | D8 | A54 | I/O | ST | |
| RD14 | — | 47 | L9 | B26 | I/O | ST | |
| RD15 | — | 48 | K9 | A31 | I/O | ST | |
| RE0 | 60 | 93 | A4 | B52 | I/O | ST | PORTE is a bidirectional I/O port |
| RE1 | 61 | 94 | B4 | A64 | I/O | ST | |
| RE2 | 62 | 98 | B3 | A66 | I/O | ST | |
| RE3 | 63 | 99 | A2 | B56 | I/O | ST | |
| RE4 | 64 | 100 | A1 | A67 | I/O | ST | |
| RE5 | 1 | 3 | D3 | B2 | I/O | ST | |
| RE6 | 2 | 4 | C1 | A4 | I/O | ST | |
| RE7 | 3 | 5 | D2 | B3 | I/O | ST | |
| RE8 | — | 18 | G1 | A11 | I/O | ST | |
| RE9 | — | 19 | G2 | B10 | I/O | ST | |
| RF0 | 58 | 87 | B6 | B49 | I/O | ST | PORTF is a bidirectional I/O port |
| RF1 | 59 | 88 | A6 | A60 | I/O | ST | |
| RF2 | — | 52 | K11 | A36 | I/O | ST | |
| RF3 | 33 | 51 | K10 | A35 | I/O | ST | |
| RF4 | 31 | 49 | L10 | B27 | I/O | ST | |
| RF5 | 32 | 50 | L11 | A32 | I/O | ST | |
| RF8 | — | 53 | J10 | B29 | I/O | ST | |
| RF12 | — | 40 | K6 | A27 | I/O | ST | |
| RF13 | — | 39 | L6 | B22 | I/O | ST | |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| RG0 | — | 90 | A5 | A61 | I/O | ST | PORTG is a bidirectional I/O port |
| RG1 | — | 89 | E6 | B50 | I/O | ST | |
| RG6 | 4 | 10 | E3 | A7 | I/O | ST | |
| RG7 | 5 | 11 | F4 | B6 | I/O | ST | |
| RG8 | 6 | 12 | F2 | A8 | I/O | ST | |
| RG9 | 8 | 14 | F3 | A9 | I/O | ST | |
| RG12 | — | 96 | C3 | A65 | I/O | ST | |
| RG13 | — | 97 | A3 | B55 | I/O | ST | |
| RG14 | — | 95 | C4 | B54 | I/O | ST | |
| RG15 | — | 1 | B2 | A2 | I/O | ST | |
| RG2 | 37 | 57 | H10 | B31 | I | ST | PORTG input pins |
| RG3 | 36 | 56 | J11 | A38 | I | ST | |
| T1CK | 48 | 74 | B11 | B40 | I | ST | Timer1 external clock input |
| T2CK | — | 6 | D1 | A5 | I | ST | Timer2 external clock input |
| T3CK | — | 7 | E4 | B4 | I | ST | Timer3 external clock input |
| T4CK | — | 8 | E2 | A6 | I | ST | Timer4 external clock input |
| T5CK | — | 9 | E1 | B5 | I | ST | Timer5 external clock input |
| $\overline{U1CTS}$ | 43 | 47 | L9 | B26 | I | ST | UART1 clear to send |
| $\overline{U1RTS}$ | 49 | 48 | K9 | A31 | O | — | UART1 ready to send |
| U1RX | 50 | 52 | K11 | A36 | I | ST | UART1 receive |
| U1TX | 51 | 53 | J10 | B29 | O | — | UART1 transmit |
| $\overline{U3CTS}$ | 8 | 14 | F3 | A9 | I | ST | UART3 clear to send |
| $\overline{U3RTS}$ | 4 | 10 | E3 | A7 | O | — | UART3 ready to send |
| U3RX | 5 | 11 | F4 | B6 | I | ST | UART3 receive |
| U3TX | 6 | 12 | F2 | A8 | O | — | UART3 transmit |
| $\overline{U2CTS}$ | 21 | 40 | K6 | A27 | I | ST | UART2 clear to send |
| $\overline{U2RTS}$ | 29 | 39 | L6 | B22 | O | — | UART2 ready to send |
| U2RX | 31 | 49 | L10 | B27 | I | ST | UART2 receive |
| U2TX | 32 | 50 | L11 | A32 | O | — | UART2 transmit |
| U4RX | 43 | 47 | L9 | B26 | I | ST | UART4 receive |
| U4TX | 49 | 48 | K9 | A31 | O | — | UART4 transmit |
| U6RX | 8 | 14 | F3 | A9 | I | ST | UART6 receive |
| U6TX | 4 | 10 | E3 | A7 | O | — | UART6 transmit |
| U5RX | 21 | 40 | K6 | A27 | I | ST | UART5 receive |
| U5TX | 29 | 39 | L6 | B22 | O | — | UART5 transmit |
| SCK1 | — | 70 | D11 | B38 | I/O | ST | Synchronous serial clock input/output for SPI1 |

**Legend:** CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| SDI1 | — | 9 | E1 | B5 | I | ST | SPI1 data in |
| SDO1 | — | 72 | D9 | B39 | O | — | SPI1 data out |
| $\overline{SS1}$ | — | 69 | E10 | A45 | I/O | ST | SPI1 slave synchronization or frame pulse I/O |
| SCK3 | 49 | 48 | K9 | A31 | I/O | ST | Synchronous serial clock input/output for SPI3 |
| SDI3 | 50 | 52 | K11 | A36 | I | ST | SPI3 data in |
| SDO3 | 51 | 53 | J10 | B29 | O | — | SPI3 data out |
| $\overline{SS3}$ | 43 | 47 | L9 | B26 | I/O | ST | SPI3 slave synchronization or frame pulse I/O |
| SCK2 | 4 | 10 | E3 | A7 | I/O | ST | Synchronous serial clock input/output for SPI2 |
| SDI2 | 5 | 11 | F4 | B6 | I | ST | SPI2 data in |
| SDO2 | 6 | 12 | F2 | A8 | O | — | SPI2 data out |
| $\overline{SS2}$ | 8 | 14 | F3 | A9 | I/O | ST | SPI2 slave synchronization or frame pulse I/O |
| SCK4 | 29 | 39 | L6 | B22 | I/O | ST | Synchronous serial clock input/output for SPI4 |
| SDI4 | 31 | 49 | L10 | B27 | I | ST | SPI4 data in |
| SDO4 | 32 | 50 | L11 | A32 | O | — | SPI4 data out |
| $\overline{SS4}$ | 21 | 40 | K6 | A27 | I/O | ST | SPI4 slave synchronization or frame pulse I/O |
| SCL1 | 44 | 66 | E11 | B36 | I/O | ST | Synchronous serial clock input/output for I2C1 |
| SDA1 | 43 | 67 | E8 | A44 | I/O | ST | Synchronous serial data input/output for I2C1 |
| SCL3 | 51 | 53 | J10 | B29 | I/O | ST | Synchronous serial clock input/output for I2C3 |
| SDA3 | 50 | 52 | K11 | A36 | I/O | ST | Synchronous serial data input/output for I2C3 |
| SCL2 | — | 58 | H11 | A39 | I/O | ST | Synchronous serial clock input/output for I2C2 |
| SDA2 | — | 59 | G10 | B32 | I/O | ST | Synchronous serial data input/output for I2C2 |
| SCL4 | 6 | 12 | F2 | A8 | I/O | ST | Synchronous serial clock input/output for I2C4 |
| SDA4 | 5 | 11 | F4 | B6 | I/O | ST | Synchronous serial data input/output for I2C4 |
| SCL5 | 32 | 50 | L11 | A32 | I/O | ST | Synchronous serial clock input/output for I2C5 |
| SDA5 | 31 | 49 | L10 | B27 | I/O | ST | Synchronous serial data input/output for I2C5 |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| TMS | 23 | 17 | G3 | B9 | I | ST | JTAG Test mode select pin |
| TCK | 27 | 38 | J6 | A26 | I | ST | JTAG test clock input pin |
| TDI | 28 | 60 | G11 | A40 | I | ST | JTAG test data input pin |
| TDO | 24 | 61 | G9 | B33 | O | — | JTAG test data output pin |
| RTCC | 42 | 68 | E9 | B37 | O | — | Real-Time Clock alarm output |
| CVREF- | 15 | 28 | L2 | A21 | I | Analog | Comparator Voltage Reference (low) |
| CVREF+ | 16 | 29 | K3 | B17 | I | Analog | Comparator Voltage Reference (high) |
| CVREFOUT | 23 | 34 | L5 | A24 | O | Analog | Comparator Voltage Reference output |
| C1IN- | 12 | 21 | H2 | B11 | I | Analog | Comparator 1 negative input |
| C1IN+ | 11 | 20 | H1 | A12 | I | Analog | Comparator 1 positive input |
| C1OUT | 21 | 32 | K4 | A23 | O | — | Comparator 1 output |
| C2IN- | 14 | 23 | J2 | B13 | I | Analog | Comparator 2 negative input |
| C2IN+ | 13 | 22 | J1 | A13 | I | Analog | Comparator 2 positive input |
| C2OUT | 22 | 33 | L4 | B19 | O | — | Comparator 2 output |
| PMA0 | 30 | 44 | L8 | A29 | I/O | TTL/ST | Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes) |
| PMA1 | 29 | 43 | K7 | B24 | I/O | TTL/ST | Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes) |
| PMA2 | 8 | 14 | F3 | A9 | O | — | Parallel Master Port address (Demultiplexed Master modes) |
| PMA3 | 6 | 12 | F2 | A8 | O | — | |
| PMA4 | 5 | 11 | F4 | B6 | O | — | |
| PMA5 | 4 | 10 | E3 | A7 | O | — | |
| PMA6 | 16 | 29 | K3 | B17 | O | — | |
| PMA7 | 22 | 28 | L2 | A21 | O | — | |
| PMA8 | 32 | 50 | L11 | A32 | O | — | |
| PMA9 | 31 | 49 | L10 | B27 | O | — | |
| PMA10 | 28 | 42 | L7 | A28 | O | — | |
| PMA11 | 27 | 41 | J7 | B23 | O | — | |
| PMA12 | 24 | 35 | J5 | B20 | O | — | |
| PMA13 | 23 | 34 | L5 | A24 | O | — | |
| PMA14 | 45 | 71 | C11 | A46 | O | — | |
| PMA15 | 44 | 70 | D11 | B38 | O | — | |
| PMCS1 | 45 | 71 | C11 | A46 | O | — | Parallel Master Port Chip Select 1 strobe |
| PMCS2 | 44 | 70 | D11 | B38 | O | — | Parallel Master Port Chip Select 2 strobe |

**Legend:** CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| PMD0 | 60 | 93 | A4 | B52 | I/O | TTL/ST | Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes) |
| PMD1 | 61 | 94 | B4 | A64 | I/O | TTL/ST | |
| PMD2 | 62 | 98 | B3 | A66 | I/O | TTL/ST | |
| PMD3 | 63 | 99 | A2 | B56 | I/O | TTL/ST | |
| PMD4 | 64 | 100 | A1 | A67 | I/O | TTL/ST | |
| PMD5 | 1 | 3 | D3 | B2 | I/O | TTL/ST | |
| PMD6 | 2 | 4 | C1 | A4 | I/O | TTL/ST | |
| PMD7 | 3 | 5 | D2 | B3 | I/O | TTL/ST | |
| PMD8 | — | 90 | A5 | A61 | I/O | TTL/ST | |
| PMD9 | — | 89 | E6 | B50 | I/O | TTL/ST | |
| PMD10 | — | 88 | A6 | A60 | I/O | TTL/ST | |
| PMD11 | — | 87 | B6 | B49 | I/O | TTL/ST | |
| PMD12 | — | 79 | A9 | B43 | I/O | TTL/ST | |
| PMD13 | — | 80 | D8 | A54 | I/O | TTL/ST | |
| PMD14 | — | 83 | D7 | B45 | I/O | TTL/ST | |
| PMD15 | — | 84 | C7 | A56 | I/O | TTL/ST | |
| PMALL | 30 | 44 | L8 | A29 | O | — | Parallel Master Port address latch enable low byte (Multiplexed Master modes) |
| PMALH | 29 | 43 | K7 | B24 | O | — | Parallel Master Port address latch enable high byte (Multiplexed Master modes) |
| PMRD | 53 | 82 | B8 | A55 | O | — | Parallel Master Port read strobe |
| PMWR | 52 | 81 | C8 | B44 | O | — | Parallel Master Port write strobe |
| VBUS | 34 | 54 | H8 | A37 | I | Analog | USB bus power monitor |
| VUSB3V3 | 35 | 55 | H9 | B30 | P | — | USB internal transceiver supply. If the USB module is *not* used, this pin must be connected to VDD. |
| VBUSON | 11 | 20 | H1 | A12 | O | — | USB Host and OTG bus power control output |
| D+ | 37 | 57 | H10 | B31 | I/O | Analog | USB D+ |
| D- | 36 | 56 | J11 | A38 | I/O | Analog | USB D- |
| USBID | 33 | 51 | K10 | A35 | I | ST | USB OTG ID detect |
| C1RX | 58 | 87 | B6 | B49 | I | ST | CAN1 bus receive pin |
| C1TX | 59 | 88 | A6 | A60 | O | — | CAN1 bus transmit pin |
| AC1RX | 32 | 40 | K6 | A27 | I | ST | Alternate CAN1 bus receive pin |
| AC1TX | 31 | 39 | L6 | B22 | O | — | Alternate CAN1 bus transmit pin |
| C2RX | 29 | 90 | A5 | A61 | I | ST | CAN2 bus receive pin |
| C2TX | 21 | 89 | E6 | B50 | O | — | CAN2 bus transmit pin |
| AC2RX | — | 8 | E2 | A6 | 1 | ST | Alternate CAN2 bus receive pin |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| AC2TX | — | 7 | E4 | B4 | O | — | Alternate CAN2 bus transmit pin |
| ERXD0 | 61 | 41 | J7 | B23 | I | ST | Ethernet Receive Data 0(2) |
| ERXD1 | 60 | 42 | L7 | A28 | I | ST | Ethernet Receive Data 1(2) |
| ERXD2 | 59 | 43 | K7 | B24 | I | ST | Ethernet Receive Data 2(2) |
| ERXD3 | 58 | 44 | L8 | A29 | I | ST | Ethernet Receive Data 3(2) |
| ERXERR | 64 | 35 | J5 | B20 | I | ST | Ethernet receive error input(2) |
| ERXDV | 62 | 12 | F2 | A8 | I | ST | Ethernet receive data valid(2) |
| ECRSDV | 62 | 12 | F2 | A8 | I | ST | Ethernet carrier sense data valid(2) |
| ERXCLK | 63 | 14 | F3 | A9 | I | ST | Ethernet receive clock(2) |
| EREFCLK | 63 | 14 | F3 | A9 | I | ST | Ethernet reference clock(2) |
| ETXD0 | 2 | 88 | A6 | A60 | O | — | Ethernet Transmit Data 0(2) |
| ETXD1 | 3 | 87 | B6 | B49 | O | — | Ethernet Transmit Data 1(2) |
| ETXD2 | 43 | 79 | A9 | B43 | O | — | Ethernet Transmit Data 2(2) |
| ETXD3 | 42 | 80 | D8 | A54 | O | — | Ethernet Transmit Data 3(2) |
| ETXERR | 54 | 89 | E6 | B50 | O | — | Ethernet transmit error(2) |
| ETXEN | 1 | 83 | D7 | B45 | O | — | Ethernet transmit enable(2) |
| ETXCLK | 55 | 84 | C7 | A56 | I | ST | Ethernet transmit clock(2) |
| ECOL | 44 | 10 | E3 | A7 | I | ST | Ethernet collision detect(2) |
| ECRS | 45 | 11 | F4 | B6 | I | ST | Ethernet carrier sense(2) |
| EMDC | 30 | 71 | C11 | A46 | O | — | Ethernet management data clock(2) |
| EMDIO | 49 | 68 | E9 | B37 | I/O | — | Ethernet management data(2) |
| AERXD0 | 43 | 18 | G1 | A11 | I | ST | Alternate Ethernet Receive Data 0(2) |
| AERXD1 | 42 | 19 | G2 | B10 | I | ST | Alternate Ethernet Receive Data 1(2) |
| AERXD2 | — | 28 | L2 | A21 | I | ST | Alternate Ethernet Receive Data 2(2) |
| AERXD3 | — | 29 | K3 | B17 | I | ST | Alternate Ethernet Receive Data 3(2) |
| AERXERR | 55 | 1 | B2 | A2 | I | ST | Alternate Ethernet receive error input(2) |
| AERXDV | — | 12 | F2 | A8 | I | ST | Alternate Ethernet receive data valid(2) |
| AECRSDV | 44 | 12 | F2 | A8 | I | ST | Alternate Ethernet carrier sense data valid(2) |
| AERXCLK | — | 14 | F3 | A9 | I | ST | Alternate Ethernet receive clock(2) |
| AEREFCLK | 45 | 14 | F3 | A9 | I | ST | Alternate Ethernet reference clock(2) |
| AETXD0 | 59 | 47 | L9 | B26 | O | — | Alternate Ethernet Transmit Data 0(2) |
| AETXD1 | 58 | 48 | K9 | A31 | O | — | Alternate Ethernet Transmit Data 1(2) |
| AETXD2 | — | 44 | L8 | A29 | O | — | Alternate Ethernet Transmit Data 2(2) |
| AETXD3 | — | 43 | K7 | B24 | O | — | Alternate Ethernet Transmit Data 3(2) |
| AETXERR | — | 35 | J5 | B20 | O | — | Alternate Ethernet transmit error(2) |
| AETXEN | 54 | 67 | E8 | A44 | O | — | Alternate Ethernet transmit enable(2) |
| AETXCLK | — | 66 | E11 | B36 | I | ST | Alternate Ethernet transmit clock(2) |
| AECOL | — | 42 | L7 | A28 | I | ST | Alternate Ethernet collision detect(2) |

**Legend:** CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; TTL = TTL input buffer; Analog = Analog input; O = Output; P = Power; I = Input

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 64-Pin QFN/TQFP | 100-Pin TQFP | 121-Pin TFBGA | 124-pin VTLA | | | |
| AECRS | — | 41 | J7 | B23 | I | ST | Alternate Ethernet carrier sense(2) |
| AEMDC | 30 | 71 | C11 | A46 | O | — | Alternate Ethernet Management Data clock(2) |
| AEMDIO | 49 | 68 | E9 | B37 | I/O | — | Alternate Ethernet Management Data(2) |
| TRCLK | — | 91 | C5 | B51 | O | — | Trace clock |
| TRD0 | — | 97 | A3 | B55 | O | — | Trace Data bits 0-3 |
| TRD1 | — | 96 | C3 | A65 | O | — | |
| TRD2 | — | 95 | C4 | B54 | O | — | |
| TRD3 | — | 92 | B5 | A62 | O | — | |
| PGED1 | 16 | 25 | K2 | B14 | I/O | ST | Data I/O pin for Programming/ Debugging Communication Channel 1 |
| PGEC1 | 15 | 24 | K1 | A15 | I | ST | Clock input pin for Programming/ Debugging Communication Channel 1 |
| PGED2 | 18 | 27 | J3 | B16 | I/O | ST | Data I/O pin for Programming/ Debugging Communication Channel 2 |
| PGEC2 | 17 | 26 | L1 | A20 | I | ST | Clock input pin for Programming/ Debugging Communication Channel 2 |
| $\overline{MCLR}$ | 7 | 13 | F1 | B7 | I/P | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD | 19 | 30 | J4 | A22 | P | P | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | 20 | 31 | L3 | B18 | P | P | Ground reference for analog modules |
| VDD | 10, 26, 38, 57 | 2, 16, 37, 46, 62, 86 | A7, C2, C9, E5, K8, F8, G5, H4, H6 | A10, A14, A30, A41, A48, A59, B1, B21, B53 | P | — | Positive supply for peripheral logic and I/O pins |
| VCAP | 56 | 85 | B7 | B48 | P | — | Capacitor for Internal Voltage Regulator |
| VSS | 9, 25, 41 | 15, 36, 45, 65, 75 | A8, B10, D4, D5, E7, F5, F10, G6, G7, H3 | A3, A25, A43, A63, B8, B12, B25, B41, B46 | P | — | Ground reference for logic and I/O pins. This pin must be connected at all times. |
| VREF+ | 16 | 29 | K3 | B17 | I | Analog | Analog voltage reference (high) input |
| VREF- | 15 | 28 | L2 | A21 | I | Analog | Analog voltage reference (low) input |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

**Note 1:** Pin numbers are only provided for reference. See the **"Device Pin Tables"** section for device pin availability.

**2:** See **25.0 "Ethernet Controller"** for more information.

**NOTES:**


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# 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUS

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

## 2.1 Basic Connection Requirements

Getting started with the PIC32MX5XX/6XX/7XX family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **2.8 "External Oscillator Pins"**)

The following pin may be required, as well: VREF+/VREF- pins used when external voltage reference for ADC module is implemented.

**Note:** The AVDD and AVSS pins must be connected, regardless of the ADC use and the ADC voltage reference source.

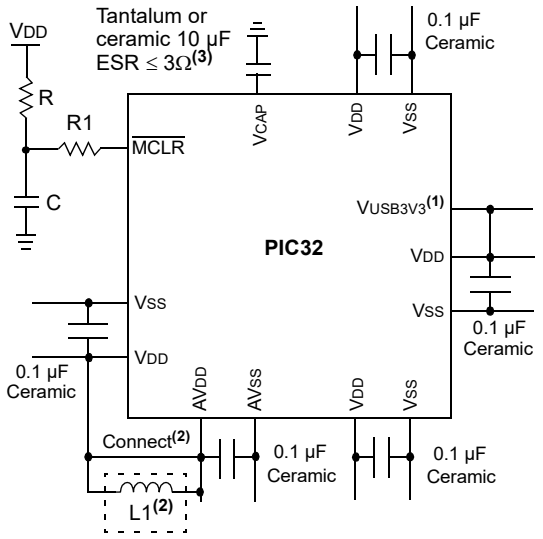
## 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




**Note 1:** If the USB module is not used, this pin must be connected to VDD.

**2:** As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 3Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

**3:** Aluminum or electrolytic capacitors should not be used. ESR ≤ 3Ω from -40°C to 125°C @ SYSCLK frequency (i.e., MIPS).

### 2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP)

### 2.3.1 INTERNAL REGULATOR MODE

A low-ESR (1 ohm) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a CEFC capacitor, with at least a 6V rating, connected to ground. The type can be ceramic or tantalum. Refer to **Section 32.0 "Electrical Characteristics"** for additional information on CEFC specifications.

## 2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

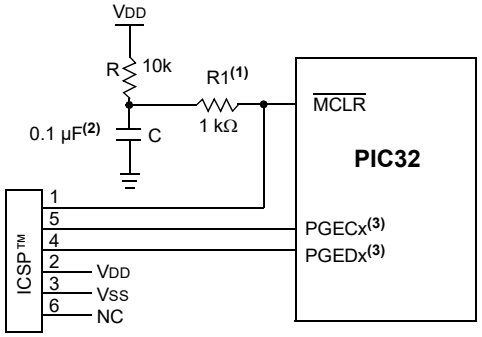
- Device Reset
- Device Programming and Debugging

Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS**




**Note 1:** 470Ω ≤ R1 ≤ 1kΩ will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the Debug/Programmer tools.

**2:** The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

**3:** No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.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## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB® REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS50001765)
- *"MPLAB® ICD 3 Design Advisory"* (DS50001764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" (*DS50001616)
- *"Using MPLAB® REAL ICE™ Emulator"* (poster) (DS50001749)

## 2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

## 2.7 Trace

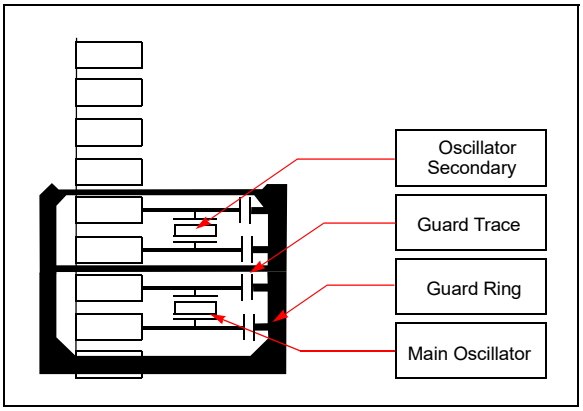
The trace pins can be connected to a hardware-trace-enabled programmer to provide a compress real time instruction trace. When used for trace the TRD3, TRD2, TRD1, TRD0 and TRCLK pins should be dedicated for this use. The trace hardware requires a 22Ω series resistor between the trace pins and the trace connector.

## 2.8 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. Refer to **Section 8.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

**FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT**



## 2.9 Configuration of Analog and Digital Pins During ICSP Operations

If MPLAB ICD 3 or REAL ICE is selected as a debugger, it automatically initializes all of the Analog-to-Digital input pins (ANx) as “digital” pins by setting all bits in the AD1PCFG register.

The bits in this register that correspond to the Analog-to-Digital pins that are initialized by MPLAB ICD 3 or REAL ICE, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain ADC pins as analog input pins during the debug session, the user application must clear the corresponding bits in the AD1PCFG register during initialization of the ADC module.

When MPLAB ICD 3 or REAL ICE is used as a programmer, the user application firmware must correctly configure the AD1PCFG register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all ADC pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

## 2.10 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to VSS through a 1k to 10k resistor and configuring the pin as an input.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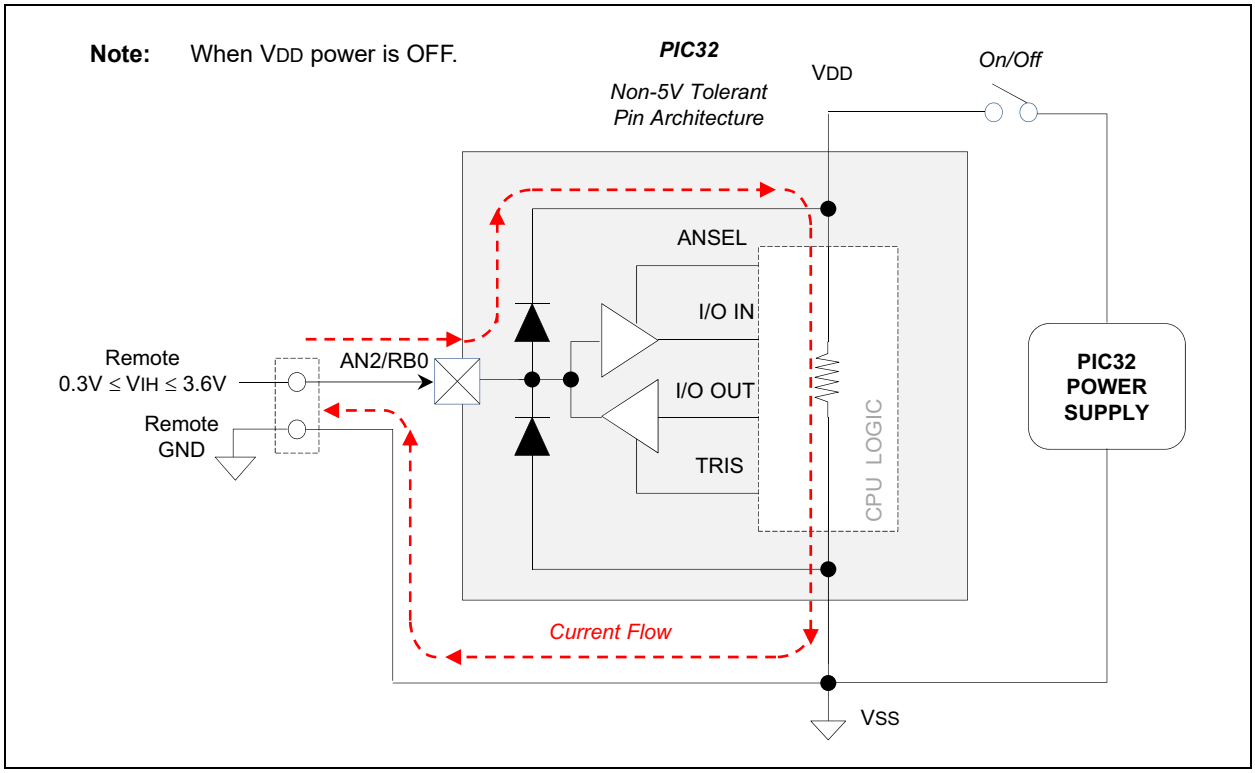
## 2.11 Considerations When Interfacing to Remotely Powered Circuits

### 2.11.1 NON-5V TOLERANT INPUT PINS

A quick review of the absolute maximum rating section in **36.0 "Electrical Characteristics"** will indicate that the voltage on any non-5v tolerant pin may not exceed VDD + 0.3V unless the input current is limited to meet the respective injection current specifications defined by parameters DI60a, DI60b, and DI60c in **TABLE 36-10: "DC Characteristics: I/O Pin Input Injection current Specifications"**. Figure 2-4 shows an example of a remote circuit using an independent power source, which is powered while connected to a PIC32 non-5V tolerant circuit that is not powered.

**FIGURE 2-4: PIC32 NON-5V TOLERANT CIRCUIT EXAMPLE**

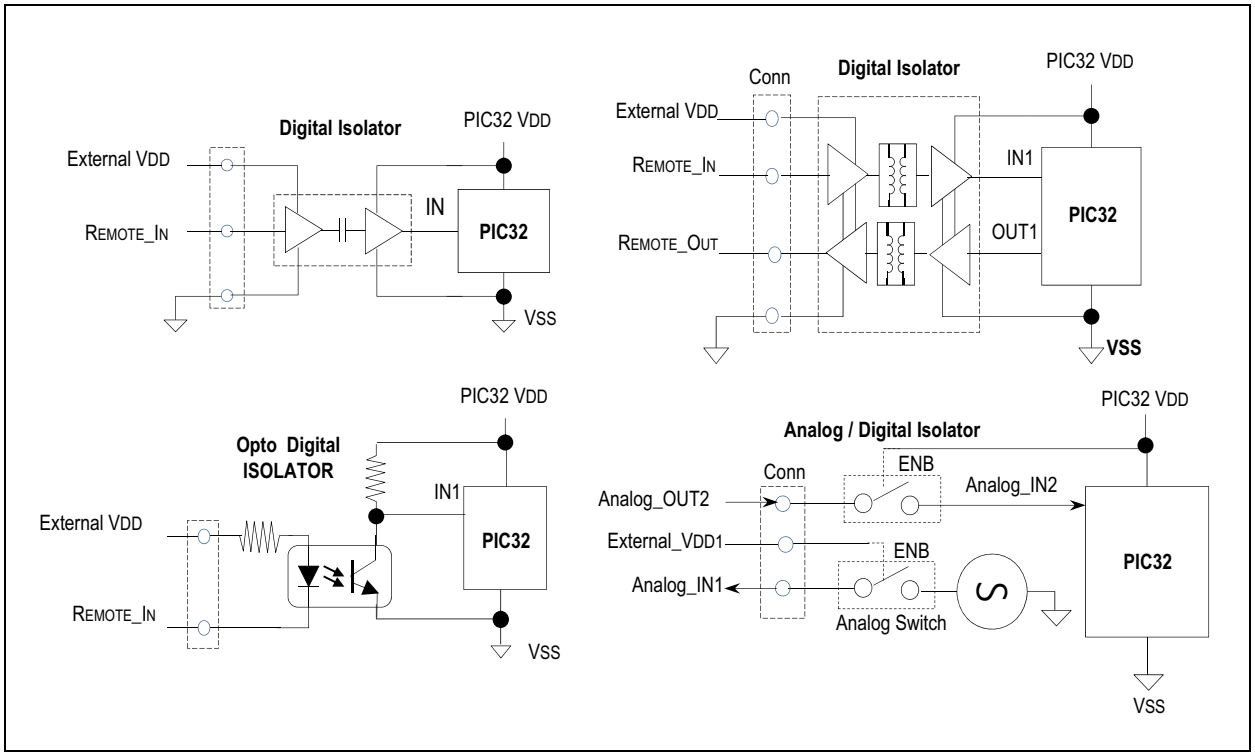



Without proper signal isolation, on non-5V tolerant pins, the remote signal can power the PIC32 device through the high side ESD protection diodes. Besides violating the absolute maximum rating specification when VDD of the PIC32 device is restored and ramping up or ramping down, it can also negatively affect the internal Power-on Reset (POR) and Brown-out Reset (BOR) circuits, which can lead to improper initialization of internal PIC32 logic circuits. In these cases, it is recommended to implement digital or analog signal isolation as depicted in Figure 2-5, as appropriate. This is indicative of all industry microcontrollers and not just Microchip products.

**TABLE 2-1: EXAMPLES OF DIGITAL/ANALOG ISOLATORS WITH OPTIONAL LEVEL TRANSLATION**

| Example Digital/Analog Signal Isolation Circuits | Inductive Coupling | Capacitive Coupling | Opto Coupling | Analog/Digital Switch |
|---|---|---|---|---|
| ADuM7241 / 40 ARZ (1 Mbps) | X | — | — | — |
| ADuM7241 / 40 CRZ (25 Mbps) | X | — | — | — |
| ISO721 | — | X | — | — |
| LTV-829S (2 Channel) | — | — | X | — |
| LTV-849S (4 Channel) | — | — | X | — |
| FSA266 / NC7WB66 | — | — | — | X |

**FIGURE 2-5: EXAMPLE DIGITAL/ANALOG SIGNAL ISOLATION CIRCUITS**




## 2.11.2 5V TOLERANT INPUT PINS

The internal high side diode on 5v tolerant pins are bussed to an internal floating node, rather than being connected to VDD, as shown in Figure 2-6. Voltages on these pins, if VDD < 2.3V, should not exceed roughly 3.2V relative to VSS of the PIC32 device. Voltage of 3.6V or higher will violate the absolute maximum specification, and will stress the oxide layer separating the high side floating node, which impacts device reliability. If a remotely powered “digital-only” signal can be guaranteed to always be ≤ 3.2V relative to Vss on the PIC32 device side, a 5V tolerant pin could be used without the need for a digital isolator. This is assuming there is not a ground loop issue, logic ground of the two circuits not at the same absolute level, and a remote logic low input is not less than VSS - 0.3V.


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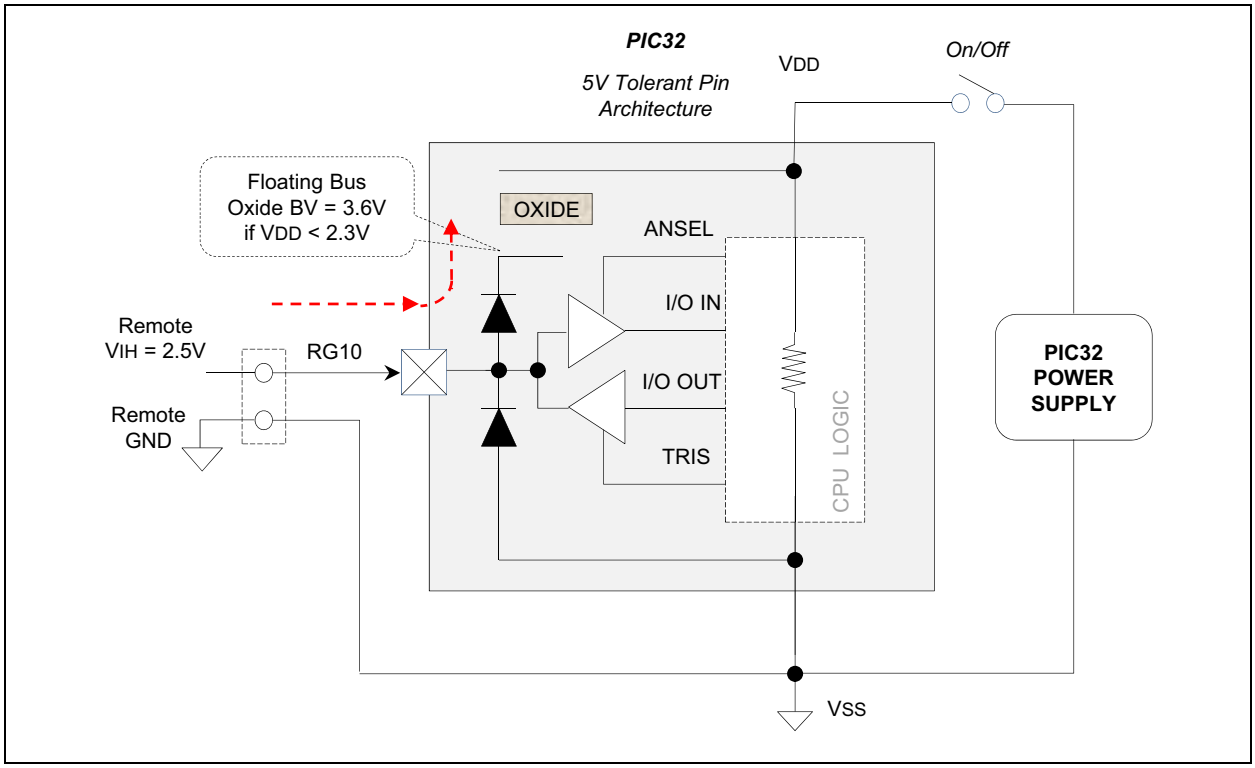
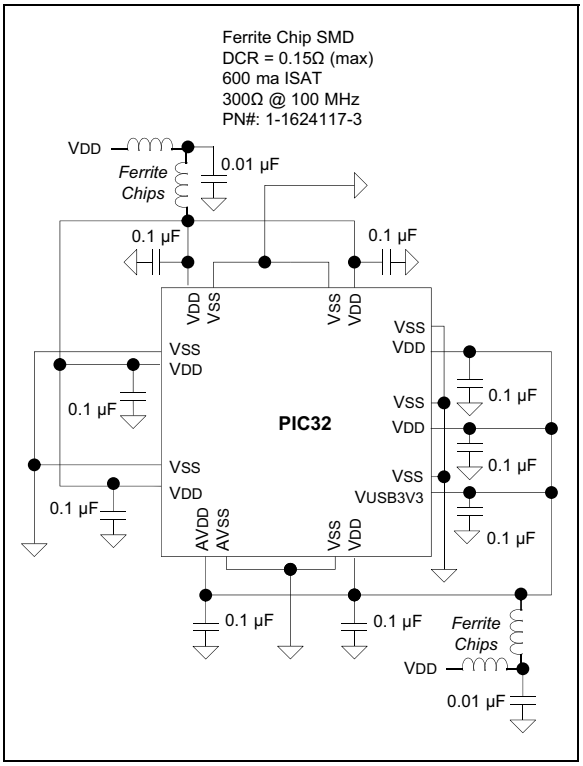
**FIGURE 2-6: PIC32 5V TOLERANT PIN ARCHITECTURE EXAMPLE**




## 2.12 EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations

The use of LDO regulators is preferred to reduce overall system noise and provide a cleaner power source. However, when utilizing switching Buck/Boost regulators as the local power source for PIC32 devices, as well as in electrically noisy environments or test conditions required for IEC 61000-4-4 and IEC 61000-4-2, users should evaluate the use of T-Filters (i.e., L-C-L) on the power pins, as shown in Figure 2-7. In addition to a more stable power source, use of this type of T-Filter can greatly reduce susceptibility to EMI sources and events.

**FIGURE 2-7: EMI/EMC/EFT SUPPRESSION CIRCUIT**



**NOTES:**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## 3.0 CPU

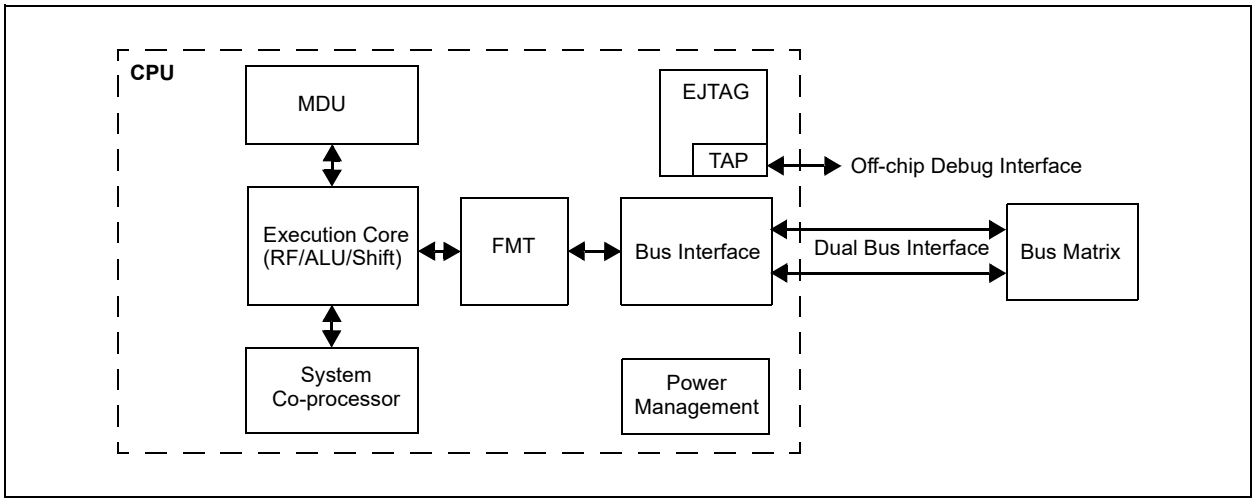
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS60001113) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). Resources for the MIPS32® M4K® Processor Core are available at http://www.imgtec.com.

The MIPS32® M4K® Processor core is the heart of the PIC32MX5XX/6XX/7XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

### 3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
- MIPS16e® code compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - `SAVE` and `RESTORE` macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8-bit and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- Simple dual bus interface
  - Independent 32-bit address and data busses
  - Transactions can be aborted to improve interrupt latency
- Autonomous multiply/divide unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG debug and instruction trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints
  - PC tracing with trace compression

**FIGURE 3-1: MIPS32® M4K® PROCESSOR CORE BLOCK DIAGRAM**



## 3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e® Support
- Enhanced JTAG (EJTAG) Controller

### 3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing bit-wise logical operations
- Shifter and store aligner

### 3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt)* operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16 bit wide *rs*, 15 iterations are skipped and for a 24 bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent `MDU` instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

**TABLE 3-1: MIPS32® M4K® CORE HIGH-PERFORMANCE INTEGER MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES**

| Opcode | Operand Size (mul *rt*) (div *rs*) | Latency | Repeat Rate |
|---|---|---|---|
| `MULT/MULTU, MADD/MADDU, MSUB/MSUBU` | 16 bits | 1 | 1 |
| | 32 bits | 2 | 2 |
| `MUL` | 16 bits | 2 | 1 |
| | 32 bits | 3 | 2 |
| `DIV/DIVU` | 8 bits | 12 | 11 |
| | 16 bits | 19 | 18 |
| | 24 bits | 26 | 25 |
| | 32 bits | 33 | 32 |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The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32 architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

### 3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

**TABLE 3-2: COPROCESSOR 0 REGISTERS**

| Register Number | Register Name | Function |
|---|---|---|
| 0-6 | Reserved | Reserved. |
| 7 | HWREna | Enables access via the RDHWR instruction to selected hardware registers. |
| 8 | BadVAddr(1) | Reports the address for the most recent address-related exception. |
| 9 | Count(1) | Processor cycle count. |
| 10 | Reserved | Reserved. |
| 11 | Compare(1) | Timer interrupt control. |
| 12 | Status(1) | Processor status and control. |
| 12 | IntCtl(1) | Interrupt system status and control. |
| 12 | SRSCtl(1) | Shadow register set status and control. |
| 12 | SRSMap(1) | Provides mapping from vectored interrupt to a shadow set. |
| 13 | Cause(1) | Cause of last general exception. |
| 14 | EPC(1) | Program counter at last exception. |
| 15 | PRId | Processor identification and revision. |
| 15 | Ebase | Exception vector base register. |
| 16 | Config | Configuration register. |
| 16 | Config1 | Configuration Register 1. |
| 16 | Config2 | Configuration Register 2. |
| 16 | Config3 | Configuration Register 3. |
| 17-22 | Reserved | Reserved. |
| 23 | Debug(2) | Debug control and exception status. |
| 24 | DEPC(2) | Program counter at last debug exception. |
| 25-29 | Reserved | Reserved. |
| 30 | ErrorEPC(1) | Program counter at last error. |
| 31 | DESAVE(2) | Debug handler scratchpad register. |

**Note 1:** Registers used in exception processing.

**2:** Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

**TABLE 3-3: PIC32MX5XX/6XX/7XX FAMILY CORE EXCEPTION TYPES**

| Exception | Description |
|---|---|
| Reset | Assertion $\overline{\text{MCLR}}$ or a Power-on Reset (POR). |
| DSS | EJTAG debug single step. |
| DINT | EJTAG debug interrupt. Caused by the assertion of the external *EJ_DINT* input or by setting the EjtagBrk bit in the ECR register. |
| NMI | Assertion of NMI signal. |
| Interrupt | Assertion of unmasked hardware or software interrupt signal. |
| DIB | EJTAG debug hardware instruction break matched. |
| AdEL | Fetch address alignment error.<br>Fetch reference to protected address. |
| IBE | Instruction fetch bus error. |
| DBp | EJTAG breakpoint (execution of SDBBP instruction). |
| Sys | Execution of SYSCALL instruction. |
| Bp | Execution of BREAK instruction. |
| RI | Execution of a reserved instruction. |
| CpU | Execution of a coprocessor instruction for a coprocessor that is not enabled. |
| CEU | Execution of a CorExtend instruction when CorExtend is not enabled. |
| Ov | Execution of an arithmetic instruction that overflowed. |
| Tr | Execution of a trap (when trap condition is true). |
| DDBL/DDBS | EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value). |
| AdEL | Load address alignment error.<br>Load reference to protected address. |
| AdES | Store address alignment error.<br>Store to protected address. |
| DBE | Load or store bus error. |
| DDBL | EJTAG data hardware breakpoint matched in load data compare. |


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## 3.3 Power Management

The MIPS32 M4K Processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during idle periods.

### 3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see **Section 28.0 "Power-Saving Features"**.

### 3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX5XX/6XX/7XX family core is in the clock tree and clocking registers. The PIC32 family uses extensive use of local gated clocks to reduce this dynamic power consumption.

## 3.4 EJTAG Debug Support

The MIPS32 M4K Processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the MIPS M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the MIPS32 M4K processor core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

**NOTES:**


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# 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX5XX/6XX/7XX devices to execute from data memory.

Key features include:

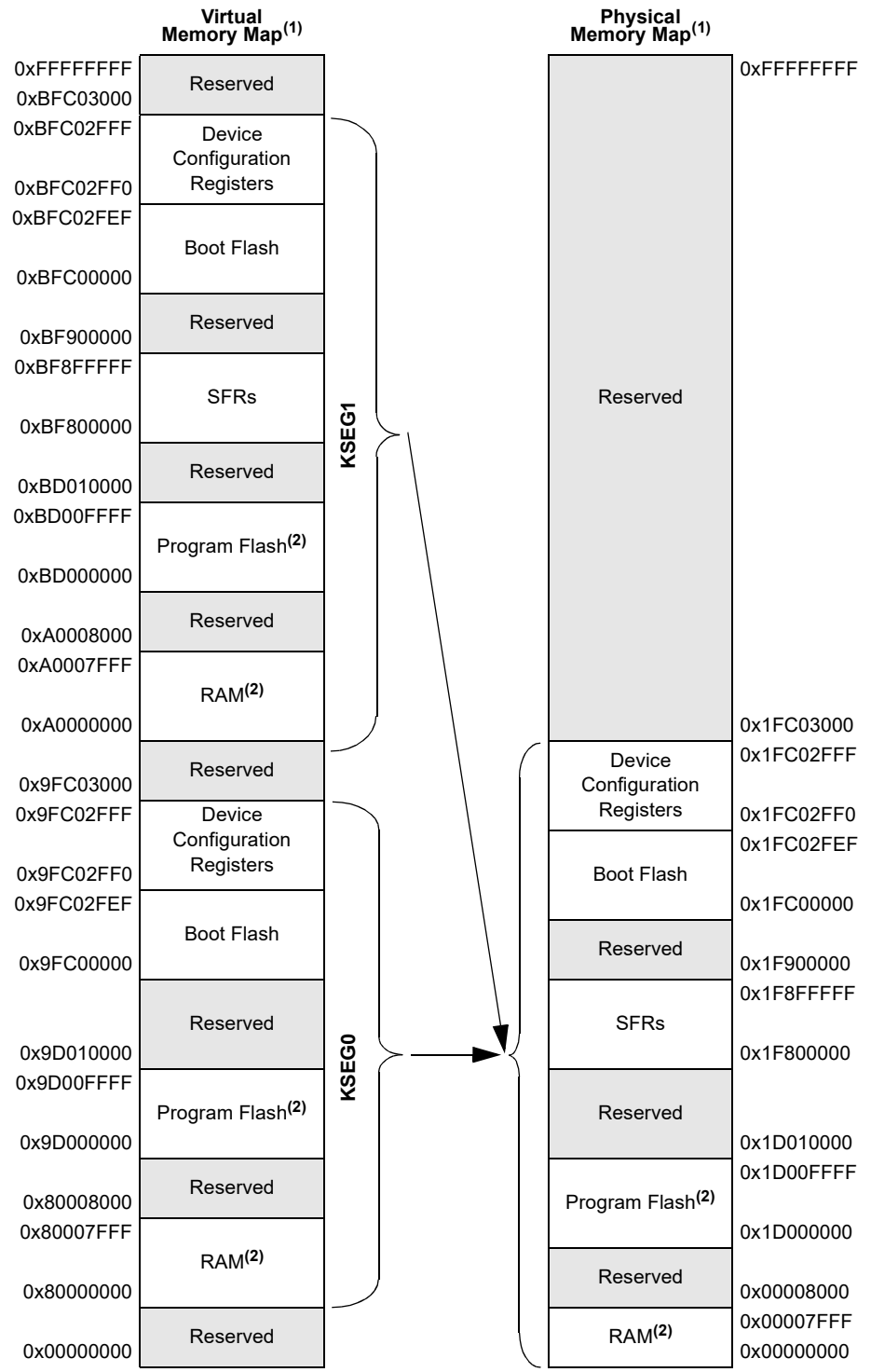
- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

## 4.1 Memory Layout

PIC32MX5XX/6XX/7XX microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX5XX/6XX/7XX devices are illustrated in Figure 4-1 through Figure 4-6. Table 4-1 provides memory map information for the Special Function Registers (SFRs).

**FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX564F064H, PIC32MX564F064L, PIC32MX664F064H AND PIC32MX664F064L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).


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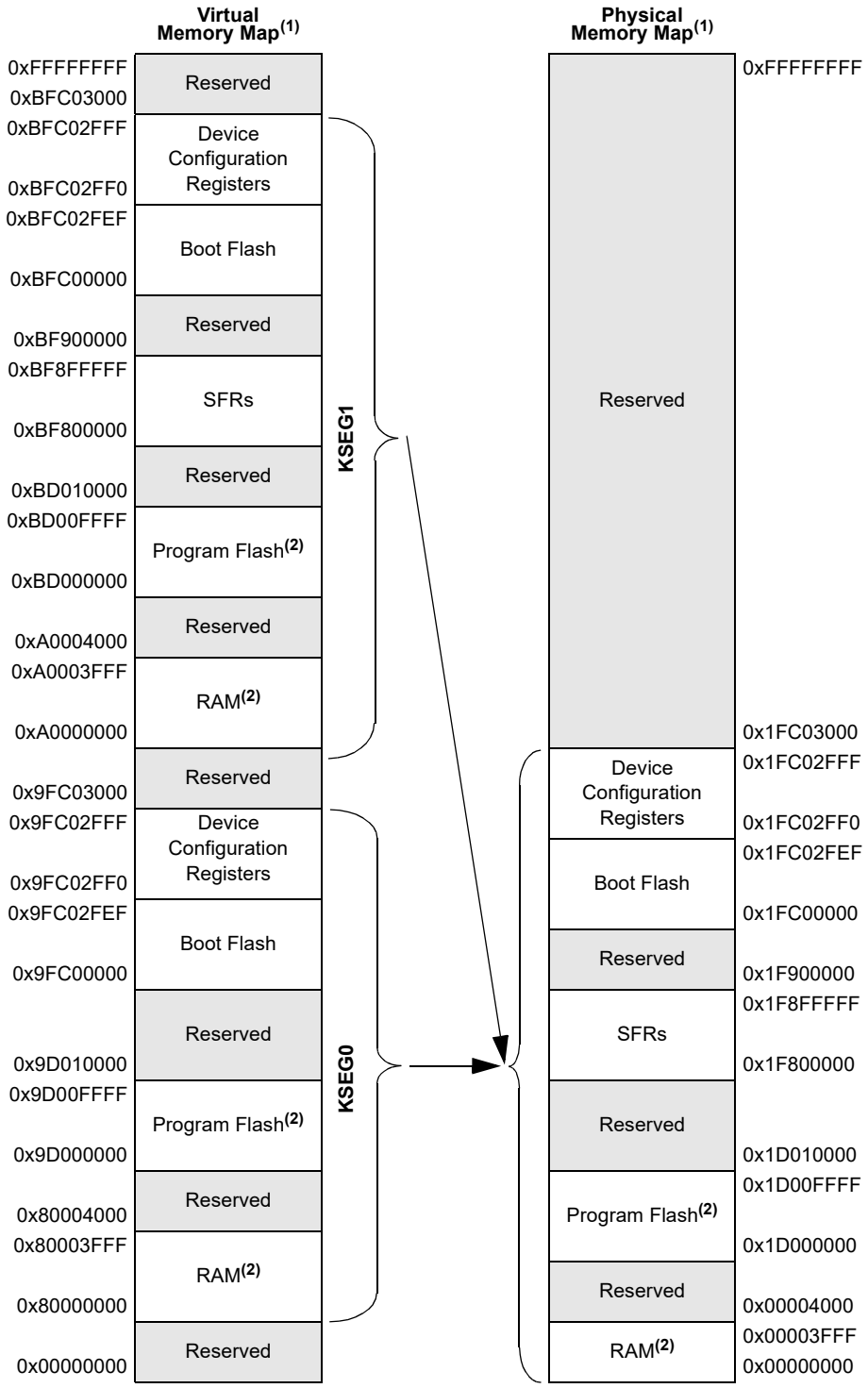
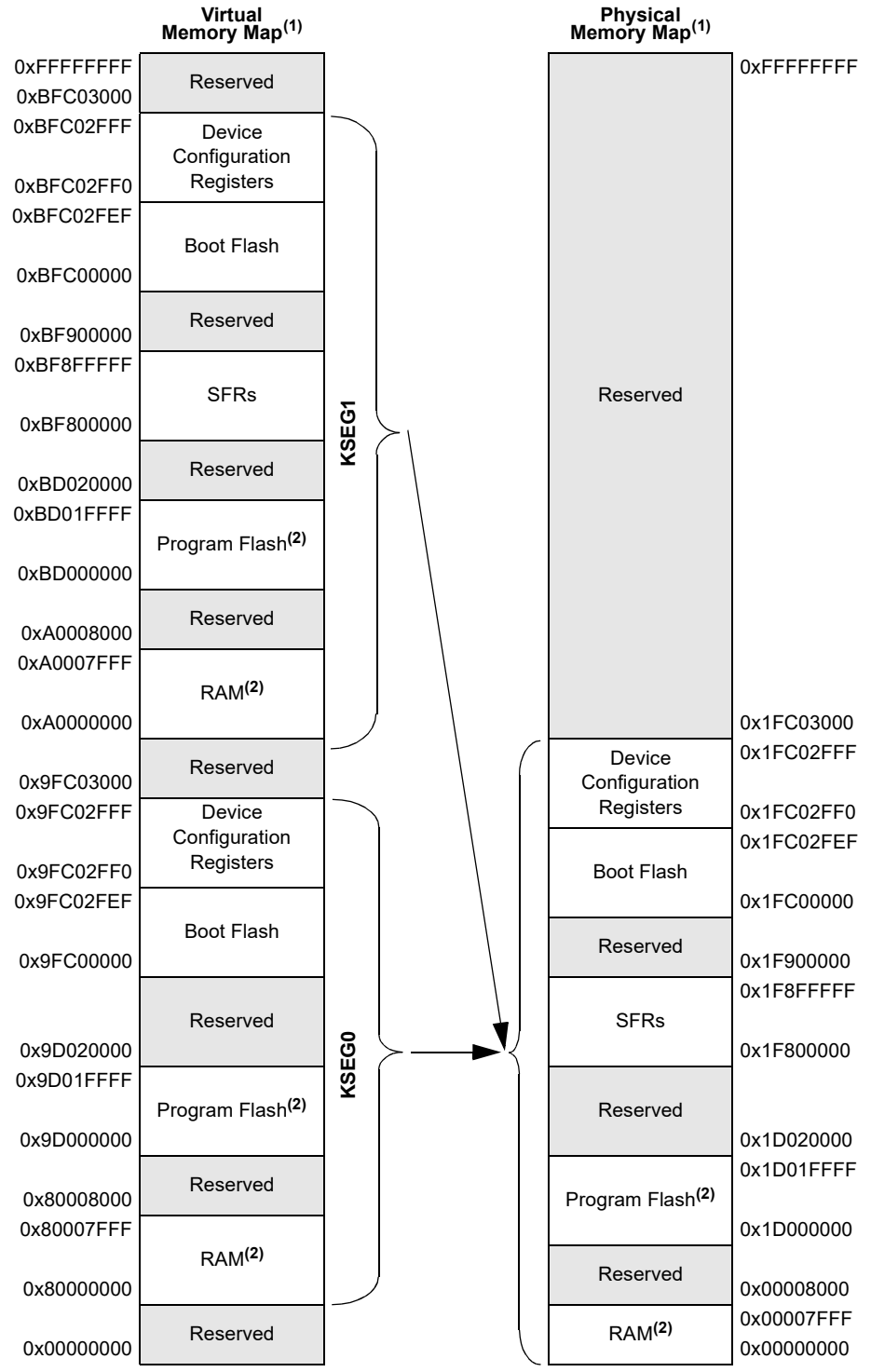
**FIGURE 4-2: MEMORY MAP ON RESET FOR PIC32MX534F064H AND PIC32MX534F064L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

**FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX564F128H, PIC32MX564F128L, PIC32MX664F128H, PIC32MX664F128L, PIC32MX764F128H AND PIC32MX764F128L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).


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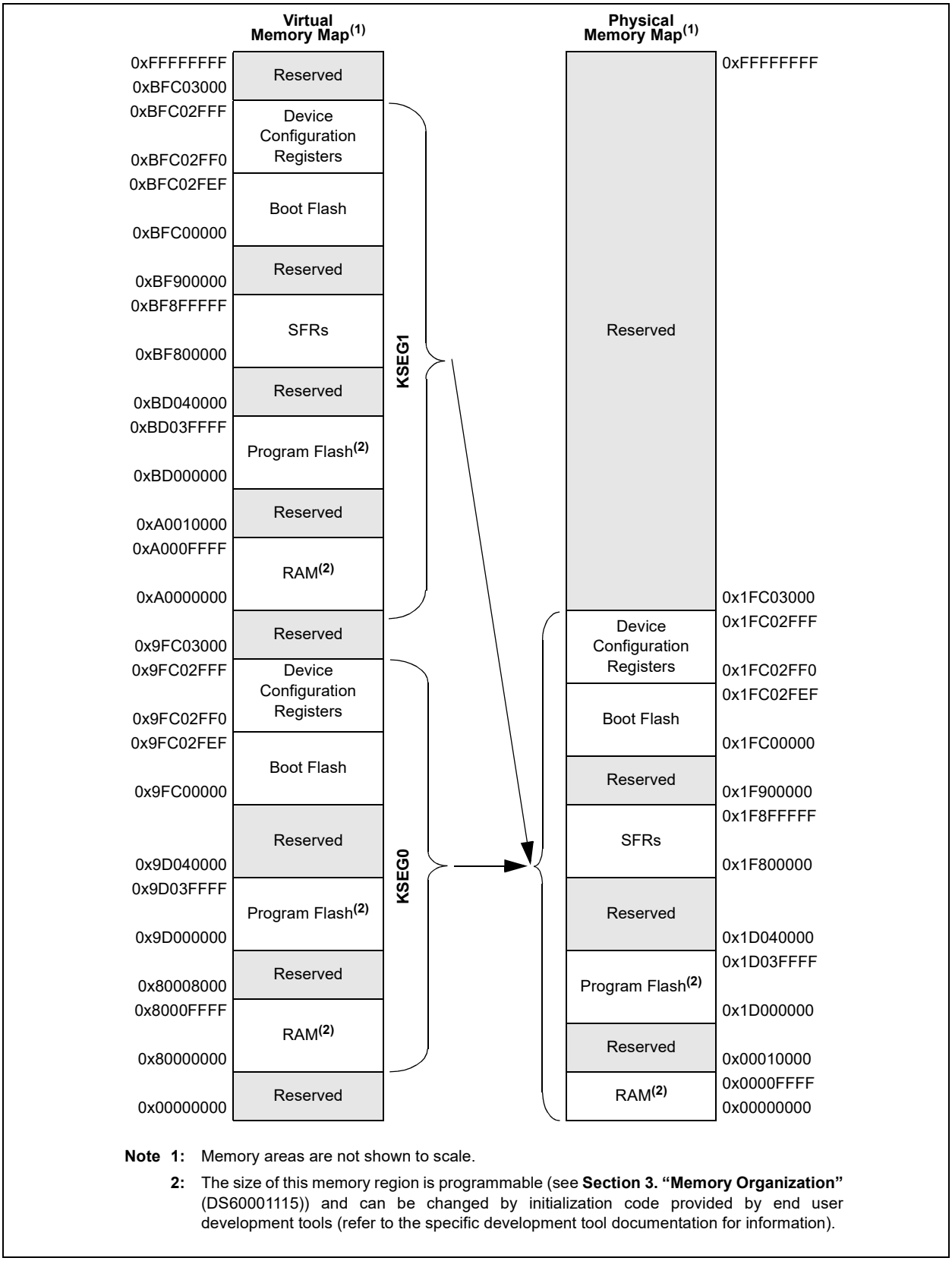
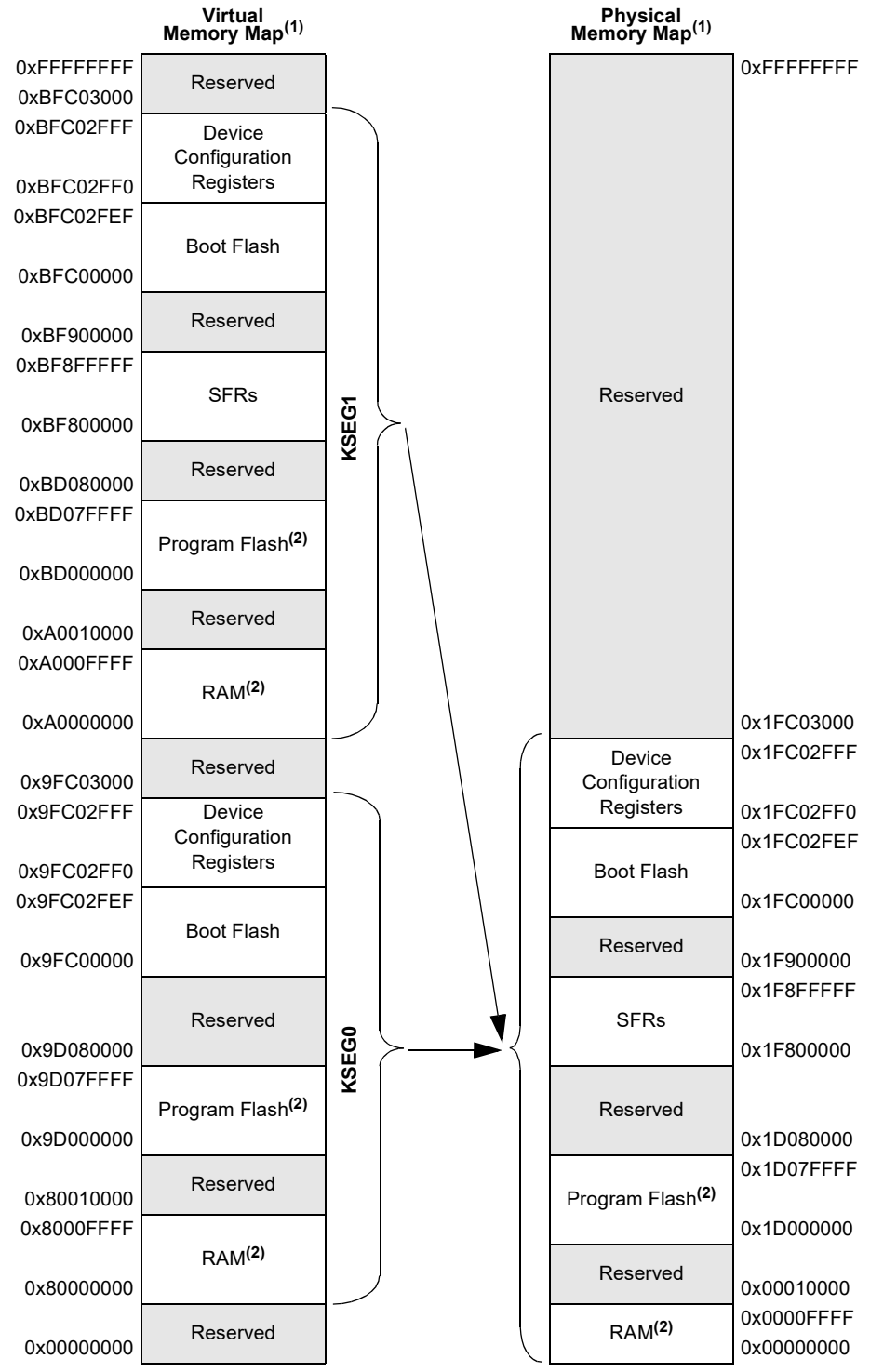
**FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX575F256H, PIC32MX575F256L, PIC32MX675F256H, PIC32MX675F256L, PIC32MX775F256H AND PIC32MX775F256L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

**FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX575F512H, PIC32MX575F512L, PIC32MX675F512H, PIC32MX675F512L, PIC32MX775F512H AND PIC32MX775F512L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).


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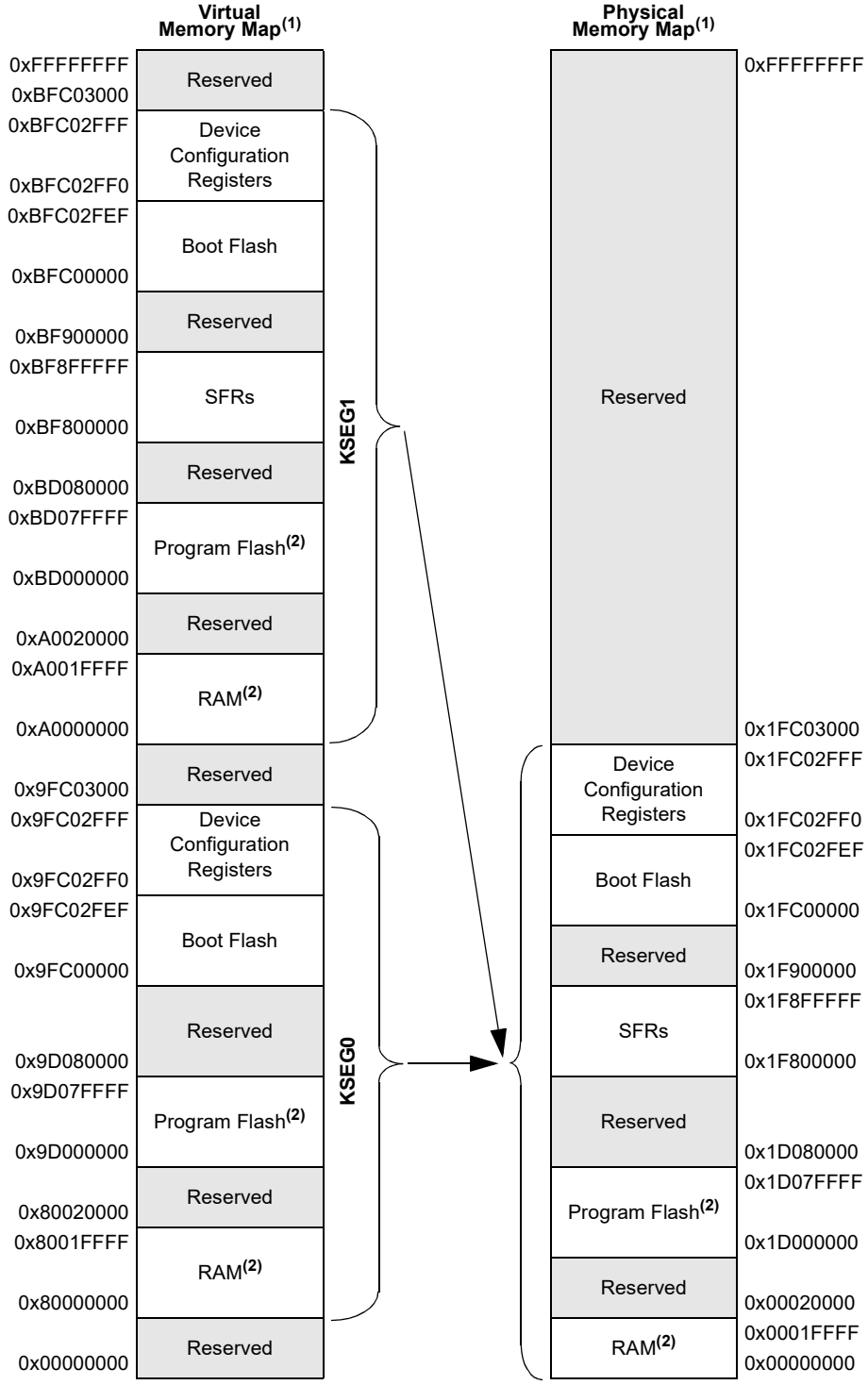
**FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX695F512H, PIC32MX695F512L, PIC32MX795F512H AND PIC32MX795F512L DEVICES**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115)) and can be changed by initialization code provided by end user development tools (refer to the specific development tool documentation for information).

**TABLE 4-1: SFR MEMORY MAP**

| Peripheral | Virtual Address | |
|---|---|---|
| | Base | Offset Start |
| Watchdog Timer | 0xBF80 | 0x0000 |
| RTCC | | 0x0200 |
| Timer1-Timer5 | | 0x0600 |
| Input Capture 1-5 | | 0x2000 |
| Output Compare 1-5 | | 0x3000 |
| I2C1-I2C5 | | 0x5000 |
| SPI1-SPI4 | | 0x5800 |
| UART1-UART6 | | 0x6000 |
| PMP | | 0x7000 |
| ADC | | 0x9000 |
| CVREF | | 0x9800 |
| Comparator | | 0xA000 |
| Oscillator | | 0xF000 |
| Device and Revision ID | | 0xF200 |
| Flash Controller | | 0xF400 |
| Reset | | 0xF600 |
| Interrupts | 0xBF88 | 0x1000 |
| Bus Matrix | | 0x2000 |
| DMA | | 0x3000 |
| Prefetch | | 0x4000 |
| USB | | 0x5040 |
| PORTA-PORTG | | 0x6000 |
| Ethernet | | 0x9000 |
| Configuration | 0xBFC0 | 0x2FF0 |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## 4.2 Control Registers

Register 4-1 through Register 4-8 are used for setting the RAM and Flash memory partitions for data and code.

**TABLE 4-2: BUS MATRIX REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | BMXCON(1) | 31:16 | — | — | — | — | — | BMXCHEDMA | — | — | — | — | — | BMXERRIXI | BMXERRICD | BMXERRDMA | BMXERRDS | BMXERRIS | 001F |
| | | 15:0 | — | — | — | — | — | — | — | — | — | BMXWSDRM | — | — | — | BMXARB<2:0> | | | 0041 |
| 2010 | BMXDKPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDKPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2020 | BMXDUDBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUDBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2030 | BMXDUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2040 | BMXDRMSZ | 31:16 | BMXDRMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2050 | BMXPUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | BMXPUPBA<19:16> | | | | 0000 |
| | | 15:0 | BMXPUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2060 | BMXPFMSZ | 31:16 | BMXPFMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2070 | BMXBOOTSZ | 31:16 | BMXBOOTSZ<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 3000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**REGISTER 4-1: BMXCON: BUS MATRIX CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | — | BMX ERRIXI | BMX ERRICD | BMX ERRDMA | BMX ERRDS | BMX ERRIS |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | R/W-1 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-1 |
| | — | BMX WSDRM | — | — | — | BMXARB<2:0> | | |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **BMXERRIXI:** Enable Bus Error from IXI bit
1 = Enable bus error exceptions for unmapped address accesses initiated from IXI shared bus
0 = Disable bus error exceptions for unmapped address accesses initiated from IXI shared bus

bit 19 **BMXERRICD:** Enable Bus Error from ICD Debug Unit bit
1 = Enable bus error exceptions for unmapped address accesses initiated from ICD
0 = Disable bus error exceptions for unmapped address accesses initiated from ICD

bit 18 **BMXERRDMA:** Bus Error from DMA bit
1 = Enable bus error exceptions for unmapped address accesses initiated from DMA
0 = Disable bus error exceptions for unmapped address accesses initiated from DMA

bit 17 **BMXERRDS:** Bus Error from CPU Data Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU data access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU data access

bit 16 **BMXERRIS:** Bus Error from CPU Instruction Access bit (disabled in Debug mode)
1 = Enable bus error exceptions for unmapped address accesses initiated from CPU instruction access
0 = Disable bus error exceptions for unmapped address accesses initiated from CPU instruction access

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **BMXWSDRM:** CPU Instruction or Data Access from Data RAM Wait State bit
1 = Data RAM accesses from CPU have one wait state for address setup
0 = Data RAM accesses from CPU have zero wait states for address setup

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BMXARB<2:0>:** Bus Matrix Arbitration Mode bits
111 = Reserved (using these Configuration modes will produce undefined behavior)
•
•
•
011 = Reserved (using these Configuration modes will produce undefined behavior)
010 = Arbitration Mode 2
001 = Arbitration Mode 1 (default)
000 = Arbitration Mode 0


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**REGISTER 4-2: BMXDKPBA: DATA RAM KERNEL PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDKPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDKPBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDKPBA<15:10>:** DRM Kernel Program Base Address bits
When non-zero, this value selects the relative base address for kernel program space in RAM

bit 9-0 **BMXDKPBA<9:0>:** DRM Kernel Program Base Address Read-Only bits
Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.

**REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUDBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUDBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUDBA<15:10>:** DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 **BMXDUDBA<9:0>:** DRM User Data Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.


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**REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |
| | BMXDUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXDUPBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-10 **BMXDUPBA<15:10>:** DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** DRM User Program Base Address Read-Only bits

Value is always '0', which forces 1 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

**2:** The value in this register must be less than or equal to BMXDRMSZ.

**REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00004000 = device has 16 KB RAM
0x00008000 = device has 32 KB RAM
0x00010000 = device has 64 KB RAM

**REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER(1,2)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | BMXPUPBA<19:16> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Program Flash (PFM) User Program Base Address Read-Only bits
Value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

**2:** The value in this register must be less than or equal to BMXPFMSZ.


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**REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXPFMSZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXPFMSZ<31:0>:** Program Flash Memory (PFM) Size bits
Static value that indicates the size of the PFM in bytes:
0x00010000 = device has 64 KB Flash
0x00020000 = device has 128 KB Flash
0x00040000 = device has 256 KB Flash
0x00080000 = device has 512 KB Flash

**REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXBOOTSZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits
Static value that indicates the size of the Boot PFM in bytes:
0x00003000 = device has 12 KB boot Flash

**NOTES:**


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## 5.0 FLASH PROGRAM MEMORY

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

**Note:** For PIC32MX5XX/6XX/7XX devices, the Flash page size is 4 KB and the row size is 512 bytes (1024 IW and 128 IW, respectively).

## 5.1 Control Registers

**TABLE 5-1: FLASH CONTROLLER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F400 | NVMCON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | WR | WREN | WRERR | LVDERR | LVDSTAT | — | — | — | — | — | — | — | NVMOP<3:0> | | | | 0000 |
| F410 | NVMKEY | 31:16 | NVMKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F420 | NVMADDR(1) | 31:16 | NVMADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F430 | NVMDATA | 31:16 | NVMDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| F440 | NVMSRC ADDR | 31:16 | NVMSRCADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0, HC | R/W-0 | R-0, HS | R-0, HS | R-0, HSC | U-0 | U-0 | U-0 |
| | WR | WREN | WRERR(1) | LVDERR(1) | LVDSTAT(1) | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | NVMOP<3:0> | | | |

| Legend: | U = Unimplemented bit, read as '0' | | HSC = Set and Cleared by hardware |
|---|---|---|---|
| R = Readable bit | W = Writable bit | HS = Set by hardware | HC = Cleared by hardware |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit
This bit is writable when WREN = 1 and the unlock sequence is followed.
1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
0 = Flash operation complete or inactive

bit 14 **WREN:** Write Enable bit
1 = Enable writes to WR bit and enables LVD circuit
0 = Disable writes to WR bit and disables LVD circuit

**Note:** This is the only bit in this register that is reset by a device Reset.

bit 13 **WRERR:** Write Error bit(1)
This bit is read-only and is automatically set by hardware.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set by hardware.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **LVDSTAT:** Low-Voltage Detect Status bit (LVD circuit must be enabled)(1)
This bit is read-only and is automatically set, and cleared, by hardware.
1 = Low-voltage event is active
0 = Low-voltage event is not active

bit 10-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are writable when WREN = 0.
1111 = Reserved
•
•
•
0111 = Reserved
0110 = No operation
0101 = Program Flash (PFM) erase operation: erases PFM if all pages are not write-protected
0100 = Page erase operation: erases page selected by NVMADDR if it is not write-protected
0011 = Row program operation: programs row selected by NVMADDR if it is not write-protected
0010 = No operation
0001 = Word program operation: programs word selected by NVMADDR if it is not write-protected
0000 = No operation

**Note 1:** This bit is cleared by setting NVMOP == 0000b, and initiating a Flash operation (i.e., WR).

**REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<31:24> | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<23:16> | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<15:8> | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read.

**Note:** This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

**REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMADDR<31:0>:** Flash Address bits
Bulk/Chip/PFM Erase: Address is ignored.
Page Erase: Address identifies the page to erase.
Row Program: Address identifies the row to program.
Word Program: Address identifies the word to program.


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**REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMDATA<31:0>:** Flash Programming Data bits

**Note:** The bits in this register are only reset by a Power-on Reset (POR).

**REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMSRCADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

**NOTES:**


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## 6.0 RESETS

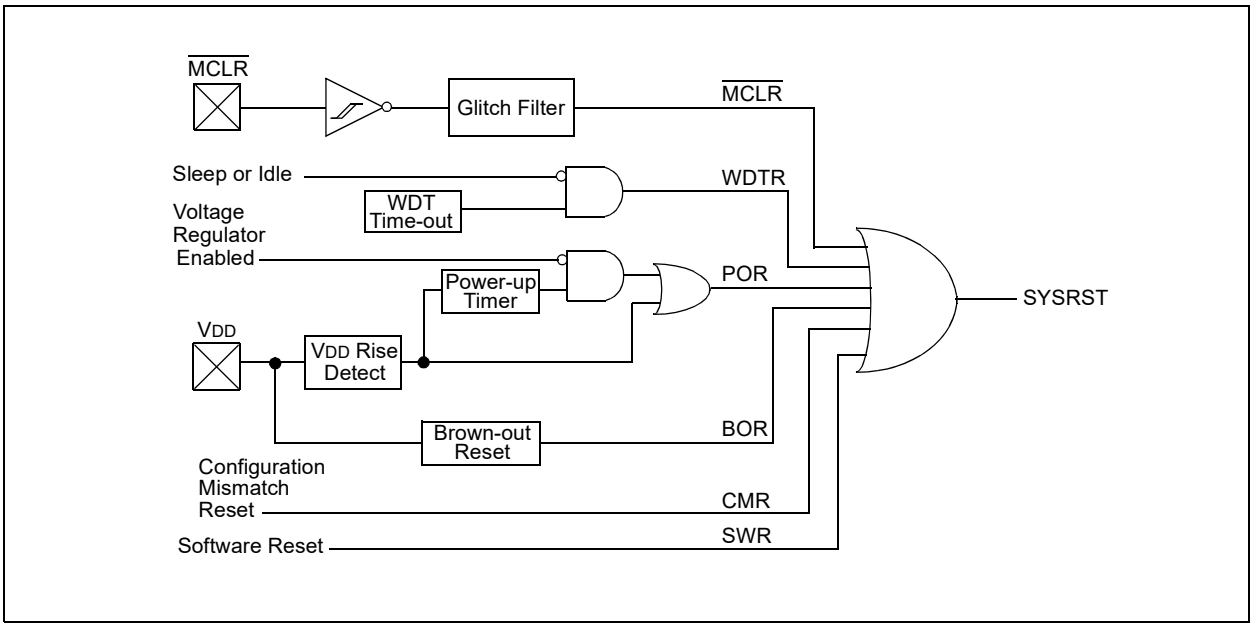
| | |
|---|---|
| **Note:** | This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). |

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

**FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM**



## 6.1 Control Registers

**TABLE 6-1: RESETS REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F600 | RCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | 0000 |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.



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**REGISTER 6-1: RCON: RESET CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0, HS | R/W-0 |
| | — | — | — | — | — | — | CMR | VREGS |
| 7:0 | R/W-0, HS | R/W-0, HS | U-0 | R/W-0, HS | R/W-0, HS | R/W-0, HS | R/W-1, HS | R/W-1, HS |
| | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR(1) | POR(1) |

| Legend: | HS = Set by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = Configuration mismatch Reset has occurred
0 = Configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator is enabled and is on during Sleep mode
0 = Regulator is set to Stand-by Tracking mode

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin Flag bit
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT Time-out has occurred
0 = WDT Time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit(1)
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit(1)
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

**Note 1:** User software must clear this bit to view the next detection.

**REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | W-0, HC |
| | — | — | — | — | — | — | — | SWRST(1) |

| Legend: | HC = Cleared by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1)
1 = Enable software Reset event
0 = No effect

**Note 1:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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## 7.0 INTERRUPT CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS60001108) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MX5XX/6XX/7XX devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The Interrupt Controller module includes the following features:

- Up to 96 interrupt sources
- Up to 64 interrupt vectors
- Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable sub-priority levels within each priority
- Dedicated shadow set for user-selectable priority level
- Software can generate any interrupt
- User-configurable interrupt vector table location
- User-configurable interrupt vector spacing

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.

**FIGURE 7-1: INTERRUPT CONTROLLER MODULE**

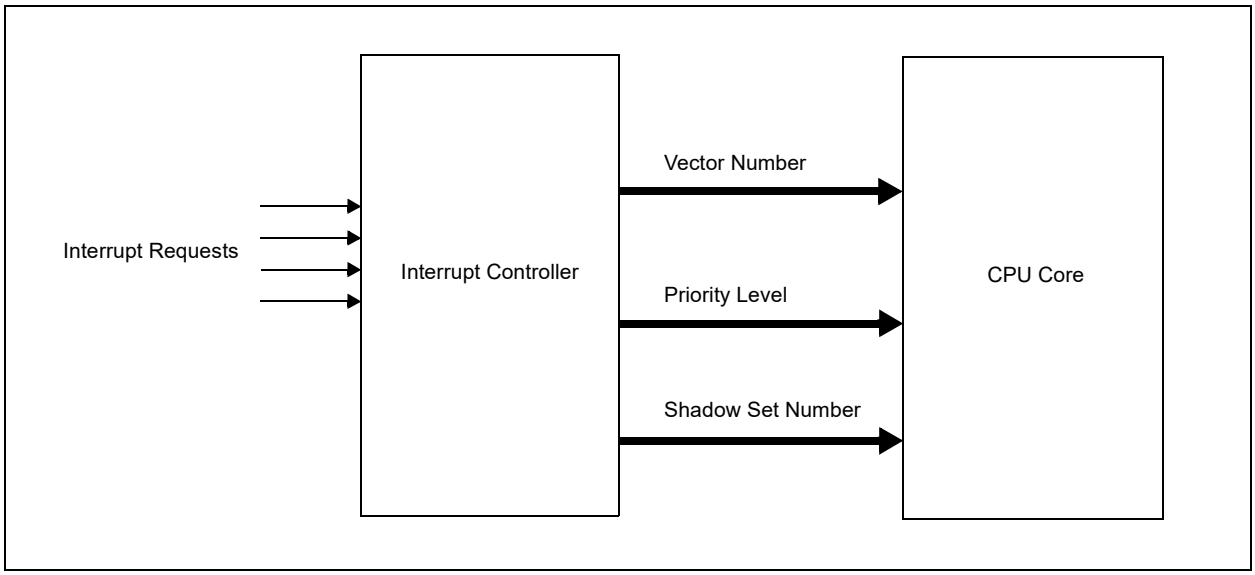

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION**

| Interrupt Source(1) | IRQ Number | Vector Number | Interrupt Bit Location | | | |
|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-Priority |
| Highest Natural Order Priority | | | | | | |
| CT – Core Timer Interrupt | 0 | 0 | IFS0<0> | IEC0<0> | IPC0<4:2> | IPC0<1:0> |
| CS0 – Core Software Interrupt 0 | 1 | 1 | IFS0<1> | IEC0<1> | IPC0<12:10> | IPC0<9:8> |
| CS1 – Core Software Interrupt 1 | 2 | 2 | IFS0<2> | IEC0<2> | IPC0<20:18> | IPC0<17:16> |
| INT0 – External Interrupt 0 | 3 | 3 | IFS0<3> | IEC0<3> | IPC0<28:26> | IPC0<25:24> |
| T1 – Timer1 | 4 | 4 | IFS0<4> | IEC0<4> | IPC1<4:2> | IPC1<1:0> |
| IC1 – Input Capture 1 | 5 | 5 | IFS0<5> | IEC0<5> | IPC1<12:10> | IPC1<9:8> |
| OC1 – Output Compare 1 | 6 | 6 | IFS0<6> | IEC0<6> | IPC1<20:18> | IPC1<17:16> |
| INT1 – External Interrupt 1 | 7 | 7 | IFS0<7> | IEC0<7> | IPC1<28:26> | IPC1<25:24> |
| T2 – Timer2 | 8 | 8 | IFS0<8> | IEC0<8> | IPC2<4:2> | IPC2<1:0> |
| IC2 – Input Capture 2 | 9 | 9 | IFS0<9> | IEC0<9> | IPC2<12:10> | IPC2<9:8> |
| OC2 – Output Compare 2 | 10 | 10 | IFS0<10> | IEC0<10> | IPC2<20:18> | IPC2<17:16> |
| INT2 – External Interrupt 2 | 11 | 11 | IFS0<11> | IEC0<11> | IPC2<28:26> | IPC2<25:24> |
| T3 – Timer3 | 12 | 12 | IFS0<12> | IEC0<12> | IPC3<4:2> | IPC3<1:0> |
| IC3 – Input Capture 3 | 13 | 13 | IFS0<13> | IEC0<13> | IPC3<12:10> | IPC3<9:8> |
| OC3 – Output Compare 3 | 14 | 14 | IFS0<14> | IEC0<14> | IPC3<20:18> | IPC3<17:16> |
| INT3 – External Interrupt 3 | 15 | 15 | IFS0<15> | IEC0<15> | IPC3<28:26> | IPC3<25:24> |
| T4 – Timer4 | 16 | 16 | IFS0<16> | IEC0<16> | IPC4<4:2> | IPC4<1:0> |
| IC4 – Input Capture 4 | 17 | 17 | IFS0<17> | IEC0<17> | IPC4<12:10> | IPC4<9:8> |
| OC4 – Output Compare 4 | 18 | 18 | IFS0<18> | IEC0<18> | IPC4<20:18> | IPC4<17:16> |
| INT4 – External Interrupt 4 | 19 | 19 | IFS0<19> | IEC0<19> | IPC4<28:26> | IPC4<25:24> |
| T5 – Timer5 | 20 | 20 | IFS0<20> | IEC0<20> | IPC5<4:2> | IPC5<1:0> |
| IC5 – Input Capture 5 | 21 | 21 | IFS0<21> | IEC0<21> | IPC5<12:10> | IPC5<9:8> |
| OC5 – Output Compare 5 | 22 | 22 | IFS0<22> | IEC0<22> | IPC5<20:18> | IPC5<17:16> |
| SPI1E – SPI1 Fault | 23 | 23 | IFS0<23> | IEC0<23> | IPC5<28:26> | IPC5<25:24> |
| SPI1RX – SPI1 Receive Done | 24 | 23 | IFS0<24> | IEC0<24> | IPC5<28:26> | IPC5<25:24> |
| SPI1TX – SPI1 Transfer Done | 25 | 23 | IFS0<25> | IEC0<25> | IPC5<28:26> | IPC5<25:24> |
| U1E – UART1 Error<br>SPI3E – SPI3 Fault<br>I2C3B – I2C3 Bus Collision Event | 26 | 24 | IFS0<26> | IEC0<26> | IPC6<4:2> | IPC6<1:0> |
| U1RX – UART1 Receiver<br>SPI3RX – SPI3 Receive Done<br>I2C3S – I2C3 Slave Event | 27 | 24 | IFS0<27> | IEC0<27> | IPC6<4:2> | IPC6<1:0> |
| U1TX – UART1 Transmitter<br>SPI3TX – SPI3 Transfer Done<br>I2C3M – I2C3 Master Event | 28 | 24 | IFS0<28> | IEC0<28> | IPC6<4:2> | IPC6<1:0> |
| I2C1B – I2C1 Bus Collision Event | 29 | 25 | IFS0<29> | IEC0<29> | IPC6<12:10> | IPC6<9:8> |
| I2C1S – I2C1 Slave Event | 30 | 25 | IFS0<30> | IEC0<30> | IPC6<12:10> | IPC6<9:8> |
| I2C1M – I2C1 Master Event | 31 | 25 | IFS0<31> | IEC0<31> | IPC6<12:10> | IPC6<9:8> |
| CN – Input Change Interrupt | 32 | 26 | IFS1<0> | IEC1<0> | IPC6<20:18> | IPC6<17:16> |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX5XX USB and CAN Features"**, **TABLE 2: "PIC32MX6XX USB and Ethernet Features"** and **TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features"** for the list of available peripherals.


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**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | IRQ Number | Vector Number | Interrupt Bit Location | | | |
|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-Priority |
| AD1 – ADC1 Convert Done | 33 | 27 | IFS1<1> | IEC1<1> | IPC6<28:26> | IPC6<25:24> |
| PMP – Parallel Master Port | 34 | 28 | IFS1<2> | IEC1<2> | IPC7<4:2> | IPC7<1:0> |
| CMP1 – Comparator Interrupt | 35 | 29 | IFS1<3> | IEC1<3> | IPC7<12:10> | IPC7<9:8> |
| CMP2 – Comparator Interrupt | 36 | 30 | IFS1<4> | IEC1<4> | IPC7<20:18> | IPC7<17:16> |
| U2E – UART2 Error<br>SPI2E – SPI2 Fault<br>I2C4B – I2C4 Bus Collision Event | 37 | 31 | IFS1<5> | IEC1<5> | IPC7<28:26> | IPC7<25:24> |
| U2RX – UART2 Receiver<br>SPI2RX – SPI2 Receive Done<br>I2C4S – I2C4 Slave Event | 38 | 31 | IFS1<6> | IEC1<6> | IPC7<28:26> | IPC7<25:24> |
| U2TX – UART2 Transmitter<br>SPI2TX – SPI2 Transfer Done<br>IC4M – I2C4 Master Event | 39 | 31 | IFS1<7> | IEC1<7> | IPC7<28:26> | IPC7<25:24> |
| U3E – UART3 Error<br>SPI4E – SPI4 Fault<br>I2C5B – I2C5 Bus Collision Event | 40 | 32 | IFS1<8> | IEC1<8> | IPC8<4:2> | IPC8<1:0> |
| U3RX – UART3 Receiver<br>SPI4RX – SPI4 Receive Done<br>I2C5S – I2C5 Slave Event | 41 | 32 | IFS1<9> | IEC1<9> | IPC8<4:2> | IPC8<1:0> |
| U3TX – UART3 Transmitter<br>SPI4TX – SPI4 Transfer Done<br>IC5M – I2C5 Master Event | 42 | 32 | IFS1<10> | IEC1<10> | IPC8<4:2> | IPC8<1:0> |
| I2C2B – I2C2 Bus Collision Event | 43 | 33 | IFS1<11> | IEC1<11> | IPC8<12:10> | IPC8<9:8> |
| I2C2S – I2C2 Slave Event | 44 | 33 | IFS1<12> | IEC1<12> | IPC8<12:10> | IPC8<9:8> |
| I2C2M – I2C2 Master Event | 45 | 33 | IFS1<13> | IEC1<13> | IPC8<12:10> | IPC8<9:8> |
| FSCM – Fail-Safe Clock Monitor | 46 | 34 | IFS1<14> | IEC1<14> | IPC8<20:18> | IPC8<17:16> |
| RTCC – Real-Time Clock and Calendar | 47 | 35 | IFS1<15> | IEC1<15> | IPC8<28:26> | IPC8<25:24> |
| DMA0 – DMA Channel 0 | 48 | 36 | IFS1<16> | IEC1<16> | IPC9<4:2> | IPC9<1:0> |
| DMA1 – DMA Channel 1 | 49 | 37 | IFS1<17> | IEC1<17> | IPC9<12:10> | IPC9<9:8> |
| DMA2 – DMA Channel 2 | 50 | 38 | IFS1<18> | IEC1<18> | IPC9<20:18> | IPC9<17:16> |
| DMA3 – DMA Channel 3 | 51 | 39 | IFS1<19> | IEC1<19> | IPC9<28:26> | IPC9<25:24> |
| DMA4 – DMA Channel 4 | 52 | 40 | IFS1<20> | IEC1<20> | IPC10<4:2> | IPC10<1:0> |
| DMA5 – DMA Channel 5 | 53 | 41 | IFS1<21> | IEC1<21> | IPC10<12:10> | IPC10<9:8> |
| DMA6 – DMA Channel 6 | 54 | 42 | IFS1<22> | IEC1<22> | IPC10<20:18> | IPC10<17:16> |
| DMA7 – DMA Channel 7 | 55 | 43 | IFS1<23> | IEC1<23> | IPC10<28:26> | IPC10<25:24> |
| FCE – Flash Control Event | 56 | 44 | IFS1<24> | IEC1<24> | IPC11<4:2> | IPC11<1:0> |
| USB – USB Interrupt | 57 | 45 | IFS1<25> | IEC1<25> | IPC11<12:10> | IPC11<9:8> |
| CAN1 – Control Area Network 1 | 58 | 46 | IFS1<26> | IEC1<26> | IPC11<20:18> | IPC11<17:16> |
| CAN2 – Control Area Network 2 | 59 | 47 | IFS1<27> | IEC1<27> | IPC11<28:26> | IPC11<25:24> |
| ETH – Ethernet Interrupt | 60 | 48 | IFS1<28> | IEC1<28> | IPC12<4:2> | IPC12<1:0> |
| IC1E – Input Capture 1 Error | 61 | 5 | IFS1<29> | IEC1<29> | IPC1<12:10> | IPC1<9:8> |
| IC2E – Input Capture 2 Error | 62 | 9 | IFS1<30> | IEC1<30> | IPC2<12:10> | IPC2<9:8> |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX5XX USB and CAN Features"**, **TABLE 2: "PIC32MX6XX USB and Ethernet Features"** and **TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features"** for the list of available peripherals.

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source(1) | IRQ Number | Vector Number | Interrupt Bit Location | | | |
|---|---|---|---|---|---|---|
| | | | Flag | Enable | Priority | Sub-Priority |
| IC3E – Input Capture 3 Error | 63 | 13 | IFS1<31> | IEC1<31> | IPC3<12:10> | IPC3<9:8> |
| IC4E – Input Capture 4 Error | 64 | 17 | IFS2<0> | IEC2<0> | IPC4<12:10> | IPC4<9:8> |
| IC5E – Input Capture 5 Error | 65 | 21 | IFS2<1> | IEC2<1> | IPC5<12:10> | IPC5<9:8> |
| PMPE – Parallel Master Port Error | 66 | 28 | IFS2<2> | IEC2<2> | IPC7<4:2> | IPC7<1:0> |
| U4E – UART4 Error | 67 | 49 | IFS2<3> | IEC2<3> | IPC12<12:10> | IPC12<9:8> |
| U4RX – UART4 Receiver | 68 | 49 | IFS2<4> | IEC2<4> | IPC12<12:10> | IPC12<9:8> |
| U4TX – UART4 Transmitter | 69 | 49 | IFS2<5> | IEC2<5> | IPC12<12:10> | IPC12<9:8> |
| U6E – UART6 Error | 70 | 50 | IFS2<6> | IEC2<6> | IPC12<20:18> | IPC12<17:16> |
| U6RX – UART6 Receiver | 71 | 50 | IFS2<7> | IEC2<7> | IPC12<20:18> | IPC12<17:16> |
| U6TX – UART6 Transmitter | 72 | 50 | IFS2<8> | IEC2<8> | IPC12<20:18> | IPC12<17:16> |
| U5E – UART5 Error | 73 | 51 | IFS2<9> | IEC2<9> | IPC12<28:26> | IPC12<25:24> |
| U5RX – UART5 Receiver | 74 | 51 | IFS2<10> | IEC2<10> | IPC12<28:26> | IPC12<25:24> |
| U5TX – UART5 Transmitter | 75 | 51 | IFS2<11> | IEC2<11> | IPC12<28:26> | IPC12<25:24> |
| (Reserved) | — | — | — | — | — | — |
| Lowest Natural Order Priority | | | | | | |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX5XX USB and CAN Features"**, **TABLE 2: "PIC32MX6XX USB and Ethernet Features"** and **TABLE 3: "PIC32MX7XX USB, Ethernet, and CAN Features"** for the list of available peripherals.


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## 7.1 Control Registers

**TABLE 7-2: INTERRUPT REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H AND PIC32MX575F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | — | — | — | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | — | — | CAN1IF | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | — | — | — | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | — | — | — | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | — | — | CAN1IE | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | — | — | — | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX534/564/664/764 devices.

**3:** This register does not have associated CLR, SET, and INV registers.

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**TABLE 7-2: INTERRUPT REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H AND PIC32MX575F512H DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | CAN1IP<2:0> | | | CAN1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX534/564/664/764 devices.

**3:** This register does not have associated CLR, SET, and INV registers.



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**TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | — | — | — | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | — | — | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | — | — | — | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | — | — | — | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | — | — | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | — | — | — | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX664 devices.

**3:** This register does not have associated CLR, SET, and INV registers.

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**TABLE 7-3: INTERRUPT REGISTER MAP FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H AND PIC32MX695F512H DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | ETHIP<2:0> | | | ETHIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX664 devices.

**3:** This register does not have associated CLR, SET, and INV registers.



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**TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | — | — | — | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | CAN2IF(2) | CAN1IF | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | — | — | — | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | — | — | — | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | CAN2IE(2) | CAN1IE | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | — | — | — | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This bit is unimplemented on PIC32MX764F128H device.

**3:** This register does not have associated CLR, SET, and INV registers.

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**TABLE 7-4: INTERRUPT REGISTER MAP FOR PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | CAN2IP<2:0>(2) | | | CAN2IS<1:0>(2) | | — | — | — | CAN1IP<2:0> | | | CAN1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | ETHIP<2:0> | | | ETHIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This bit is unimplemented on PIC32MX764F128H device.

**3:** This register does not have associated CLR, SET, and INV registers.



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**TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | SPI1TXIF | SPI1RXIF | SPI1EIF | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | — | — | CAN1IF | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | SPI1TXIE | SPI1RXIE | SPI1EIE | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | — | — | CAN1IE | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | I2C2SIE | I2C2BIE | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX534/564 devices.

**3:** This register does not have associated CLR, SET, and INV registers.

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**TABLE 7-5: INTERRUPT REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L AND PIC32MX575F256L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | SPI1IP<2:0> | | | SPI1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | CAN1IP<2:0> | | | CAN1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX534/564 devices.

**3:** This register does not have associated CLR, SET, and INV registers.



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**TABLE 7-6: INTERRUPT REGISTER MAP FOR PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L AND PIC32MX695F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | SPI1TXIF | SPI1RXIF | SPI1EIF | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | — | — | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | SPI1TXIE | SPI1RXIE | SPI1EIE | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | — | — | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | I2C2SIE | I2C2BIE | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX664 devices.

**3:** This register does note have associated CLR, SET, and INV registers.

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**TABLE 7-6: INTERRUPT REGISTER MAP FOR PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L AND PIC32MX695F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | SPI1IP<2:0> | | | SPI1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | ETHIP<2:0> | | | ETHIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX664 devices.

**3:** This register does note have associated CLR, SET, and INV registers.



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**TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 1000 | INTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SS0 | 0000 |
| | | 15:0 | — | — | — | MVEC | — | TPC<2:0> | | | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 |
| 1010 | INTSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | SRIPL<2:0> | | | — | — | VEC<5:0> | | | | | | 0000 |
| 1020 | IPTMR | 31:16 | IPTMR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 1030 | IFS0 | 31:16 | I2C1MIF | I2C1SIF | I2C1BIF | U1TXIF<br>SPI3TXIF<br>I2C3MIF | U1RXIF<br>SPI3RXIF<br>I2C3SIF | U1EIF<br>SPI3EIF<br>I2C3BIF | SPI1TXIF | SPI1RXIF | SPI1EIF | OC5IF | IC5IF | T5IF | INT4IF | OC4IF | IC4IF | T4IF | 0000 |
| | | 15:0 | INT3IF | OC3IF | IC3IF | T3IF | INT2IF | OC2IF | IC2IF | T2IF | INT1IF | OC1IF | IC1IF | T1IF | INT0IF | CS1IF | CS0IF | CTIF | 0000 |
| 1040 | IFS1 | 31:16 | IC3EIF | IC2EIF | IC1EIF | ETHIF | CAN2IF(2) | CAN1IF | USBIF | FCEIF | DMA7IF(2) | DMA6IF(2) | DMA5IF(2) | DMA4IF(2) | DMA3IF | DMA2IF | DMA1IF | DMA0IF | 0000 |
| | | 15:0 | RTCCIF | FSCMIF | I2C2MIF | I2C2SIF | I2C2BIF | U3TXIF<br>SPI4TXIF<br>I2C5MIF | U3RXIF<br>SPI4RXIF<br>I2C5SIF | U3EIF<br>SPI4EIF<br>I2C5BIF | U2TXIF<br>SPI2TXIF<br>I2C4MIF | U2RXIF<br>SPI2RXIF<br>I2C4SIF | U2EIF<br>SPI2EIF<br>I2C4BIF | CMP2IF | CMP1IF | PMPIF | AD1IF | CNIF | 0000 |
| 1050 | IFS2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIF | U5RXIF | U5EIF | U6TXIF | U6RXIF | U6EIF | U4TXIF | U4RXIF | U4EIF | PMPEIF | IC5EIF | IC4EIF | 0000 |
| 1060 | IEC0 | 31:16 | I2C1MIE | I2C1SIE | I2C1BIE | U1TXIE<br>SPI3TXIE<br>I2C3MIE | U1RXIE<br>SPI3RXIE<br>I2C3SIE | U1EIE<br>SPI3EIE<br>I2C3BIE | SPI1TXIE | SPI1RXIE | SPI1EIE | OC5IE | IC5IE | T5IE | INT4IE | OC4IE | IC4IE | T4IE | 0000 |
| | | 15:0 | INT3IE | OC3IE | IC3IE | T3IE | INT2IE | OC2IE | IC2IE | T2IE | INT1IE | OC1IE | IC1IE | T1IE | INT0IE | CS1IE | CS0IE | CTIE | 0000 |
| 1070 | IEC1 | 31:16 | IC3EIE | IC2EIE | IC1EIE | ETHIE | CAN2IE(2) | CAN1IE | USBIE | FCEIE | DMA7IE(2) | DMA6IE(2) | DMA5IE(2) | DMA4IE(2) | DMA3IE | DMA2IE | DMA1IE | DMA0IE | 0000 |
| | | 15:0 | RTCCIE | FSCMIE | I2C2MIE | I2C2SIE | I2C2BIE | U3TXIE<br>SPI4TXIE<br>I2C5MIE | U3RXIE<br>SPI4RXIE<br>I2C5SIE | U3EIE<br>SPI4EIE<br>I2C5BIE | U2TXIE<br>SPI2TXIE<br>I2C4MIE | U2RXIE<br>SPI2RXIE<br>I2C4SIE | U2EIE<br>SPI2EIE<br>I2C4BIE | CMP2IE | CMP1IE | PMPIE | AD1IE | CNIE | 0000 |
| 1080 | IEC2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | U5TXIE | U5RXIE | U5EIE | U6TXIE | U6RXIE | U6EIE | U4TXIE | U4RXIE | U4EIE | PMPEIE | IC5EIE | IC4EIE | 0000 |
| 1090 | IPC0 | 31:16 | — | — | — | INT0IP<2:0> | | | INT0IS<1:0> | | — | — | — | CS1IP<2:0> | | | CS1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | CS0IP<2:0> | | | CS0IS<1:0> | | — | — | — | CTIP<2:0> | | | CTIS<1:0> | | 0000 |
| 10A0 | IPC1 | 31:16 | — | — | — | INT1IP<2:0> | | | INT1IS<1:0> | | — | — | — | OC1IP<2:0> | | | OC1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC1IP<2:0> | | | IC1IS<1:0> | | — | — | — | T1IP<2:0> | | | T1IS<1:0> | | 0000 |
| 10B0 | IPC2 | 31:16 | — | — | — | INT2IP<2:0> | | | INT2IS<1:0> | | — | — | — | OC2IP<2:0> | | | OC2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC2IP<2:0> | | | IC2IS<1:0> | | — | — | — | T2IP<2:0> | | | T2IS<1:0> | | 0000 |
| 10C0 | IPC3 | 31:16 | — | — | — | INT3IP<2:0> | | | INT3IS<1:0> | | — | — | — | OC3IP<2:0> | | | OC3IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC3IP<2:0> | | | IC3IS<1:0> | | — | — | — | T3IP<2:0> | | | T3IS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This bit is unimplemented on PIC32MX764F128L device.

**3:** This register does not have associated CLR, SET, and INV registers.

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**TABLE 7-7: INTERRUPT REGISTER MAP FOR PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 10D0 | IPC4 | 31:16 | — | — | — | INT4IP<2:0> | | | INT4IS<1:0> | | — | — | — | OC4IP<2:0> | | | OC4IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC4IP<2:0> | | | IC4IS<1:0> | | — | — | — | T4IP<2:0> | | | T4IS<1:0> | | 0000 |
| 10E0 | IPC5 | 31:16 | — | — | — | SPI1IP<2:0> | | | SPI1IS<1:0> | | — | — | — | OC5IP<2:0> | | | OC5IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | IC5IP<2:0> | | | IC5IS<1:0> | | — | — | — | T5IP<2:0> | | | T5IS<1:0> | | 0000 |
| 10F0 | IPC6 | 31:16 | — | — | — | AD1IP<2:0> | | | AD1IS<1:0> | | — | — | — | CNIP<2:0> | | | CNIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C1IP<2:0> | | | I2C1IS<1:0> | | — | — | — | U1IP<2:0> | | | U1IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI3IP<2:0> | | | SPI3IS<1:0> | | |
| | | | | | | | | | | | | | | I2C3IP<2:0> | | | I2C3IS<1:0> | | |
| 1100 | IPC7 | 31:16 | — | — | — | U2IP<2:0> | | | U2IS<1:0> | | — | — | — | CMP2IP<2:0> | | | CMP2IS<1:0> | | 0000 |
| | | | | | | SPI2IP<2:0> | | | SPI2IS<1:0> | | | | | | | | | | |
| | | | | | | I2C4IP<2:0> | | | I2C4IS<1:0> | | | | | | | | | | |
| | | 15:0 | — | — | — | CMP1IP<2:0> | | | CMP1IS<1:0> | | — | — | — | PMPIP<2:0> | | | PMPIS<1:0> | | 0000 |
| 1110 | IPC8 | 31:16 | — | — | — | RTCCIP<2:0> | | | RTCCIS<1:0> | | — | — | — | FSCMIP<2:0> | | | FSCMIS<1:0> | | 0000 |
| | | 15:0 | — | — | — | I2C2IP<2:0> | | | I2C2IS<1:0> | | — | — | — | U3IP<2:0> | | | U3IS<1:0> | | 0000 |
| | | | | | | | | | | | | | | SPI4IP<2:0> | | | SPI4IS<1:0> | | |
| | | | | | | | | | | | | | | I2C5IP<2:0> | | | I2C5IS<1:0> | | |
| 1120 | IPC9 | 31:16 | — | — | — | DMA3IP<2:0> | | | DMA3IS<1:0> | | — | — | — | DMA2IP<2:0> | | | DMA2IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | DMA1IP<2:0> | | | DMA1IS<1:0> | | — | — | — | DMA0IP<2:0> | | | DMA0IS<1:0> | | 0000 |
| 1130 | IPC10 | 31:16 | — | — | — | DMA7IP<2:0>(2) | | | DMA7IS<1:0>(2) | | — | — | — | DMA6IP<2:0>(2) | | | DMA6IS<1:0>(2) | | 0000 |
| | | 15:0 | — | — | — | DMA5IP<2:0>(2) | | | DMA5IS<1:0>(2) | | — | — | — | DMA4IP<2:0>(2) | | | DMA4IS<1:0>(2) | | 0000 |
| 1140 | IPC11 | 31:16 | — | — | — | CAN2IP<2:0>(2) | | | CAN2IS<1:0>(2) | | — | — | — | CAN1IP<2:0> | | | CAN1IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | USBIP<2:0> | | | USBIS<1:0> | | — | — | — | FCEIP<2:0> | | | FCEIS<1:0> | | 0000 |
| 1150 | IPC12 | 31:16 | — | — | — | U5IP<2:0> | | | U5IS<1:0> | | — | — | — | U6IP<2:0> | | | U6IS<1:0> | | 0000 |
| | | 15:0 | — | — | — | U4IP<2:0> | | | U4IS<1:0> | | — | — | — | ETHIP<2:0> | | | ETHIS<1:0> | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Except where noted, all registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This bit is unimplemented on PIC32MX764F128L device.

**3:** This register does not have associated CLR, SET, and INV registers.



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**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | SS0 |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | MVEC | — | TPC<2:0> | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **SS0:** Single Vector Shadow Register Set bit
- 1 = Single vector is presented with a shadow register set
- 0 = Single vector is not presented with a shadow register set

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multiple Vector Configuration bit
- 1 = Interrupt controller configured for Multi-vector mode
- 0 = Interrupt controller configured for Single-vector mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
- 111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
- 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
- 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
- 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
- 011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
- 010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
- 001 = Interrupts of group priority 1 start the Interrupt Proximity timer
- 000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

**REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | RIPL<2:0>(1) | | |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | VEC<5:0>(1) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **RIPL<2:0>:** Requested Priority Level bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits(1)

11111-00000 = The interrupt vector that is presented to the CPU

**Note 1:** This value should only be used when the interrupt controller is configured for Single-vector mode.

**REGISTER 7-3: TPTMR: TEMPORAL PROXIMITY TIMER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TPTMR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **TPTMR<31:0>:** Temporal Proximity Timer Reload bits
Used by the Temporal Proximity Timer as a reload value when the Temporal Proximity timer is triggered by an interrupt event.


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**REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS31 | IFS30 | IFS29 | IFS28 | IFS27 | IFS26 | IFS25 | IFS24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS23 | IFS22 | IFS21 | IFS20 | IFS19 | IFS18 | IFS17 | IFS16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS15 | IFS14 | IFS13 | IFS12 | IFS11 | IFS10 | IFS09 | IFS08 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IFS07 | IFS06 | IFS05 | IFS04 | IFS03 | IFS02 | IFS01 | IFS00 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IFS31-IFS00:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

**Note:** This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

**REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC31 | IEC30 | IEC29 | IEC28 | IEC27 | IEC26 | IEC25 | IEC24 |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC23 | IEC22 | IEC21 | IEC20 | IEC19 | IEC18 | IEC17 | IEC16 |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC15 | IEC14 | IEC13 | IEC12 | IEC11 | IEC10 | IEC09 | IEC08 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | IEC07 | IEC06 | IEC05 | IEC04 | IEC03 | IEC02 | IEC01 | IEC00 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **IEC31-IEC00:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note:** This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP03<2:0> | | | IS03<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP02<2:0> | | | IS02<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP01<2:0> | | | IS01<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP00<2:0> | | | IS00<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS03<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt sub-priority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS02<1:0>:** Interrupt Sub-priority bits
- 11 = Interrupt sub-priority is 3
- 10 = Interrupt sub-priority is 2
- 01 = Interrupt sub-priority is 1
- 00 = Interrupt sub-priority is 0

bit 15-13 **Unimplemented:** Read as '0'

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.


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**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)**

bit 12-10 **IP01<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 9-8 **IS01<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP00<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS00<1:0>:** Interrupt Sub-priority bits
11 = Interrupt sub-priority is 3
10 = Interrupt sub-priority is 2
01 = Interrupt sub-priority is 1
00 = Interrupt sub-priority is 0

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

**NOTES:**


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## 8.0 OSCILLATOR CONFIGURATION

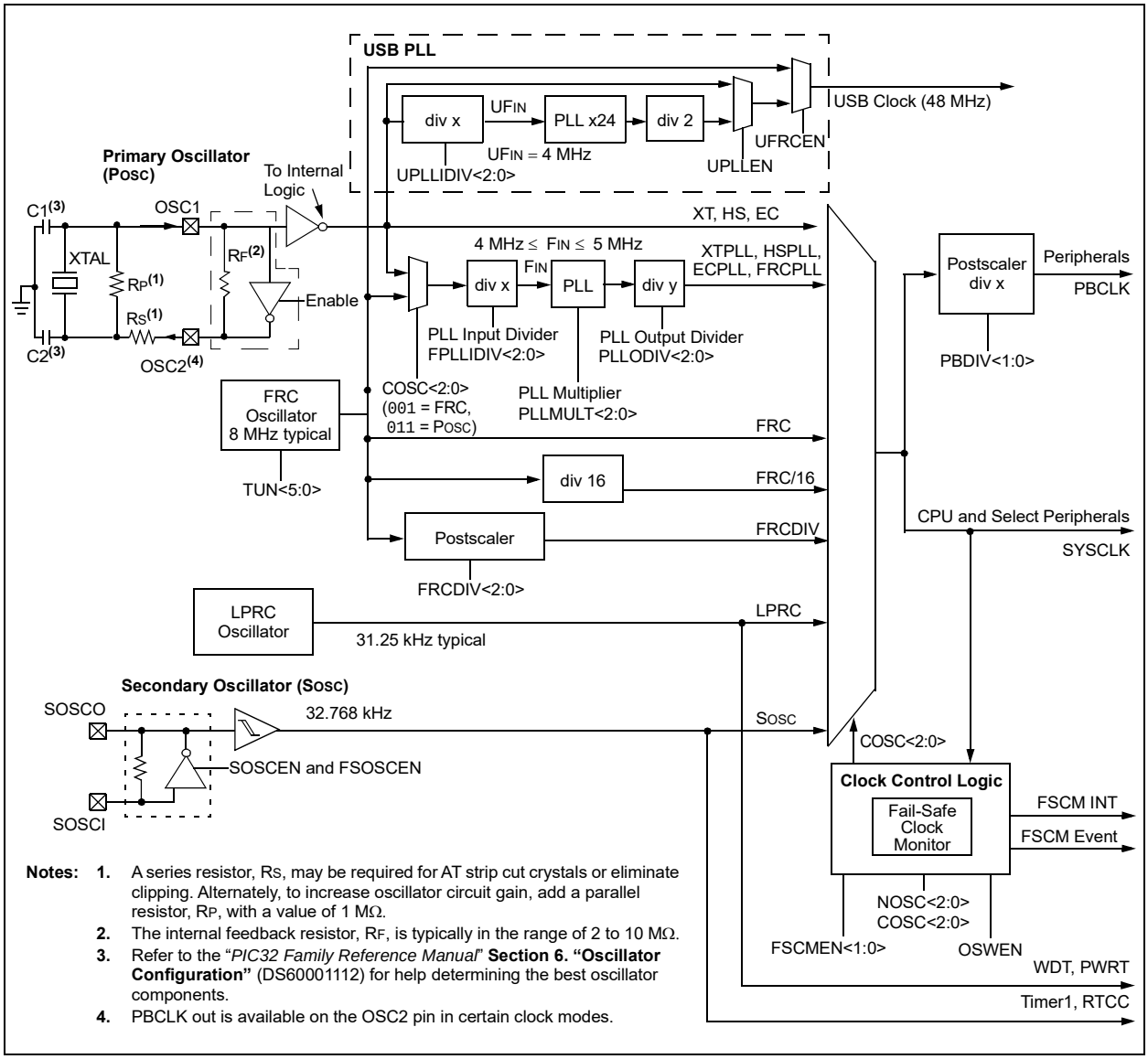
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Oscillator module has the following features:

- A total of four external and internal oscillator options as clock sources
- On-chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

Figure 8-1shows the Oscillator module block diagram.

**FIGURE 8-1: OSCILLATOR BLOCK DIAGRAM**




**Notes:**
1. A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. The internal feedback resistor, RF, is typically in the range of 2 to 10 MΩ.
3. Refer to the "*PIC32 Family Reference Manual*" **Section 6. "Oscillator Configuration"** (DS60001112) for help determining the best oscillator components.
4. PBCLK out is available on the OSC2 pin in certain clock modes.

## 8.1 Control Registers

**TABLE 8-1: OSCILLATOR REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F000 | OSCCON | 31:16 | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | | — | SOSCRDY | — | PBDIV<1:0> | | PLLMULT<2:0> | | | 0000 |
| | | 15:0 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN | SOSCEN | OSWEN | 0000 |
| F010 | OSCTUN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.



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**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-y | R/W-y | R/W-y | R/W-0 | R/W-0 | R/W-1 |
| | — | — | PLLODIV<2:0> | | | FRCDIV<2:0> | | |
| 23:16 | U-0 | R-0 | R-1 | R/W-y | R/W-y | R/W-y | R/W-y | R/W-y |
| | — | SOSCRDY | PBDIVRDY | PBDIV<1:0> | | PLLMULT<2:0> | | |
| 15:8 | U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
| | — | COSC<2:0> | | | — | NOSC<2:0> | | |
| 7:0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-y | R/W-0 |
| | CLKLOCK | ULOCK | SLOCK | SLPEN | CF | UFRCEN | SOSCEN | OSWEN |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2 (default setting)
000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Indicator bit

1 = Indicates that the Secondary Oscillator is running and is stable
0 = Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

1 = PBDIV<1:0> bits can be written
0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

11 = PBCLK is SYSCLK divided by 8 (default)
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 18-16 **PLLMULT<2:0>:** Phase-Locked Loop (PLL) Multiplier bits
- 111 = Clock is multiplied by 24
- 110 = Clock is multiplied by 21
- 101 = Clock is multiplied by 20
- 100 = Clock is multiplied by 19
- 011 = Clock is multiplied by 18
- 010 = Clock is multiplied by 17
- 001 = Clock is multiplied by 16
- 000 = Clock is multiplied by 15

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
- 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC (FRC) Oscillator divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator (POSC) with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (POSC) (XT, HS or EC)
- 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast RC (FRC) Oscillator

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
- 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
- 110 = Internal Fast RC Oscillator (FRC) divided by 16
- 101 = Internal Low-Power RC (LPRC) Oscillator
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
- 010 = Primary Oscillator (XT, HS or EC)
- 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
- 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit

If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
- 1 = Clock and PLL selections are locked
- 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x):
Clock and PLL selections are never locked and may be modified.

bit 6 **ULOCK:** USB PLL Lock Status bit
- 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
- 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled

bit 5 **SLOCK:** PLL Lock Status bit
- 1 = PLL module is in lock or PLL module start-up timer is satisfied
- 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **SLPEN:** Sleep Mode Enable bit
- 1 = Device will enter Sleep mode when a WAIT instruction is executed
- 0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
- 1 = FSCM has detected a clock failure
- 0 = No clock failure has been detected

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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**REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)**

bit 2 **UFRCEN:** USB FRC Clock Enable bit
- 1 = Enable FRC as the clock source for the USB clock source
- 0 = Use the Primary Oscillator or USB PLL as the USB clock source

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
- 1 = Enable Secondary Oscillator
- 0 = Disable Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Initiate an oscillator switch to selection specified by NOSC<2:0> bits
- 0 = Oscillator switch is complete

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

**REGISTER 8-2: OSCTUN: FRC TUNING REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | TUN<5:0>(1) | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits(1)

100000 = Center frequency -12.5% for PIC32MX575/595/675/695/775/795 devices
100000 = Center frequency -1.5% for PIC32MX534/564/664/764 devices
100001 =
•
•
•
111111 =
000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)
000001 =
•
•
•
011110 =
011111 = Center frequency +12.5% for PIC32MX575/595/675/695/775/795 devices
011111 = Center frequency +1.5% for PIC32MX534/564/664/764 devices

**Note 1:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

**Note:** Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.


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## 9.0 PREFETCH CACHE

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 4. "Prefetch Cache"** (DS60001119) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

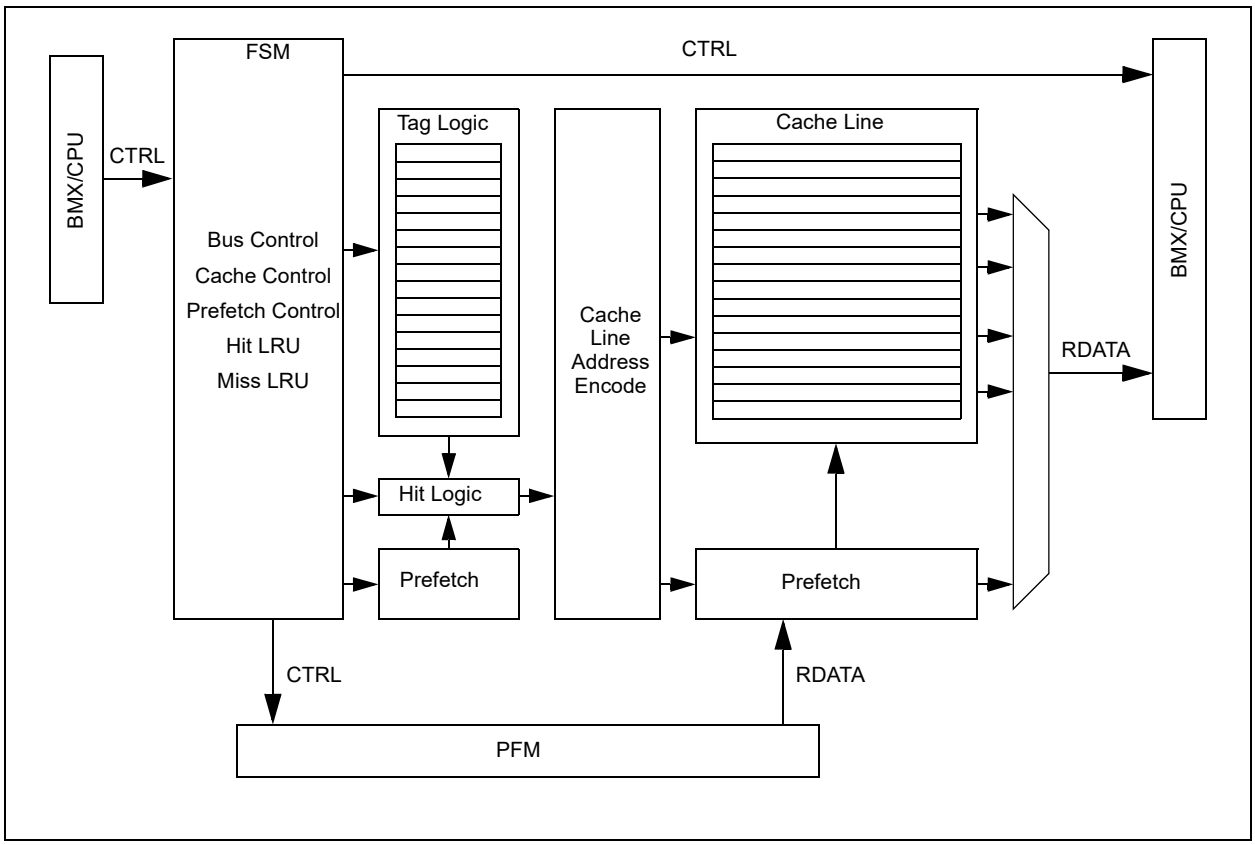
Prefetch cache increases performance for applications executing out of the cacheable program Flash memory regions by implementing instruction caching, constant data caching and instruction prefetching.

### 9.1 Features

- 16 fully-associative lockable cache lines
- 16-byte cache lines
- Up to four cache lines allocated to data
- Two cache lines with address mask to hold repeated instructions
- Pseudo-LRU replacement policy
- All cache lines are software writable
- 16-byte parallel memory fetch
- Predictive instruction prefetch

A simplified block diagram of the Prefetch Cache module is illustrated in Figure 9-1.

**FIGURE 9-1: PREFETCH CACHE MODULE BLOCK DIAGRAM**



## 9.2 Control Registers

**TABLE 9-1: PREFETCH REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 4000 | CHECON(1,2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CHECOH | 0000 |
| | | 15:0 | — | — | — | — | — | — | DCSZ<1:0> | | — | — | PREFEN<1:0> | | — | PFMWS<2:0> | | | 0007 |
| 4010 | CHEACC(1) | 31:16 | CHEWEN | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | CHEIDX<3:0> | | | | 0000 |
| 4020 | CHETAG(1) | 31:16 | LTAGBOOT | — | — | — | — | — | — | — | LTAG<23:16> | | | | | | | | 00xx |
| | | 15:0 | LTAG<15:4> | | | | | | | | | | | | LVALID | LLOCK | LTYPE | — | xxx2 |
| 4030 | CHEMSK(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LMASK<15:5> | | | | | | | | | | | — | — | — | — | — | 0000 |
| 4040 | CHEW0 | 31:16 | CHEW0<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4050 | CHEW1 | 31:16 | CHEW1<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4060 | CHEW2 | 31:16 | CHEW2<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4070 | CHEW3 | 31:16 | CHEW3<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 4080 | CHELRU | 31:16 | — | — | — | — | — | — | — | CHELRU<24:16> | | | | | | | | | 0000 |
| | | 15:0 | CHELRU<15:0> | | | | | | | | | | | | | | | | 0000 |
| 4090 | CHEHIT | 31:16 | CHEHIT<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 40A0 | CHEMIS | 31:16 | CHEMIS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 40C0 | CHEPFABT | 31:16 | CHEPFABT<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset value is dependent on DEVCFGx configuration.



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**REGISTER 9-1: CHECON: CACHE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | CHECOH |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | DCSZ<1:0> | |
| 7:0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | PREFEN<1:0> | | — | PFMWS<2:0> | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-17 **Unimplemented:** Write '0'; ignore read

bit 16 **CHECOH:** Cache Coherency Setting on a PFM Program Cycle bit
- 1 = Invalidate all data and instruction lines
- 0 = Invalidate all data lnes and instruction lines that are not locked

bit 15-10 **Unimplemented:** Write '0'; ignore read

bit 9-8 **DCSZ<1:0>:** Data Cache Size in Lines bits

Changing these bits causes all lines to be reinitialized to the "invalid" state.
- 11 = Enable data caching with a size of 4 lines
- 10 = Enable data caching with a size of 2 lines
- 01 = Enable data caching with a size of 1 line
- 00 = Disable data caching

bit 7-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits
- 11 = Enable predictive prefetch for both cacheable and non-cacheable regions
- 10 = Enable predictive prefetch only for non-cacheable regions
- 01 = Enable predictive prefetch only for cacheable regions
- 00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSLK Wait States bits
- 111 = Seven Wait states
- 110 = Six Wait states
- 101 = Five Wait states
- 100 = Four Wait states
- 011 = Three Wait states
- 010 = Two Wait states
- 001 = One Wait state
- 000 = Zero Wait state

**REGISTER 9-2: CHEACC: CACHE ACCESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | CHEWEN | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | CHEIDX<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **CHEWEN:** Cache Access Enable bits

These bits apply to registers CHETAG, CHEMSK, CHEW0, CHEW1, CHEW2, and CHEW3.

1 = The cache line selected by CHEIDX<3:0> is writeable

0 = The cache line selected by CHEIDX<3:0> is not writeable

bit 30-4 **Unimplemented:** Write '0'; ignore read

bit 3-0 **CHEIDX<3:0>:** Cache Line Index bits

The value selects the cache line for reading or writing.


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**REGISTER 9-3: CHETAG: CACHE TAG REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | LTAGBOOT | — | — | — | — | — | — | — |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | LTAG<19:12> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | LTAG<11:4> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-0 | R/W-0 | R/W-1 | U-0 |
| | LTAG<3:0> | | | | LVALID | LLOCK | LTYPE | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **LTAGBOOT:** Line Tag Address Boot bit
1 = The line is in the 0x1D000000 (physical) area of memory
0 = The line is in the 0x1FC00000 (physical) area of memory

bit 30-24 **Unimplemented:** Write '0'; ignore read

bit 23-4 **LTAG<19:0>:** Line Tag Address bits
LTAG<19:0> bits are compared against physical address to determine a hit. Because its address range and position of PFM in kernel space and user space, the LTAG PFM address is identical for virtual addresses, (system) physical addresses, and PFM physical addresses.

bit 3 **LVALID:** Line Valid bit
1 = The line is valid and is compared to the physical address for hit detection
0 = The line is not valid and is not compared to the physical address for hit detection

bit 2 **LLOCK:** Line Lock bit
1 = The line is locked and will not be replaced
0 = The line is not locked and can be replaced

bit 1 **LTYPE:** Line Type bit
1 = The line caches instruction words
0 = The line caches data words

bit 0 **Unimplemented:** Write '0'; ignore read

**REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LMASK<10:3> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | LMASK<2:0> | | | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-5 **LMASK<10:0>:** Line Mask bits

1 = Enables mask logic to force a match on the corresponding bit position in LTAG<19:0> bits (CHETAG<23:4>) and the physical address

0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B (disables mask logic)

bit 4-0 **Unimplemented:** Write '0'; ignore read

**REGISTER 9-5: CHEW0: CACHE WORD 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW0<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.


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**REGISTER 9-6: CHEW1: CACHE WORD 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW1<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW1<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW1<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW1<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW1<31:0>:** Word 1 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

**REGISTER 9-7: CHEW2: CACHE WORD 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW2<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW2<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW2<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW2<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW2<31:0>:** Word 2 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

**REGISTER 9-8: CHEW3: CACHE WORD 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEW3<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEW3<31:0>:** Word 3 of the cache line selected by CHEIDX<3:0> bits (CHEACC<3:0>)
Readable only if the device is not code-protected.

**Note:** This register is a window into the cache data array and is only readable if the device is not code-protected.

**REGISTER 9-9: CHELRU: CACHE LRU REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | — | — | — | — | — | — | — | CHELRU<24> |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHELRU<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-25 **Unimplemented:** Write '0'; ignore read

bit 24-0 **CHELRU<24:0>:** Cache Least Recently Used State Encoding bits
Indicates the pseudo-LRU state of the cache.


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**REGISTER 9-10: CHEHIT: CACHE HIT STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEHIT<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEHIT<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEHIT<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEHIT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEHIT<31:0>:** Cache Hit Count bits

Incremented each time the processor issues an instruction fetch or load that hits the prefetch cache from a cacheable region. Non-cacheable accesses do not modify this value.

**REGISTER 9-11: CHEMIS: CACHE MISS STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEMIS<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEMIS<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEMIS<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEMIS<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEMIS<31:0>:** Cache Miss Count bits

Incremented each time the processor issues an instruction fetch from a cacheable region that misses the prefetch cache. Non-cacheable accesses do not modify this value.

**REGISTER 9-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEPFABT<31:24> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEPFABT<23:16> | | | | | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEPFABT<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | CHEPFABT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHEPFABT<31:0>:** Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.


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## 10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

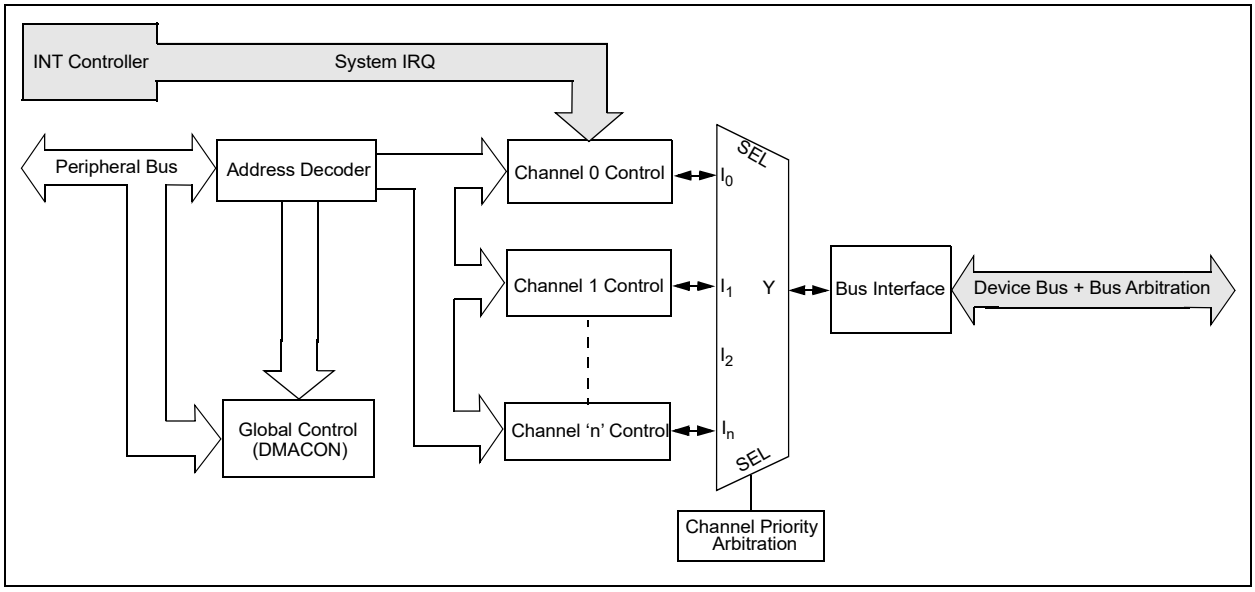
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as SPI, UART, PMP, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

**FIGURE 10-1: DMA BLOCK DIAGRAM**



## 10.1 Control Registers

### TABLE 10-1: DMA GLOBAL REGISTER MAP

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3000 | DMACON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | SUSPEND | DMABUSY | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 3010 | DMASTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RDWR | DMACH<2:0>(2) | | | 0000 |
| 3020 | DMAADDR | 31:16 | DMAADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMACH<3> bit is not available on PIC32MX534/564/664/764 devices.

### TABLE 10-2: DMA CRC REGISTER MAP(1)

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3030 | DCRCCON | 31:16 | — | — | BYTO<1:0> | | WBO | — | — | BITO | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | PLEN<4:0> | | | | | CRCEN | CRCAPP | CRCTYP | — | — | CRCCH<2:0> | | | 0000 |
| 3040 | DCRCDATA | 31:16 | DCRCDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3050 | DCRCXOR | 31:16 | DCRCXOR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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## TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3060 | DCH0CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3070 | DCH0ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3080 | DCH0INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3090 | DCH0SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30A0 | DCH0DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30B0 | DCH0SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30C0 | DCH0DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30D0 | DCH0SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30E0 | DCH0DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30F0 | DCH0CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3100 | DCH0CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3110 | DCH0DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 3120 | DCH1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3130 | DCH1ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3140 | DCH1INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3150 | DCH1SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3160 | DCH1DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3170 | DCH1SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

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**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3180 | DCH1DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3190 | DCH1SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31A0 | DCH1DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31B0 | DCH1CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31C0 | DCH1CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 31D0 | DCH1DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 31E0 | DCH2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 31F0 | DCH2ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3200 | DCH2INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3210 | DCH2SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3220 | DCH2DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3230 | DCH2SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3240 | DCH2DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3250 | DCH2SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3260 | DCH2DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3270 | DCH2CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3280 | DCH2CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.



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**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3290 | DCH2DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 32A0 | DCH3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 32B0 | DCH3ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 32C0 | DCH3INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 32D0 | DCH3SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 32E0 | DCH3DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 32F0 | DCH3SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3300 | DCH3DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3310 | DCH3SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3320 | DCH3DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3330 | DCH3CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3340 | DCH3CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3350 | DCH3DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 3360 | DCH4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3370 | DCH4ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3380 | DCH4INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3390 | DCH4SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 33A0 | DCH4DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

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**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 33B0 | DCH4SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ15:0> | | | | | | | | | | | | | | | | 0000 |
| 33C0 | DCH4DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 33D0 | DCH4SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 33E0 | DCH4DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 33F0 | DCH4CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3400 | DCH4CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3410 | DCH4DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 3420 | DCH5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3430 | DCH5ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3440 | DCH5INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3450 | DCH5SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3460 | DCH5DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3470 | DCH5SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3480 | DCH5DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3490 | DCH5SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 34A0 | DCH5DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 34B0 | DCH5CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 34C0 | DCH5CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.



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**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 34D0 | DCH5DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 34E0 | DCH6CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 34F0 | DCH6ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 3500 | DCH6INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3510 | DCH6SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3520 | DCH6DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3530 | DCH6SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3540 | DCH6DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3550 | DCH6SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3560 | DCH6DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3570 | DCH6CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3580 | DCH6CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3590 | DCH6DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 35A0 | DCH7CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 35B0 | DCH7ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FF00 |
| 35C0 | DCH7INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 35D0 | DCH7SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 35E0 | DCH7DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.

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**TABLE 10-3: DMA CHANNELS 0-7 REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 35F0 | DCH7SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3600 | DCH7DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3610 | DCH7SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3620 | DCH7DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3630 | DCH7CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3640 | DCH7CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3650 | DCH7DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** DMA channels 4-7 are not available on PIC32MX534/564/664/764 devices.



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**REGISTER 10-1: DMACON: DMA CONTROLLER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | — | SUSPEND | DMABUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 10-2: DMASTAT: DMA STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RDWR | DMACH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

**REGISTER 10-3: DMAADDR: DMA ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<31:24> | | | | | | | |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<23:16> | | | | | | | |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | DMAADDR<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.


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**REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | — | — | BYTO<1:0> | | WBO(1) | — | — | BITO |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | PLEN<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | CRCEN | CRCAPP(1) | CRCTYP | — | — | CRCCH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (reverse source byte order)
- 00 = No swapping (source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

**REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)**

bit 6 **CRCAPP:** CRC Append Mode bit(1)
1 = The DMA transfers data from the source into the CRC but not to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.


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**REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCDATA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return '0' on any read.

**REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DCRCXOR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
1 = Enable the XOR input to the Shift register
0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

**REGISTER 10-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | CHBUSY | — | — | — | — | — | — | CHCHNS(1) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R-0 | R/W-0 | R/W-0 |
| | CHEN(2) | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
- 1 = Channel is active or has been enabled
- 0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
- 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
- 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit
- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit
- 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
- 0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
- 1 = An event has been detected
- 0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
- 11 = Channel has priority 3 (highest)
- 10 = Channel has priority 2
- 01 = Channel has priority 1
- 00 = Channel has priority 0

**Note 1:** The chain selection bit takes effect when chaining is enabled (CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.


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**REGISTER 10-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHAIRQ<7:0>(1) | | | | | | | |
| 15:8 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | CHSIRQ<7:0>(1) | | | | | | | |
| 7:0 | S-0 | S-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — |

| Legend: | S = Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** See **Table 7-1: "Interrupt IRQ, Vector and Bit Location"** for the list of available interrupt IRQ sources.

**REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTR = CHSSIZ)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTR = CHSSIZ/2)
0 = No interrupt is pending


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**REGISTER 10-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)**

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected (either the source or the destination address is invalid)
0 = No interrupt is pending

**REGISTER 10-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
**Note:** This must be the physical address of the source.

**REGISTER 10-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
**Note:** This must be the physical address of the destination.


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**REGISTER 10-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size
•
•
•
0000000000000010 = 2 byte source size
0000000000000001 = 1 byte source size
0000000000000000 = 65,536 byte source size

**REGISTER 10-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size
•
•
•
0000000000000010 = 2 byte destination size
0000000000000001 = 1 byte destination size
0000000000000000 = 65,536 byte destination size

**REGISTER 10-14: DCHxSPTR: DMA CHANNEL 'x' SOURCE POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHSPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHSPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

1111111111111111 = Points to byte 65,535 of the source
•
•
•
0000000000000001 = Points to byte 1 of the source
0000000000000000 = Points to byte 0 of the source

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.

**REGISTER 10-15: DCHxDPTR: DMA CHANNEL 'x' DESTINATION POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHDPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHDPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

1111111111111111 = Points to byte 65,535 of the destination
•
•
•
0000000000000001 = Points to byte 1 of the destination
0000000000000000 = Points to byte 0 of the destination


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**REGISTER 10-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHCSIZ<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event
•
•
•
0000000000000010 = 2 bytes transferred on an event
0000000000000001 = 1 byte transferred on an event
0000000000000000 = 65,536 bytes transferred on an event

**REGISTER 10-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | CHCPTR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.

**REGISTER 10-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPDAT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.


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## 11.0 USB ON-THE-GO (OTG)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS60001126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation with a minimum of external components. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 11-1.

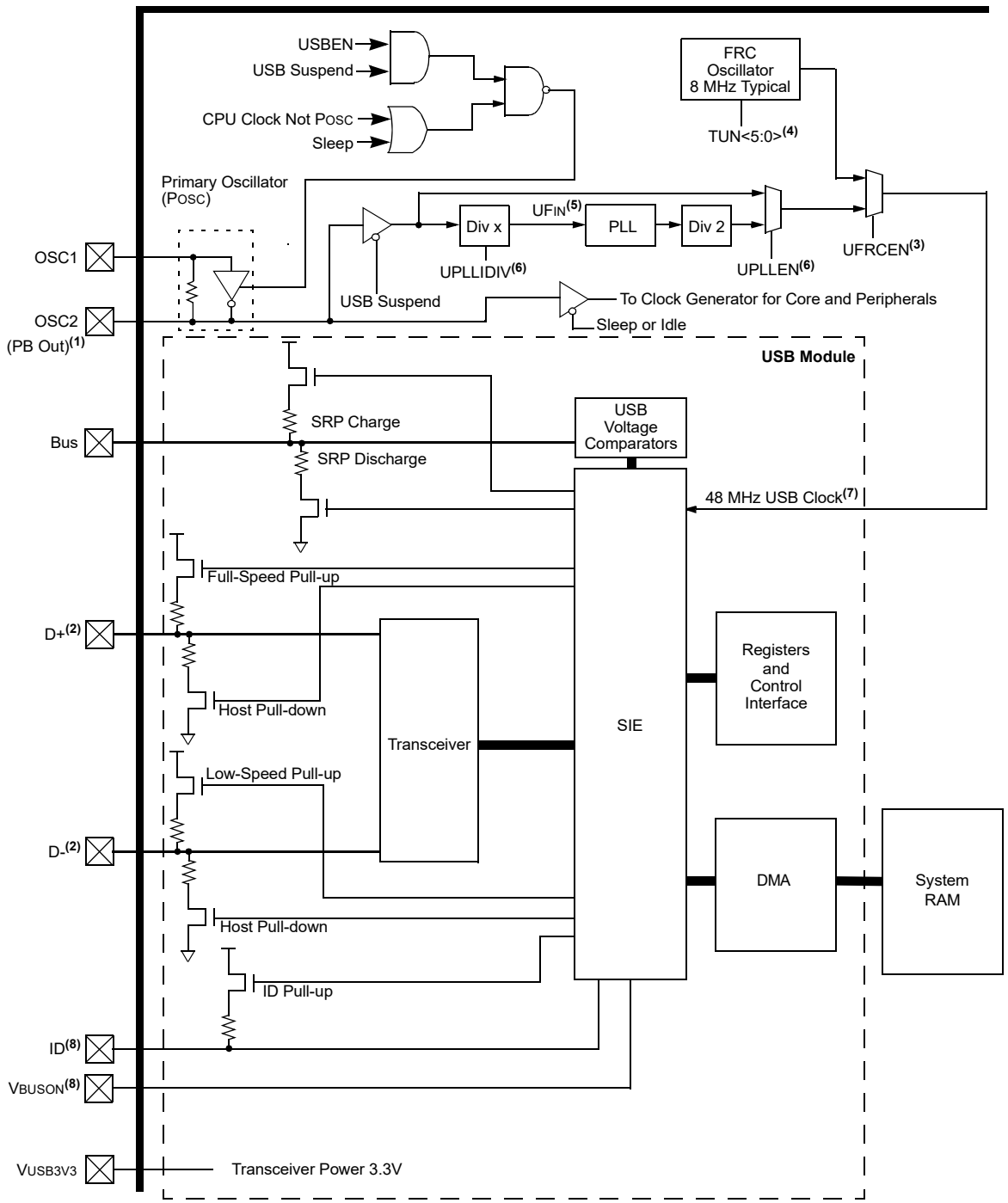
The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-speed support for host and device
- Low-speed host support
- USB OTG support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM and Flash

**Note:** The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

**FIGURE 11-1: PIC32MX5XX/6XX/7XX FAMILY USB INTERFACE DIAGRAM**




**Note 1:** PB clock is only available on this pin for select EC modes.
**2:** Pins can be used as digital inputs when USB is not enabled.
**3:** This bit field is contained in the OSCCON register.
**4:** This bit field is contained in the OSCTRM register.
**5:** USB PLL UFIN requirements: 4 MHz.
**6:** This bit field is contained in the DEVCFG2 register.
**7:** A 48 MHz clock is required for proper USB operation.
**8:** Pins can be used as GPIO when the USB module is disabled.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## 11.1 Control Registers

### TABLE 11-1: USB REGISTER MAP

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5040 | U1OTGIR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF | 0000 |
| 5050 | U1OTGIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE | 0000 |
| 5060 | U1OTGSTAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD | 0000 |
| 5070 | U1OTGCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS | 0000 |
| 5080 | U1PWRC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UACTPND(4) | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR | 0000 |
| 5200 | U1IR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIF | ATTACHIF | RESUMEIF | IDLEIF | TRNIF | SOFIF | UERRIF | URSTIF | 0000 |
| | | | | | | | | | | | | | | | | | | DETACHIF | 0000 |
| 5210 | U1IE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE | URSTIE | 0000 |
| | | | | | | | | | | | | | | | | | | DETACHIE | 0000 |
| 5220 | U1EIR(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEF | BMXEF | DMAEF | BTOEF | DFN8EF | CRC16EF | CRC5EF | PIDEF | 0000 |
| | | | | | | | | | | | | | | | | | EOFEF | | 0000 |
| 5230 | U1EIE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE | PIDEE | 0000 |
| | | | | | | | | | | | | | | | | | EOFEE | | 0000 |
| 5240 | U1STAT(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ENDPT<3:0>(4) | | | | DIR | PPBI | — | — | 0000 |
| 5250 | U1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | JSTATE(4) | SE0(4) | PKTDIS | USBRST | HOSTEN | RESUME | PPBRST | USBEN | 0000 |
| | | | | | | | | | | | | | TOKBUSY | | | | | SOFEN | 0000 |
| 5260 | U1ADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPDEN | DEVADDR<6:0> | | | | | | | 0000 |
| 5270 | U1BDTP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRL<7:1> | | | | | | | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.

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## TABLE 11-1: USB REGISTER MAP (CONTINUED)

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5280 | U1FRML(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | FRML<7:0> | | | | | | | | 0000 |
| 5290 | U1FRMH(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | FRMH<2:0> | | | 0000 |
| 52A0 | U1TOK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | PID<3:0> | | | | EP<3:0> | | | | 0000 |
| 52B0 | U1SOF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CNT<7:0> | | | | | | | | 0000 |
| 52C0 | U1BDTP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRH<7:0> | | | | | | | | 0000 |
| 52D0 | U1BDTP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BDTPTRU<7:0> | | | | | | | | 0000 |
| 52E0 | U1CNFG1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | UTEYE | UOEMON | — | USBSIDL | — | — | — | UASUSPND | 0001 |
| 5300 | U1EP0 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5310 | U1EP1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5320 | U1EP2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5330 | U1EP3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5340 | U1EP4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5350 | U1EP5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5360 | U1EP6 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5370 | U1EP7 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5380 | U1EP8 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 5390 | U1EP9 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.



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**TABLE 11-1: USB REGISTER MAP (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 53A0 | U1EP10 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53B0 | U1EP11 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53C0 | U1EP12 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53D0 | U1EP13 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53E0 | U1EP14 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |
| 53F0 | U1EP15 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (except as noted) have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register does not have associated SET and INV registers.

**3:** This register does not have associated CLR, SET and INV registers.

**4:** Reset value for this bit is undefined.

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**REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | U-0 | R/WC-0, HS |
| | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |

| **Legend:** | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state detected
- 0 = No change in ID state detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input detected
- 0 = No change on the session valid input detected


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**REGISTER 11-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
| | IDIE | T1MSECIE | LSTATEIE | ACTVIE | SESVDIE | SESENDIE | — | VBUSVDIE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit
- 1 = ID interrupt enabled
- 0 = ID interrupt disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
- 1 = 1 millisecond timer interrupt enabled
- 0 = 1 millisecond timer interrupt disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
- 1 = Line state interrupt enabled
- 0 = Line state interrupt disabled

bit 4 **ACTVIE:** Bus ACTIVITY Interrupt Enable bit
- 1 = ACTIVITY interrupt enabled
- 0 = ACTIVITY interrupt disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
- 1 = Session valid interrupt enabled
- 0 = Session valid interrupt disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
- 1 = B-session end interrupt enabled
- 0 = B-session end interrupt disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
- 1 = A-VBUS valid interrupt enabled
- 0 = A-VBUS valid interrupt disabled

**REGISTER 11-3: U1OTGSTAT: USB OTG STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | R-0 | U-0 | R-0 | R-0 | U-0 | R-0 |
| | ID | — | LSTATE | — | SESVD | SESEND | — | VBUSVD |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit
- 1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle
- 0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit
- 1 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has been stable for the previous 1 ms
- 0 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A or B device
- 0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit
- 1 = VBUS voltage is below Session Valid on the B device
- 0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
- 1 = VBUS voltage is above Session Valid on the A device
- 0 = VBUS voltage is below Session Valid on the A device


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**REGISTER 11-4: U1OTGCON: USB OTG CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor is enabled
0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor is enabled
0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
1 = D+ data line pull-down resistor is enabled
0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit
1 = D- data line pull-down resistor is enabled
0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit
1 = VBUS line is powered
0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit
1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit
1 = VBUS line is charged through a pull-up resistor
0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit
1 = VBUS line is discharged through a pull-down resistor
0 = VBUS line is not discharged through a resistor

**REGISTER 11-5: U1PWRC: USB POWER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | UACTPND | — | — | USLPGRD | USBBUSY | — | USUSPEND | USBPWR |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit
- 1 = USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
- 0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit
- 1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
- 0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit
- 1 = USB module is active or disabled, but not ready to be enabled
- 0 = USB module is not active and is ready to be enabled

**Note:** When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit
- 1 = USB module is placed in Suspend mode
  (The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
- 0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit
- 1 = USB module is turned on
- 0 = USB module is disabled
  (Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)


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**REGISTER 11-6: U1IR: USB INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R-0 | R/WC-0, HS |
| | STALLIF | ATTACHIF(1) | RESUMEIF(2) | IDLEIF | TRNIF(3) | SOFIF | UERRIF(4) | URSTIF(5) / DETACHIF(6) |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** STALL Handshake Interrupt bit
- 1 = In Host mode a STALL handshake was received during the handshake phase of the transaction. In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction.
- 0 = STALL handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
- 1 = Peripheral attachment was detected by the USB module
- 0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
- 1 = K-State is observed on the D+ or D- pin for 2.5 µs
- 0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
- 1 = Idle condition detected (constant Idle state of 3 ms or more)
- 0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
- 1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
- 0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
- 1 = SOF token received by the peripheral or the SOF threshold reached by the host
- 0 = SOF token was not received nor threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit(4)
- 1 = Unmasked error condition has occurred
- 0 = Unmasked error condition has not occurred

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)(5)
- 1 = Valid USB Reset has occurred
- 0 = No USB Reset has occurred

**DETACHIF:** USB Detach Interrupt bit (Host mode)(6)
- 1 = Peripheral detachment was detected by the USB module
- 0 = Peripheral detachment was not detected

**Note 1:** This bit is only valid if the HOSTEN bit is set (see Register 11-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.

**2:** When not in Suspend mode, this interrupt should be disabled.

**3:** Clearing this bit will cause the STAT FIFO to advance.

**4:** Only error conditions enabled through the U1EIE register will set this bit.

**5:** Device mode.

**6:** Host mode.

**REGISTER 11-7: U1IE: USB INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | STALLIE | ATTACHIE | RESUMEIE | IDLEIE | TRNIE | SOFIE | UERRIE(1) | URSTIE(2) / DETACHIE(3) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit
- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit
- 1 = ATTACH interrupt is enabled
- 0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
- 1 = RESUME interrupt is enabled
- 0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
- 1 = Idle interrupt is enabled
- 0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
- 1 = TRNIF interrupt is enabled
- 0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
- 1 = SOFIF interrupt is enabled
- 0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
- 1 = USB Error interrupt is enabled
- 0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
- 1 = URSTIF interrupt is enabled
- 0 = URSTIF interrupt is disabled

**DETACHIE:** USB Detach Interrupt Enable bit(3)
- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

**Note 1:** For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
**2:** Device mode.
**3:** Host mode.


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**REGISTER 11-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS |
| | BTSEF | BMXEF | DMAEF(1) | BTOEF(2) | DFN8EF | CRC16EF | CRC5EF(4) / EOFEF(3,5) | PIDEF |

| Legend: | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEF:** Bit Stuff Error Flag bit
- 1 = Packet is rejected due to bit stuff error
- 0 = Packet is accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
- 1 = Invalid base address of the BDT, or the address of an individual buffer pointed to by a BDT entry
- 0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
- 1 = USB DMA error condition detected
- 0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-Out Error Flag bit(2)
- 1 = Bus turnaround time-out has occurred
- 0 = No bus turnaround time-out

bit 3 **DFN8EF:** Data Field Size Error Flag bit
- 1 = Data field received is not an integral number of bytes
- 0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
- 1 = Data packet is rejected due to CRC16 error
- 0 = Data packet is accepted

bit 1 **CRC5EF:** CRC5 Host Error Flag bit(4)
- 1 = Token packet is rejected due to CRC5 error
- 0 = Token packet is accepted

**EOFEF:** EOF Error Flag bit(3,5)
- 1 = EOF error condition is detected
- 0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit
- 1 = PID check is failed
- 0 = PID check is passed

**Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

**2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.

**3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

**4:** Device mode.

**5:** Host mode.

**REGISTER 11-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BTSEE | BMXEE | DMAEE | BTOEE | DFN8EE | CRC16EE | CRC5EE(1) / EOFEE(2) | PIDEE |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

**EOFEE:** EOF Error Interrupt Enable bit(2)
- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

**Note 1:** Device mode.
**2:** Host mode.

**Note:** For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.


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**REGISTER 11-10: U1STAT: USB STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | U-0 | U-0 |
| | ENDPT<3:0> | | | | DIR | PPBI | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

1111 = Endpoint 15
1110 = Endpoint 14
•
•
•
0001 = Endpoint 1
0000 = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit

1 = Last transaction was a transmit transfer (TX)
0 = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit

1 = The last transaction was to the Odd buffer descriptor bank
0 = The last transaction was to the Even buffer descriptor bank

bit 1-0 **Unimplemented:** Read as '0'

**Note:** The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. U1STAT value is only valid when U1IR<TRNIF> is active. Clearing the U1IR<TRNIF> bit advances the FIFO. Data in register is invalid when U1IR<TRNIF> = 0.

**REGISTER 11-11: U1CON: USB CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | JSTATE | SE0 | PKTDIS(4) / TOKBUSY(1,5) | USBRST | HOSTEN(2) | RESUME(3) | PPBRST | USBEN(4) / SOFEN(5) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE was detected on the USB
0 = JSTATE was not detected

bit 6 **SE0:** Live Single-Ended Zero flag bit
1 = Single-ended zero was detected on the USB
0 = Single-ended zero was not detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
1 = Token and packet processing disabled (set upon SETUP token received)
0 = Token and packet processing enabled
**TOKBUSY:** Token Busy Indicator bit(1,5)
1 = Token being executed by the USB module
0 = No token being executed

bit 4 **USBRST:** Module Reset bit(5)
1 = USB reset is generated
0 = USB reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit(3)
1 = RESUME signaling is activated
0 = RESUME signaling is disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
**2:** All host control logic is reset any time that the value of this bit is toggled.
**3:** Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
**4:** Device mode.
**5:** Host mode.


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**REGISTER 11-11: U1CON: USB CONTROL REGISTER (CONTINUED)**

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Reset all Even/Odd buffer pointers to the Even buffer descriptor banks
0 = Even/Odd buffer pointers are not reset

bit 0 **USBEN:** USB Module Enable bit(4)
1 = USB module and supporting circuitry is enabled
0 = USB module and supporting circuitry is disabled

**SOFEN:** SOF Enable bit(5)
1 = SOF token is sent every 1 ms
0 = SOF token is disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).

**2:** All host control logic is reset any time that the value of this bit is toggled.

**3:** Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

**4:** Device mode.

**5:** Host mode.

**REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LSPDEN | DEVADDR<6:0> | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low-speed
0 = Next token command to be executed at full-speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

**REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FRML<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.


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**REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | FRMH<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** Upper 3 bits of the Frame Numbers bits
These register bits are updated with the current frame number whenever a SOF TOKEN is received.

**REGISTER 11-15: U1TOK: USB TOKEN REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PID<3:0> | | | | EP<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
1101 = SETUP (TX) token type transaction
1001 = IN (RX) token type transaction
0001 = OUT (TX) token type transaction
**Note:** All other values not listed, are Reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

**REGISTER 11-16: U1SOF: USB SOF THRESHOLD REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:
01001010 = 64-byte packet
00101010 = 32-byte packet
00011010 = 16-byte packet
00010010 = 8-byte packet

**REGISTER 11-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
| | BDTPTRL<15:9> | | | | | | | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** BDT Base Address bits

This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'


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**REGISTER 11-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRH<23:16> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRH<23:16>:** BDT Base Address bits

This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

**REGISTER 11-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BDTPTRU<31:24> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **BDTPTRU<31:24>:** BDT Base Address bits

This 8-bit value provides address bits 31 through 24 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

**REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | UTEYE | UOEMON | — | USBSIDL | — | — | — | UASUSPND |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit
1 = Eye-Pattern Test is enabled
0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB $\overline{OE}$ Monitor Enable bit
1 = $\overline{OE}$ signal is active; it indicates intervals during which the D+/D- lines are driving
0 = $\overline{OE}$ signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit
1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.
0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.


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**REGISTER 11-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | LSPD | RETRYDIS | — | EPCONDIS | EPRXEN | EPTXEN | EPSTALL | EPHSHK |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
1 = Direct connection to a low-speed device enabled
0 = Direct connection to a low-speed device disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
1 = Retry NACK'd transactions disabled
0 = Retry NACK'd transactions enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disable Endpoint 'n' from control transfers; only TX and RX transfers are allowed
0 = Enable Endpoint 'n' for control (SETUP) transfers; TX and RX transfers are also allowed
Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint 'n' receive is enabled
0 = Endpoint 'n' receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint 'n' transmit is enabled
0 = Endpoint 'n' transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint 'n' was stalled
0 = Endpoint 'n' was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint Handshake is enabled
0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

**NOTES:**


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## 12.0 I/O PORTS

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

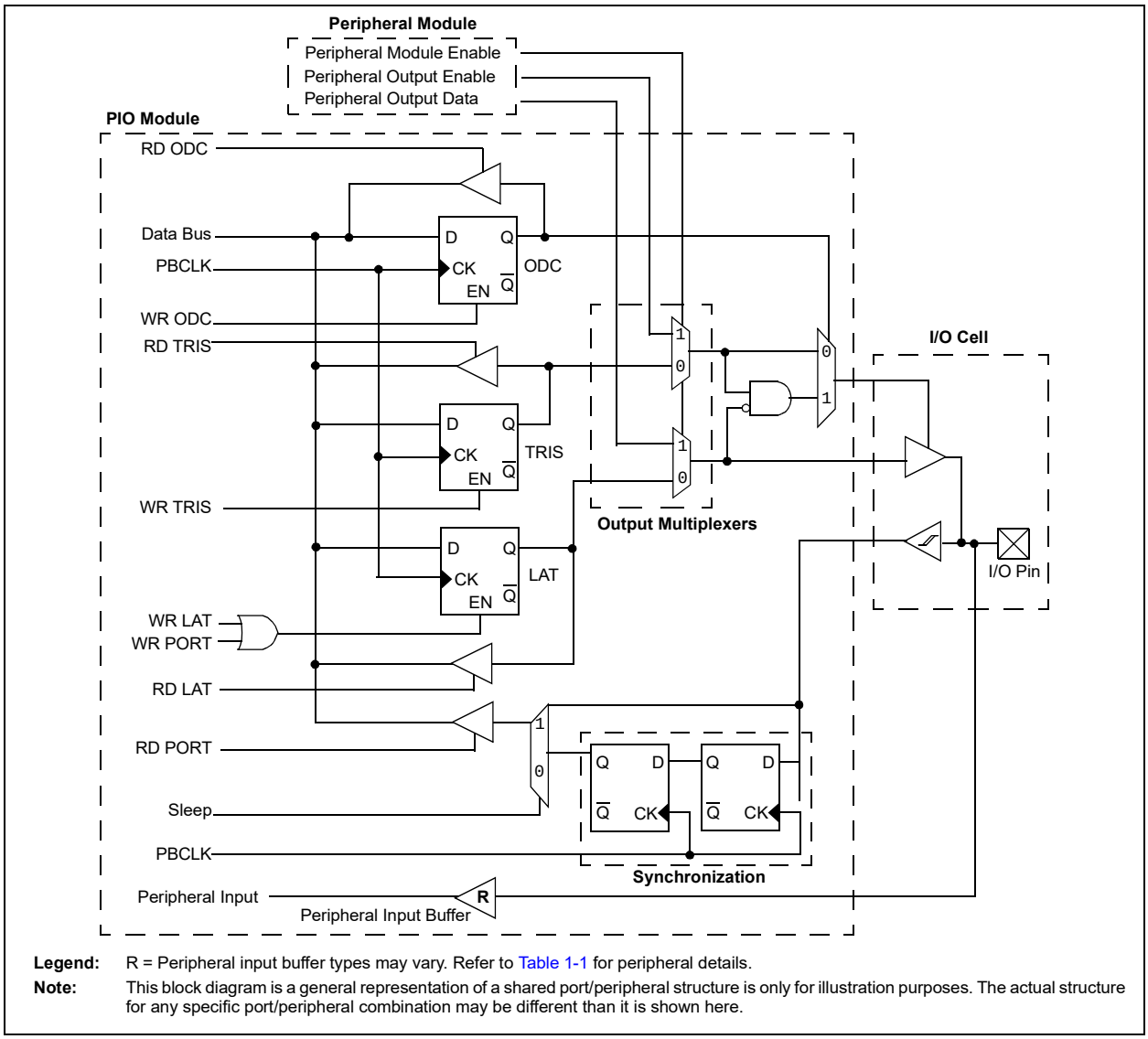
General purpose I/O pins are the simplest of peripherals. They allow the PIC32 MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Following are some of the key features of this module:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up enable/disable
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

**FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE**




**Legend:** R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

**Note:** This block diagram is a general representation of a shared port/peripheral structure is only for illustration purposes. The actual structure for any specific port/peripheral combination may be different than it is shown here.

## 12.1 Parallel I/O (PIO) Ports

All port pins have three registers (TRIS, LAT and PORT) that are directly associated with their operation.

TRIS is a Data Direction or Tri-State Control register that determines whether a digital pin is an input or an output. Setting a TRISx register bit = 1, configures the corresponding I/O pin as an input; setting a TRISx register bit = 0, configures the corresponding I/O pin as an output. All port I/O pins are defined as inputs after a device Reset. Certain I/O pins are shared with analog peripherals and default to analog inputs after a device Reset.

PORT is a register used to read the current state of the signal applied to the port I/O pins. Writing to a PORTx register performs a write to the port's latch, LATx register, latching the data to the port's I/O pins.

LAT is a register used to write data to the port I/O pins. The LATx Latch register holds the data written to either the LATx or PORTx registers. Reading the LATx Latch register reads the last value written to the corresponding PORT or Latch register.

Not all port I/O pins are implemented on some devices, therefore, the corresponding PORTx, LATx and TRISx register bits will read as zeros.

### 12.1.1 CLR, SET AND INV REGISTERS

Every I/O module register has a corresponding Clear (CLR), Set (SET) and Invert (INV) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

| | |
|---|---|
| **Note:** | Using a PORTxINV register to toggle a bit is recommended because the operation is performed in hardware atomically, using fewer instructions, as compared to the traditional read-modify-write method, as follows:<br>`PORTC ^ = 0x0001;` |

### 12.1.2 DIGITAL INPUTS

Pins are configured as digital inputs by setting the corresponding TRIS register bits = 1. When configured as inputs, they are either TTL buffers or Schmitt Triggers. Several digital pins share functionality with analog inputs and default to the analog inputs at POR. Setting the corresponding bit in the AD1PCFG register = 1 enables the pin as a digital pin.

The maximum input voltage allowed on the input pins is the same as the maximum VIH specification. Refer to **Section 32.0 "Electrical Characteristics"** for VIH specification details.

| | |
|---|---|
| **Note:** | Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications. |

### 12.1.3 ANALOG INPUTS

Certain pins can be configured as analog inputs used by the ADC and comparator modules. Setting the corresponding bits in the AD1PCFG register = 0 enables the pin as an analog input pin and must have the corresponding TRIS bit set = 1 (input). If the TRIS bit is cleared = 0 (output), the digital output level (VOH or VOL) will be converted. Any time a port I/O pin is configured as analog, its digital input is disabled and the corresponding PORTx register bit will read '0'. The AD1PCFG register has a default value of 0x0000; therefore, all pins that share ANx functions are analog (not digital) by default.

### 12.1.4 DIGITAL OUTPUTS

Pins are configured as digital outputs by setting the corresponding TRIS register bits = 0. When configured as digital outputs, these pins are CMOS drivers or can be configured as open-drain outputs by setting the corresponding bits in the Open-Drain Configuration (ODCx) register.

The open-drain feature allows generation of outputs higher than VDD (e.g., 5V) on any desired 5V tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the **"Device Pin Tables"** section for the available pins and their functionality.

### 12.1.5 ANALOG OUTPUTS

Certain pins can be configured as analog outputs, such as the CVREF output voltage used by the comparator module. Configuring the comparator reference module to provide this output will present the analog output voltage on the pin, independent of the TRIS register setting for the corresponding pin.

### 12.1.6 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports (CNx) allows devices to generate interrupt requests in response to change-of-state on selected pin.

Each CNx pin also has a weak pull-up, which acts as a current source connected to the pin. The pull-ups are enabled by setting the corresponding bit in the CNPUE register.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## 12.2 Control Registers

**TABLE 12-1: PORTA REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | TRISA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISA15 | TRISA14 | — | — | — | TRISA10 | TRISA9 | — | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | C6FF |
| 6010 | PORTA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RA15 | RA14 | — | — | — | RA10 | RA9 | — | RA7 | RA6 | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| 6020 | LATA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATA15 | LATA14 | — | — | — | LATA10 | LATA9 | — | LATA7 | LATA6 | LATA5 | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| 6030 | ODCA | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCA15 | ODCA14 | — | — | — | ODCA10 | ODCA9 | — | ODCA7 | ODCA6 | ODCA5 | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-2: PORTB REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6040 | TRISB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| 6050 | PORTB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| 6060 | LATB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| 6070 | ODCB | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCB15 | ODCB14 | ODCB13 | ODCB12 | ODCB11 | ODCB10 | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 12-3: PORTC REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6080 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | — | — | — | — | — | F000 |
| 6090 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| 60A0 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| 60B0 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-4: PORTC REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6080 | TRISC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISC15 | TRISC14 | TRISC13 | TRISC12 | — | — | — | — | — | — | — | TRISC4 | TRISC3 | TRISC2 | TRISC1 | — | F00F |
| 6090 | PORTC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RC15 | RC14 | RC13 | RC12 | — | — | — | — | — | — | — | RC4 | RC3 | RC2 | RC1 | — | xxxx |
| 60A0 | LATC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATC15 | LATC14 | LATC13 | LATC12 | — | — | — | — | — | — | — | LATC4 | LATC3 | LATC2 | LATC1 | — | xxxx |
| 60B0 | ODCC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCC15 | ODCC14 | ODCC13 | ODCC12 | — | — | — | — | — | — | — | ODCC4 | ODCC3 | ODCC2 | ODCC1 | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**TABLE 12-5: PORTD REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 60C0 | TRISD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | 0FFF |
| 60D0 | PORTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| 60E0 | LATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| 60F0 | ODCD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | ODCD11 | ODCD10 | ODCD9 | ODCD8 | ODCD7 | ODCD6 | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-6: PORTD REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 60C0 | TRISD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISD15 | TRISD14 | TRISD13 | TRISD12 | TRISD11 | TRISD10 | TRISD9 | TRISD8 | TRISD7 | TRISD6 | TRISD5 | TRISD4 | TRISD3 | TRISD2 | TRISD1 | TRISD0 | FFFF |
| 60D0 | PORTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RD15 | RD14 | RD13 | RD12 | RD11 | RD10 | RD9 | RD8 | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RD0 | xxxx |
| 60E0 | LATD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LAT15 | LAT14 | LAT13 | LAT12 | LATD11 | LATD10 | LATD9 | LATD8 | LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 | xxxx |
| 60F0 | ODCD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCD15 | ODCD14 | ODCD13 | ODCD12 | ODCD11 | ODCD10 | ODCD9 | ODCD8 | ODCD7 | ODCD6 | ODCD5 | ODCD4 | ODCD3 | ODCD2 | ODCD1 | ODCD0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 12-7: PORTE REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 00FF |
| 6110 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6120 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6130 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | ODCE7 | 0DCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-8: PORTE REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6100 | TRISE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISE9 | TRISE8 | TRISE7 | TRISE6 | TRISE5 | TRISE4 | TRISE3 | TRISE2 | TRISE1 | TRISE0 | 03FF |
| 6110 | PORTE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RE9 | RE8 | RE7 | RE6 | RE5 | RE4 | RE3 | RE2 | RE1 | RE0 | xxxx |
| 6120 | LATE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATE9 | LATE8 | LATE7 | LATE6 | LATE5 | LATE4 | LATE3 | LATE2 | LATE1 | LATE0 | xxxx |
| 6130 | ODCE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCE9 | ODCE8 | ODCE7 | 0DCE6 | ODCE5 | ODCE4 | ODCE3 | ODCE2 | ODCE1 | ODCE0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**TABLE 12-9: PORTF REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | — | TRISF1 | TRISF0 | 003B |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | — | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | — | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | — | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-10: PORTF REGISTER MAP PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX775F256L, PIC32MX764F128L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6140 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | TRISF13 | TRISF12 | — | — | — | TRISF8 | — | — | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | 313F |
| 6150 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | RF13 | RF12 | — | — | — | RF8 | — | — | RF5 | RF4 | RF3 | RF2 | RF1 | RF0 | xxxx |
| 6160 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | LATF13 | LATF12 | — | — | — | LATF8 | — | — | LATF5 | LATF4 | LATF3 | LATF2 | LATF1 | LATF0 | xxxx |
| 6170 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | ODCF13 | ODCF12 | — | — | — | ODCF8 | — | — | ODCF5 | ODCF4 | ODCF3 | ODCF2 | ODCF1 | ODCF0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 12-11: PORTG REGISTER MAP FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6180 | TRISG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | — | — | 03CC |
| 6190 | PORTG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3 | RG2 | — | — | xxxx |
| 61A0 | LATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | — | — | xxxx |
| 61B0 | ODCG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | ODCG3 | ODCG2 | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-12: PORTG REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6180 | TRISG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TRISG15 | TRISG14 | TRISG13 | TRISG12 | — | — | TRISG9 | TRISG8 | TRISG7 | TRISG6 | — | — | TRISG3 | TRISG2 | TRISG1 | TRISG0 | F3CF |
| 6190 | PORTG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RG15 | RG14 | RG13 | RG12 | — | — | RG9 | RG8 | RG7 | RG6 | — | — | RG3 | RG2 | RG1 | RG0 | xxxx |
| 61A0 | LATG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | LATG15 | LATG14 | LATG13 | LATG12 | — | — | LATG9 | LATG8 | LATG7 | LATG6 | — | — | LATG3 | LATG2 | LATG1 | LATG0 | xxxx |
| 61B0 | ODCG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ODCG15 | ODCG14 | ODCG13 | ODCG12 | — | — | ODCG9 | ODCG8 | ODCG7 | ODCG6 | — | — | ODCG3 | ODCG2 | ODCG1 | ODCG0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**TABLE 12-13: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX695F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512 AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 61C0 | CNCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 61D0 | CNEN | 31:16 | — | — | — | — | — | — | — | — | — | — | CNEN21 | CNEN20 | CNEN19 | CNEN18 | CNEN17 | CNEN16 | 0000 |
| | | 15:0 | CNEN15 | CNEN14 | CNEN13 | CNEN12 | CNEN11 | CNEN10 | CNEN9 | CNEN8 | CNEN7 | CNEN6 | CNEN5 | CNEN4 | CNEN3 | CNEN2 | CNEN1 | CNEN0 | 0000 |
| 61E0 | CNPUE | 31:16 | — | — | — | — | — | — | — | — | — | — | CNPUE21 | CNPUE20 | CNPUE19 | CNPUE18 | CNPUE17 | CNPUE16 | 0000 |
| | | 15:0 | CNPUE15 | CNPUE14 | CNPUE13 | CNPUE12 | CNPUE11 | CNPUE10 | CNPUE9 | CNPUE8 | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**TABLE 12-14: CHANGE NOTICE AND PULL-UP REGISTER MAP FOR PIC32MX575F256H, PIC32MX575F512H, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H AND PIC32MX795F512H DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 61C0 | CNCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 61D0 | CNEN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | CNEN18 | CNEN17 | CNEN16 | 0000 |
| | | 15:0 | CNEN15 | CNEN14 | CNEN13 | CNEN12 | CNEN11 | CNEN10 | CNEN9 | CNEN8 | CNEN7 | CNEN6 | CNEN5 | CNEN4 | CNEN3 | CNEN2 | CNEN1 | CNEN0 | 0000 |
| 61E0 | CNPUE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | CNPUE18 | CNPUE17 | CNPUE16 | 0000 |
| | | 15:0 | CNPUE15 | CNPUE14 | CNPUE13 | CNPUE12 | CNPUE11 | CNPUE10 | CNPUE9 | CNPUE8 | CNPUE7 | CNPUE6 | CNPUE5 | CNPUE4 | CNPUE3 | CNPUE2 | CNPUE1 | CNPUE0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**REGISTER 12-1: CNCON: CHANGE NOTICE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Change Notice (CN) Control ON bit
- 1 = CN is enabled
- 0 = CN is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Idle mode halts CN operation
- 0 = Idle mode does not affect CN operation

bit 12-0 **Unimplemented:** Read as '0'


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## 13.0 TIMER1

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the low-power Secondary Oscillator (SOSC) for Real-Time Clock (RTC) applications. The following modes are supported:

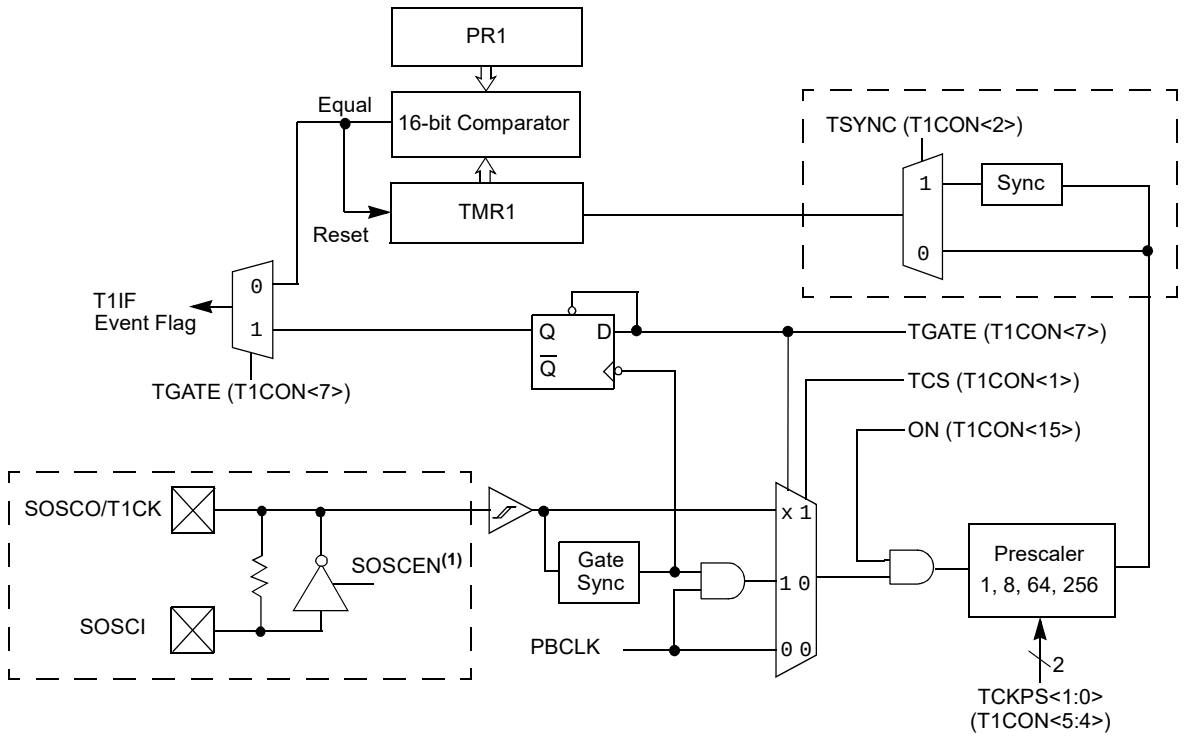
- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

## 13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a Real-Time Clock (RTC)

A simplified block diagram of the Timer1 module is illustrated in Figure 13-1.

**FIGURE 13-1: TIMER1 BLOCK DIAGRAM**




**Note 1:** The default state of the SOSCEN (OSCCON<1>) during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

## 13.2 Control Registers

**TABLE 13-1: TIMER1 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0600 | T1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | TWDIS | TWIP | — | — | — | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — | 0000 |
| 0610 | TMR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR1<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0620 | PR1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR1<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | TWDIS | TWIP | — | — | — |
| 7:0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
| | TGATE | — | TCKPS<1:0> | | — | TSYNC | TCS | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Timer is enabled
- 0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device is in Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit
- 1 = Writes to TMR1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:
- 1 = Asynchronous write to TMR1 register in progress
- 0 = Asynchronous write to TMR1 register complete

In Synchronous Timer mode:
This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:
This bit is ignored.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 13-1: T1CON: TYPE A TIMER CONTROL REGISTER (CONTINUED)**

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer Clock Source Select bit

1 = External clock from TxCKI pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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## 14.0 TIMER2/3, TIMER4/5

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-bit Timer
- Synchronous Internal 16-bit Gated Timer
- Synchronous External 16-bit Timer

Two 32-bit synchronous timers are available by combining Timer2 with Timer3 and Timer4 with Timer5. The 32-bit timers can operate in three modes:

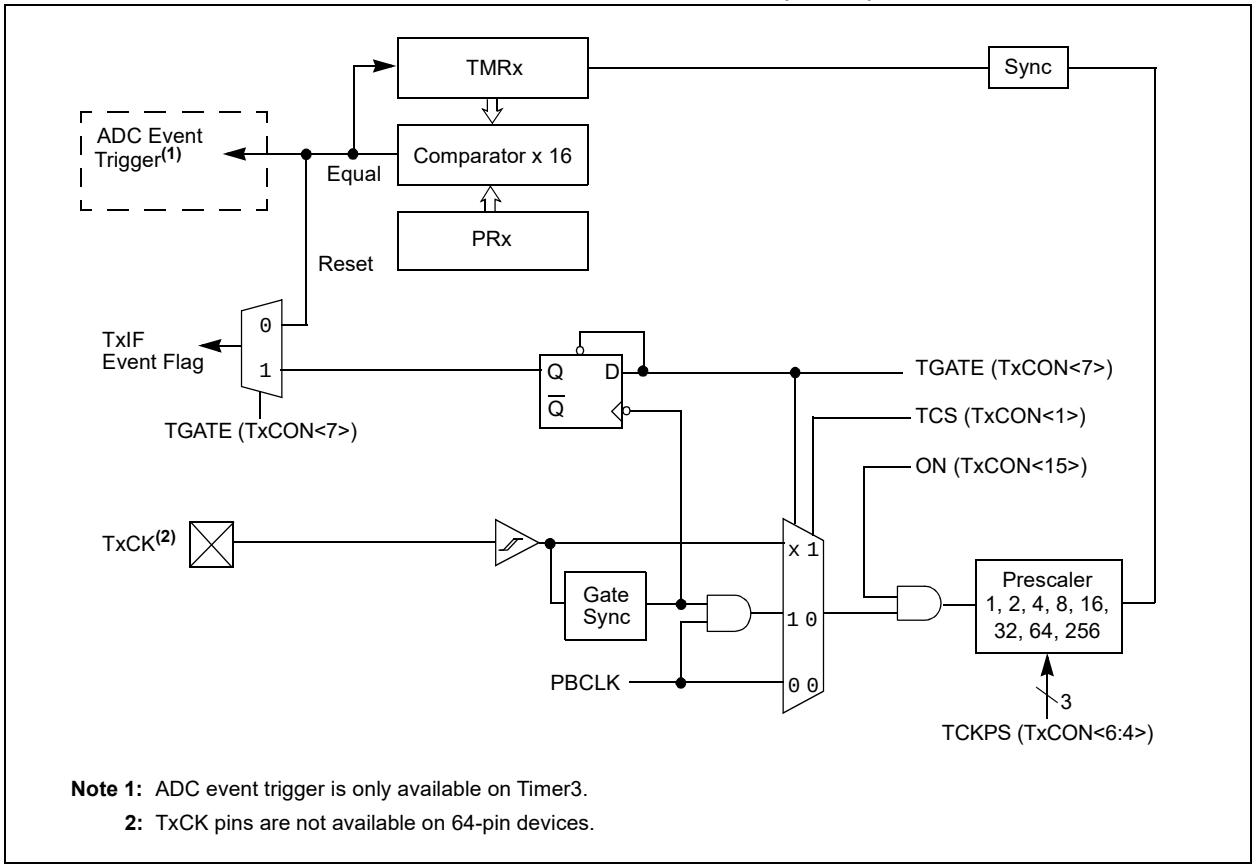
- Synchronous Internal 32-bit Timer
- Synchronous Internal 32-bit Gated Timer
- Synchronous External 32-bit Timer

**Note:** In this chapter, references to registers, TxCON, TMRx and PRx, use 'x' to represent Timer2 through Timer5 in 16-bit modes. In 32-bit modes, 'x' represents Timer2 or Timer4; 'y' represents Timer3 or Timer5.

### 14.1 Additional Supported Features

- Selectable clock prescaler
- Timers operational during CPU idle
- Time base for Input Capture and Output Compare modules (only Timer2 and Timer3)
- ADC event trigger (only Timer3)
- Fast bit manipulation using CLR, SET and INV registers

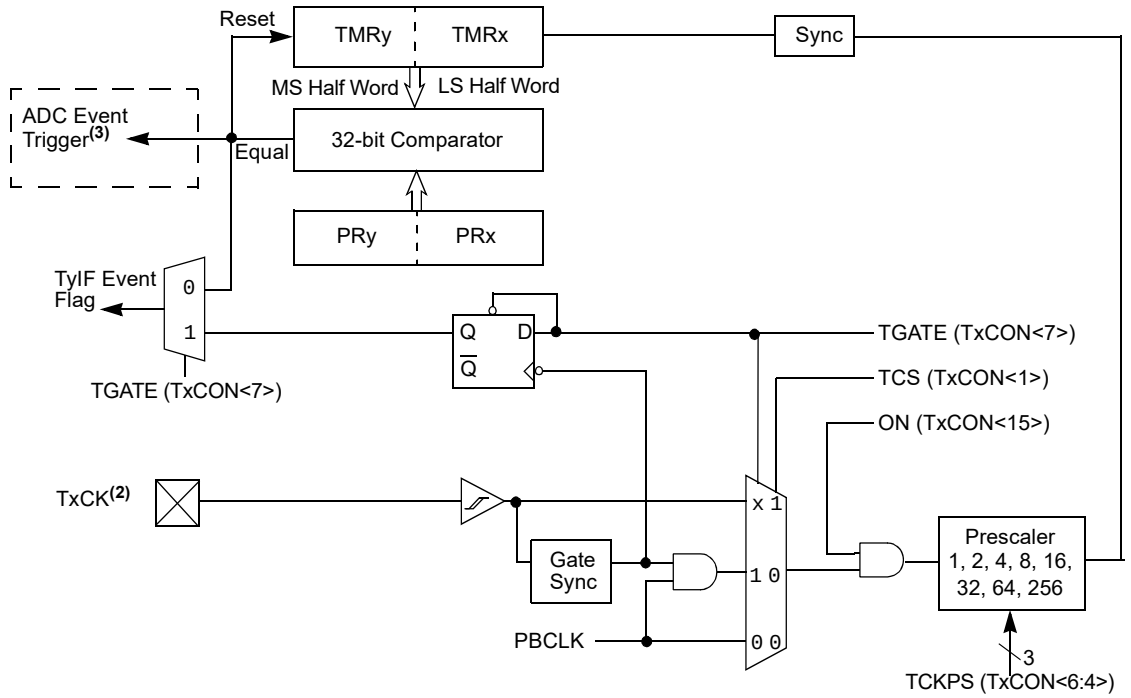
**FIGURE 14-1: TIMER2/3 AND TIMER4/5 BLOCK DIAGRAM (16-BIT)**




**Note 1:** ADC event trigger is only available on Timer3.

**2:** TxCK pins are not available on 64-pin devices.

**FIGURE 14-2: TIMER2/3 AND TIMER4/5 BLOCK DIAGRAM (32-BIT)**




**Note 1:** In this diagram, the use of 'x' in registers, TxCON, TMRx, PRx and TxCK, refers to either Timer2 or Timer4; the use of 'y' in registers, TyCON, TMRy, PRy, TyIF, refers to either Timer3 or Timer5.

**2:** TxCK pins are not available on 64-pin devices.

**3:** ADC event trigger is only available on the Timer2/3 pair.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## 14.2 Control Registers

### TABLE 14-1: TIMER2 THROUGH TIMER5 REGISTER MAP

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0800 | T2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS(2) | — | 0000 |
| 0810 | TMR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR2<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0820 | PR2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR2<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0A00 | T3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS(2) | — | 0000 |
| 0A10 | TMR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR3<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0A20 | PR3 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR3<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0C00 | T4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | T32 | — | TCS(2) | — | 0000 |
| 0C10 | TMR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR4<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0C20 | PR4 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR4<15:0> | | | | | | | | | | | | | | | | FFFF |
| 0E00 | T5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | TGATE | TCKPS<2:0> | | | — | — | TCS(2) | — | 0000 |
| 0E10 | TMR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | TMR5<15:0> | | | | | | | | | | | | | | | | 0000 |
| 0E20 | PR5 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PR5<15:0> | | | | | | | | | | | | | | | | FFFF |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on 64-pin devices.

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**REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,3) | — | SIDL(4) | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
| | TGATE(3) | TCKPS<2:0>(3) | | | T32(2) | — | TCS(3) | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1,3)
- 1 = Module is enabled
- 0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(4)
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device is in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(3)

When TCS = 1:
This bit is ignored and is read as '0'.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(3)
- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only available on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.


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**REGISTER 14-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)**

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from TxCK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only available on even numbered timers (Timer2 and Timer4).

**3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, and Timer5). All timer functions are set through the even numbered timers.

**4:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

**NOTES:**


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## 15.0 WATCHDOG TIMER (WDT)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Watchdog Timer and Power-up Timer"** (DS60001114) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

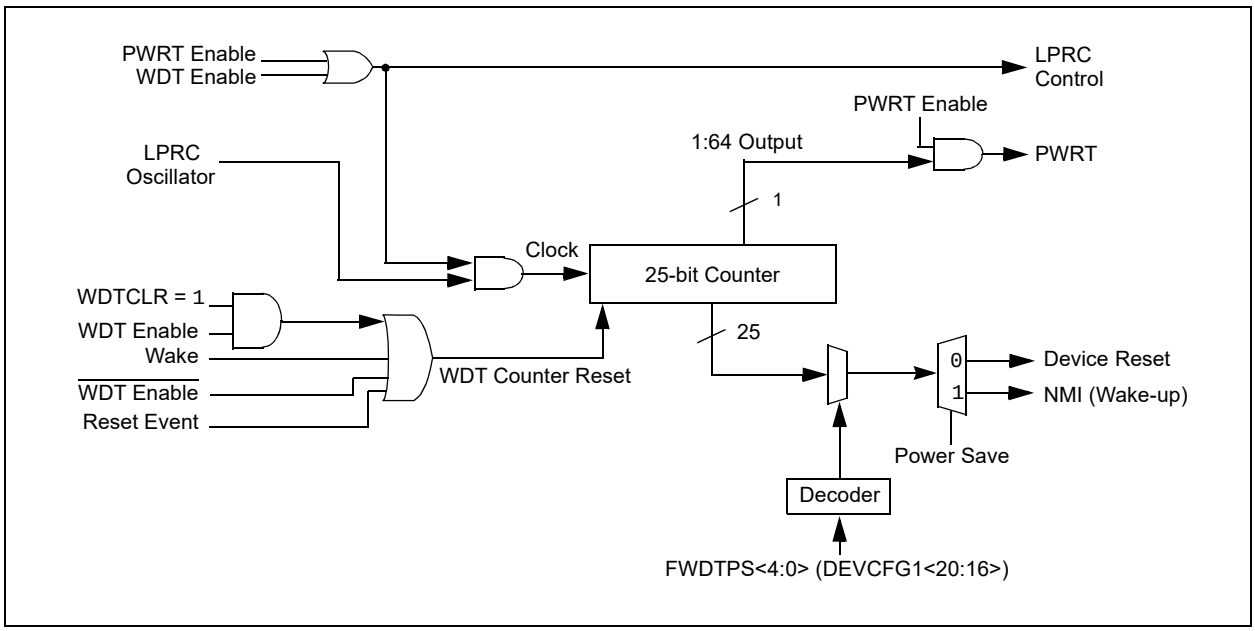
This section describes the operation of the WDT and Power-up Timer of the PIC32MX5XX/6XX/7XX.

The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are key features of the WDT module:

- Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode

**FIGURE 15-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM**



## 15.1 Control Registers

**TABLE 15-1: WATCHDOG TIMER REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0000 | WDTCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | — | — | — | — | SWDTPS<4:0> | | | | | — | WDTCLR | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of Reset.



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**REGISTER 15-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | — | — | — | — | — | — |
| 7:0 | U-0 | R-y | R-y | R-y | R-y | R-y | R/W-0 | R/W-0 |
| | — | SWDTPS<4:0> | | | | | WDTWINEN | WDTCLR |

| Legend: | y = Values set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Watchdog Timer Enable bit(1,2)
- 1 = Enables the WDT if it is not enabled by the device configuration
- 0 = Disable the WDT if it was enabled in software

bit 14-7 **Unimplemented:** Read as '0'

bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits
On reset, these bits are set to the values of the WDTPS <4:0> Configuration bits.

bit 1 **WDTWINEN:** Watchdog Timer Window Enable bit
- 1 = Enable windowed Watchdog Timer
- 0 = Disable windowed Watchdog Timer

bit 0 **WDTCLR:** Watchdog Timer Reset bit
- 1 = Writing a '1' will clear the WDT
- 0 = Software cannot force this bit to a '0'

**Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**NOTES:**


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## 16.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. "Input Capture"** (DS60001122) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

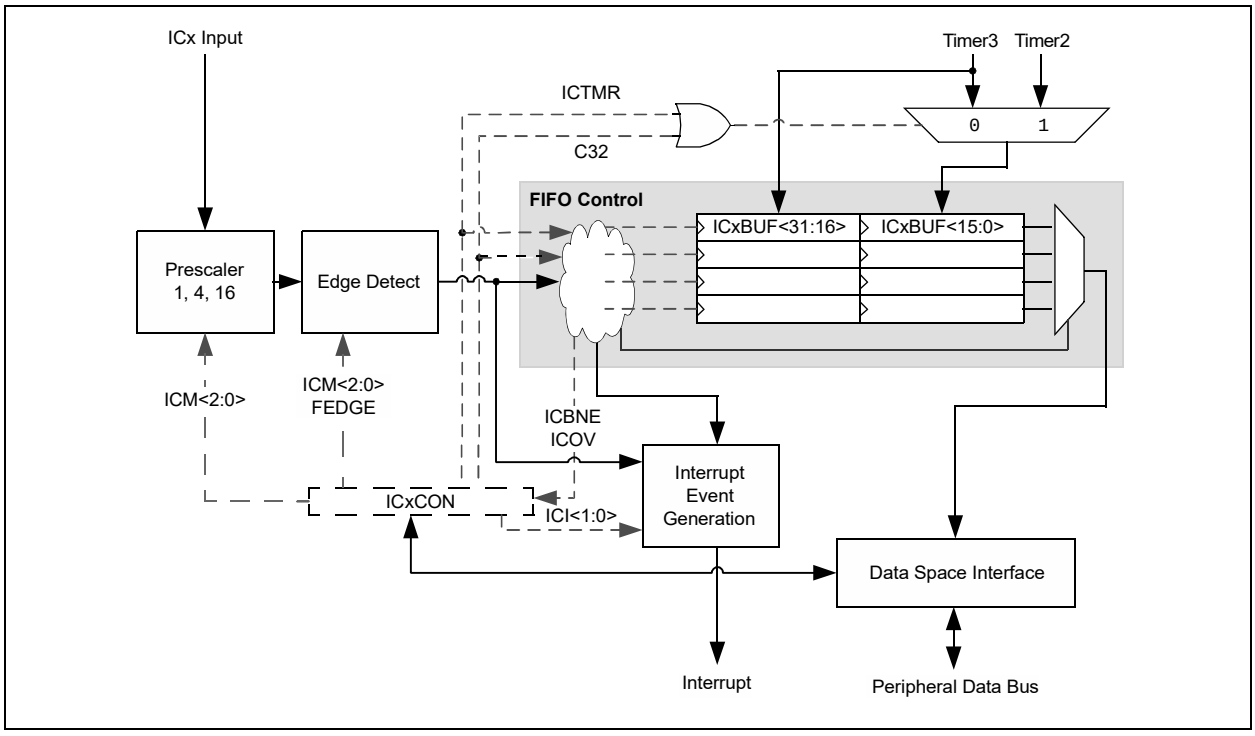
- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
- Capture timer value on every edge (rising and falling)
- Capture timer value on every edge (rising and falling), specified edge first.
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values
  Interrupt optionally generated after 1, 2, 3 or 4 buffer locations are filled
- Input Capture module can also be used to provide additional sources of external interrupts

**FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM**



## 16.1 Control Registers

**TABLE 16-1: INPUT CAPTURE 1-INPUT CAPTURE 5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | IC1CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2010 | IC1BUF | 31:16 | IC1BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2200 | IC2CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2210 | IC2BUF | 31:16 | IC2BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2400 | IC3CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2410 | IC3BUF | 31:16 | IC3BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2600 | IC4CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2610 | IC4BUF | 31:16 | IC4BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2800 | IC5CON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | FEDGE | C32 | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | | 0000 |
| 2810 | IC5BUF | 31:16 | IC5BUF<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | — | FEDGE | C32 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in Idle mode
- 0 = Continue to operate in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 1 = Timer2 is the counter source for capture
- 0 = Timer3 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow is occurred
- 0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)**

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits

111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
101 = Prescaled Capture Event mode – every sixteenth rising edge
100 = Prescaled Capture Event mode – every fourth rising edge
011 = Simple Capture Event mode – every rising edge
010 = Simple Capture Event mode – every falling edge
001 = Edge Detect mode – every edge (rising and falling)
000 = Input Capture module is disabled

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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## 17.0 OUTPUT COMPARE

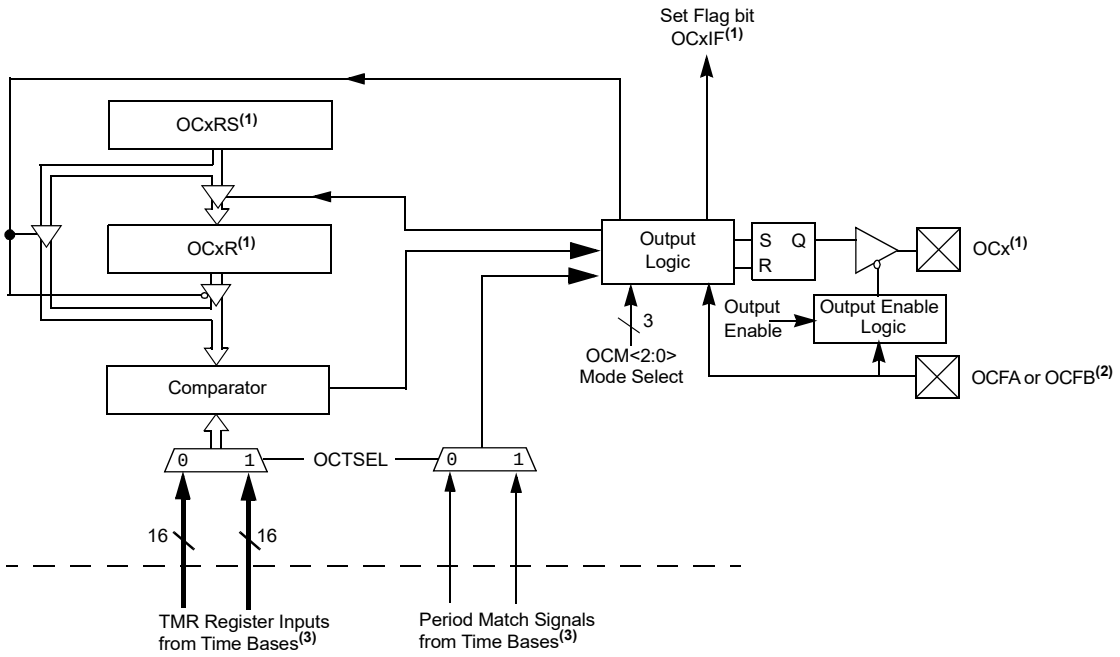
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Output Compare module is used to generate a single pulse or a series of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

**FIGURE 17-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM**




**Note 1:** Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 5.

**2:** The OCFA pin controls the OC1-OC4 channels. The OCFB pin controls the OC5 channel.

**3:** Each output compare channel can use one of two selectable 16-bit time bases or a single 32-bit timer base.

## 17.1 Control Registers

**TABLE 17-1: OUTPUT COMPARE 1-OUTPUT COMPARE 5 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3000 | OC1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3010 | OC1R | 31:16 | OC1R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3020 | OC1RS | 31:16 | OC1RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3200 | OC2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3210 | OC2R | 31:16 | OC2R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3220 | OC2RS | 31:16 | OC2RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3400 | OC3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3410 | OC3R | 31:16 | OC3R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3420 | OC3RS | 31:16 | OC3RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3600 | OC4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3610 | OC4R | 31:16 | OC4R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3620 | OC4RS | 31:16 | OC4RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3800 | OC5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | OC32 | OCFLT | OCTSEL | OCM<2:0> | | | 0000 |
| 3810 | OC5R | 31:16 | OC5R<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 3820 | OC5RS | 31:16 | OC5RS<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | OC32 | OCFLT(2) | OCTSEL | OCM<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Module On bit(1)
- 1 = Output Compare module is enabled
- 0 = Output Compare module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation when CPU is in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (only cleared in hardware)
- 0 = PWM Fault condition has not occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only used when OCM<2:0> = 111. It is read as '0' in all other modes.

**NOTES:**


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## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

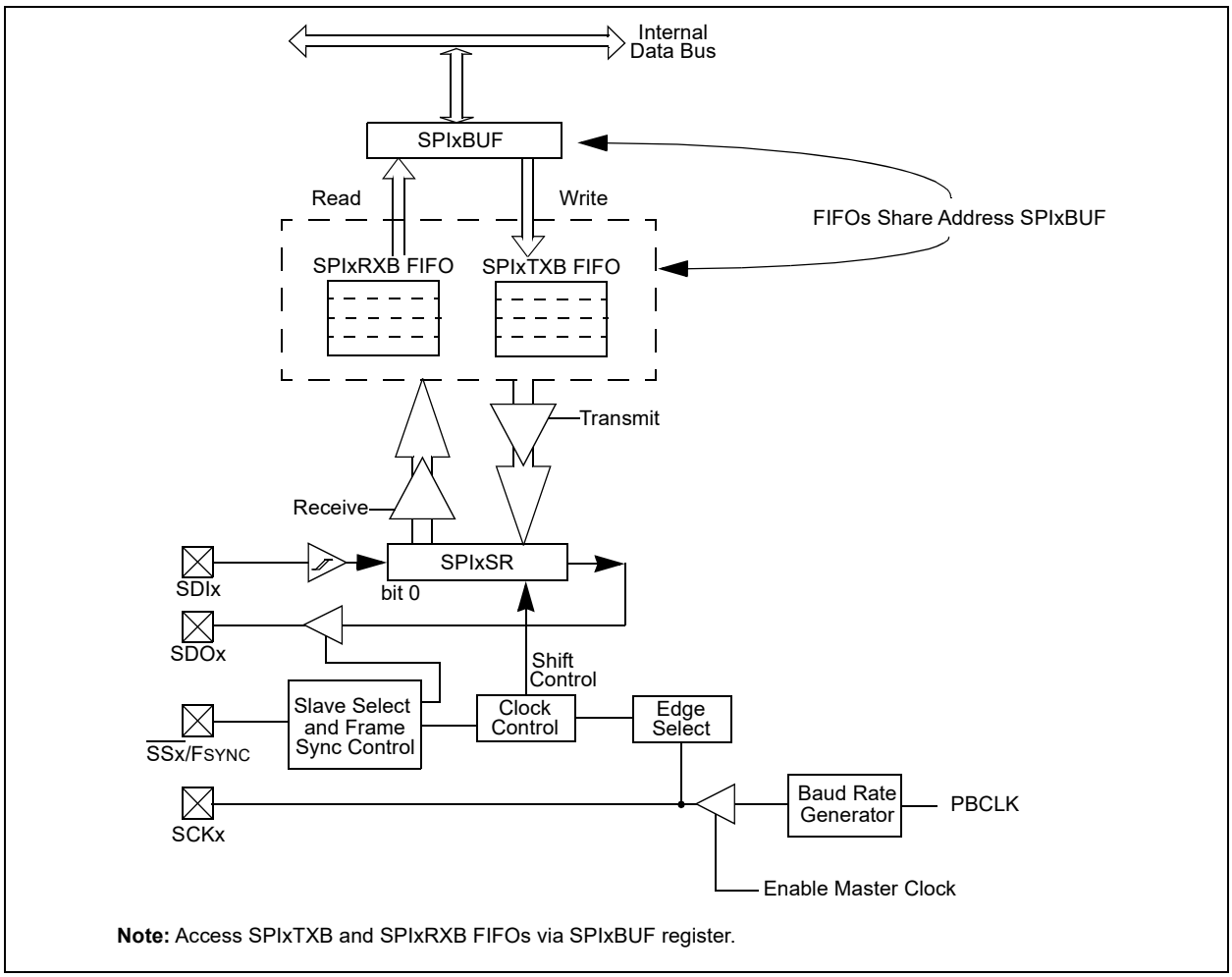
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, etc. The PIC32 SPI module is compatible with Motorola® SPI and SIOP interfaces.

The following are some of the key features of the SPI module:

- Master mode and Slave mode support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

**FIGURE 18-1: SPI MODULE BLOCK DIAGRAM**




**Note:** Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

## 18.1 Control Registers

**TABLE 18-1: SPI1 THROUGH SPI4 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5E00 | SPI1CON(2) | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | — | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5E10 | SPI1STAT(2) | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | — | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 5E20 | SPI1BUF(2) | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5E30 | SPI1BRG(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5800 | SPI3CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | — | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5810 | SPI3STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | — | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 5820 | SPI3BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5830 | SPI3BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5A00 | SPI2CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | — | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5A10 | SPI2STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | — | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 5A20 | SPI2BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5A30 | SPI2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |
| 5C00 | SPI4CON | 31:16 | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | | — | — | — | — | — | — | SPIFE | ENHBUF | 0000 |
| | | 15:0 | ON | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | | 0000 |
| 5C10 | SPI4STAT | 31:16 | — | — | — | RXBUFELM<4:0> | | | | | — | — | — | TXBUFELM<4:0> | | | | | 0000 |
| | | 15:0 | — | — | — | — | SPIBUSY | — | — | SPITUR | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF | 0008 |
| 5C20 | SPI4BUF | 31:16 | DATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 5C30 | SPI4BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | BRG<8:0> | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register is not available on 64-pin devices.



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**REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMEN | FRMSYNC | FRMPOL | MSSEN | FRMSYPW | FRMCNT<2:0> | | |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | SPIFE | ENHBUF(2) |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | DISSDO | MODE32 | MODE16 | SMP | CKE(3) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SSEN | CKP | MSTEN | — | STXISEL<1:0> | | SRXISEL<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin used as FSYNC input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ pin bit (only Framed SPI mode)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync/Slave Select Polarity bit (Framed SPI or Master Transmit modes only)
1 = Frame pulse or SSx pin is active-high
0 = Frame pulse or SSx pin is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support enabled. The $\overline{SS}$ pin is automatically driven during transmission in Master mode. Polarity is determined by the FRMPOL bit.
0 = Slave select SPI support is disabled.

bit 27 **FRMSYPW:** Frame Sync Pulse Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits. Controls the number of data characters transmitted per pulse. This bit is only valid in Framed Sync mode.
111 = Reserved
110 = Reserved
101 = Generate a frame sync pulse on every 32 data characters
100 = Generate a frame sync pulse on every 16 data characters
011 = Generate a frame sync pulse on every 8 data characters
010 = Generate a frame sync pulse on every 4 data characters
001 = Generate a frame sync pulse on every 2 data characters
000 = Generate a frame sync pulse on every data character

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (only Framed SPI mode)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit(2)
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

**REGISTER 18-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)**

bit 15 **ON:** SPI Peripheral On bit(1)
1 = SPI Peripheral is enabled
0 = SPI Peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue operation when CPU enters in Idle mode
0 = Continue operation in Idle mode

bit 12 **DISSDO:** Disable SDOx pin bit
1 = SDOx pin is not used by the module (pin is controlled by associated PORT register)
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits

| MODE32 | MODE16 | Communication |
|---|---|---|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |

bit 9 **SMP:** SPI Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

Slave mode (MSTEN = 0):
SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPI Clock Edge Select bit(3)
1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{SSx}$ pin used for Slave mode
0 = $\overline{SSx}$ pin not used for Slave mode (pin is controlled by port function)

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **Unimplemented:** Read as '0'

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit can only be written when the ON bit = 0.

**3:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).


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**REGISTER 18-2: SPIxSTAT: SPI STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | RXBUFELM<4:0> | | | | |
| 23:16 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | TXBUFELM<4:0> | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | R-0 | U-0 | U-0 | R-0 |
| | — | — | — | — | SPIBUSY | — | — | SPITUR |
| 7:0 | R-0 | R/W-0 | R-0 | U-0 | R-1 | U-0 | R-0 | R-0 |
| | SRMT | SPIROV | SPIRBE | — | SPITBE | — | SPITBF | SPIRBF |

| **Legend:** | C = Clearable bit | HS = Set in hardware | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (only valid when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (only valid when ENHBUF = 1)

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **SPIBUSY:** SPI Activity Status bit
1 = SPI peripheral is currently busy with some transactions
0 = SPI peripheral is currently idle

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPITUR:** Transmit Under Run bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (only valid when ENHBUF = 1)
1 = When SPI module shift register is empty
0 = When SPI module shift register is not empty

bit 6 **SPIROV:** Receive Overflow Flag bit
1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
0 = No overflow has occurred
This bit is set in hardware; can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (only valid when ENHBUF = 1)
1 = RX FIFO is empty (CRPTR = SWPTR)
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as '0'

bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

**REGISTER 18-2: SPIxSTAT: SPI STATUS REGISTER**

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit

1 = Transmit not yet started, SPITXB is full

0 = Transmit buffer is not full

Standard Buffer Mode:

Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.

Enhanced Buffer Mode:

Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit

1 = Receive buffer, SPIxRXB is full

0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise


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## 19.0 INTER-INTEGRATED CIRCUIT ($I^2C$)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit ($I^2C$)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

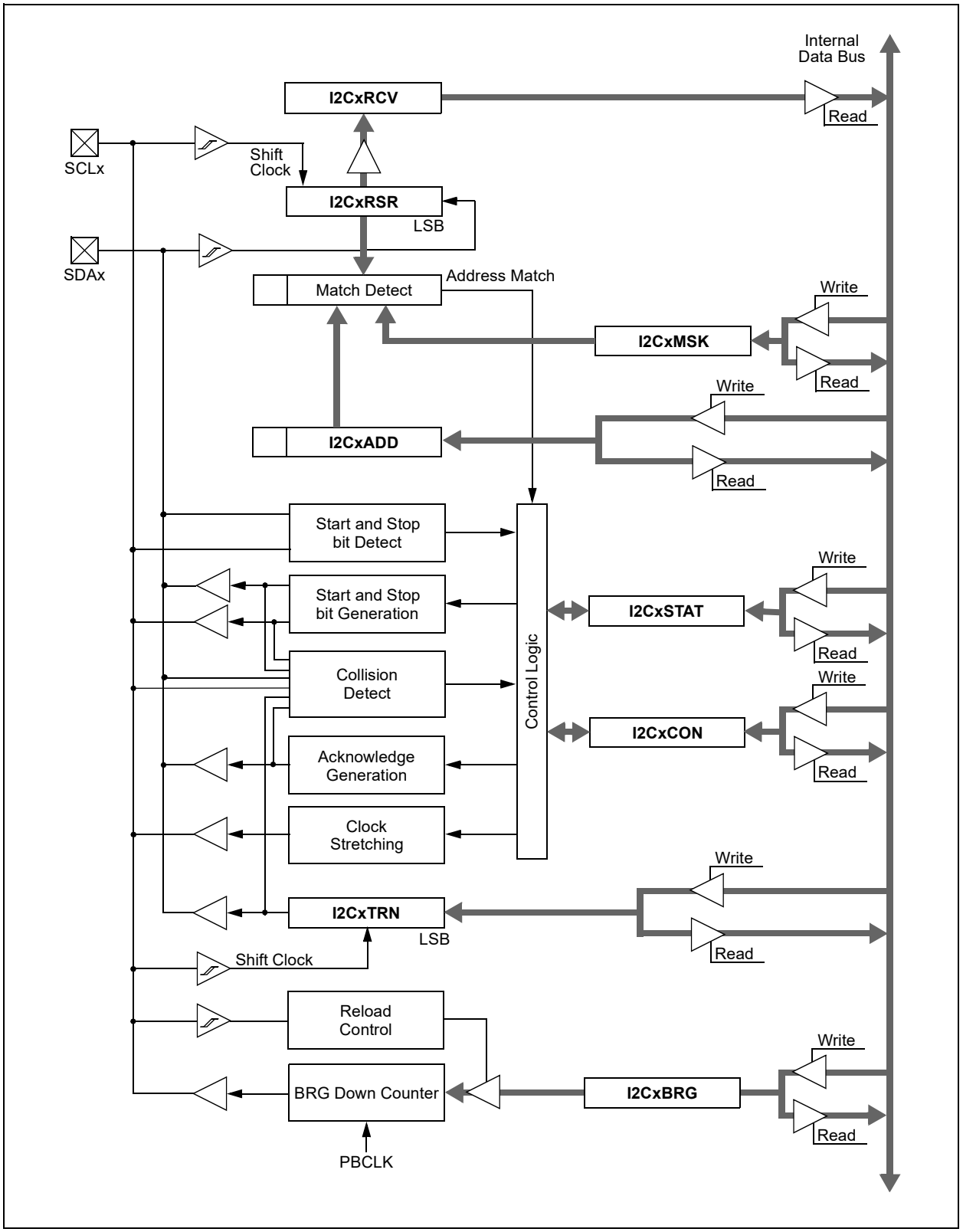
The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard. Figure 19-1 illustrates the $I^2C$ module block diagram.

Each $I^2C$ module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each $I^2C$ module offers the following key features:

- $I^2C$ interface supporting both master and slave operation
- $I^2C$ Slave mode supports 7-bit and 10-bit addressing
- $I^2C$ Master mode supports 7-bit and 10-bit addressing
- $I^2C$ port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the $I^2C$ port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- $I^2C$ supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking

**FIGURE 19-1: I²C BLOCK DIAGRAM**





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## 19.1 Control Registers

### TABLE 19-1: I2C1THROUGH I2C5 REGISTER MAP

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5000 | I2C3CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5010 | I2C3STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5020 | I2C3ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5030 | I2C3MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5040 | I2C3BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5050 | I2C3TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5060 | I2C3RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5100 | I2C4CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5110 | I2C4STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5120 | I2C4ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5130 | I2C4MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5140 | I2C4BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5150 | I2C4TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5160 | I2C4RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5200 | I2C5CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5210 | I2C5STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5220 | I2C5ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register is not available on 64-pin devices.

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## TABLE 19-1: I2C1THROUGH I2C5 REGISTER MAP (CONTINUED)

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5230 | I2C5MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5240 | I2C5BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5250 | I2C5TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5260 | I2C5RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5300 | I2C1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5310 | I2C1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5320 | I2C1ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5330 | I2C1MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5340 | I2C1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5350 | I2C1TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5360 | I2C1RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5400 | I2C2CON(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5410 | I2C2STAT(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D/A | P | S | R/W | RBF | TBF | 0000 |
| 5420 | I2C2ADD(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | ADD<9:0> | | | | | | | | | | 0000 |
| 5430 | I2C2MSK(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | MSK<9:0> | | | | | | | | | | 0000 |
| 5440 | I2C2BRG(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5450 | I2C2TRN(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5460 | I2C2RCV(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** This register is not available on 64-pin devices.



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**REGISTER 19-1: I2CxCON: I$^2$C CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-1, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC |
| | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |

| Legend: | HC = Cleared by hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** I$^2$C Enable bit(1)
- 1 = Enables the I$^2$C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I$^2$C module; all I$^2$C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation when device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I$^2$C slave)
- 1 = Release SCLx clock
- 0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (software can write '0' to initiate stretch and write '1' to release clock). Cleared by hardware at the beginning of a slave transmission and at the end of slave reception.

If STREN = 0:
Bit is R/S (software can only write '1' to release clock). Cleared by hardware at the beginning of slave transmission.

bit 11 **STRICT:** Strict I$^2$C Reserved Address Rule Enable bit
- 1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
- 0 = Strict I$^2$C reserved address rule is not enabled

bit 10 **A10M:** 10-bit Slave Address bit
- 1 = I2CxADD is a 10-bit slave address
- 0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
- 1 = Slew rate control is disabled
- 0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
- 1 = Enable I/O pin thresholds compliant with SMBus specification
- 0 = Disable SMBus input thresholds

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 19-1: I2CxCON: I$^2$C CONTROL REGISTER (CONTINUED)**

bit 7 **GCEN:** General Call Enable bit (when operating as I$^2$C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I$^2$C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I$^2$C master, applicable during master receive)
Value that is transmitted when the software initiates an acknowledge sequence.
1 = Send NACK during an acknowledge
0 = Send ACK during an acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (when operating as I$^2$C master, applicable during master receive)
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I$^2$C master)
1 = Enables Receive mode for I$^2$C. Hardware clear at end of eighth bit of master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I$^2$C master)
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
0 = Start condition is not in progress

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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**REGISTER 19-2: I2CxSTAT: I$^2$C STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| 7:0 | R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |

| **Legend:** | HS = Set by hardware | HSC = Hardware set/cleared | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | C = Clearable bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I$^2$C master, applicable to master transmit operation)
This bit is set or cleared by hardware at the end of a slave Acknowledge.
1 = NACK received from slave
0 = ACK received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I$^2$C master, applicable to master transmit operation)
This bit is set by hardware at the beginning of a master transmission, and is cleared by hardware at the end of a slave Acknowledge.
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
This bit is set by hardware at the detection of a bus collision.
1 = A bus collision has been detected during a master operation
0 = No collision

bit 9 **GCSTAT:** General Call Status bit
This bit is set by hardware when the address matches the general call address, and is cleared by hardware clear at a Stop detection.
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-bit Address Status bit
This bit is set by hardware upon a match of the 2nd byte of the matched 10-bit address, and is cleared by hardware at a Stop detection.
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** Write Collision Detect bit
This bit is set by hardware at the occurrence of a write to I2CxTRN while busy (cleared by software).
1 = An attempt to write the I2CxTRN register failed because the I$^2$C module is busy
0 = No collision

bit 6 **I2COV:** Receive Overflow Flag bit
This bit is set by hardware at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow

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**REGISTER 19-2: I2CxSTAT: $I^2C$ STATUS REGISTER (CONTINUED)**

bit 5 **D_A:** Data/Address bit (when operating as $I^2C$ slave)
This bit is cleared by hardware upon a device address match, and is set by hardware by reception of the slave byte.
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address

bit 4 **P:** Stop bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

bit 3 **S:** Start bit
This bit is set or cleared by hardware when a Start, Repeated Start, or Stop condition is detected.
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)
This bit is set or cleared by hardware after reception of an $I^2C$ device address byte.
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave

bit 1 **RBF:** Receive Buffer Full Status bit
This bit is set by hardware when the I2CxRCV register is written with a received byte, and is cleared by hardware when software reads I2CxRCV.
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty

bit 0 **TBF:** Transmit Buffer Full Status bit
This bit is set by hardware when software writes to the I2CxTRN register, and is cleared by hardware upon completion of data transmission.
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty


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## 20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

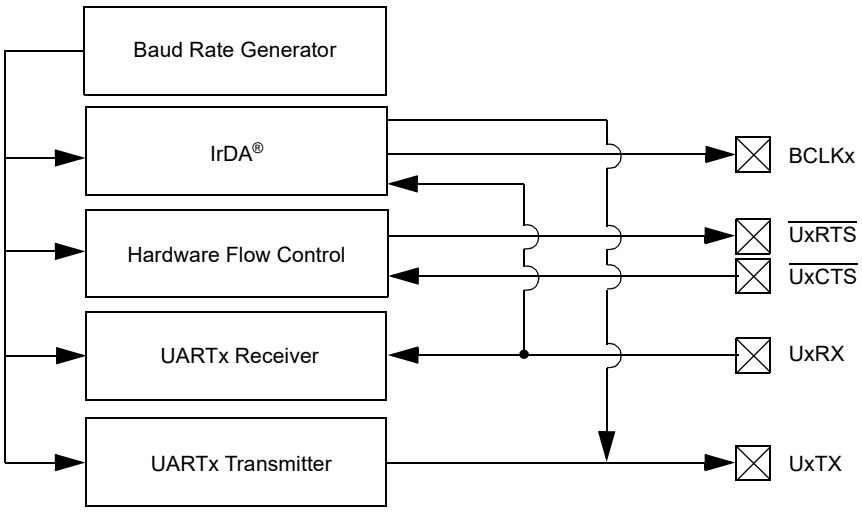
The UART module is one of the serial I/O modules available in the PIC32MX5XX/6XX/7XX family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN 1.2 and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The following are primary features of the UART module:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 20 Mbps at 80 MHz
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (ninth bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN 2.1 Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 20-1 illustrates a simplified block diagram of the UART module.

**FIGURE 20-1: UART SIMPLIFIED BLOCK DIAGRAM**




**Note:** Not all pins are available for all UART modules. Refer to the device-specific pin diagram for more information (see **"Device Pin Tables"**).

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 20-2: UART RECEPTION**

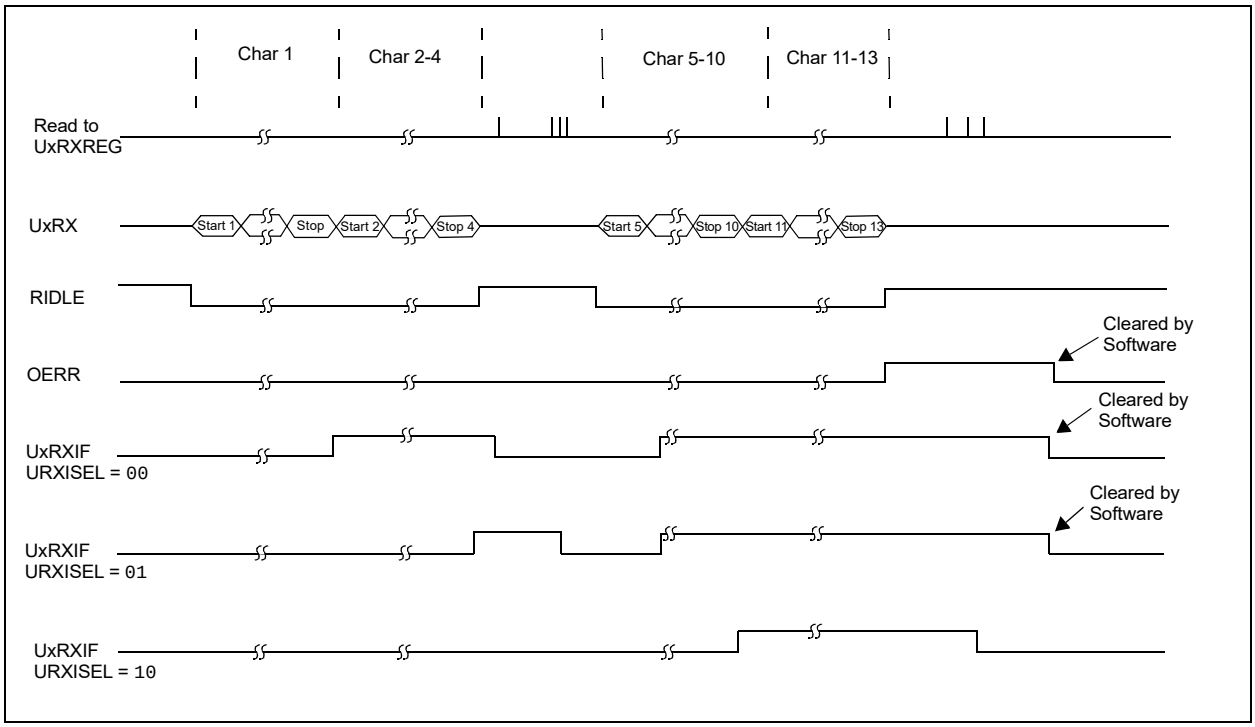
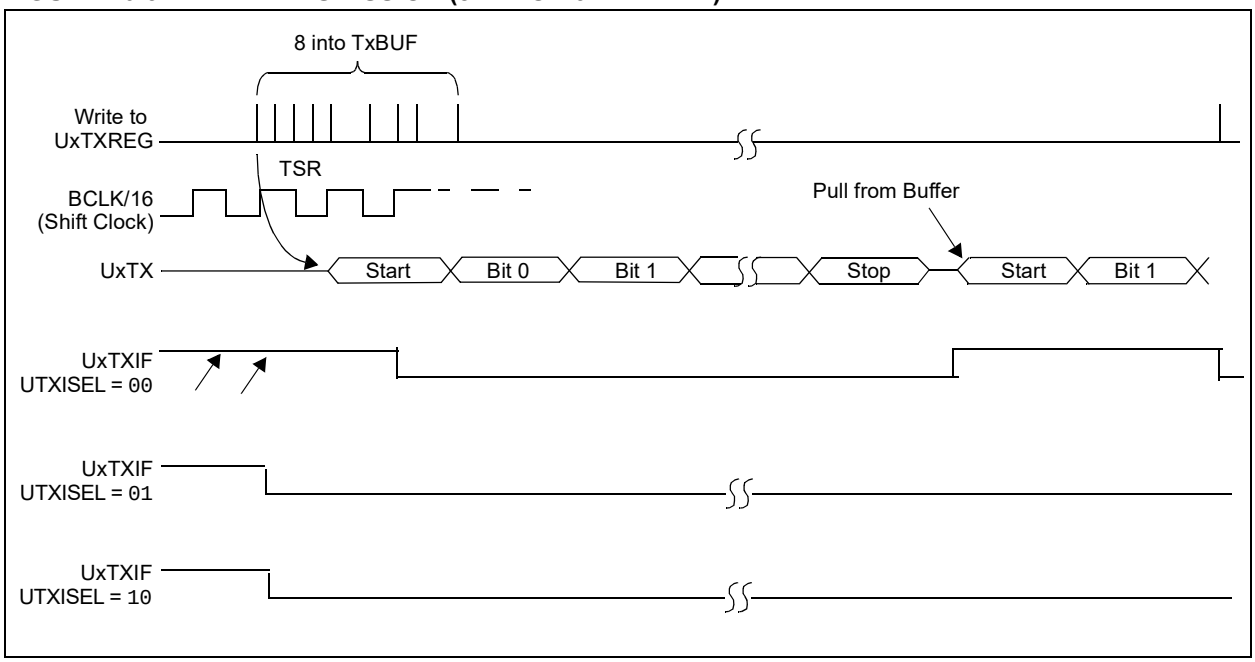



**FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**





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## 20.1 Control Registers

### TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6000 | U1MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6010 | U1STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6020 | U1TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6030 | U1RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6040 | U1BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6200 | U4MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | — | — | — | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6210 | U4STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6220 | U4TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6230 | U4RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6240 | U4BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6400 | U3MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6410 | U3STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6420 | U3TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6430 | U3RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6440 | U3BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6600 | U6MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | — | — | — | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6610 | U6STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 20-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6620 | U6TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6630 | U6RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6640 | U6BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6800 | U2MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | RTSMD | — | UEN<1:0> | | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6810 | U2STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6820 | U2TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6830 | U2RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6840 | U2BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |
| 6A00 | U5MODE(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | IREN | — | — | — | — | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL | 0000 |
| 6A10 | U5STA(1) | 31:16 | — | — | — | — | — | — | — | ADM_EN | ADDR<7:0> | | | | | | | | 0000 |
| | | 15:0 | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| 6A20 | U5TXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | TX8 | Transmit Register | | | | | | | | 0000 |
| 6A30 | U5RXREG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | RX8 | Receive Register | | | | | | | | 0000 |
| 6A40 | U5BRG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BRG<15:0> | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | IREN | RTSMD | — | UEN<1:0> | |
| 7:0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAKE | LPBACK | ABAUD | RXINV | BRGH | PDSEL<1:0> | | STSEL |

| Legend: | | HC = Cleared by hardware | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** UARTx Enable bit(1)
- 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by UEN<1:0> and UTXEN control bits.
- 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation when device enters Idle mode

bit 12 **IREN:** IrDA Encoder and Decoder Enable bit
- 1 = IrDA is enabled
- 0 = IrDA is disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits
- 11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
- 1 = Wake-up is enabled
- 0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.


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**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | — | — | — | ADM_EN |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
| | UTXISEL<1:0> | | UTXINV | URXEN | UTXBRK | UTXEN | UTXBF | TRMT |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/W-0, HS | R-0 |
| | URXISEL<1:0> | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |

| **Legend:** | HS = Set by hardware | HC = Cleared by hardware | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ADM_EN:** Automatic Address Detect Mode Enable bit
- 1 = Automatic Address Detect mode is enabled
- 0 = Automatic Address Detect mode is disabled

bit 23-16 **ADDR<7:0>:** Automatic Address Mask bits

When the ADM_EN bit is '1', this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** TX Interrupt Mode Selection bits
- 11 = Reserved, do not use
- 10 = Interrupt is generated and asserted while the transmit buffer is empty
- 01 = Interrupt is generated and asserted when all characters have been transmitted
- 00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** Transmit Polarity Inversion bit

If IrDA mode is disabled (i.e., IREN (UxMODE<12>) is '0'):
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IrDA mode is enabled (i.e., IREN (UxMODE<12>) is '1'):
- 1 = IrDA encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **URXEN:** Receiver Enable bit
- 1 = UARTx receiver is enabled. UxRX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx receiver is disabled. UxRX pin is ignored by the UARTx module. UxRX pin is controlled by port.

bit 11 **UTXBRK:** Transmit Break bit
- 1 = Send Break on next transmission. Start bit followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion.
- 0 = Break transmission is disabled or completed

bit 10 **UTXEN:** Transmit Enable bit
- 1 = UARTx transmitter is enabled. UxTX pin is controlled by UARTx (if ON = 1)
- 0 = UARTx transmitter is disabled. Any pending transmission is aborted and buffer is reset. UxTX pin is controlled by port.

bit 9 **UTXBF:** Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 8 **TRMT:** Transmit Shift Register is Empty bit (read-only)
1 = Transmit shift register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit shift register is not empty, a transmission is in progress or queued in the transmit buffer

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty


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## 21.0 PARALLEL MASTER PORT (PMP)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 13. "Parallel Master Port (PMP)"** (DS60001128) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

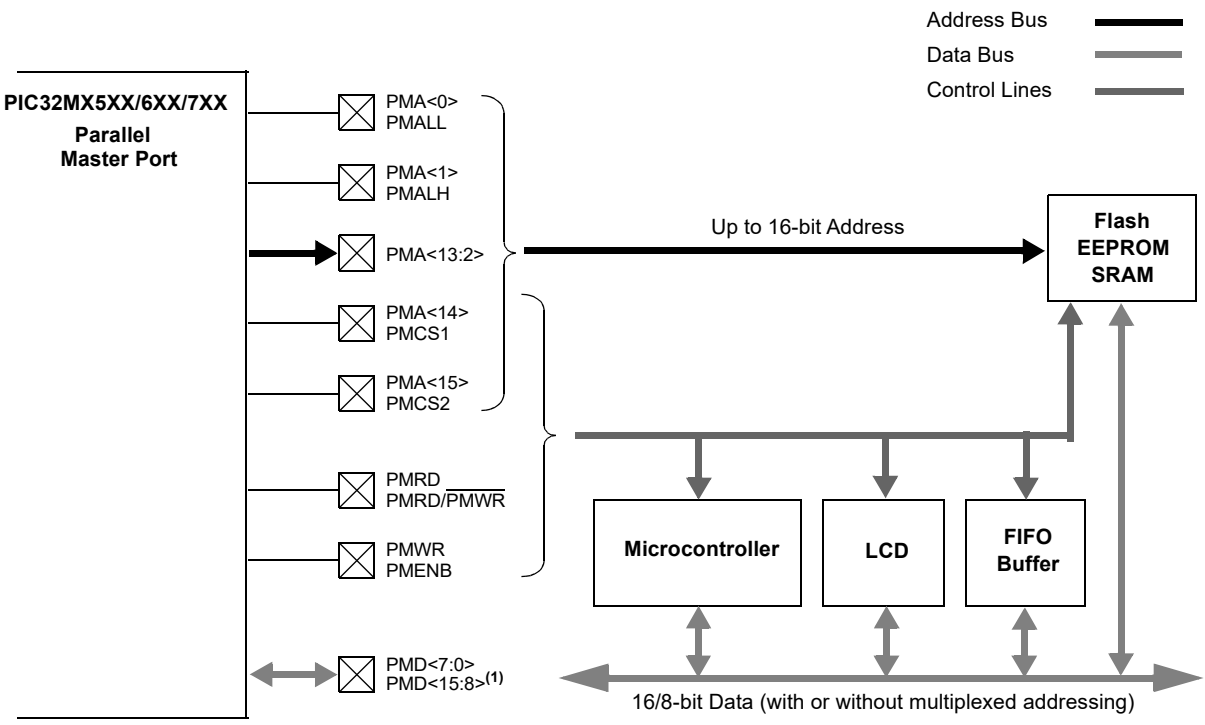
The PMP is a parallel 8-bit/16-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. Figure 21-1 shows the PMP module pinout and its connections to external devices.

The following are key features of the PMP module:

- 8-bit and 16-bit interface
- Up to 16 programmable address lines
- Up to two Chip Select lines
- Programmable strobe options
  - Individual read and write strobes, or
  - Read/$\overline{\text{Write}}$ strobe with enable strobe
- Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- Parallel Slave Port support
  - Legacy addressable
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable wait states
- Operates during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

**Note:** On 64-pin devices, the PMD<15:8> data pins are not available.

**FIGURE 21-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES**




**Note 1:** On 64-pin devices, data pins, PMD<15:8>, are not available in 16-bit Master modes.

## 21.1 Control Registers

**TABLE 21-1: PARALLEL MASTER PORT REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 7000 | PMCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | ADRMUX<1:0> | | PMPTTL | PTWREN | PTRDEN | CSF<1:0> | | ALP | CS2P | CS1P | — | WRSP | RDSP | 0000 |
| 7010 | PMMODE | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | | WAITB<1:0> | | WAITM<3:0> | | | | WAITE<1:0> | | 0000 |
| 7020 | PMADDR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CS2EN/A15 | CS1EN/A14 | ADDR<13:0> | | | | | | | | | | | | | | 0000 |
| 7030 | PMDOUT | 31:16 | DATAOUT<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 7040 | PMDIN | 31:16 | DATAIN<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 7050 | PMAEN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PTEN<15:0> | | | | | | | | | | | | | | | | 0000 |
| 7060 | PMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E | 008F |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | ADRMUX<1:0> | | PMPTTL | PTWREN | PTRDEN |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | CSF<1:0>(2) | | ALP(2) | — | CS1P(2) | — | WRSP | RDSP |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit(1)
- 1 = PMP is enabled
- 0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation when device enters Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
- 11 = All 16 bits of address are multiplexed on PMD<15:0> pins
- 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
- 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
- 00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
- 1 = PMP module uses TTL input buffers
- 0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
- 1 = PMWR/PMENB port is enabled
- 0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
- 1 = PMRD/PMWR port is enabled
- 0 = PMRD/PMWR port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits(2)
- 11 = Reserved
- 10 = PMCS2 and PMCS1 function as Chip Select
- 01 = PMCS2 functions as Chip Select, PMCS1 functions as address bit 14
- 00 = PMCS2 and PMCS1 function as address bits 15 and 14(2)

bit 5 **ALP:** Address Latch Polarity bit(2)
- 1 = Active-high (PMALL and PMALH)
- 0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **Unimplemented:** Read as '0'

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.

**REGISTER 21-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)**

bit 3 **CS1P:** Chip Select 0 Polarity bit(2)
1 = Active-high (PMCS1)
0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit
For Slave Modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Write strobe active-high (PMWR)
0 = Write strobe active-low ($\overline{\text{PMWR}}$)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Enable strobe active-high (PMENB)
0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit
For Slave modes and Master mode 2 (PMMODE<9:8> = 00,01,10):
1 = Read Strobe active-high (PMRD)
0 = Read Strobe active-low ($\overline{\text{PMRD}}$)
For Master mode 1 (PMMODE<9:8> = 11):
1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

**2:** These bits have no effect when their corresponding pins are used as address lines.


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**REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUSY | IRQM<1:0> | | INCM<1:0> | | MODE16 | MODE<1:0> | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | WAITB<1:0>(1) | | WAITM<3:0>(1) | | | | WAITE<1:0>(1) | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (only Master mode)
- 1 = Port is busy
- 0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits (4)
- 11 = Reserved
- 10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> =11 (only Addressable Slave mode)
- 01 = Interrupt generated at the end of the read/write cycle
- 00 = Interrupt is not generated

bit 12-11 **INCM<1:0>:** Increment Mode bits
- 11 = Slave mode read and write buffers auto-increment (only PMMODE<1:0> = 00)
- 10 = Decrement ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 01 = Increment ADDR<10:2> and ADDR<14> by 1 every read/write cycle(2)
- 00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit
- 1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer
- 0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits
- 11 = Master mode 1 PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>(3))
- 01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS1, PMD<7:0>, and PMA<1:0>)
- 00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS1, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits(1)
- 11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB
- 10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB
- 01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB
- 00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, the WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bit A14 is not subject to auto-increment or auto-decrement if configured as Chip Select CS1.

**3:** These pins are active when MODE16 = 1 (16-bit mode).

**4:** These bits only control generating the Parallel Master Port (PMP) interrupt. The Parallel Master Port Error (PMPE) is always generated.

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**REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER (CONTINUED)**

bit 5-2 **WAITM<3:0>:** Data Read/Write Strobe Wait States bits(1)

1111 = Wait of 16 TPB
•
•
•
0001 = Wait of 2 TPB
0000 = Wait of 1 TPB (default)

bit 1-0 **WAITE<1:0>:** Data Hold After Read/Write Strobe Wait States bits(1)

11 = Wait of 4 TPB
10 = Wait of 3 TPB
01 = Wait of 2 TPB
00 = Wait of 1 TPB (default)

For Read operations:
11 = Wait of 3 TPB
10 = Wait of 2 TPB
01 = Wait of 1 TPB
00 = Wait of 0 TPB (default)

**Note 1:** Whenever WAITM<3:0> = 0000, the WAITB and WAITE bits are ignored and forced to 1 TPBCLK cycle for a write operation; WAITB = 1 TPBCLK cycle, WAITE = 0 TPBCLK cycles for a read operation.

**2:** Address bit A14 is not subject to auto-increment or auto-decrement if configured as Chip Select CS1.

**3:** These pins are active when MODE16 = 1 (16-bit mode).

**4:** These bits only control generating the Parallel Master Port (PMP) interrupt. The Parallel Master Port Error (PMPE) is always generated.


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**REGISTER 21-3: PMADDR: PARALLEL PORT ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CS2(1) | CS1(3) | ADDR<13:8> | | | | | |
| | ADDR15(2) | ADDR14(4) | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Destination Address bit 15(2)

bit 14 **CS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Destination Address bit 14(4)

bit 13-0 **ADDR<13:0>:** Address bits

**Note 1:** When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
**2:** When the CSF<1:0> bits (PMCON<7:6>) = 00.
**3:** When the CSF<1:0> bits (PMCON<7:6>) = 10.
**4:** When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

**REGISTER 21-4: PMAEN: PARALLEL PORT PIN ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<15:14>(1) | | — | — | — | PTEN<10:8> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTEN<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-14 **PTEN<15:14>:** PMCSx Address Port Enable bits
- 1 = PMA15 and PMA14 function as either PMA<15:14> or PMCS2 and PMCS1(1)
- 0 = PMA15 and PMA14 function as port I/O

bit 13-11 **Unimplemented:** Read as '0'

bit 10-2 **PTEN<10:2>:** PMP Address Port Enable bits
- 1 = PMA<10:2> function as PMP address lines
- 0 = PMA<10:2> function as port I/O

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
- 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL(2)
- 0 = PMA1 and PMA0 pads function as port I/O

**Note 1:** The use of these pins as PMA15/PMA14 or CS2/CS1 is selected by the CSF<1:0> bits (PMCON<7:6>).

**2:** The use of these pins as PMA1/PMA0 or PMALH/PMALL depends on the Address/Data Multiplex mode selected by bits ADRMUX<1:0> in the PMCON register.


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**REGISTER 21-5: PMSTAT: PARALLEL PORT STATUS REGISTER (ONLY SLAVE MODES)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R-0 | R/W-0, HS, SC | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
| | IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F |
| 7:0 | R-1 | R/W-0, HS, SC | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
| | OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E |

| **Legend:** | HS = Set by Hardware | SC = Cleared by software | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit
- 1 = All writable input buffer registers are full
- 0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
- 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)**(1)**
- 0 = An overflow has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits
- 1 = Input buffer contains data that has not been read (reading buffer will clear this bit)
- 0 = Input buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
- 1 = All readable output buffer registers are empty
- 0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
- 1 = A read occurred from an empty output byte buffer (must be cleared in software)**(1)**
- 0 = An underflow has not occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
- 1 = Output buffer is empty (writing data to the buffer will clear this bit)
- 0 = Output buffer contains data that has not been transmitted

**Note 1:** This will generate a PMPE – Parallel Master Port Error interrupt.

**NOTES:**


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## 22.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

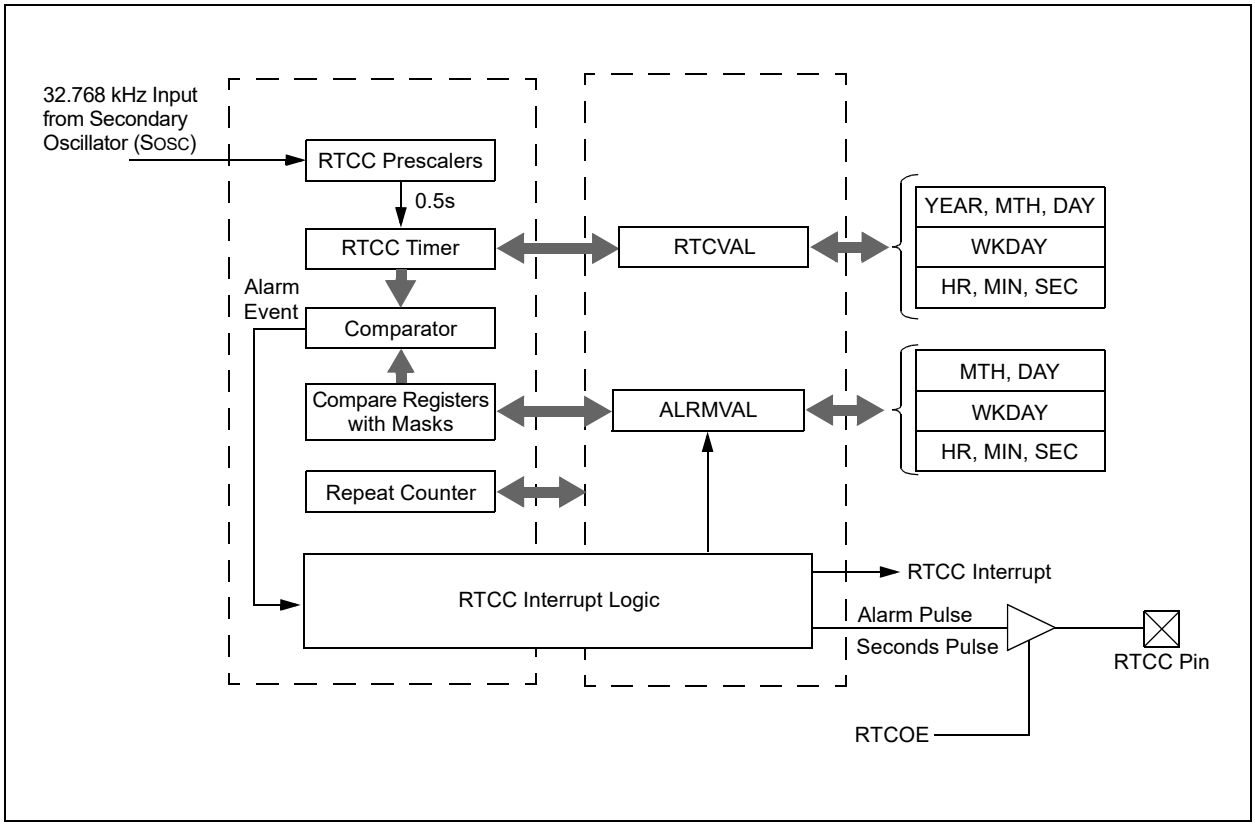
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time. A simplified block diagram of the RTCC module is illustrated in Figure 22-1.

Key features of the RTCC module include:

- Time: hours, minutes and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin

**FIGURE 22-1: RTCC BLOCK DIAGRAM**



## 22.1 Control Registers

**TABLE 22-1: RTCC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 0200 | RTCCON | 31:16 | — | — | — | — | — | — | CAL<9:0> | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | RTSECSEL | RTCCLKON | — | — | RTCWREN | RTCSYNC | HALFSEC | RTCOE | 0000 |
| 0210 | RTCALRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ALRMEN | CHIME | PIV | ALRMSYNC | AMASK<3:0> | | | | ARPT<7:0> | | | | | | | | 0000 |
| 0220 | RTCTIME | 31:16 | HR10<3:0> | | | | HR01<3:0> | | | | MIN10<3:0> | | | | MIN01<3:0> | | | | xxxx |
| | | 15:0 | SEC10<3:0> | | | | SEC01<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0230 | RTCDATE | 31:16 | YEAR10<3:0> | | | | YEAR01<3:0> | | | | MONTH10<3:0> | | | | MONTH01<3:0> | | | | xxxx |
| | | 15:0 | DAY10<3:0> | | | | DAY01<3:0> | | | | — | — | — | — | WDAY01<3:0> | | | | xx00 |
| 0240 | ALRMTIME | 31:16 | HR10<3:0> | | | | HR01<3:0> | | | | MIN10<3:0> | | | | MIN01<3:0> | | | | xxxx |
| | | 15:0 | SEC10<3:0> | | | | SEC01<3:0> | | | | — | — | — | — | — | — | — | — | xx00 |
| 0250 | ALRMDATE | 31:16 | — | — | — | — | — | — | — | — | MONTH10<3:0> | | | | MONTH01<3:0> | | | | 00xx |
| | | 15:0 | DAY10<3:0> | | | | DAY01<3:0> | | | | — | — | — | — | WDAY01<3:0> | | | | xx0x |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 22-1: RTCCON: RTC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | CAL<9:8> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CAL<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | SIDL | — | — | — | — | — |
| 7:0 | R/W-0 | R-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 |
| | RTSECSEL(3) | RTCCLKON | — | — | RTCWREN(4) | RTCSYNC | HALFSEC(5) | RTCOE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** RTC Drift Calibration bits, which contain a signed 10-bit integer value

1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute
0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute
0000000000 = No adjustment

bit 15 **ON:** RTCC On bit(1,2)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables the PBCLK to the RTCC when CPU enters in Idle mode
0 = Continue normal operation in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **RTSECSEL:** RTCC Seconds Clock Output Select bit(3)

1 = RTCC Seconds Clock is selected for the RTCC pin
0 = RTCC Alarm Pulse is selected for the RTCC pin

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can only be set when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

**Note:** This register is only reset on a Power-on Reset (POR).

**REGISTER 22-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)**

bit 3 **RTCWREN:** RTC Value Registers Write Enable bit(4)
- 1 = RTC Value registers can be written to by the user
- 0 = RTC Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
- 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read. If the register is read twice and results in the same data, the data can be assumed to be valid.
- 0 = RTC Value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(5)
- 1 = Second half period of a second
- 0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit
- 1 = RTCC clock output is enabled (clock presented onto an I/O)
- 0 = RTCC clock output is disabled

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can only be set when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

| **Note:** | This register is only reset on a Power-on Reset (POR). |
|---|---|


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**REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALRMEN(1,2) | CHIME(2) | PIV(2) | ALRMSYNC(3) | AMASK<3:0>(2) | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ARPT<7:0>(2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(3)
When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit(3)
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 1111 = Reserved
- •
- •
- •
- 1010 = Reserved
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1000 = Once a month
- 0111 = Once a week
- 0110 = Once a day
- 0101 = Every hour
- 0100 = Every 10 minutes
- 0011 = Every minute
- 0010 = Every 10 seconds
- 0001 = Every second
- 0000 = Every half-second

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

**Note:** This register is only reset on a Power-on Reset (POR).

**REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)**

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times
•
•
•
00000000 = Alarm will trigger one time
The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

**Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

**2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

**3:** This assumes a CPU read will execute in less than 32 PBCLKs.

| **Note:** | This register is only reset on a Power-on Reset (POR). |
|---|---|


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**REGISTER 22-3: RTCTIME: RTC TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

**REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | YEAR10<3:0> | | | | YEAR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MONTH10<3:0> | | | | MONTH01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | DAY10<3:0> | | | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | WDAY01<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **YEAR10<3:0>:** Binary-Coded Decimal Value of Years bits, 10 digits

bit 27-24 **YEAR01<3:0>:** Binary-Coded Decimal Value of Years bits, 1 digit

bit 23-20 **MONTH10<3:0>:** Binary-Coded Decimal Value of Months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary-Coded Decimal Value of Months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary-Coded Decimal Value of Days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary-Coded Decimal Value of Days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary-Coded Decimal Value of Weekdays bits,1 digit; contains a value from 0 to 6

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).


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**REGISTER 22-5: ALRMTIME: ALARM TIME VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | HR10<3:0> | | | | HR01<3:0> | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MIN10<3:0> | | | | MIN01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SEC10<3:0> | | | | SEC01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **HR10<3:0>:** Binary Coded Decimal value of hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>:** Binary Coded Decimal value of minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>:** Binary Coded Decimal value of seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 22-6: ALRMDATE: ALARM DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | MONTH10<3:0> | | | | MONTH01<3:0> | | | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | DAY10<1:0> | | | | DAY01<3:0> | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
| | — | — | — | — | WDAY01<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6


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## 23.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 16 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold (S&H) circuit
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

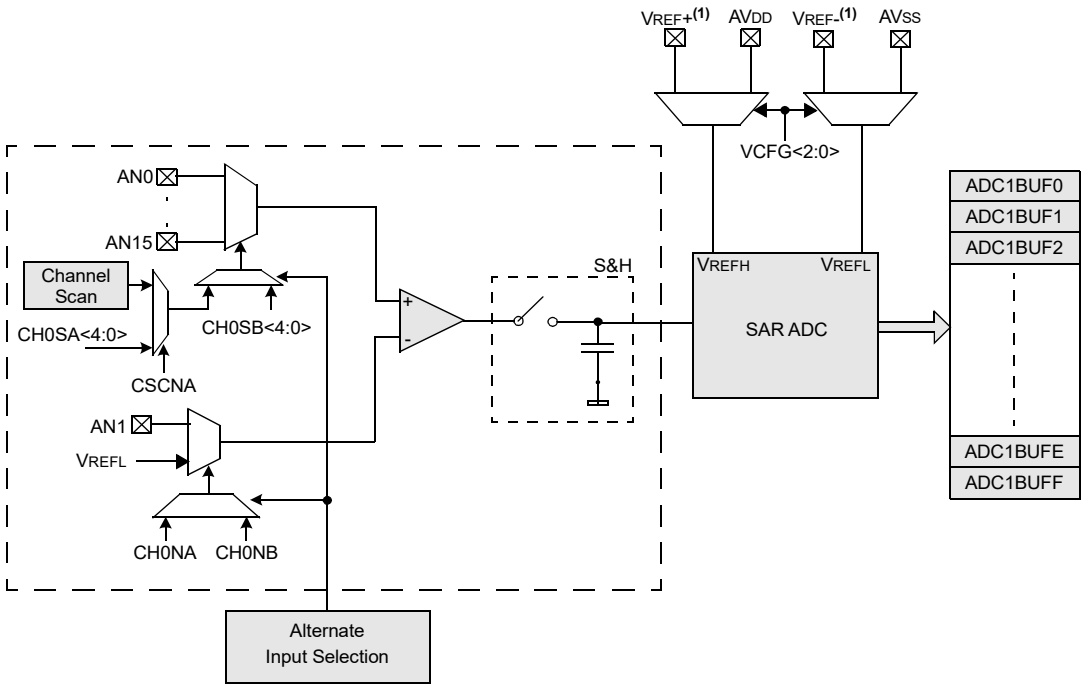
A block diagram of the 10-bit ADC is illustrated in Figure 23-1. The 10-bit ADC has up to 16 analog input pins, designated AN0-AN15. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

The analog inputs are connected through two multiplexers to one S&H. The analog input multiplexers can be switched between two sets of analog inputs between conversions. Unipolar differential conversions are possible on all channels, other than the pin used as the reference, using a reference input pin (see Figure 23-1).

The Analog Input Scan mode sequentially converts user-specified channels. A control register specifies which analog input channels will be included in the scanning sequence.

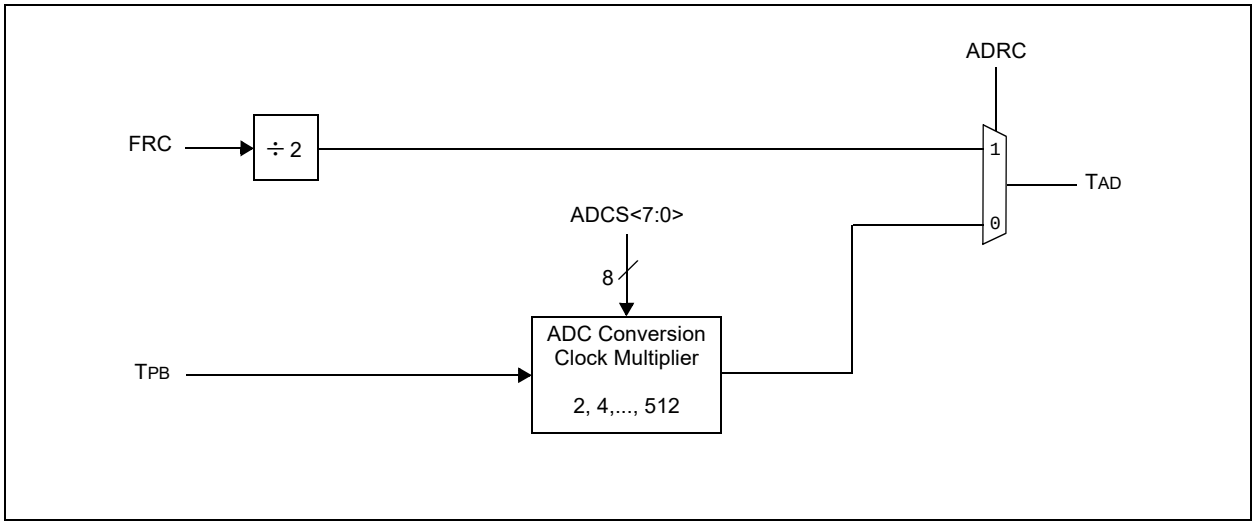
The 10-bit ADC is connected to a 16-word result buffer. Each 10-bit result is converted to one of eight 32-bit output formats when it is read from the result buffer.

**FIGURE 23-1: ADC1 MODULE BLOCK DIAGRAM**




**Note 1:** VREF+ and VREF- inputs can be multiplexed with other analog inputs.

**FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM**





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## 23.1 Control Registers

**TABLE 23-1: ADC REGISTER MAP**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9000 | AD1CON1(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | FORM<2:0> | | | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP | DONE | 0000 |
| 9010 | AD1CON2(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | VCFG2 | VCFG1 | VCFG0 | OFFCAL | — | CSCNA | — | — | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS | 0000 |
| 9020 | AD1CON3(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ADRC | — | — | SAMC<4:0> | | | | | ADCS<7:0> | | | | | | | | 0000 |
| 9040 | AD1CHS(1) | 31:16 | CH0NB | — | — | — | CH0SB<3:0> | | | | CH0NA | — | — | — | CH0SA<3:0> | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 9060 | AD1PCFG(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PCFG15 | PCFG14 | PCFG13 | PCFG12 | PCFG11 | PCFG10 | PCFG9 | PCFG8 | PCFG7 | PCFG6 | PCFG5 | PCFG4 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | 0000 |
| 9050 | AD1CSSL(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CSSL15 | CSSL14 | CSSL13 | CSSL12 | CSSL11 | CSSL10 | CSSL9 | CSSL8 | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 | 0000 |
| 9070 | ADC1BUF0 | 31:16 | ADC Result Word 0 (ADC1BUF0<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9080 | ADC1BUF1 | 31:16 | ADC Result Word 1 (ADC1BUF1<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9090 | ADC1BUF2 | 31:16 | ADC Result Word 2 (ADC1BUF2<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90A0 | ADC1BUF3 | 31:16 | ADC Result Word 3 (ADC1BUF3<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90B0 | ADC1BUF4 | 31:16 | ADC Result Word 4 (ADC1BUF4<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90C0 | ADC1BUF5 | 31:16 | ADC Result Word 5 (ADC1BUF5<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90D0 | ADC1BUF6 | 31:16 | ADC Result Word 6 (ADC1BUF6<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90E0 | ADC1BUF7 | 31:16 | ADC Result Word 7 (ADC1BUF7<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 90F0 | ADC1BUF8 | 31:16 | ADC Result Word 8 (ADC1BUF8<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9100 | ADC1BUF9 | 31:16 | ADC Result Word 9 (ADC1BUF9<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9110 | ADC1BUFA | 31:16 | ADC Result Word A (ADC1BUFA<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 23-1: ADC REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9120 | ADC1BUFB | 31:16 | ADC Result Word B (ADC1BUFB<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9130 | ADC1BUFC | 31:16 | ADC Result Word C (ADC1BUFC<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9140 | ADC1BUFD | 31:16 | ADC Result Word D (ADC1BUFD<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9150 | ADC1BUFE | 31:16 | ADC Result Word E (ADC1BUFE<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9160 | ADC1BUFF | 31:16 | ADC Result Word F (ADC1BUFF<31:0>) | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | FORM<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0, HSC | R/C-0, HSC |
| | SSRC<2:0> | | | CLRASAM | — | ASAM | SAMP(2) | DONE(3) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit(1)
- 1 = ADC module is operating
- 0 = ADC module is not operating

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
- 111 = Signed Fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
- 110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
- 101 = Signed Integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
- 100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
- 011 = Signed Fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
- 010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
- 001 = Signed Integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
- 000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
- 111 = Internal counter ends sampling and starts conversion (auto convert)
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CTMU ends sampling and starts conversion
- 010 = Timer 3 period match ends sampling and starts conversion
- 001 = Active transition on INT0 pin ends sampling and starts conversion
- 000 = Clearing the SAMP bit ends sampling and starts conversion

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

**REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)**

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)
1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** ADC Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)
1 = The ADC S&H circuit is sampling
0 = The ADC S&H circuit is holding
When ASAM = 0, writing '1' to this bit starts sampling.
When SSRC<2:0> = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** Analog-to-Digital Conversion Status bit(3)
Clearing this bit will not affect any operation in progress.
1 = Analog-to-digital conversion is done
0 = Analog-to-digital conversion is not done or has not started

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write a '0' to end sampling and start conversion. If SSRC<2:0> ≠ '000', this bit is automatically cleared by hardware to end sampling and start conversion.

**3:** This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.


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**REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 |
| | VCFG<2:0> | | | OFFCAL | — | CSCNA | — | — |
| 7:0 | R-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

| Bit Value | VREFH | VREFL |
|---|---|---|
| 1xx | AVDD | AVss |
| 011 | External VREF+ pin | External VREF- pin |
| 010 | AVDD | External VREF- pin |
| 001 | External VREF+ pin | AVSS |
| 000 | AVDD | AVss |

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enable Offset Calibration mode
Positive and negative inputs of the S&H circuit are connected to VREFL.
0 = Disable Offset Calibration mode
The inputs to the S&H circuit are controlled by AD1CHS or AD1CSSL.

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scan inputs
0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1.
1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADCBUF8
0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses Sample A input multiplexer settings for first sample, and then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples
0 = Always use Sample A input multiplexer settings

**REGISTER 23-3: AD1CON3: ADC CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ADRC | — | — | SAMC<4:0>(1) | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W | R/W-0 |
| | ADCS<7:0>(2) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ADRC:** ADC Conversion Clock Source bit
1 = Clock derived from FRC
0 = Clock derived from Peripheral Bus Clock (PBCLK)

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits(2)
11111111 = TPB • 2 • (ADCS<7:0> + 1) = 512 • TPB = TAD
•
•
•
00000001 = TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD
00000000 = TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD

**Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
**2:** This bit is not used if the ADRC bit (AD1CON3<15>) = 1.


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**REGISTER 23-4: AD1CHS: ADC INPUT SELECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NB | — | — | — | CH0SB<3:0> | | | |
| 23:16 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CH0NA | — | — | — | CH0SA<3:0> | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **CH0NB:** Negative Input Select bit for Sample B
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CH0SB<3:0>:** Positive Input Select bits for Sample B
1111 = Channel 0 positive input is AN15
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREFL

bit 22-20 **Unimplemented:** Read as '0'

bit 19-16 **CH0SA<3:0>:** Positive Input Select bits for Sample A Multiplexer Setting
1111 = Channel 0 positive input is AN15
•
•
•
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

**REGISTER 23-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL15 | CSSL14 | CSSL13 | CSSL12 | CSSL11 | CSSL10 | CSSL9 | CSSL8 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CSSL<15:0>:** ADC Input Pin Scan Selection bits(1)

1 = Select ANx for input scan

0 = Skip ANx for input scan

**Note 1:** CSSL = ANx, where 'x' = 0-15.



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## 24.0 CONTROLLER AREA NETWORK (CAN)

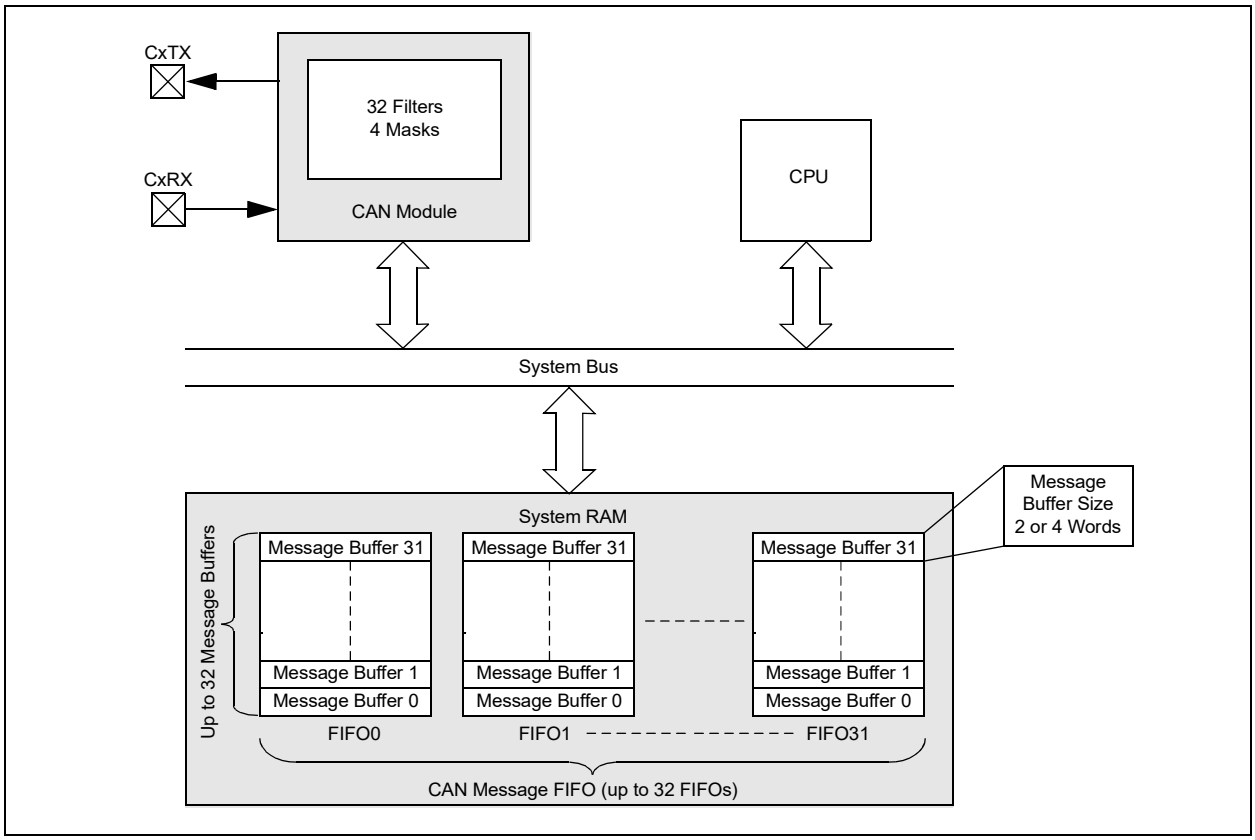
**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 34. "Controller Area Network (CAN)"** (DS60001154) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Controller Area Network (CAN) module supports the following key features:

- Standards Compliance:
  - Full CAN 2.0B compliance
  - Programmable bit rate up to 1 Mbps
- Message Reception and Transmission:
  - 32 message FIFOs
  - Each FIFO can have up to 32 messages for a total of 1024 messages
  - FIFO can be a transmit message FIFO or a receive message FIFO
  - User-defined priority levels for message FIFOs used for transmission
  - 32 acceptance filters for message filtering
  - Four acceptance filter mask registers for message filtering
  - Automatic response to remote transmit request
  - DeviceNet™ addressing support
- Additional Features:
  - Loopback, Listen All Messages, and Listen Only modes for self-test, system diagnostics and bus monitoring
  - Low-power operating modes
  - CAN module is a bus master on the PIC32 system bus
  - Use of DMA is not required
  - Dedicated time-stamp timer
  - Dedicated DMA channels
  - Data-only Message Reception mode

Figure 24-1 illustrates the general structure of the CAN module.

**FIGURE 24-1: PIC32 CAN MODULE BLOCK DIAGRAM**



## 24.1 Control Registers

**TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| B000 | C1CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| B010 | C1CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | 0000 |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| B020 | C1INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| B030 | C1VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| B040 | C1TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| B050 | C1FSTAT | 31:16 | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| B060 | C1RXOVF | 31:16 | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| B070 | C1TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| B080 | C1RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B090 | C1RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0A0 | C1RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0B0 | C1RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | -— | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B0C0 | C1FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| B0D0 | C1FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| B0E0 | C1FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**TABLE 24-1: CAN1 REGISTER SUMMARY FOR PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H, PIC32MX575F512H, PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L, PIC32MX575F512L, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| B0F0 | C1FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | | 0000 |
| B100 | C1FLTCON4 | 31:16 | FLTEN19 | MSEL19<1:0> | | FSEL19<4:0> | | | | | FLTEN18 | MSEL18<1:0> | | FSEL18<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN17 | MSEL17<1:0> | | FSEL17<4:0> | | | | | FLTEN16 | MSEL16<1:0> | | FSEL16<4:0> | | | | | 0000 |
| B110 | C1FLTCON5 | 31:16 | FLTEN23 | MSEL23<1:0> | | FSEL23<4:0> | | | | | FLTEN22 | MSEL22<1:0> | | FSEL22<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN21 | MSEL21<1:0> | | FSEL21<4:0> | | | | | FLTEN20 | MSEL20<1:0> | | FSEL20<4:0> | | | | | 0000 |
| B120 | C1FLTCON6 | 31:16 | FLTEN27 | MSEL27<1:0> | | FSEL27<4:0> | | | | | FLTEN26 | MSEL26<1:0> | | FSEL26<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN25 | MSEL25<1:0> | | FSEL25<4:0> | | | | | FLTEN24 | MSEL24<1:0> | | FSEL24<4:0> | | | | | 0000 |
| B130 | C1FLTCON7 | 31:16 | FLTEN31 | MSEL31<1:0> | | FSEL31<4:0> | | | | | FLTEN30 | MSEL30<1:0> | | FSEL30<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN29 | MSEL29<1:0> | | FSEL29<4:0> | | | | | FLTEN28 | MSEL28<1:0> | | FSEL28<4:0> | | | | | 0000 |
| B140 | C1RXFn (n = 0-31) | 31:16 | SID<10:0> | | | | | | | | | | | -— | EXID | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| B340 | C1FIFOBA | 31:16 | C1FIFOBA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| B350 | C1FIFOCONn (n = 0-31) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |
| B360 | C1FIFOINTn (n = 0-31) | 31:16 | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXN EMPTYIE | 0000 |
| | | 15:0 | — | — | — | — | — | TXNFULLIF | TXHALFIF | TXEMPTYIF | — | — | — | — | RXOVFLIF | RXFULLIF | RXHALFIF | RXN EMPTYIF | 0000 |
| B370 | C1FIFOUAn (n = 0-31) | 31:16 | C1FIFOUA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| B380 | C1FIFOCIn (n = 0-31) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | C1FIFOCI<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| C000 | C2CON | 31:16 | — | — | — | — | ABAT | REQOP<2:0> | | | OPMOD<2:0> | | | CANCAP | — | — | — | — | 0480 |
| | | 15:0 | ON | — | SIDLE | — | CANBUSY | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| C010 | C2CFG | 31:16 | — | — | — | — | — | — | — | — | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | 0000 |
| | | 15:0 | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | SJW<1:0> | | BRP<5:0> | | | | | 0000 |
| C020 | C2INT | 31:16 | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE | 0000 |
| | | 15:0 | IVRIF | WAKIF | CERRIF | SERRIF | RBOVIF | — | — | — | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF | 0000 |
| C030 | C2VEC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0040 |
| C040 | C2TREC | 31:16 | — | — | — | — | — | — | — | — | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN | 0000 |
| | | 15:0 | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| C050 | C2FSTAT | 31:16 | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 | 0000 |
| | | 15:0 | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 | 0000 |
| C060 | C2RXOVF | 31:16 | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| | | 15:0 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| C070 | C2TMR | 31:16 | CANTS<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | CANTSPRE<15:0> | | | | | | | | | | | | | | | | 0000 |
| C080 | C2RXM0 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C0A0 | C2RXM1 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C0B0 | C2RXM2 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C0B0 | C2RXM3 | 31:16 | SID<10:0> | | | | | | | | | | | — | MIDE | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C0C0 | C2FLTCON0 | 31:16 | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | | 0000 |
| C0D0 | C2FLTCON1 | 31:16 | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | | 0000 |
| C0E0 | C2FLTCON2 | 31:16 | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | | 0000 |
| C0F0 | C2FLTCON3 | 31:16 | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**TABLE 24-2: CAN2 REGISTER SUMMARY FOR PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| C100 | C2FLTCON4 | 31:16 | FLTEN19 | MSEL19<1:0> | | FSEL19<4:0> | | | | | FLTEN18 | MSEL18<1:0> | | FSEL18<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN17 | MSEL17<1:0> | | FSEL17<4:0> | | | | | FLTEN16 | MSEL16<1:0> | | FSEL16<4:0: | | | | | 0000 |
| C110 | C2FLTCON5 | 31:16 | FLTEN23 | MSEL23<1:0> | | FSEL23<4:0> | | | | | FLTEN22 | MSEL22<1:0> | | FSEL22<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN21 | MSEL21<1:0> | | FSEL21<4:0> | | | | | FLTEN20 | MSEL20<1:0> | | FSEL20<4:0> | | | | | 0000 |
| C120 | C2FLTCON6 | 31:16 | FLTEN27 | MSEL27<1:0> | | FSEL27<4:0> | | | | | FLTEN26 | MSEL26<1:0> | | FSEL26<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN25 | MSEL25<1:0> | | FSEL25<4:0> | | | | | FLTEN24 | MSEL24<1:0> | | FSEL24<4:0> | | | | | 0000 |
| C130 | C2FLTCON7 | 31:16 | FLTEN31 | MSEL31<1:0> | | FSEL31<4:0> | | | | | FLTEN30 | MSEL30<1:0> | | FSEL30<4:0> | | | | | 0000 |
| | | 15:0 | FLTEN29 | MSEL29<1:0> | | FSEL29<4:0> | | | | | FLTEN28 | MSEL28<1:0> | | FSEL28<4:0> | | | | | 0000 |
| C140 | C2RXFn (n = 0-31) | 31:16 | SID<10:0> | | | | | | | | | | | — | EXID | — | EID<17:16> | | xxxx |
| | | 15:0 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C340 | C2FIFOBA | 31:16 | C2FIFOBA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| C350 | C2FIFOCONn (n = 0-31) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | FSIZE<4:0> | | | | | 0000 |
| | | 15:0 | — | FRESET | UINC | DONLY | — | — | — | — | TXEN | TXABAT | TXLARB | TXERR | TXREQ | RTREN | TXPRI<1:0> | | 0000 |
| C360 | C2FIFOINTn (n = 0-31) | 31:16 | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXN EMPTYIE | 0000 |
| | | 15:0 | — | — | — | — | — | TXNFULLIF | TXHALFIF | TXEMPTYIF | — | — | — | — | RXOVFLIF | RXFULLIF | RXHALFIF | RXN EMPTYIF | 0000 |
| C370 | C2FIFOUAn (n = 0-31) | 31:16 | C2FIFOUA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| C380 | C2FIFOCIn (n = 0-31) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | C2FIFOCI<4:0> | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

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**REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | S/HC-0 | R/W-1 | R/W-0 | R/W-0 |
| | — | — | — | — | ABAT | REQOP<2:0> | | |
| 23:16 | R-1 | R-0 | R-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | OPMOD<2:0> | | | CANCAP | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | R-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDLE | — | CANBUSY | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | DNCNT<4:0> | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
- 1 = Signal all transmit buffers to abort transmission
- 0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
- 111 = Set Listen All Messages mode
- 110 = Reserved
- 101 = Reserved
- 100 = Set Configuration mode
- 011 = Set Listen Only mode
- 010 = Set Loopback mode
- 001 = Set Disable mode
- 000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
- 111 = Module is in Listen All Messages mode
- 110 = Reserved
- 101 = Reserved
- 100 = Module is in Configuration mode
- 011 = Module is in Listen Only mode
- 010 = Module is in Loopback mode
- 001 = Module is in Disable mode
- 000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
- 1 = CANTMR value is stored on valid message reception and is stored with the message
- 0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit(1)
- 1 = CAN module is enabled
- 0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

**Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.


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**REGISTER 24-1: CiCON: CAN MODULE CONTROL REGISTER (CONTINUED)**

bit 13 **SIDLE:** CAN Stop in Idle bit
1 = CAN Stops operation when system enters Idle mode
0 = CAN continues operation when system enters Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **CANBUSY:** CAN Module is Busy bit
1 = The CAN module is active
0 = The CAN module is completely disabled

bit 10-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT<4:0>:** Device Net Filter Bit Number bits
10011-11111 = Invalid Selection (compare up to 18-bits of data with EID)
10010 = Compare up to data byte 2 bit 6 with EID17 (CiRXFn<17>)
•
•
•
00001 = Compare up to data byte 0 bit 7 with EID0 (CiRXFn<0>)
00000 = Do not compare data bytes

**Note 1:** If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

**REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | WAKFIL | — | — | — | SEG2PH<2:0>(1,4) | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SEG2PHTS(1) | SAM(2) | SEG1PH<2:0> | | | PRSEG<2:0> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SJW<1:0>(3) | | BRP<5:0> | | | | | |

| Legend: | HC = Hardware Clear | S = Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).


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**REGISTER 24-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)**

bit 10-8 **PRSEG<2:0>:** Propagation Time Segment bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7-6 **SJW<1:0>:** Synchronization Jump Width bits(3)
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP<5:0>:** Baud Rate Prescaler bits
111111 = TQ = (2 x 64)/FSYS
111110 = TQ = (2 x 63)/FSYS
•
•
•
000001 = TQ = (2 x 2)/FSYS
000000 = TQ = (2 x 1)/FSYS

**Note 1:** SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
**2:** 3 Time bit sampling is not allowed for BRP < 2.
**3:** SJW ≤ SEG2PH.
**4:** The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 24-3: CiINT: CAN INTERRUPT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | IVRIE | WAKIE | CERRIE | SERRIE | RBOVIE | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | MODIE | CTMRIE | RBIE | TBIE |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
| | IVRIF | WAKIF | CERRIF | SERRIF(1) | RBOVIF | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | MODIF | CTMRIF | RBIF | TBIF |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 28 **SERRIE:** System Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 26-20 **Unimplemented:** Read as '0'

bit 19 **MODIE:** Mode Change Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
1 = An invalid messages interrupt has occurred
0 = An invalid message interrupt has not occurred

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).


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**REGISTER 24-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)**

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the system bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

**Note 1:** This bit can only be cleared by turning the CAN module Off and On by clearing or setting the ON bit (CiCON<15>).

**REGISTER 24-4: CiVEC: CAN INTERRUPT CODE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | FILHIT<4:0> | | | | |
| 7:0 | U-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | ICODE<6:0>(1) | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bit
- 11111 = Filter 31
- 11110 = Filter 30
- .
- .
- .
- 00001 = Filter 1
- 00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits(1)
- 1111111 = Reserved
- .
- .
- .
- 1001001 = Reserved
- 1001000 = Invalid message received (IVRIF)
- 1000111 = CAN module mode change (MODIF)
- 1000110 = CAN timestamp timer (CTMRIF)
- 1000101 = Bus bandwidth error (SERRIF)
- 1000100 = Address error interrupt (SERRIF)
- 1000011 = Receive FIFO overflow interrupt (RBOVIF)
- 1000010 = Wake-up interrupt (WAKIF)
- 1000001 = Error Interrupt (CERRIF)
- 1000000 = No interrupt
- 0111111 = Reserved
- .
- .
- .
- 0100000 = Reserved
- 0011111 = FIFO31 Interrupt (CiFSTAT<31> set)
- 0011110 = FIFO30 Interrupt (CiFSTAT<30> set)
- .
- .
- .
- 0000001 = FIFO1 Interrupt (CiFSTAT<1> set)
- 0000000 = FIFO0 Interrupt (CiFSTAT<0> set)

**Note 1:** These bits are only updated for enabled interrupts.


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**REGISTER 24-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | TXBO | TXBP | RXBP | TXWARN | RXWARN | EWARN |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | TERRCNT<7:0> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RERRCNT<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

**REGISTER 24-6: CiFSTAT: CAN FIFO STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP31 | FIFOIP30 | FIFOIP29 | FIFOIP28 | FIFOIP27 | FIFOIP26 | FIFOIP25 | FIFOIP24 |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP23 | FIFOIP22 | FIFOIP21 | FIFOIP20 | FIFOIP19 | FIFOIP18 | FIFOIP17 | FIFOIP16 |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP15 | FIFOIP14 | FIFOIP13 | FIFOIP12 | FIFOIP11 | FIFOIP10 | FIFOIP9 | FIFOIP8 |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | FIFOIP7 | FIFOIP6 | FIFOIP5 | FIFOIP4 | FIFOIP3 | FIFOIP2 | FIFOIP1 | FIFOIP0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **FIFOIP<31:0>:** FIFOn Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

**REGISTER 24-7: CiRXOVF: CAN RECEIVE FIFO OVERFLOW STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| 23:16 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| 15:8 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF9 | RXOVF8 |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **RXOVF<31:0>:** FIFOn Receive Overflow Interrupt Pending bit
1 = FIFO has overflowed
0 = FIFO has not overflowed

**REGISTER 24-8: CiTMR: CAN TIMER REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTS<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTS<7:0> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTSPRE<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CANTSPRE<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CANTS<15:0>:** CAN Time Stamp Timer bits
This is a free-running timer that increments every CANTSPRE system clocks when the CANCAP bit (CiCON<20>) is set.

bit 15-0 **CANTSPRE<15:0>:** CAN Time Stamp Timer Prescaler bits
1111 1111 1111 1111 = CAN time stamp timer (CANTS) increments every 65,535 system clocks
.
.
.
0000 0000 0000 0000 = CAN time stamp timer (CANTS) increments every system clock

**Note 1:** CiTMR will be paused when CANCAP = 0.
**2:** The CiTMR prescaler count will be reset on any write to CiTMR (CANTSPRE will be unaffected).


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**REGISTER 24-9: CiRXMn: CAN ACCEPTANCE FILTER MASK 'n' REGISTER (n = 0, 1, 2 OR 3)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | SID<2:0> | | | — | MIDE | — | EID<17:16> | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Include the SIDx bit in filter comparison
0 = The SIDx bit is a 'don't care' in filter operation

bit 20 **Unimplemented:** Read as '0'

bit 19 **MIDE:** Identifier Receive Mode bit
1 = Match only message types (standard/extended address) that correspond to the EXID bit in filter
0 = Match either standard or extended address message if filters match (that is, if (Filter SID) = (Message SID) or if (FILTER SID/EID) = (Message SID/EID))

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Include the EIDx bit in filter comparison
0 = The EIDx bit is a 'don't care' in filter operation

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 24-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN3 | MSEL3<1:0> | | FSEL3<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN2 | MSEL2<1:0> | | FSEL2<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN1 | MSEL1<1:0> | | FSEL1<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN0 | MSEL0<1:0> | | FSEL0<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN3:** Filter 3 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)**

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN7 | MSEL7<1:0> | | FSEL7<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN6 | MSEL6<1:0> | | FSEL6<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN5 | MSEL5<1:0> | | FSEL5<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN4 | MSEL4<1:0> | | FSEL4<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN7:** Filter 7 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL7<1:0>:** Filter 7 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL7<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6:** Filter 6 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL6<1:0>:** Filter 6 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL6<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1 (CONTINUED)**

bit 15 **FLTEN5:** Filter 17 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL5<1:0>:** Filter 5 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL5<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN4:** Filter 4 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL4<1:0>:** Filter 4 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL4<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN11 | MSEL11<1:0> | | FSEL11<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN10 | MSEL10<1:0> | | FSEL10<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN9 | MSEL9<1:0> | | FSEL9<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN8 | MSEL8<1:0> | | FSEL8<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)**

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN15 | MSEL15<1:0> | | FSEL15<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN14 | MSEL14<1:0> | | FSEL14<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN13 | MSEL13<1:0> | | FSEL13<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN12 | MSEL12<1:0> | | FSEL12<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN15:** Filter 15 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL15<1:0>:** Filter 15 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL15<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN14:** Filter 14 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL14<1:0>:** Filter 14 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL14<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-13: CiFLTCON3: CAN FILTER CONTROL REGISTER 3 (CONTINUED)**

bit 15 **FLTEN13:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL13<1:0>:** Filter 13 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL13<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN12:** Filter 12 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL12<1:0>:** Filter 12 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL12<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN19 | MSEL19<1:0> | | FSEL19<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN18 | MSEL18<1:0> | | FSEL18<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN17 | MSEL17<1:0> | | FSEL17<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN16 | MSEL16<1:0> | | FSEL16<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN19:** Filter 19 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL19<1:0>:** Filter 19 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL19<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN18:** Filter 18 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL18<1:0>:** Filter 18 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL18<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-14: CiFLTCON4: CAN FILTER CONTROL REGISTER 4 (CONTINUED)**

bit 15 **FLTEN17:** Filter 13 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL17<1:0>:** Filter 17 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL17<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN16:** Filter 16 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL16<1:0>:** Filter 16 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL16<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN23 | MSEL23<1:0> | | FSEL23<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN22 | MSEL22<1:0> | | FSEL22<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN21 | MSEL21<1:0> | | FSEL21<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN20 | MSEL20<1:0> | | FSEL20<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)**

bit 15 **FLTEN21:** Filter 21 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL21<1:0>:** Filter 21 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL21<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN20:** Filter 20 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL20<1:0>:** Filter 20 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL20<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN27 | MSEL27<1:0> | | FSEL27<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN26 | MSEL26<1:0> | | FSEL26<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN25 | MSEL25<1:0> | | FSEL25<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN24 | MSEL24<1:0> | | FSEL24<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN27:** Filter 27 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL27<1:0>:** Filter 27 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL27<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN26:** Filter 26 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL26<1:0>:** Filter 26 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL26<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6 (CONTINUED)**

bit 15 **FLTEN25:** Filter 25 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL25<1:0>:** Filter 25 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL25<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN24:** Filter 24 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL24<1:0>:** Filter 24 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL24<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

| **Note:** | The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'. |
|---|---|

**REGISTER 24-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN31 | MSEL31<1:0> | | FSEL31<4:0> | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN30 | MSEL30<1:0> | | FSEL30<4:0> | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN29 | MSEL29<1:0> | | FSEL29<4:0> | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FLTEN28 | MSEL28<1:0> | | FSEL28<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FLTEN31:** Filter 31 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL31<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN30:** Filter 30Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL30<1:0>:** Filter 30Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL30<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
.
.
.
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.


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**REGISTER 24-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7 (CONTINUED)**

bit 15 **FLTEN29:** Filter 29 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL29<1:0>:** Filter 29 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL29<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN28:** Filter 28 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL28<1:0>:** Filter 28 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL28<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

**Note:** The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

**REGISTER 24-18: CiRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | SID<10:3> | | | | | | | |
| 23:16 | R/W-x | R/W-x | R/W-x | U-0 | R/W-0 | U-0 | R/W-x | R/W-x |
| | SID<2:0> | | | — | EXID | — | EID<17:16> | |
| 15:8 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | EID<15:8> | | | | | | | |
| 7:0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| | EID<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

**Note:** This register can only be modified when the filter is disabled (FLTENn = 0).


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**REGISTER 24-19: CiFIFOBA: CAN MESSAGE BUFFER BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CiFIFOBA<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CiFIFOBA<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CiFIFOBA<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0(1) | R-0(1) |
| | CiFIFOBA<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CiFIFOBA<31:0>:** CAN FIFO Base Address bits

These bits define the base address of all message buffers. Individual message buffers are located based on the size of the previous message buffers. This address is a physical address. Bits <1:0> are read-only and read as '0', forcing the messages to be 32-bit word-aligned in device RAM.

**Note 1:** This bit is unimplemented and will always read '0', which forces word-alignment of messages.

**Note:** This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

**REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | FSIZE<4:0>(1) | | | | |
| 15:8 | U-0 | S/HC-0 | S/HC-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | — | FRESET | UINC | DONLY(1) | — | — | — | — |
| 7:0 | R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXEN | TXABAT(2) | TXLARB(3) | TXERR(3) | TXREQ | RTREN | TXPR<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits(1)

11111 = FIFO is 32 messages deep

•

•

•

00010 = FIFO is 3 messages deep

00001 = FIFO is 2 messages deep

00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user should poll whether this bit is clear before taking any action.

0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)

When this bit is set the FIFO head will increment by a single message

TXEN = 0: (FIFO configured as a Receive FIFO)

When this bit is set the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit(1)

TXEN = 1: (FIFO configured as a Transmit FIFO)

This bit is not used and has no effect.

TXEN = 0: (FIFO configured as a Receive FIFO)

1 = Only data bytes will be stored in the FIFO

0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **TXEN:** TX/RX Buffer Selection bit

1 = FIFO is a Transmit FIFO

0 = FIFO is a Receive FIFO

**Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).

**2:** This bit is updated when a message completes (or aborts) or when the FIFO is reset.

**3:** This bit is reset on any read of this register or when the FIFO is reset.


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**REGISTER 24-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' (n = 0 THROUGH 31)**

bit 6 **TXABAT:** Message Aborted bit(2)
1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)
1 = A bus error occured while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request
TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
Clearing the bit to '0' while set ('1') will request a message abort.
TXEN = 0: (FIFO configured as a receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
**2:** This bit is updated when a message completes (or aborts) or when the FIFO is reset.
**3:** This bit is reset on any read of this register or when the FIFO is reset.

**REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TXNFULLIE | TXHALFIE | TXEMPTYIE |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | RXOVFLIE | RXFULLIE | RXHALFIE | RXNEMPTYIE |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | — | TXNFULLIF(1) | TXHALFIF | TXEMPTYIF(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 |
| | — | — | — | — | RXOVFLIF | RXFULLIF(1) | RXHALFIF(1) | RXNEMPTYIF(1) |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-27 **Unimplemented:** Read as '0'

bit 26 **TXNFULLIE:** Transmit FIFO Not Full Interrupt Enable bit
1 = Interrupt enabled for FIFO not full
0 = Interrupt disabled for FIFO not full

bit 25 **TXHALFIE:** Transmit FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 24 **TXEMPTYIE:** Transmit FIFO Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO empty
0 = Interrupt disabled for FIFO empty

bit 23-20 **Unimplemented:** Read as '0'

bit 19 **RXOVFLIE:** Overflow Interrupt Enable bit
1 = Interrupt enabled for overflow event
0 = Interrupt disabled for overflow event

bit 18 **RXFULLIE:** Full Interrupt Enable bit
1 = Interrupt enabled for FIFO full
0 = Interrupt disabled for FIFO full

bit 17 **RXHALFIE:** FIFO Half Full Interrupt Enable bit
1 = Interrupt enabled for FIFO half full
0 = Interrupt disabled for FIFO half full

bit 16 **RXNEMPTYIE:** Empty Interrupt Enable bit
1 = Interrupt enabled for FIFO not empty
0 = Interrupt disabled for FIFO not empty

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **TXNFULLIF:** Transmit FIFO Not Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is not full
0 = FIFO is full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

**Note 1:** This bit is read-only and reflects the status of the FIFO.


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**REGISTER 24-21: CiFIFOINTn: CAN FIFO INTERRUPT REGISTER 'n' (n = 0 THROUGH 31)**

bit 9 **TXHALFIF:** FIFO Transmit FIFO Half Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is ≤ half full
0 = FIFO is > half full
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 8 **TXEMPTYIF:** Transmit FIFO Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
1 = FIFO is empty
0 = FIFO is not empty, at least 1 message queued to be transmitted
TXEN = 0: (FIFO configured as a receive buffer)
Unused, reads '0'

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **RXOVFLIF:** Receive FIFO Overflow Interrupt Flag bit
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = Overflow event has occurred
0 = No overflow event occured

bit 2 **RXFULLIF:** Receive FIFO Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is full
0 = FIFO is not full

bit 1 **RXHALFIF:** Receive FIFO Half Full Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is ≥ half full
0 = FIFO is < half full

bit 0 **RXNEMPTYIF:** Receive Buffer Not Empty Interrupt Flag bit(1)
TXEN = 1: (FIFO configured as a transmit buffer)
Unused, reads '0'
TXEN = 0: (FIFO configured as a receive buffer)
1 = FIFO is not empty, has at least 1 message
0 = FIFO is empty

**Note 1:** This bit is read-only and reflects the status of the FIFO.

**REGISTER 24-22: CiFIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | CiFIFOUAn<31:24> | | | | | | | |
| 23:16 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | CiFIFOUAn<23:16> | | | | | | | |
| 15:8 | R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
| | CiFIFOUAn<15:8> | | | | | | | |
| 7:0 | R-x | R-x | R-x | R-x | R-x | R-x | R-0(1) | R-0(1) |
| | CiFIFOUAn<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **CiFIFOUAn<31:0>:** CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

**Note 1:** This bit will always read '0', which forces byte-alignment of messages.

**Note:** This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

**REGISTER 24-23: CiFIFOCIN: CAN MODULE MESSAGE INDEX REGISTER 'n' (n = 0 THROUGH 31)**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | — | — | — | CiFIFOCI<4:0> | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **CiFIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a transmit buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a receive buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.


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## 25.0 ETHERNET CONTROLLER

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. "Ethernet Controller"** (DS60001155) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation
- Supports RMII and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
  - CRC check
  - 64-byte pattern match
  - Broadcast, multicast and unicast packets
  - Magic Packet™
  - 64-bit hash table
  - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 25-1 illustrates a block diagram of the Ethernet controller.

**FIGURE 25-1: ETHERNET CONTROLLER BLOCK DIAGRAM**

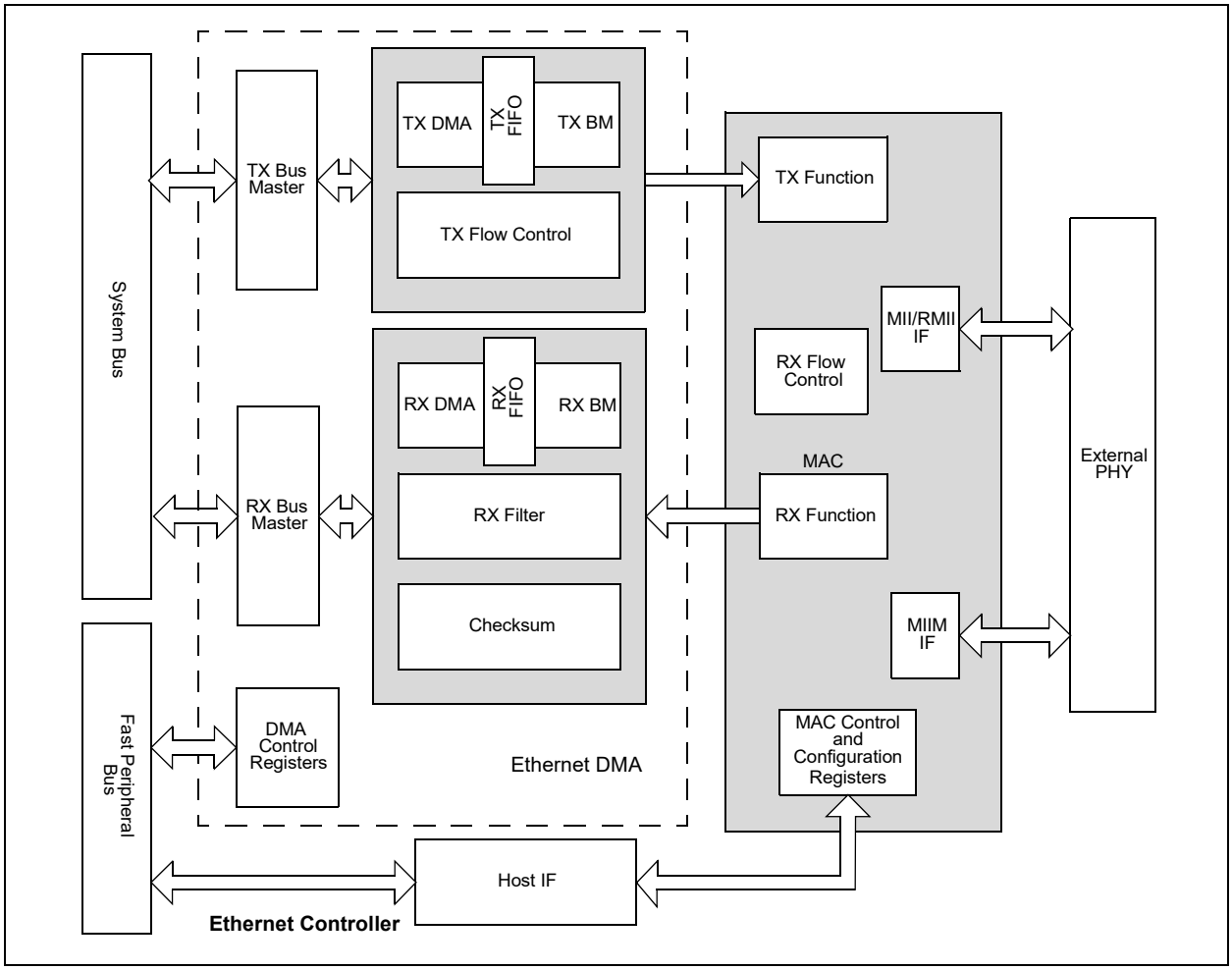

Table 25-1, Table 25-2, Table 25-3 and Table 25-4 show four interfaces and the associated pins that can be used with the Ethernet Controller.

**TABLE 25-1: MII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 1)**

| Pin Name | Description |
|---|---|
| EMDC | Management Clock |
| EMDIO | Management I/O |
| ETXCLK | Transmit Clock |
| ETXEN | Transmit Enable |
| ETXD0 | Transmit Data |
| ETXD1 | Transmit Data |
| ETXD2 | Transmit Data |
| ETXD3 | Transmit Data |
| ETXERR | Transmit Error |
| ERXCLK | Receive Clock |
| ERXDV | Receive Data Valid |
| ERXD0 | Receive Data |
| ERXD1 | Receive Data |
| ERXD2 | Receive Data |
| ERXD3 | Receive Data |
| ERXERR | Receive Error |
| ECRS | Carrier Sense |
| ECOL | Collision Indication |

**TABLE 25-2: RMII MODE DEFAULT INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 1)**

| Pin Name | Description |
|---|---|
| EMDC | Management Clock |
| EMDIO | Management I/O |
| ETXEN | Transmit Enable |
| ETXD0 | Transmit Data |
| ETXD1 | Transmit Data |
| EREFCLK | Reference Clock |
| ECRSDV | Carrier Sense – Receive Data Valid |
| ERXD0 | Receive Data |
| ERXD1 | Receive Data |
| ERXERR | Receive Error |

**Note:** Ethernet controller pins that are not used by selected interface can be used by other peripherals.

**TABLE 25-3: MII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 1, FETHIO = 0)**

| Pin Name | Description |
|---|---|
| AEMDC | Management Clock |
| AEMDIO | Management I/O |
| AETXCLK | Transmit Clock |
| AETXEN | Transmit Enable |
| AETXD0 | Transmit Data |
| AETXD1 | Transmit Data |
| AETXD2 | Transmit Data |
| AETXD3 | Transmit Data |
| AETXERR | Transmit Error |
| AERXCLK | Receive Clock |
| AERXDV | Receive Data Valid |
| AERXD0 | Receive Data |
| AERXD1 | Receive Data |
| AERXD2 | Receive Data |
| AERXD3 | Receive Data |
| AERXERR | Receive Error |
| AECRS | Carrier Sense |
| AECOL | Collision Indication |

**Note:** The MII mode Alternate Interface is not available on 64-pin devices.

**TABLE 25-4: RMII MODE ALTERNATE INTERFACE SIGNALS (FMIIEN = 0, FETHIO = 0)**

| Pin Name | Description |
|---|---|
| AEMDC | Management Clock |
| AEMDIO | Management I/O |
| AETXEN | Transmit Enable |
| AETXD0 | Transmit Data |
| AETXD1 | Transmit Data |
| AEREFCLK | Reference Clock |
| AECRSDV | Carrier Sense – Receive Data Valid |
| AERXD0 | Receive Data |
| AERXD1 | Receive Data |
| AERXERR | Receive Error |


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## 25.1 Control Registers

**TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9000 | ETHCON1 | 31:16 | PTV<15:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | TXRTS | RXEN | AUTOFC | — | — | MANFC | — | — | — | BUFCDEC | 0000 |
| 9010 | ETHCON2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | RXBUFSZ<6:0> | | | | | | | — | — | — | — | 0000 |
| 9020 | ETHTXST | 31:16 | TXSTADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | TXSTADDR<15:2> | | | | | | | | | | | | | | — | — | 0000 |
| 9030 | ETHRXST | 31:16 | RXSTADDR<31:16> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | RXSTADDR<15:2> | | | | | | | | | | | | | | — | — | 0000 |
| 9040 | ETHHT0 | 31:16 | HT<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9050 | ETHHT1 | 31:16 | HT<63:32> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9060 | ETHPMM0 | 31:16 | PMM<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9070 | ETHPMM1 | 31:16 | PMM<63:32> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 9080 | ETHPMCS | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PMCS<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9090 | ETHPMO | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | PMO<15:0> | | | | | | | | | | | | | | | | 0000 |
| 90A0 | ETHRXFC | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | HTEN | MPEN | — | NOTPM | PMMODE<3:0> | | | | CRC ERREN | CRC OKEN | RUNT ERREN | RUNTEN | UCEN | NOT MEEN | MCEN | BCEN | 0000 |
| 90B0 | ETHRXWM | 31:16 | — | — | — | — | — | — | — | — | RXFWM<7:0> | | | | | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | RXEWM<7:0> | | | | | | | | 0000 |
| 90C0 | ETHIEN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | TX BUSEIE | RX BUSEIE | — | — | — | EW MARKIE | FW MARKIE | RX DONEIE | PK TPENDIE | RX ACTIE | — | TX DONEIE | TX ABORTIE | RX BUFNAIE | RX OVFLWIE | 0000 |
| 90D0 | ETHIRQ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | TXBUSE | RXBUSE | — | — | — | EWMARK | FWMARK | RXDONE | PKTPEND | RXACT | — | TXDONE | TXABORT | RXBUFNA | RXOVFLW | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values default to the factory programmed value.

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**TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 90E0 | ETHSTAT | 31:16 | — | — | — | — | — | — | — | — | BUFCNT<7:0> | | | | | | | | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | BUSY | TXBUSY | RXBUSY | — | — | — | — | — | 0000 |
| 9100 | ETH RXOVFLOW | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RXOVFLWCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9110 | ETH FRMTXOK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | FRMTXOKCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9120 | ETH SCOLFRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SCOLFRMCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9130 | ETH MCOLFRM | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | MCOLFRMCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9140 | ETH FRMRXOK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | FRMRXOKCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9150 | ETH FCSERR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | FCSERRCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9160 | ETH ALGNERR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ALGNERRCNT<15:0> | | | | | | | | | | | | | | | | 0000 |
| 9200 | EMAC1 CFG1 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | SOFT RESET | SIM RESET | — | — | RESET RMCS | RESET RFUN | RESET TMCS | RESET TFUN | — | — | — | LOOPBACK | TXPAUSE | RXPAUSE | PASSALL | RXENABLE | 800D |
| 9210 | EMAC1 CFG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | EXCESS DFR | BP NOBKOFF | NOBKOFF | — | — | LONGPRE | PUREPRE | AUTOPAD | VLANPAD | PAD ENABLE | CRC ENABLE | DELAYCRC | HUGEFRM | LENGTHCK | FULLDPLX | 4082 |
| 9220 | EMAC1 IPGT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | B2BIPKTGP<6:0> | | | | | | | 0012 |
| 9230 | EMAC1 IPGR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | NB2BIPKTGP1<6:0> | | | | | | | — | NB2BIPKTGP2<6:0> | | | | | | | 0C12 |
| 9240 | EMAC1 CLRT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | CWINDOW<5:0> | | | | | | — | — | — | — | RETX<3:0> | | | | 370F |
| 9250 | EMAC1 MAXF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | MACMAXF<15:0> | | | | | | | | | | | | | | | | 05EE |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values default to the factory programmed value.



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**TABLE 25-5: ETHERNET CONTROLLER REGISTER SUMMARY FOR PIC32MX664F064H, PIC32MX664F128H, PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256H, PIC32MX675F512H, PIC32MX695F512H, PIC32MX775F256H, PIC32MX775F512H, PIC32MX795F512H, PIC32MX695F512L, PIC32MX675F256L, PIC32MX675F512L, PIC32MX764F128H, PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L AND PIC32MX795F512L DEVICES (CONTINUED)**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9260 | EMAC1 SUPP | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | RESET RMII | — | — | SPEED RMII | — | — | — | — | — | — | — | — | 1000 |
| 9270 | EMAC1 TEST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | TESTBP | TESTPAUSE | SHRTQNTA | 0000 |
| 9280 | EMAC1 MCFG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | RESET MGMT | — | — | — | — | — | — | — | — | — | CLKSEL<3:0> | | | | NOPRE | SCANINC | 0020 |
| 9290 | EMAC1 MCMD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SCAN | READ | 0000 |
| 92A0 | EMAC1 MADR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | PHYADDR<4:0> | | | | | — | — | — | REGADDR<4:0> | | | | | 0100 |
| 92B0 | EMAC1 MWTD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | MWTD<15:0> | | | | | | | | | | | | | | | | 0000 |
| 92C0 | EMAC1 MRDD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | MRDD<15:0> | | | | | | | | | | | | | | | | 0000 |
| 92D0 | EMAC1 MIND | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | LINKFAIL | NOTVALID | SCAN | MIIMBUSY | 0000 |
| 9300 | EMAC1 SA0(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | STNADDR6<7:0> | | | | | | | | STNADDR5<7:0> | | | | | | | | xxxx |
| 9310 | EMAC1 SA1(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | STNADDR4<7:0> | | | | | | | | STNADDR3<7:0> | | | | | | | | xxxx |
| 9320 | EMAC1 SA2(2) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| | | 15:0 | STNADDR2<7:0> | | | | | | | | STNADDR1<7:0> | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table (with the exception of ETHSTAT) have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** Reset values default to the factory programmed value.

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**REGISTER 25-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTV<15:8> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PTV<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON | — | SIDL | — | — | — | TXRTS | RXEN(1) |
| 7:0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
| | AUTOFC | — | — | MANFC | — | — | — | BUFCDEC |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **PTV<15:0>:** PAUSE Timer Value bits

PAUSE Timer Value used for Flow Control.
This register should only be written when RXEN (ETHCON1<8>) is not set.

These bits are only used for Flow Control operations.

bit 15 **ON:** Ethernet ON bit

1 = Ethernet module is enabled
0 = Ethernet module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Ethernet Stop in Idle Mode bit

1 = Ethernet module transfers are paused during Idle mode
0 = Ethernet module transfers continue during Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **TXRTS:** Transmit Request to Send bit

1 = Activate the TX logic and send the packet(s) defined in the TX EDT
0 = Stop transmit (when cleared by software) or transmit done (when cleared by hardware)

After the bit is written with a '1', it will clear to a '0' whenever the transmit logic has finished transmitting the requested packets in the Ethernet Descriptor Table (EDT). If a '0' is written by the CPU, the transmit logic finishes the current packet's transmission and then stops any further.

This bit only affects TX operations.

bit 8 **RXEN:** Receive Enable bit(1)

1 = Enable RX logic, packets are received and stored in the RX buffer as controlled by the filter configuration
0 = Disable RX logic, no packets are received in the RX buffer

This bit only affects RX operations.

**Note 1:** It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.


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**REGISTER 25-1: ETHCON1: ETHERNET CONTROLLER CONTROL REGISTER 1 (CONTINUED)**

bit 7 **AUTOFC:** Automatic Flow Control bit

1 = Automatic Flow Control is enabled
0 = Automatic Flow Control is disabled

Setting this bit will enable automatic Flow Control. If set, the full and empty watermarks are used to automatically enable and disable the Flow Control, respectively. When the number of received buffers BUFCNT (ETHSTAT<16:23>) rises to the full watermark, Flow Control is automatically enabled. When the BUFCNT falls to the empty watermark, Flow Control is automatically disabled.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **MANFC:** Manual Flow Control bit

1 = Manual Flow Control is enabled
0 = Manual Flow Control is disabled

Setting this bit will enable manual Flow Control. If set, the Flow Control logic will send a PAUSE frame using the PAUSE timer value in the PTV register. It will then resend a PAUSE frame every 128 * PTV<15:0>/2 TX clock cycles until the bit is cleared.

**Note:** For 10 Mbps operation, TX clock runs at 2.5 MHz. For 100 Mbps operation, TX clock runs at 25 MHz.

When this bit is cleared, the Flow Control logic will automatically send a PAUSE frame with a 0x0000 PAUSE timer value to disable Flow Control.

This bit is only used for Flow Control operations and affects both TX and RX operations.

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **BUFCDEC:** Descriptor Buffer Count Decrement bit

The BUFCDEC bit is a write-1 bit that reads as '0'. When written with a '1', the Descriptor Buffer Counter, BUFCNT, will decrement by one. If BUFCNT is incremented by the RX logic at the same time that this bit is written, the BUFCNT value will remain unchanged. Writing a '0' will have no effect.

This bit is only used for RX operations.

**Note 1:** It is not recommended to clear the RXEN bit and then make changes to any RX related field/register. The Ethernet Controller must be reinitialized (ON cleared to '0'), and then the RX changes applied.

**REGISTER 25-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | RXBUFSZ<6:4> | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
| | RXBUFSZ<3:0> | | | | — | — | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-11 **Unimplemented:** Read as '0'

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes
.
.
.
1100000 = RX data Buffer size for descriptors is 1536 bytes
.
.
.
0000011 = RX data Buffer size for descriptors is 48 bytes
0000010 = RX data Buffer size for descriptors is 32 bytes
0000001 = RX data Buffer size for descriptors is 16 bytes
0000000 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.


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**REGISTER 25-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | TXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | TXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for TX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 25-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXSTADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
| | RXSTADDR<7:2> | | | | | | — | — |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

**Note 1:** This register is only used for RX operations.
**2:** This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

**REGISTER 25-5: ETHHT0: ETHERNET CONTROLLER HASH TABLE 0 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **HT<31:0>:** Hash Table Bytes 0-3 bits

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.

**REGISTER 25-6: ETHHT1: ETHERNET CONTROLLER HASH TABLE 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<63:56> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<55:48> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<47:40> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HT<39:32> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **HT<63:32>:** Hash Table Bytes 4-7 bits

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the HTEN bit (ETHRXFC<15>) = 0.


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**REGISTER 25-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **PMM<31:24>:** Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>:** Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>:** Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>:** Pattern Match Mask 0 bits

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

**REGISTER 25-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<63:56> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<55:48> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<47:40> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMM<39:32> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **PMM<63:56>:** Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>:** Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>:** Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>:** Pattern Match Mask 4 bits

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

**REGISTER 25-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMCS<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMCS<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits

bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

**REGISTER 25-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMO<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | PMO<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

**Note 1:** This register is only used for RX operations.

**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.


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**REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | HTEN | MPEN | — | NOTPM | PMMODE<3:0> | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CRCERREN | CRCOKEN | RUNTERREN | RUNTEN | UCEN | NOTMEEN | MCEN | BCEN |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit
1 = Enable Hash Table Filtering
0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit
1 = Enable Magic Packet Filtering
0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit
1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur
0 = The Pattern Match Checksum must match for a successful Pattern Match to occur
This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits
1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)**(1,3)**
1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)**(1,2)**
0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)**(1)**
0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)**(1)**
0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)**(1)**
0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)**(1)**
0000 = Pattern Match is disabled; pattern match is always unsuccessful

**Note 1:** XOR = True when either one or the other conditions are true, but not both.
**2:** This Hash Table Filter match is active regardless of the value of the HTEN bit.
**3:** This Magic Packet Filter match is active regardless of the value of the MPEN bit.

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

**REGISTER 25-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER (CONTINUED)**

bit 7 **CRCERREN:** CRC Error Collection Enable bit
1 = The received packet CRC must be invalid for the packet to be accepted
0 = Disable CRC Error Collection filtering
This bit allows the user to collect all packets that have an invalid CRC.

bit 6 **CRCOKEN:** CRC OK Enable bit
1 = The received packet CRC must be valid for the packet to be accepted
0 = Disable CRC filtering
This bit allows the user to reject all packets that have an invalid CRC.

bit 5 **RUNTERREN:** Runt Error Collection Enable bit
1 = The received packet must be a runt packet for the packet to be accepted
0 = Disable Runt Error Collection filtering

This bit allows the user to collect all packets that are runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes (when CRCOKEN = 0) or any packet with a size of less than 64 bytes that has a valid CRC (when CRCOKEN = 1).

bit 4 **RUNTEN:** Runt Enable bit
1 = The received packet must not be a runt packet for the packet to be accepted
0 = Disable Runt filtering

This bit allows the user to reject all runt packets. For this filter, a runt packet is defined as any packet with a size of less than 64 bytes.

bit 3 **UCEN:** Unicast Enable bit
1 = Enable Unicast Filtering
0 = Disable Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address matches the Station Address.

bit 2 **NOTMEEN:** Not Me Unicast Enable bit
1 = Enable Not Me Unicast Filtering
0 = Disable Not Me Unicast Filtering

This bit allows the user to accept all unicast packets whose Destination Address does not match the Station Address.

bit 1 **MCEN:** Multicast Enable bit
1 = Enable Multicast Filtering
0 = Disable Multicast Filtering

This bit allows the user to accept all Multicast Address packets.

bit 0 **BCEN:** Broadcast Enable bit
1 = Enable Broadcast Filtering
0 = Disable Broadcast Filtering

This bit allows the user to accept all Broadcast Address packets.

**Note 1:** XOR = True when either one or the other conditions are true, but not both.
**2:** This Hash Table Filter match is active regardless of the value of the HTEN bit.
**3:** This Magic Packet Filter match is active regardless of the value of the MPEN bit.

**Note 1:** This register is only used for RX operations.
**2:** The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.


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**REGISTER 25-12: ETHRXWM: ETHERNET CONTROLLER RECEIVE WATERMARKS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXFWM<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXEWM<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **RXFWM<7:0>:** Receive Full Watermark bits

The software controlled RX Buffer Full Watermark Pointer is compared against the RX BUFCNT to determine the full watermark condition for the FWMARK interrupt and for enabling Flow Control when automatic Flow Control is enabled. The Full Watermark Pointer should always be greater than the Empty Watermark Pointer.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXEWM<7:0>:** Receive Empty Watermark bits

The software controlled RX Buffer Empty Watermark Pointer is compared against the RX BUFCNT to determine the empty watermark condition for the EWMARK interrupt and for disabling Flow Control when automatic Flow Control is enabled. The Empty Watermark Pointer should always be less than the Full Watermark Pointer.

**Note:** This register is only used for RX operations.

**REGISTER 25-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | TXBUSEIE(1) | RXBUSEIE(2) | — | — | — | EWMARKIE(2) | FWMARKIE(2) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXDONEIE(2) | PKTPENDIE(2) | RXACTIE(2) | — | TXDONEIE(1) | TXABORTIE(1) | RXBUFNAIE(2) | RXOVFLWIE(2) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit(1)
1 = Enable TXBUS Error Interrupt
0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit(2)
1 = Enable RXBUS Error Interrupt
0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit(2)
1 = Enable EWMARK Interrupt
0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit(2)
1 = Enable FWMARK Interrupt
0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit(2)
1 = Enable RXDONE Interrupt
0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit(2)
1 = Enable PKTPEND Interrupt
0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit
1 = Enable RXACT Interrupt
0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit(1)
1 = Enable TXDONE Interrupt
0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit(1)
1 = Enable TXABORT Interrupt
0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit(2)
1 = Enable RXBUFNA Interrupt
0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit(2)
1 = Enable RXOVFLW Interrupt
0 = Disable RXOVFLW Interrupt

**Note 1:** This bit is only used for TX operations.
**2:** This bit is only used for RX operations.


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**REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | TXBUSE | RXBUSE | — | — | — | EWMARK | FWMARK |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXDONE | PKTPEND | RXACT | — | TXDONE | TXABORT | RXBUFNA | RXOVFLW |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the TX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVCI Bus Error Interrupt bit

1 = BVCI Bus Error has occurred
0 = BVCI Bus Error has not occurred

This bit is set when the RX DMA encounters a BVCI Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit

1 = Empty Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit

1 = Full Watermark pointer reached
0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 7 **RXDONE:** Receive Done Interrupt bit

1 = RX packet was successfully received
0 = No interrupt pending

This bit is set whenever an RX packet is successfully received. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

**Note:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER**

bit 6 **PKTPEND:** Packet Pending Interrupt bit

1 = RX packet pending in memory
0 = RX packet is not pending in memory

This bit is set when the BUFCNT counter has a value other than '0'. It is cleared by either a Reset or by writing the BUFCDEC bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

bit 5 **RXACT:** Receive Activity Interrupt bit

1 = RX packet data was successfully received
0 = No interrupt pending

This bit is set whenever RX packet data is stored in the RXBM FIFO. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONE:** Transmit Done Interrupt bit

1 = TX packet was successfully sent
0 = No interrupt pending

This bit is set when the currently transmitted TX packet completes transmission, and the Transmit Status Vector is loaded into the first descriptor used for the packet. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 2 **TXABORT:** Transmit Abort Condition Interrupt bit

1 = TX abort condition occurred on the last TX packet
0 = No interrupt pending

This bit is set when the MAC aborts the transmission of a TX packet for one of the following reasons:

- Jumbo TX packet abort
- Underrun abort
- Excessive defer abort
- Late collision abort
- Excessive collisions abort

This bit is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 1 **RXBUFNA:** Receive Buffer Not Available Interrupt bit

1 = RX Buffer Descriptor Not Available condition has occurred
0 = No interrupt pending

This bit is set by a RX Buffer Descriptor Overrun condition. It is cleared by either a Reset or a CPU write of a '1' to the CLR register.

bit 0 **RXOVFLW:** Receive FIFO Over Flow Error bit

1 = RX FIFO Overflow Error condition has occurred
0 = No interrupt pending

RXOVFLW is set by the RXBM Logic for an RX FIFO Overflow condition. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

**Note:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.


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**REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | BUFCNT<7:0> | | | | | | | |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ETHBUSY(1) | TXBUSY(2) | RXBUSY(2) | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

**Note:** BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit(1)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

bit 6 **TXBUSY:** Transmit Busy bit(2)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

**Note 1:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

**2:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

**REGISTER 25-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)**

bit 5 **RXBUSY:** Receive Busy bit(2)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

**Note 1:** This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

**2:** This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.


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**REGISTER 25-16: ETHRXOVFLOW: ETHERNET CONTROLLER RECEIVE OVERFLOW STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXOVFLWCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | RXOVFLWCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **RXOVFLWCNT<15:0>:** Dropped Receive Frames Count bits

Increment counter for frames accepted by the RX filter and subsequently dropped due to internal receive error (RXFIFO overrun). This event also sets the RXOVFLW bit (ETHIRQ<0>) interrupt flag.

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-17: ETHFRMTXOK: ETHERNET CONTROLLER FRAMES TRANSMITTED OK STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMTXOKCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMTXOKCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMTXOKCNT<15:0>:** Frame Transmitted OK Count bits
Increment counter for frames successfully transmitted.

**Note 1:** This register is only used for TX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.


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**REGISTER 25-18: ETHSCOLFRM: ETHERNET CONTROLLER SINGLE COLLISION FRAMES STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SCOLFRMCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SCOLFRMCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **SCOLFRMCNT<15:0>:** Single Collision Frame Count bits
Increment count for frames that were successfully transmitted on the second try.

**Note 1:** This register is only used for TX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MCOLFRMCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MCOLFRMCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

**Note 1:** This register is only used for TX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.


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**REGISTER 25-20: ETHFRMRXOK: ETHERNET CONTROLLER FRAMES RECEIVED OK STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMRXOKCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FRMRXOKCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FRMRXOKCNT<15:0>:** Frames Received OK Count bits

Increment count for frames received successfully by the RX Filter. This count will not be incremented if there is a Frame Check Sequence (FCS) or Alignment error.

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

**REGISTER 25-21: ETHFCSERR: ETHERNET CONTROLLER FRAME CHECK SEQUENCE ERROR STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FCSERRCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | FCSERRCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **FCSERRCNT<15:0>:** FCS Error Count bits
Increment count for frames received with FCS error and the frame length in bits is an integral multiple of 8 bits.

**Note 1:** This register is only used for RX operations.
**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.
**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.


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**REGISTER 25-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALGNERRCNT<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ALGNERRCNT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

**Note 1:** This register is only used for RX operations.

**2:** This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

**3:** It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

**REGISTER 25-23: EMAC1CFG1: ETHERNET CONTROLLER MAC CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-1 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SOFT RESET | SIM RESET | — | — | RESET RMCS | RESET RFUN | RESET TMCS | RESET TFUN |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 |
| | — | — | — | LOOPBACK | TX PAUSE | RX PAUSE | PASSALL | RX ENABLE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SOFTRESET:** Soft Reset bit
Setting this bit will put the MACMII in reset. Its default value is '1'.

bit 14 **SIMRESET:** Simulation Reset bit
Setting this bit will cause a reset to the random number generator within the Transmit Function.

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMCS:** Reset MCS/RX bit
Setting this bit will put the MAC Control Sub-layer/Receive domain logic in reset.

bit 10 **RESETRFUN:** Reset RX Function bit
Setting this bit will put the MAC Receive function logic in reset.

bit 9 **RESETTMCS:** Reset MCS/TX bit
Setting this bit will put the MAC Control Sub-layer/TX domain logic in reset.

bit 8 **RESETTFUN:** Reset TX Function bit
Setting this bit will put the MAC Transmit function logic in reset.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **LOOPBACK:** MAC Loopback mode bit
1 = MAC Transmit interface is loop backed to the MAC Receive interface
0 = MAC normal operation

bit 3 **TXPAUSE:** MAC TX Flow Control bit
1 = PAUSE Flow Control frames are allowed to be transmitted
0 = PAUSE Flow Control frames are blocked

bit 2 **RXPAUSE:** MAC RX Flow Control bit
1 = The MAC acts upon received PAUSE Flow Control frames
0 = Received PAUSE Flow Control frames are ignored

bit 1 **PASSALL:** MAC Pass all Receive Frames bit
1 = The MAC will accept all frames regardless of type (Normal vs. Control)
0 = The received Control frames are ignored

bit 0 **RXENABLE:** MAC Receive Enable bit
1 = Enable the MAC receiving of frames
0 = Disable the MAC receiving of frames

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 25/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | EXCESS DFR | BPNOBK OFF | NOBK OFF | — | — | LONGPRE | PUREPRE |
| 7:0 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| | AUTO PAD(1,2) | VLAN PAD(1,2) | PAD ENABLE(1,3) | CRC ENABLE | DELAYCRC | HUGEFRM | LENGTHCK | FULLDPLX |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **EXCESSDER:** Excess Defer bit
1 = The MAC will defer to carrier indefinitely as per the Standard
0 = The MAC will abort when the excessive deferral limit is reached

bit 13 **BPNOBKOFF:** Backpressure/No Backoff bit
1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent
0 = The MAC will not remove the backoff

bit 12 **NOBKOFF:** No Backoff bit
1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Back-off algorithm as specified in the Standard
0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **LONGPRE:** Long Preamble Enforcement bit
1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length
0 = The MAC allows any length preamble as per the Standard

bit 8 **PUREPRE:** Pure Preamble Enforcement bit
1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded
0 = The MAC does not perform any preamble checking

bit 7 **AUTOPAD:** Automatic Detect Pad Enable bit(1,2)
1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly
0 = The MAC does not perform automatic detection

**Note 1:** Table 25-6 provides a description of the pad function based on the configuration of this register.
**2:** This bit is ignored if the PADENABLE bit is cleared.
**3:** This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

**REGISTER 25-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER**

bit 6 **VLANPAD:** VLAN Pad Enable bit(1,2)
1 = The MAC will pad all short frames to 64 bytes and append a valid CRC
0 = The MAC does not perform padding of short frames

bit 5 **PADENABLE:** Pad/CRC Enable bit(1,3)
1 = The MAC will pad all short frames
0 = The frames presented to the MAC have a valid length

bit 4 **CRCENABLE:** CRC Enable1 bit
1 = The MAC will append a CRC to every frame whether padding was required or not. Must be set if the PADENABLE bit is set.
0 = The frames presented to the MAC have a valid CRC

bit 3 **DELAYCRC:** Delayed CRC bit
This bit determines the number of bytes, if any, of proprietary header information that exist on the front of the IEEE 802.3 frames.
1 = Four bytes of header (ignored by the CRC function)
0 = No proprietary header

bit 2 **HUGEFRM:** Huge Frame enable bit
1 = Frames of any length are transmitted and received
0 = Huge frames are not allowed for receive or transmit

bit 1 **LENGTHCK:** Frame Length checking bit
1 = Both transmit and receive frame lengths are compared to the Length/Type field. If the Length/Type field represents a length then the check is performed. Mismatches are reported on the transmit/receive statistics vector.
0 = Length/Type field check is not performed

bit 0 **FULLDPLX:** Full-Duplex Operation bit
1 = The MAC operates in Full-Duplex mode
0 = The MAC operates in Half-Duplex mode

**Note 1:** Table 25-6 provides a description of the pad function based on the configuration of this register.
**2:** This bit is ignored if the PADENABLE bit is cleared.
**3:** This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

| **Note:** | Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware |
|---|---|

**TABLE 25-6: PAD OPERATION**

| Type | AUTOPAD | VLANPAD | PADENABLE | Action |
|---|---|---|---|---|
| Any | x | x | 0 | No pad, check CRC |
| Any | 0 | 0 | 1 | Pad to 60 Bytes, append CRC |
| Any | x | 1 | 1 | Pad to 64 Bytes, append CRC |
| Any | 1 | 0 | 1 | If untagged: Pad to 60 Bytes, append CRC<br>If VLAN tagged: Pad to 64 Bytes, append CRC |


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**REGISTER 25-25: EMAC1IPGT: ETHERNET CONTROLLER MAC BACK-TO-BACK INTERPACKET GAP REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| | — | B2BIPKTGP<6:0> | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-7 **Unimplemented:** Read as '0'

bit 6-0 **B2BIPKTGP<6:0>:** Back-to-Back Interpacket Gap bits

This is a programmable field representing the nibble time offset of the minimum possible period between the end of any transmitted packet, to the beginning of the next. In Full-Duplex mode, the register value should be the desired period in nibble times minus 3. In Half-Duplex mode, the register value should be the desired period in nibble times minus 6. In Full-Duplex the recommended setting is 0x15 (21d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps). In Half-Duplex mode, the recommended setting is 0x12 (18d), which also represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-26: EMAC1IPGR: ETHERNET CONTROLLER MAC NON-BACK-TO-BACK INTERPACKET GAP REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
| | — | NB2BIPKTGP1<6:0> | | | | | | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| | — | NB2BIPKTGP2<6:0> | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **NB2BIPKTGP1<6:0>:** Non-Back-to-Back Interpacket Gap Part 1 bits

This is a programmable field representing the optional carrierSense window referenced in section 4.2.3.2.1 "Deference" of the IEEE 80.23 Specification. If the carrier is detected during the timing of IPGR1, the MAC defers to the carrier. If, however, the carrier comes after IPGR1, the MAC continues timing IPGR2 and transmits, knowingly causing a collision, thus ensuring fair access to the medium. Its range of values is 0x0 to IPGR2. Its recommend value is 0xC (12d).

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **NB2BIPKTGP2<6:0>:** Non-Back-to-Back Interpacket Gap Part 2 bits

This is a programmable field representing the non-back-to-back Inter-Packet-Gap. Its recommended value is 0x12 (18d), which represents the minimum IPG of 0.96 µs (in 100 Mbps) or 9.6 µs (in 10 Mbps).

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-27: EMAC1CLRT: ETHERNET CONTROLLER MAC COLLISION WINDOW/RETRY LIMIT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | CWINDOW<5:0> | | | | | |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
| | — | — | — | — | RETX<3:0> | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13-8 **CWINDOW<5:0>:** Collision Window bits

This is a programmable field representing the slot time or collision window during which collisions occur in properly configured networks. Since the collision window starts at the beginning of transmission, the preamble and SFD is included. Its default of 0x37 (55d) corresponds to the count of frame bytes at the end of the window.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **RETX<3:0>:** Retransmission Maximum bits

This is a programmable field specifying the number of retransmission attempts following a collision before aborting the packet due to excessive collisions. The Standard specifies the maximum number of attempts (attemptLimit) to be 0xF (15d). Its default is '0xF'.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |
| | MACMAXF<15:8>(1) | | | | | | | |
| 7:0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-0 |
| | MACMAXF<7:0>(1) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits(1)

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

**Note 1:** If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
| | — | — | — | — | RESETRMII(1) | — | — | SPEEDRMII(1) |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is only used for the RMII module.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-30: EMAC1TEST: ETHERNET CONTROLLER MAC TEST REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | TESTBP | TESTPAUSE(1) | SHRTQNTA(1) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-3 **Unimplemented:** Read as '0'

bit 2 **TESTBP:** Test Backpressure bit

1 = The MAC will assert backpressure on the link. Backpressure causes preamble to be transmitted, raising carrier sense. A transmit packet from the system will be sent during backpressure.

0 = Normal operation

bit 1 **TESTPAUSE:** Test PAUSE bit(1)

1 = The MAC Control sub-layer will inhibit transmissions, just as if a PAUSE Receive Control frame with a non-zero pause time parameter was received

0 = Normal operation

bit 0 **SHRTQNTA:** Shortcut PAUSE Quanta bit(1)

1 = The MAC reduces the effective PAUSE Quanta from 64 byte-times to 1 byte-time

0 = Normal operation

**Note 1:** This bit is only for testing purposes.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | RESETMGMT | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | CLKSEL<3:0>(1) | | | | NOPRE | SCANINC |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits(1)
These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

**Note 1:** Table 25-7 provides a description of the clock divider encoding.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**TABLE 25-7: MIIM CLOCK SELECTION**

| MIIM Clock Select | EMAC1MCFG<5:2> |
|---|---|
| SYSCLK divided by 4 | 000x |
| SYSCLK divided by 6 | 0010 |
| SYSCLK divided by 8 | 0011 |
| SYSCLK divided by 10 | 0100 |
| SYSCLK divided by 14 | 0101 |
| SYSCLK divided by 20 | 0110 |
| SYSCLK divided by 28 | 0111 |
| SYSCLK divided by 40 | 1000 |
| Undefined | Any other combination |

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**REGISTER 25-32: EMAC1MCMD: ETHERNET CONTROLLER MAC MII MANAGEMENT COMMAND REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | SCAN | READ |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-2 **Unimplemented:** Read as '0'

bit 1 **SCAN:** MII Management Scan Mode bit
1 = The MII Management module will perform read cycles continuously (for example, useful for monitoring the Link Fail)
0 = Normal Operation

bit 0 **READ:** MII Management Read Command bit
1 = The MII Management module will perform a single read cycle. The read data is returned in the EMAC1MRDD register
0 = The MII Management module will perform a write cycle. The write data is taken from the EMAC1MWTD register

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-33: EMAC1MADR: ETHERNET CONTROLLER MAC MII MANAGEMENT ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
| | — | — | — | PHYADDR<4:0> | | | | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | REGADDR<4:0> | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-13 **Unimplemented:** Read as '0'

bit 12-8 **PHYADDR<4:0>:** MII Management PHY Address bits

This field represents the 5-bit PHY Address field of Management cycles. Up to 31 PHYs can be addressed (0 is reserved).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **REGADDR<4:0>:** MII Management Register Address bits

This field represents the 5-bit Register Address field of Management cycles. Up to 32 registers can be accessed.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-34: EMAC1MWTD: ETHERNET CONTROLLER MAC MII MANAGEMENT WRITE DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MWTD<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MWTD<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MWTD<15:0>:** MII Management Write Data bits
When written, a MII Management write cycle is performed using the 16-bit data and the pre-configured PHY and Register addresses from the EMAC1MADR register.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-35: EMAC1MRDD: ETHERNET CONTROLLER MAC MII MANAGEMENT READ DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MRDD<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | MRDD<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MRDD<15:0>:** MII Management Read Data bits
Following a MII Management Read Cycle, the 16-bit data can be read from this location.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.


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**REGISTER 25-36: EMAC1MIND: ETHERNET CONTROLLER MAC MII MANAGEMENT INDICATORS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | LINKFAIL | NOTVALID | SCAN | MIIMBUSY |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **LINKFAIL:** Link Fail bit

When '1' is returned - indicates link fail has occurred. This bit reflects the value last read from the PHY status register.

bit 2 **NOTVALID:** MII Management Read Data Not Valid bit

When '1' is returned - indicates an MII management read cycle has not completed and the Read Data is not yet valid.

bit 1 **SCAN:** MII Management Scanning bit

When '1' is returned - indicates a scan operation (continuous MII Management Read cycles) is in progress.

bit 0 **MIIMBUSY:** MII Management Busy bit

When '1' is returned - indicates MII Management module is currently performing an MII Management Read or Write cycle.

**Note:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**REGISTER 25-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR6<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR5<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.


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**REGISTER 25-38: EMAC1SA1: ETHERNET CONTROLLER MAC STATION ADDRESS 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR4<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR3<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR4<7:0>:** Station Address Octet 4 bits
These bits hold the fourth transmitted octet of the station address.

bit 7-0 **STNADDR3<7:0>:** Station Address Octet 3 bits
These bits hold the third transmitted octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.

**REGISTER 25-39: EMAC1SA2: ETHERNET CONTROLLER MAC STATION ADDRESS 2 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR2<7:0> | | | | | | | |
| 7:0 | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P | R/W-P |
| | STNADDR1<7:0> | | | | | | | |

| **Legend:** | | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Reserved:** Maintain as '0'; ignore read

bit 15-8 **STNADDR2<7:0>:** Station Address Octet 2 bits
These bits hold the second transmitted octet of the station address.

bit 7-0 **STNADDR1<7:0>:** Station Address Octet 1 bits
These bits hold the most significant (first transmitted) octet of the station address.

**Note 1:** Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

**2:** This register is loaded at reset from the factory preprogrammed station address.


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## 26.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

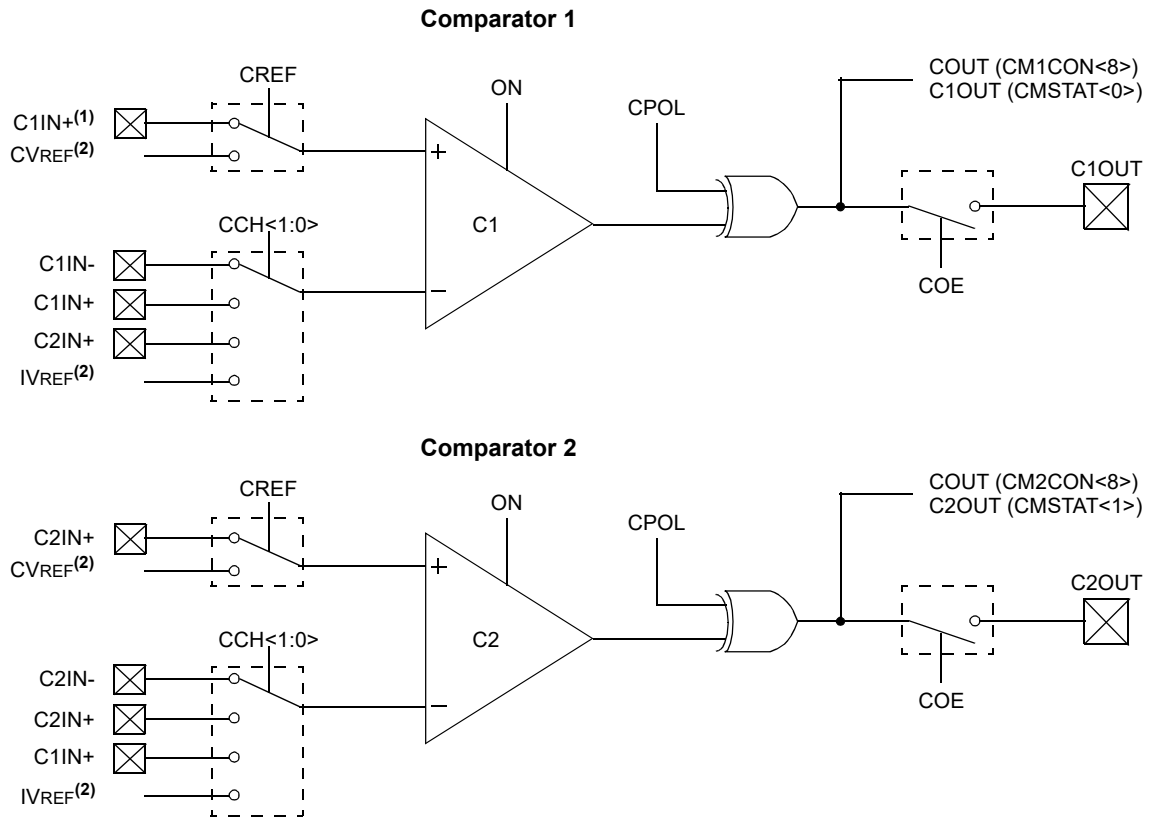
The Comparator module contains two comparators that can be configured in a variety of ways.

Key features of the Comparator module include:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be inverted
- Selectable interrupt generation

A block diagram of the Comparator module is illustrated in Figure 26-1.

**FIGURE 26-1: COMPARATOR MODULE BLOCK DIAGRAM**




**Note 1:** On devices with a USB module, and when the module is enabled, this pin is controlled by the USB module, and therefore, is not available as a comparator input.

**2:** Internally connected. See **Section 27.0 "Comparator Voltage Reference (CVREF)"**.

## 26.1 Control Registers

**TABLE 26-1: COMPARATOR REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| A000 | CM1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | — | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 00C3 |
| A010 | CM2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | COE | CPOL | — | — | — | — | COUT | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | | 00C3 |
| A060 | CMSTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | C2OUT | C1OUT | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.



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**REGISTER 26-1: CMxCON: COMPARATOR 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R-0 |
| | ON(1) | COE | CPOL(2) | — | — | — | — | COUT |
| 7:0 | R/W-1 | R/W-1 | U-0 | R/W-0 | U-0 | U-0 | R/W-1 | R/W-1 |
| | EVPOL<1:0> | | — | CREF | — | — | CCH<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit(1)

Clearing this bit does not affect the other bits in this register.

1 = Module is enabled. Setting this bit does not affect the other bits in this register
0 = Module is disabled and does not consume current.

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin
0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit(2)

1 = Output is inverted
0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'
0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal $CV_{REF}$
0 = Comparator non-inverting input is connected to the CxIN+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the $IV_{REF}$
10 = Comparator inverting input is connected to the C2IN+ pin for C1 and C1IN+ pin for C2
01 = Comparator inverting input is connected to the C1IN+ pin for C1 and C2IN+ pin for C2
00 = Comparator inverting input is connected to the C1IN- pin for C1 and C2IN- pin for C2

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

**REGISTER 26-2: CMSTAT: COMPARATOR STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R-0 | R-0 |
| | — | — | — | — | — | — | C2OUT | C1OUT |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = All Comparator modules are disabled while in Idle mode
- 0 = All Comparator modules continue to operate while in Idle mode

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'


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## 27.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference (CVREF)"** (DS60001109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

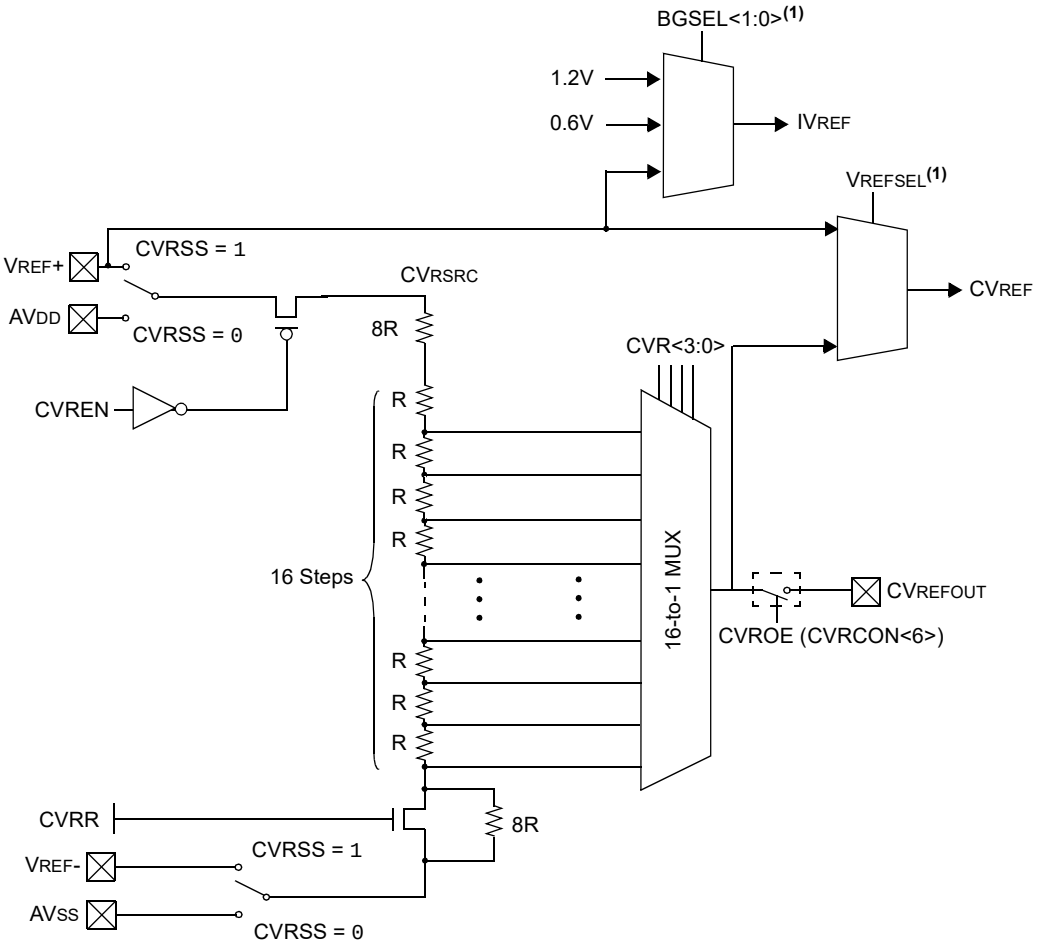
The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 27-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

Key features of the CVREF module include:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

**FIGURE 27-1: COMPARATOR VOLTAGE REFERENCE MODULE BLOCK DIAGRAM**




**Note 1:** This bit is not available on PIC32MX575/675/695/775/795 devices. On these devices CVREF is generated by the Register network and IVREF is connected to 0.6V.

## 27.1 Control Register

**TABLE 27-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 9800 | CVRCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | — | — | VREFSEL(2) | BGSEL<1:0>(2) | | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | | 0100 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.1.1 "CLR, SET and INV Registers"** for more information.

**2:** These bits are not available on PIC32MX575/675/695/775/795 devices. On these devices, reset value for CVRCON is '0000'.



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**REGISTER 27-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-1 |
| | ON(1) | — | — | — | — | VREFSEL(2) | BGSEL<1:0>(2) | |
| 7:0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | CVROE | CVRR | CVRSS | CVR<3:0> | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Voltage Reference On bit(1)
Setting or clearing this bit does not affect the other bits in this register.
1 = Module is enabled
0 = Module is disabled and does not consume current

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Voltage Reference Select bit(2)
1 = CVREF = VREF+
0 = CVREF is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source bits(2)
11 = IVREF = VREF+
10 = Reserved
01 = IVREF = 0.6V (nominal, default)
00 = IVREF = 1.2V (nominal)

bit 7 **Unimplemented:** Read as '0'

bit 6 **CVROE:** CVREFOUT Enable bit
1 = Voltage level is output on CVREFOUT pin
0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit
1 = 0 to 0.625 CVRSRC, with CVRSRC/24 step size
0 = 0.25 CVRSRC to 0.719 CVRSRC, with CVRSRC/32 step size

bit 4 **CVRSS:** CVREF Source Selection bit
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (VREF-)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR<3:0>:** CVREF Value Selection 0 ≤ CVR<3:0> ≤ 15 bits
When CVRR = 1:
CVREF = (CVR<3:0>/24) • (CVRSRC)
When CVRR = 0:
CVREF = 1/4 • (CVRSRC) + (CVR<3:0>/32) • (CVRSRC)

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** These bits are not available on PIC32MX575/675/775/795 devices. On these devices, the reset value for CVRON is '0000'.

**NOTES:**


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## 28.0 POWER-SAVING FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This section describes power-saving features for the PIC32MX5XX/6XX/7XX family of devices. These devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

## 28.1 Power-Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the Peripheral Bus Clock (PBCLK) and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers.
- LPRC Run mode: the CPU is clocked from the LPRC clock source.
- SOSC Run mode: the CPU is clocked from the SOSC clock source.

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

## 28.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as listed below:

- **Posc Idle mode:** the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- **FRC Idle mode:** the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- **Sosc Idle mode:** the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- **LPRC Idle mode:** the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- **Sleep mode:** the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

## 28.3 Power-Saving Operation

Peripherals and the CPU can be halted or disabled to further reduce power consumption.

### 28.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 28.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit, if enabled, remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

The processor will exit, or 'wake-up', from Sleep mode on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep mode. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 28.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

**Note 1:** Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

**2:** Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

### 28.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus (PB) can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as USB, interrupt controller, DMA, bus matrix and prefetch cache are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.


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## 29.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the PIC32MX5XX/6XX/7XX family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. "Programming and Diagnostics"** (DS60001129) in the *"PIC32 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com/PIC32).

The PIC32MX5XX/6XX/7XX family of devices include several features intended to maximize application flexibility and reliability and minimize cost through elimination of external components. Key features include:

- Flexible device configuration
- Watchdog Timer (WDT)
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming™ (ICSP™)

### 29.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- DEVID: Device and Revision ID Register

## TABLE 29-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

| Virtual Address (BFC0_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2FF0 | DEVCFG3 | 31:16 | FVBUSONIO | FUSBIDIO | — | — | — | FCANIO | FETHIO | FMIIEN | — | — | — | — | — | FSRSSEL<2:0> | | | xxxx |
| | | 15:0 | USERID<15:0> | | | | | | | | | | | | | | | | xxxx |
| 2FF4 | DEVCFG2 | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | FPLLODIV<2:0> | | | xxxx |
| | | 15:0 | UPLLEN | — | — | — | — | UPLLIDIV<2:0> | | | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | | xxxx |
| 2FF8 | DEVCFG1 | 31:16 | — | — | — | — | — | — | — | — | FWDTEN | — | — | WDTPS<4:0> | | | | | xxxx |
| | | 15:0 | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | | xxxx |
| 2FFC | DEVCFG0 | 31:16 | — | — | — | CP | — | — | — | BWP | — | — | — | — | PWP<7:4> | | | | xxxx |
| | | 15:0 | PWP<3:0> | | | | — | — | — | — | — | — | — | — | ICESEL | — | DEBUG<1:0> | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 29-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F200 | DDPCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | JTAGEN | TROEN | — | TDOEN | 0008 |
| F220 | DEVID | 31:16 | VER<3:0> | | | | DEVID<27:16> | | | | | | | | | | | | xxxx |
| | | 15:0 | DEVID<15:0> | | | | | | | | | | | | | | | | xxxx |
| F230 | SYSKEY | 31:16 | SYSKEY<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Reset values are dependent on the device variant. Refer to *"PIC32MX5XX/6XX/7XX Family Silicon Errata and Data Sheet Clarification"* (DS80000480) for more information.



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**REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-0 | r-1 | r-1 | R/P | r-1 | r-1 | r-1 | R/P |
| | — | — | — | CP | — | — | — | BWP |
| 23:16 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P |
| | — | — | — | — | PWP<7:4> | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | r-1 | r-1 | r-1 |
| | PWP<3:0> | | | | — | — | — | — |
| 7:0 | r-1 | r-1 | r-1 | r-1 | R/P | r-1 | R/P | R/P |
| | — | — | — | — | ICESEL | — | DEBUG<1:0> | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **Reserved:** Write '0'

bit 30-29 **Reserved:** Write '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-25 **Reserved:** Write '1'

bit 24 **BWP:** Boot Flash Write-Protect bit

Prevents boot Flash memory from being modified during code execution.
1 = Boot Flash is writable
0 = Boot Flash is not writable

bit 23-20 **Reserved:** Write '1'

bit 19-12 **PWP<7:0>:** Program Flash Write-Protect bits

Prevents selected program Flash memory pages from being modified during code execution. The PWP bits represent the 1's complement of the number of write-protected program Flash memory pages.
11111111 = Disabled
11111110 = 0xBD00_0FFF
11111101 = 0xBD00_1FFF
11111100 = 0xBD00_2FFF
11111011 = 0xBD00_3FFF
11111010 = 0xBD00_4FFF
11111001 = 0xBD00_5FFF
11111000 = 0xBD00_6FFF
11110111 = 0xBD00_7FFF
11110110 = 0xBD00_8FFF
11110101 = 0xBD00_9FFF
11110100 = 0xBD00_AFFF
11110011 = 0xBD00_BFFF
11110010 = 0xBD00_CFFF
11110001 = 0xBD00_DFFF
11110000 = 0xBD00_EFFF
11101111 = 0xBD00_FFFF
•
•
•
01111111 = 0xBD07_FFFF

bit 11-4 **Reserved:** Write '1'

**REGISTER 29-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)**

bit 3 **ICESEL:** In-Circuit Emulator/Debugger Communication Channel Select bit
1 = PGEC2/PGED2 pair is used
0 = PGEC1/PGED1 pair is used

bit 2 **Reserved:** Write '1'

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
11 = Debugger is disabled
10 = Debugger is enabled
01 = Reserved (same as '11' setting)
00 = Reserved (same as '11' setting)


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**REGISTER 29-2: DEVCFG1: DEVICE CONFIGURATION WORD 1**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | R/P | r-1 | r-1 | R/P | R/P | R/P | R/P | R/P |
| | FWDTEN | — | — | WDTPS<4:0> | | | | |
| 15:8 | R/P | R/P | R/P | R/P | r-1 | R/P | R/P | R/P |
| | FCKSM<1:0> | | FPBDIV<1:0> | | — | OSCIOFNC | POSCMOD<1:0> | |
| 7:0 | R/P | r-1 | R/P | r-1 | r-1 | R/P | R/P | R/P |
| | IESO | — | FSOSCEN | — | — | FNOSC<2:0> | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-24 **Reserved:** Write '1'

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = The WDT is enabled and cannot be disabled by software
0 = The WDT is not enabled; it can be enabled in software

bit 22-21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>:** Watchdog Timer Postscale Select bits
10100 = 1:1048576
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1
All other combinations not shown result in operation = 10100

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

**Note 1:** Do not disable the POSC (POSCMOD = 11) when using this oscillator source.

**REGISTER 29-2: DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)**

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits
11 = PBCLK is SYSCLK divided by 8
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '1'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit
1 = CLKO output is disabled
0 = CLKO output signal is active on the OSCO pin; the Primary Oscillator must be disabled or configured for External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = 11 or 00)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits
11 = Primary Oscillator is disabled
10 = HS Oscillator mode is selected
01 = XT Oscillator mode is selected
00 = External Clock mode is selected

bit 7 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
0 = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved:** Write '1'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit
1 = Enable the Secondary Oscillator
0 = Disable the Secondary Oscillator

bit 4-3 **Reserved:** Write '1'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
111 = Fast RC Oscillator with divide-by-N (FRCDIV)
110 = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator (POSC) with PLL module (XT+PLL, HS+PLL, EC+PLL)
010 = Primary Oscillator (XT, HS, EC)(1)
001 = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
000 = Fast RC Oscillator (FRC)

**Note 1:** Do not disable the POSC (POSCMOD = 11) when using this oscillator source.


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**REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | FPLLODIV<2:0> | | |
| 15:8 | R/P | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | UPLLEN | — | — | — | — | UPLLIDIV<2:0> | | |
| 7:0 | r-1 | R/P-1 | R/P | R/P-1 | r-1 | R/P | R/P | R/P |
| | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** PLL Output Divider bits
111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit
1 = Disable and bypass USB PLL
0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Divider bits
111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
111 = 24x multiplier
110 = 21x multiplier
101 = 20x multiplier
100 = 19x multiplier
011 = 18x multiplier
010 = 17x multiplier
001 = 16x multiplier
000 = 15x multiplier

bit 3 **Reserved:** Write '1'

**REGISTER 29-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)**

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
111 = 12x divider
110 = 10x divider
101 = 6x divider
100 = 5x divider
011 = 4x divider
010 = 3x divider
001 = 2x divider
000 = 1x divider


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**REGISTER 29-4: DEVCFG3: DEVICE CONFIGURATION WORD 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/P | R/P | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | FVBUSONIO | FUSBIDIO | — | — | — | FCANIO(1) | FETHIO(2) | FMIIEN(2) |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | FSRSSEL<2:0> | | |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<15:8> | | | | | | | |
| 7:0 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<7:0> | | | | | | | |

| Legend: | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FVBUSONIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29-27 **Reserved:** Write '1'

bit 26 **FCANIO:** CAN I/O Pin Selection bit(1)
1 = Default CAN I/O Pins
0 = Alternate CAN I/O Pins

bit 25 **FETHIO:** Ethernet I/O Pin Selection bit(2)
1 = Default Ethernet I/O Pins
0 = Alternate Ethernet I/O Pins

bit 24 **FMIIEN:** Ethernet MII Enable bit(2)
1 = MII is enabled
0 = RMII is enabled

bit 23-19 **Reserved:** Write '1'

bit 18-16 **FSRSSEL<2:0>:** SRS Select bits
111 = Assign Interrupt Priority 7 to a shadow register set
110 = Assign Interrupt Priority 6 to a shadow register set
•
•
•
001 = Assign Interrupt Priority 1 to a shadow register set
000 = All interrupt priorities are assigned to a shadow register set

bit 15-0 **USERID<15:0>:** User ID bits
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

**Note 1:** This bit is Reserved and reads '1' on PIC32MX664/675/695 devices.
**2:** This bit is Reserved and reads '1' on PIC32MX534/564/575 devices.

**REGISTER 29-5: DEVID: DEVICE AND REVISION ID REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | VER<3:0>(1) | | | | DEVID<27:24>(1) | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | DEVID<23:16>(1) | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | DEVID<15:8>(1) | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | DEVID<7:0>(1) | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

**Note 1:** See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

**REGISTER 29-6: DDPCON: DEBUG DATA PORT CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | U-0 | U-0 | U-0 | U-0 | R/W-1 | R/W-0 | U-0 | R/W-0 |
| | — | — | — | — | JTAGEN | TROEN | — | TDOEN |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Port Enable bit
- 1 = Enable the JTAG port
- 0 = Disable the JTAG port

bit 2 **TROEN:** Trace Output Enable bit
- 1 = Enable the trace port
- 0 = Disable the trace port

bit 1 **Unimplemented:** Read as '0'

bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG
- 1 = 2-wire JTAG protocol uses TDO
- 0 = 2-wire JTAG protocol does not use TDO


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## 29.2 On-Chip Voltage Regulator

All PIC32MX5XX/6XX/7XX devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX-5XX/6XX/7XX family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 29-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 32.1 "DC Characteristics"**.

| **Note:** | It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin. |
|---|---|

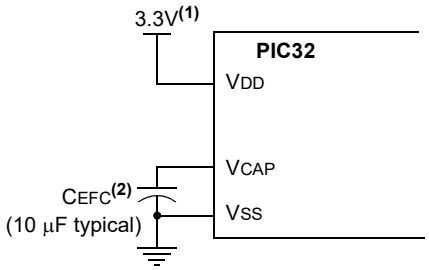
### 29.2.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

### 29.2.2 ON-CHIP REGULATOR AND BOR

PIC32MX5XX/6XX/7XX devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset (BOR). This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specified in **Section 32.1 "DC Characteristics"**.

**FIGURE 29-1: CONNECTIONS FOR THE ON-CHIP REGULATOR**




**Note 1:** These are typical operating voltages. Refer to **Section 32.1 "DC Characteristics"** for the full operating ranges of VDD.

**2:** It is important that the low-ESR capacitor is placed as close as possible to the VCAP pin.

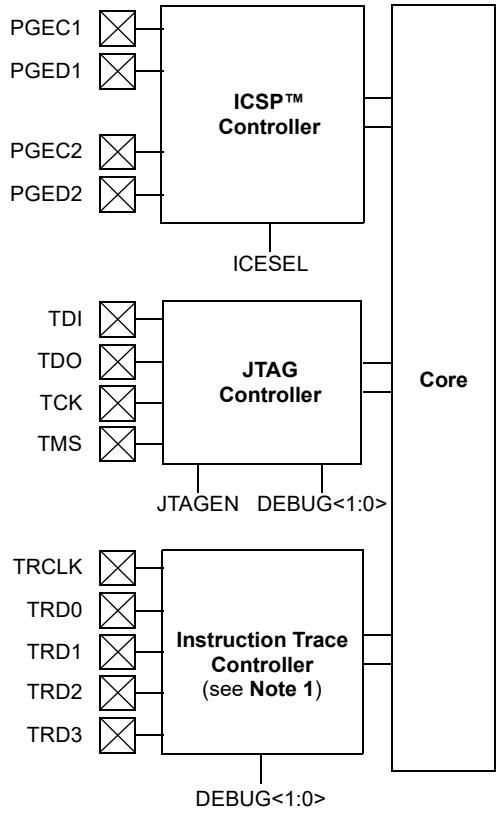
## 29.3 Programming and Diagnostics

PIC32MX5XX/6XX/7XX devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

**FIGURE 29-2: PROGRAMMING, DEBUGGING, AND TRACE PORTS BLOCK DIAGRAM**




**Note 1:** Trace is not available on 64-pin devices.

**NOTES:**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## 30.0 INSTRUCTION SET

The PIC32MX5XX/6XX/7XX family instruction set complies with the MIPS32 Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core Extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

**Note:** Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

**NOTES:**


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## 31.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

### 31.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

## 31.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

## 31.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

## 31.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 31.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility


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## 31.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 31.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 31.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 31.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

## 31.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

## 31.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 31.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®


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## 32.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX5XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX5XX/6XX/7XX devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

**(See Note 1)**

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$ **(Note 3)** ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on $V_{BUS}$ with respect to $V_{SS}$ ..... -0.3V to +5.5V
Maximum current out of $V_{SS}$ pin(s) ..... 300 mA
Maximum current into $V_{DD}$ pin(s) **(Note 2)** ..... 300 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports **(Note 2)** ..... 200 mA

**Note 1:** Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 32-2).

**3:** See the **"Device Pin Tables"** section for the 5V tolerant pins.

## 32.1 DC Characteristics

**TABLE 32-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts)(1) | Temp. Range (in °C) | Max. Frequency |
|---|---|---|---|
| | | | PIC32MX5XX/6XX/7XX |
| DC5 | 2.3-3.6V | -40°C to +85°C | 80 MHz |
| DC5b | 2.3-3.6V | -40°C to +105°C | 80 MHz |

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 32-10 for BOR values.

**TABLE 32-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| **Industrial Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| **V-Temp Temperature Devices** | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +105 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>PINT = VDD x (IDD – S IOH)<br>I/O Pin Power Dissipation:<br>I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL)) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 32-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristics | Symbol | Typical | Max. | Unit | See Note |
|---|---|---|---|---|---|
| Package Thermal Resistance, 121-Pin TFBGA (10x10x1.1 mm) | θJA | 40 | — | °C/W | 1 |
| Package Thermal Resistance, 100-Pin TQFP (14x14x1 mm) | θJA | 43 | — | °C/W | 1 |
| Package Thermal Resistance, 100-Pin TQFP (12x12x1 mm) | θJA | 43 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin TQFP (10x10x1 mm) | θJA | 47 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin QFN (9x9x0.9 mm) | θJA | 28 | — | °C/W | 1 |
| Package Thermal Resistance, 124-Pin VTLA (9x9x0.9 mm) | θJA | 21 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.


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**TABLE 32-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage** | 2.3 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage**(1) | 1.75 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | 1.75 | — | 2.1 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.00005 | — | 0.115 | V/μs | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 32-10 for BOR values.

**TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | | | |
| **Operating Current (IDD)(1,2,4) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | | |
| DC20 | 6 | 9 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC20b | 7 | 10 | | | +105ºC | | |
| DC20a | 4 | — | | Code executing from SRAM | — | | |
| DC21 | 37 | 40 | mA | Code executing from Flash | — | — | 25 MHz |
| DC21a | 25 | — | | Code executing from SRAM | | | |
| DC22 | 64 | 70 | mA | Code executing from Flash | — | — | 60 MHz |
| DC22a | 61 | — | | Code executing from SRAM | | | |
| DC23 | 85 | 98 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC23b | 90 | 120 | | | +105ºC | | |
| DC23a | 85 | — | | Code executing from SRAM | — | | |
| DC25a | 125 | 150 | µA | — | +25°C | 3.3V | LPRC (31 kHz) |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.


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**TABLE 32-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(3)** | **Max.** | **Units** | **Conditions** | | | |
| **Operating Current (IDD)(1,2) for PIC32MX534/564/664/764 Family Devices** | | | | | | | |
| DC20c | 6 | 9 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC20d | 7 | 10 | | | +105ºC | | |
| DC20e | 2 | — | | Code executing from SRAM | — | | |
| DC21b | 19 | 32 | mA | Code executing from Flash | — | — | 25 MHz **(Note 4)** |
| DC21c | 14 | — | | Code executing from SRAM | | | |
| DC22b | 31 | 50 | mA | Code executing from Flash | — | — | 60 MHz **(Note 4)** |
| DC22c | 29 | — | | Code executing from SRAM | | | |
| DC23c | 39 | 65 | mA | Code executing from Flash | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC23d | 49 | 70 | | | +105ºC | | |
| DC23e | 39 | — | | Code executing from SRAM | — | | |
| DC25b | 100 | 150 | µA | — | +25°C | 3.3V | LPRC (31 kHz) **(Note 4)** |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing while(1) statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

**TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(1,3) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC30 | 4.5 | 6.5 | mA | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC30b | 5 | 7 | | +105°C | | |
| DC31 | 13 | 15 | mA | -40ºC, +25ºC, +85ºC | — | 25 MHz |
| DC32 | 28 | 30 | mA | -40ºC, +25ºC, +85ºC | — | 60 MHz |
| DC33 | 36 | 42 | mA | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC33b | 39 | 45 | mA | +105°C | | |
| DC34 | — | 40 | µA | -40°C | 2.3V | LPRC (31 kHz) |
| DC34a | | 75 | | +25°C | | |
| DC34b | | 800 | | +85°C | | |
| DC34c | | 1000 | | +105°C | | |
| DC35 | 35 | — | µA | -40°C | 3.3V | |
| DC35a | 65 | | | +25°C | | |
| DC35b | 600 | | | +85°C | | |
| DC35c | 800 | | | +105°C | | |
| DC36 | — | 43 | µA | -40°C | 3.6V | |
| DC36a | | 106 | | +25°C | | |
| DC36b | | 800 | | +85°C | | |
| DC36c | | 1000 | | +105°C | | |

**Note 1:** The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.


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**TABLE 32-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(1) for PIC32MX534/564/664/764 Family Devices** | | | | | | |
| DC30a | 1.5 | 5 | mA | -40ºC, +25ºC, +85ºC | — | 4 MHz |
| DC30c | 3.5 | 6 | | +105ºC | | |
| DC31a | 7 | 11 | | -40ºC, +25ºC, +85ºC | — | 25 MHz **(Note 3)** |
| DC32a | 13 | 20 | mA | -40ºC, +25ºC, +85ºC | — | 60 MHz **(Note 3)** |
| DC33a | 17 | 25 | mA | -40ºC, +25ºC, +85ºC | — | 80 MHz |
| DC33c | 20 | 27 | | +105ºC | | |
| DC34c | — | 40 | µA | -40°C | 2.3V | LPRC (31 kHz) **(Note 3)** |
| DC34d | | 75 | | +25°C | | |
| DC34e | | 800 | | +85°C | | |
| DC34f | | 1000 | | +105ºC | | |
| DC35c | 30 | — | µA | -40°C | 3.3V | |
| DC35d | 55 | | | +25°C | | |
| DC35e | 230 | | | +85°C | | |
| DC35f | 800 | | | +105ºC | | |
| DC36c | — | 43 | µA | -40°C | 3.6V | |
| DC36d | | 106 | | +25°C | | |
| DC36e | | 800 | | +85°C | | |
| DC36f | | 1000 | | +105ºC | | |

**Note 1:** The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

**4:** All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

**TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Power-Down Current ($I_{PD}$)(1) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC40 | 10 | 40 | μA | -40°C | 2.3V | Base Power-Down Current **(Note 6)** |
| DC40a | 36 | 100 | | +25°C | | |
| DC40b | 400 | 720 | | +85°C | | |
| DC40h | 900 | 1800 | | +105°C | | |
| DC40c | 41 | 120 | | +25°C | 3.3V | Base Power-Down Current |
| DC40d | 22 | 80 | | -40°C | 3.6V | Base Power-Down Current **(Note 6)** |
| DC40e | 42 | 120 | | +25°C | | |
| DC40g | 315 | 400(5) | | +70°C | | |
| DC40f | 410 | 800 | | +85°C | | |
| DC40i | 1000 | 2000 | | +105°C | | |
| **Module Differential Current for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| DC41 | — | 10 | μA | — | 2.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Notes 3,6)** |
| DC41a | 5 | — | | | 3.3V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3)** |
| DC41b | — | 20 | | | 3.6V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3,6)** |
| DC42 | — | 40 | μA | — | 2.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Notes 3,6)** |
| DC42a | 23 | — | | | 3.3V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3)** |
| DC42b | — | 50 | | | 3.6V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3,6)** |
| DC43 | — | 1300 | μA | — | 2.5V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |
| DC43a | 1100 | — | | | 3.3V | ADC: $\Delta I_{ADC}$ **(Notes 3,4)** |
| DC43b | — | 1300 | | | 3.6V | ADC: $\Delta I_{ADC}$ **(Notes 3,4,6)** |

**Note 1:** The test conditions for $I_{PD}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.

**6:** This parameter is characterized, but not tested in manufacturing.


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**TABLE 32-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Power-Down Current (IPD)(1) for PIC32MX534/564/664/764 Family Devices** | | | | | | |
| DC40g | 12 | 40 | μA | -40°C | 2.3V | Base Power-Down Current **(Note 6)** |
| DC40h | 20 | 120 | | +25°C | | |
| DC40i | 210 | 600 | | +85°C | | |
| DC40o | 400 | 1000 | | +105°C | | |
| DC40j | 20 | 120 | | +25°C | 3.3V | Base Power-Down Current |
| DC40k | 15 | 80 | | -40°C | 3.6V | Base Power-Down Current |
| DC40l | 20 | 120 | | +25°C | | |
| DC40m | 113 | 350(5) | | +70°C | | |
| DC40n | 220 | 650 | | +85°C | | |
| DC40p | 500 | 1000 | | +105°C | | |
| **Module Differential Current for PIC32MX534/564/664/764 Family Devices** | | | | | | |
| DC41c | — | 10 | μA | — | 2.5V | Watchdog Timer Current: ΔIWDT **(Notes 3,6)** |
| DC41d | 5 | — | | | 3.3V | Watchdog Timer Current: ΔIWDT **(Note 3)** |
| DC41e | — | 20 | | | 3.6V | Watchdog Timer Current: ΔIWDT **(Note 3)** |
| DC42c | — | 40 | μA | — | 2.5V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Notes 3,6)** |
| DC42d | 23 | — | | | 3.3V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)** |
| DC42e | — | 50 | | | 3.6V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)** |
| DC43c | — | 1300 | μA | — | 2.5V | ADC: ΔIADC **(Notes 3,4,6)** |
| DC43d | 1100 | — | | | 3.3V | ADC: ΔIADC **(Notes 3,4)** |
| DC43e | — | 1300 | | | 3.6V | ADC: ΔIADC **(Notes 3,4)** |

**Note 1:** The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** Data is characterized at +70°C and not tested. Parameter is for design guidance only.

**6:** This parameter is characterized, but not tested in manufacturing.

**TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | I/O Pins: | | | | | |
| | | with TTL Buffer | VSS | — | 0.15 VDD | V | |
| | | with Schmitt Trigger Buffer | VSS | — | 0.2 VDD | V | |
| DI15 | | $\overline{MCLR}$(2) | VSS | — | 0.2 VDD | V | |
| DI16 | | OSC1 (XT mode) | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI17 | | OSC1 (HS mode) | VSS | — | 0.2 VDD | V | **(Note 4)** |
| DI18 | | SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled **(Note 4)** |
| DI19 | | SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled **(Note 4)** |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins not 5V-tolerant(5) | 0.65 VDD | — | VDD | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant with PMP(5) | 0.25 VDD + 0.8V | — | 5.5 | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant(5) | 0.65 VDD | — | 5.5 | V | |
| DI28 | | SDAx, SCLx | 0.65 VDD | — | 5.5 | V | SMBus disabled **(Note 4,6)** |
| DI29 | | SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)** |
| DI30 | ICNPU | **Change Notification Pull-up Current** | — | — | -50 | µA | VDD = 3.3V, VPIN = VSS **(Note 3,6)** |
| DI31 | ICNPD | **Change Notification Pull-down Current(4)** | — | 50 | — | µA | VDD = 3.3V, VPIN = VDD |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** See the **"Device Pin Tables"** section for the 5V-tolerant pins.

**6:** The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

**7:** VIL source < (VSS - 0.3). Characterized but not tested.

**8:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

**11:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.


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**TABLE 32-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | IIL | **Input Leakage Current(3)** | | | | | |
| DI50 | | I/O Ports | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI55 | | $\overline{MCLR}$(2) | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, XT and HS modes |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(7,10) | mA | This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA. |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(8,9,10) | mA | This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSCI, and RB10. Maximum IICH current for these exceptions is 0 mA. |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(11) | — | +20(11) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins ( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** See the **"Device Pin Tables"** section for the 5V-tolerant pins.

**6:** The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

**7:** VIL source < (VSS - 0.3). Characterized but not tested.

**8:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**9:** Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**10:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

**11:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

**TABLE 32-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>I/O Pins:<br>4x Sink Driver Pins - All I/O output pins not defined as 8x Sink Driver pins | — | — | 0.4 | V | IOL ≤ 10 mA, VDD = 3.3V |
| | | **Output Low Voltage**<br>I/O Pins:<br>8x Sink Driver Pins - RC15 | — | — | 0.4 | V | IOL ≤ 15 mA, VDD = 3.3V |
| DO20 | VOH | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins - All I/O output pins not defined as 8x Source Driver pins | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins - RC15 | 2.4 | — | — | V | IOH ≥ -15 mA, VDD = 3.3V |
| DO20A | VOH1 | **Output High Voltage**<br>I/O Pins:<br>4x Source Driver Pins - All I/O output pins not defined as 8x Sink Driver pins | 1.5(1) | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -7 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>I/O Pins:<br>8x Source Driver Pins - RC15 | 1.5(1) | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -10 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized, but not tested.

**2:** This driver pin only applies to devices with less than 64 pins.

**3:** This driver pin only applies to devices with 64 pins.

**TABLE 32-10: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.(1)** | **Typical** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD transition high-to-low (**Note 2**) | 2.0 | — | 2.3 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.


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**TABLE 32-11: DC CHARACTERISTICS: PROGRAM MEMORY(3)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| D130 | EP | Cell Endurance | 1000 | — | — | E/W | — |
| D130a | EP | Cell Endurance | 20,000 | — | — | E/W | See **Note 5** |
| D131 | VPR | VDD for Read | 2.3 | — | 3.6 | V | — |
| D132 | VPEW | VDD for Erase or Write | 3.0 | — | 3.6 | V | — |
| D132a | VPEW | VDD for Erase or Write | 2.3 | — | 3.6 | V | See **Note 5** |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | — |
| D138 | TWW | Word Write Cycle Time(4) | — | 411 | — | FRC Cycles | — |
| D136 | TRW | Row Write Cycle Time(2,4) | — | 26067 | — | FRC Cycles | — |
| D137 | TPE | Page Erase Cycle Time(4) | — | 201060 | — | FRC Cycles | — |
| D139 | TCE | Chip Erase Cycle Time(4) | — | 804652 | — | FRC Cycles | — |

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to *“PIC32 Flash Programming Specification”* (DS60001145) for operating conditions during programming and erase cycles.

**4:** Translating this value to seconds depends on the FRC accuracy (see Table 32-19) and the FRC tuning values (see Register 8-2).

**5:** This parameter only applies to PIC32MX534/564/664/764 devices.

**TABLE 32-12: PROGRAM FLASH MEMORY WAIT STATE CHARACTERISTICS**

| DC CHARACTERISTICS | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | |
|---|---|---|---|
| **Required Flash Wait States** | **SYSCLK** | **Units** | **Comments** |
| 0 Wait State | 0 to 30 | MHz | — |
| 1 Wait State | 31 to 60 | | |
| 2 Wait States | 61 to 80 | | |

**TABLE 32-13: COMPARATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Comments** |
| D300 | VIOFF | Input Offset Voltage | — | ±7.5 | ±25 | mV | AVDD = VDD,<br>AVSS = VSS |
| D301 | VICM | Input Common Mode Voltage | 0 | — | VDD | V | AVDD = VDD,<br>AVSS = VSS<br>**(Note 2)** |
| D302 | CMRR | Common Mode Rejection Ratio | 55 | — | — | dB | Max VICM = (VDD - 1)V<br>**(Note 2)** |
| D303 | TRESP | Response Time | — | 150 | 400 | ns | AVDD = VDD,<br>AVSS = VSS<br>**(Notes 1, 2)** |
| D304 | ON2OV | Comparator Enabled to Output Valid | — | — | 10 | μs | Comparator module is configured before setting the comparator ON bit<br>**(Note 2)** |
| D305 | IVREF | Internal Voltage Reference | 0.57 | 0.6 | 0.63 | V | For devices without BGSEL<1:0> |
| | | | 1.14 | 1.2 | 1.26 | V | BGSEL<1:0> = 00 |
| | | | 0.57 | 0.6 | 0.63 | V | BGSEL<1:0> = 01 |

**Note 1:** Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

**2:** These parameters are characterized but not tested.

**3:** The Comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.


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**TABLE 32-14: VOLTAGE REFERENCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Comments** |
| D312 | TSET | Internal 4-bit DAC Comparator Reference Settling time. | — | — | 10 | µs | See **Note 1** |
| D313 | DACREFH | CVREF Input Voltage Reference Range | AVSS | — | AVDD | V | CVRSRC with CVRSS = 0 |
| | | | VREF- | — | VREF+ | V | CVRSRC with CVRSS = 1 |
| D314 | DVREF | CVREF Programmable Output Range | 0 | — | 0.625 x DACREFH | V | 0 to 0.625 DACREFH with DACREFH/24 step size |
| | | | 0.25 x DACREFH | — | 0.719 x DACREFH | V | 0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size |
| D315 | DACRES | Resolution | — | — | DACREFH/ 24 | | CVRCON<CVRR> = 1 |
| | | | — | — | DACREFH/ 32 | | CVRCON<CVRR> = 0 |
| D316 | DACACC | Absolute Accuracy(2) | — | — | 1/4 | LSB | DACREFH/24, CVRCON<CVRR> = 1 |
| | | | — | — | 1/2 | LSB | DACREFH/32, CVRCON<CVRR> = 0 |

**Note 1:** Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but not tested in manufacturing.

**2:** These parameters are characterized but not tested.

**TABLE 32-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Comments** |
| D321 | CEFC | External Filter Capacitor Value | 8 | 10 | — | µF | Capacitor must be low series resistance (1 ohm) |
| D322 | TPWRT | Power-up Timer Period | — | 64 | — | ms | — |

## 32.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX5XX/6XX/7XX AC characteristics and timing parameters.

**FIGURE 32-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

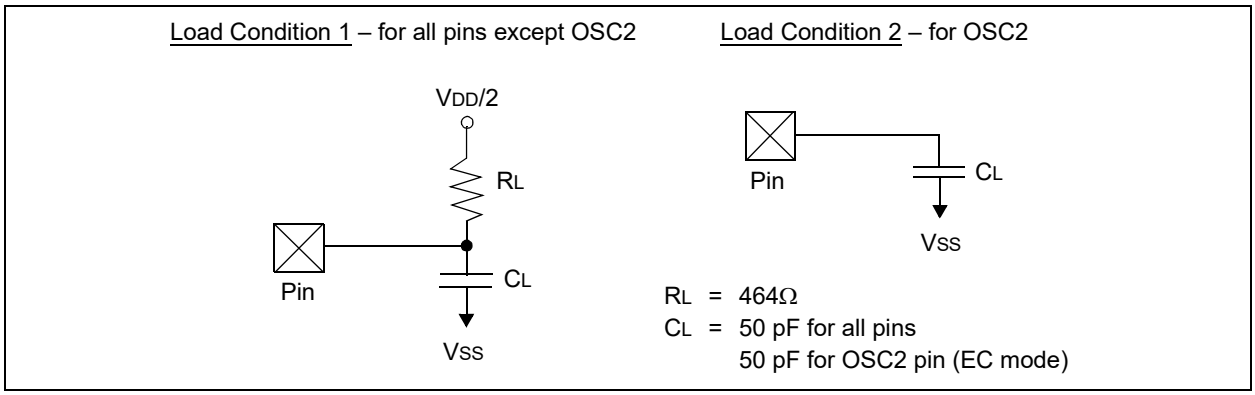


**TABLE 32-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO50 | Cosco | OSC2 pin | — | — | 15 | pF | In XT and HS modes when an external crystal is used to drive OSC1 |
| DO56 | CIO | All I/O pins and OSC2 | — | — | 50 | pF | In EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$ mode |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 32-2: EXTERNAL CLOCK TIMING**

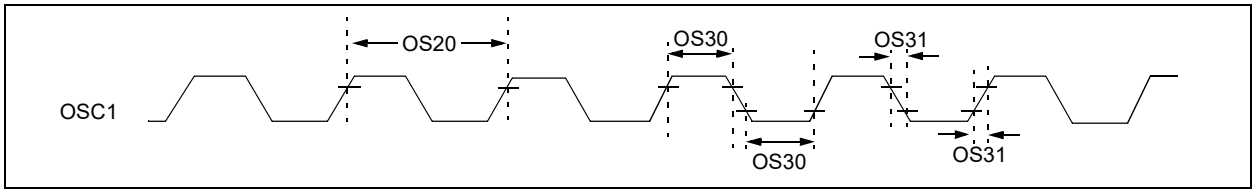



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**TABLE 32-17: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FOSC | External CLKI Frequency (External clocks only allowed in EC and ECPLL modes) | DC<br>4 | —<br>— | 50<br>50 | MHz<br>MHz | EC **(Note 4)**<br>ECPLL **(Note 3)** |
| OS11 | | Oscillator Crystal Frequency | 3 | — | 10 | MHz | XT **(Note 4)** |
| OS12 | | | 4 | — | 10 | MHz | XTPLL **(Notes 3,4)** |
| OS13 | | | 10 | — | 25 | MHz | HS **(Note 4)** |
| OS14 | | | 10 | — | 25 | MHz | HSPLL **(Notes 3,4)** |
| OS15 | | | 32 | 32.768 | 100 | kHz | SOSC **(Note 4)** |
| OS20 | TOSC | TOSC = 1/FOSC = TCY(2) | — | — | — | — | See parameter OS10 for FOSC value |
| OS30 | TOSL, TOSH | External Clock In (OSC1) High or Low Time | 0.45 x TOSC | — | — | ns | EC **(Note 4)** |
| OS31 | TOSR, TOSF | External Clock In (OSC1) Rise or Fall Time | — | — | 0.05 x TOSC | ns | EC **(Note 4)** |
| OS40 | TOST | Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes) | — | 1024 | — | TOSC | **(Note 4)** |
| OS41 | TFSCM | Primary Clock Fail Safe Time-out Period | — | 2 | — | ms | **(Note 4)** |
| OS42 | GM | External Oscillator Transconductance (Primary Oscillator only) | — | 12 | — | mA/V | VDD = 3.3V, TA = +25°C **(Note 4)** |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

**2:** Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

**3:** PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but is only tested at 10 MHz at manufacturing.

**4:** This parameter is characterized, but not tested in manufacturing.

**TABLE 32-18: PLL CLOCK TIMING SPECIFICATIONS ($V_{DD}$ = 2.3V TO 3.6V)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 3.92 | — | 5 | MHz | ECPLL, HSPLL, XTPLL, FRCPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 60 | — | 120 | MHz | — |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | — | — | 2 | ms | — |
| OS53 | DCLK | CLKO Stability(2) (Period Jitter or Cumulative) | -0.25 | — | +0.25 | % | Measured over 100 ms period |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 80 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{80}{20}}} = \frac{D_{CLK}}{2}$$

**TABLE 32-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX575/675/695/775/795 Family Devices** | | | | | | |
| F20a | FRC | -2 | — | +2 | % | — |
| **Internal FRC Accuracy @ 8.00 MHz(1) for PIC32MX534/564/664/764 Family Devices** | | | | | | |
| F20b | FRC | -0.9 | — | +0.9 | % | — |

**Note 1:** Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.


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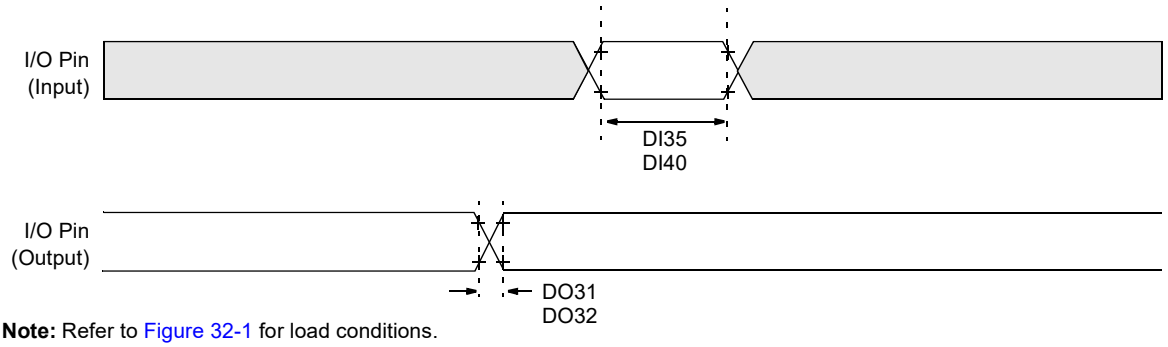
**TABLE 32-20: INTERNAL RC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **LPRC @ 31.25 kHz(1)** | | | | | | |
| F21 | LPRC | -15 | — | +15 | % | — |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 32-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-21: I/O TIMING REQUIREMENTS**

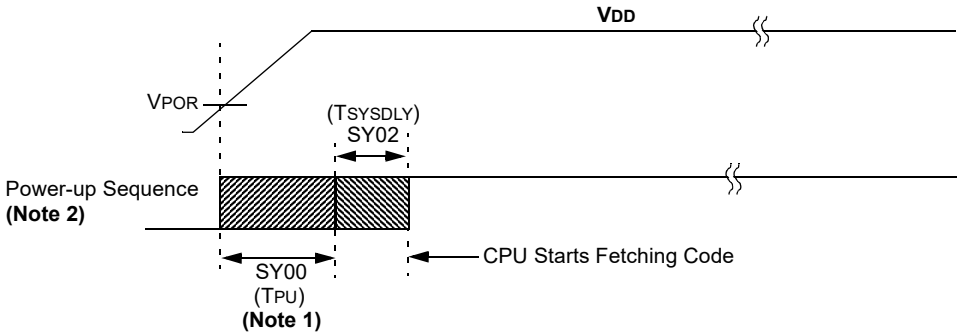
| AC CHARACTERISTICS | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DI35 | TINP | INTx Pin High or Low Time | 10 | — | — | ns | — |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TSYSCLK | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

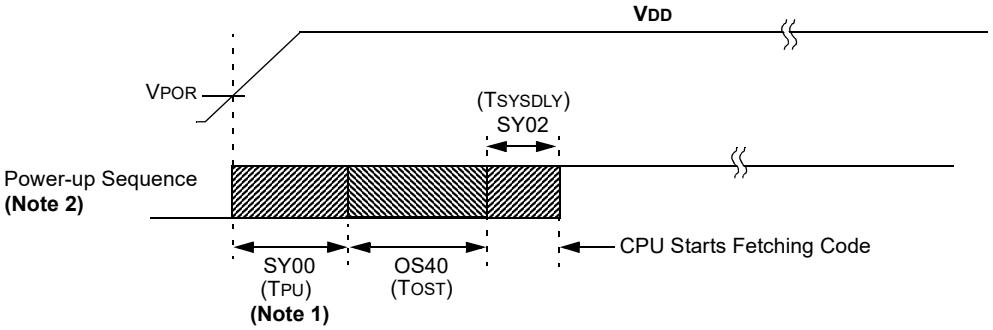
**2:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 32-4: POWER-ON RESET TIMING CHARACTERISTICS**

**Internal Voltage Regulator Enabled**
**Clock Sources = (FRC, FRCDIV, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)**




**Internal Voltage Regulator Enabled**
**Clock Sources = (HS, HSPLL, XT, XTPLL and SOSC)**




**Note 1:** The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{DDMIN}$).

**2:** Includes interval voltage regulator stabilization delay.


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**FIGURE 32-5: EXTERNAL RESET TIMING CHARACTERISTICS**

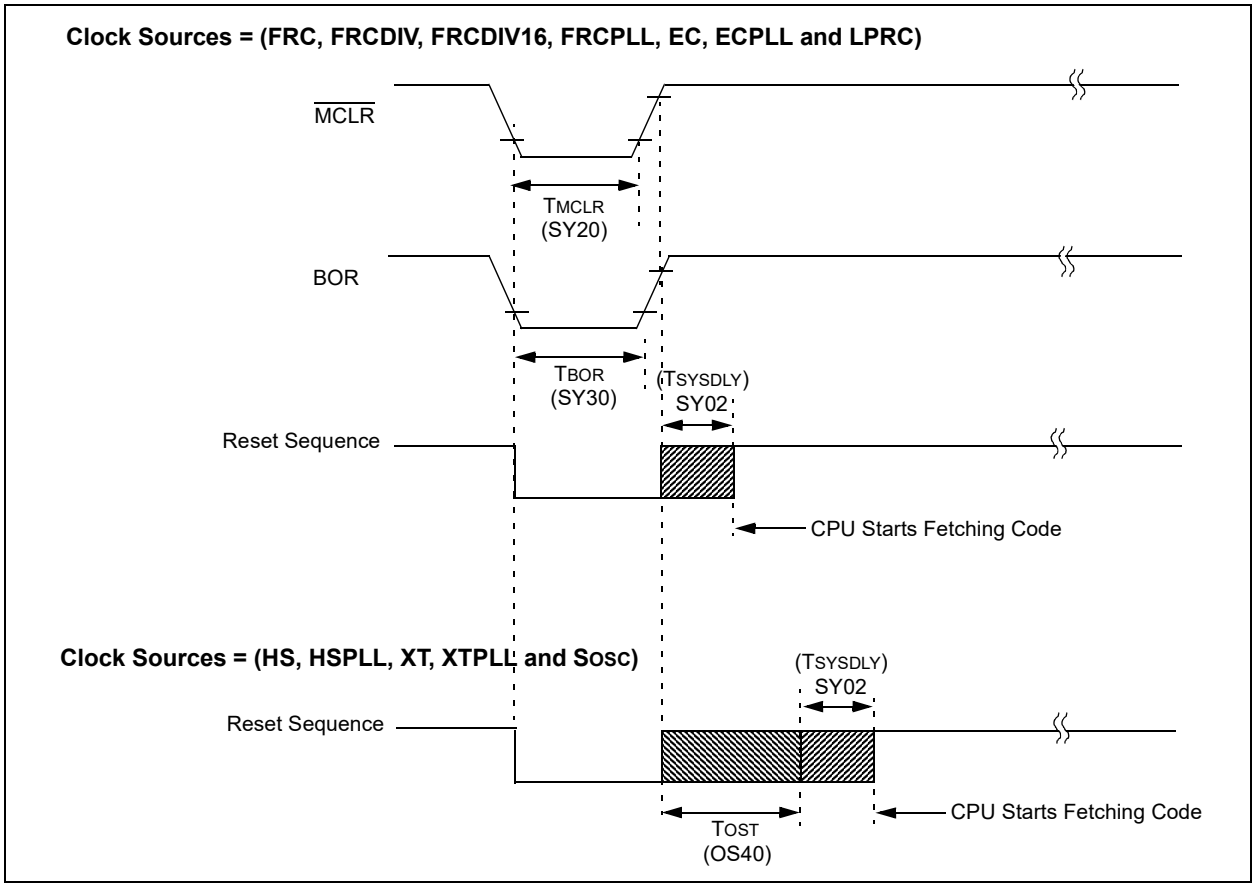


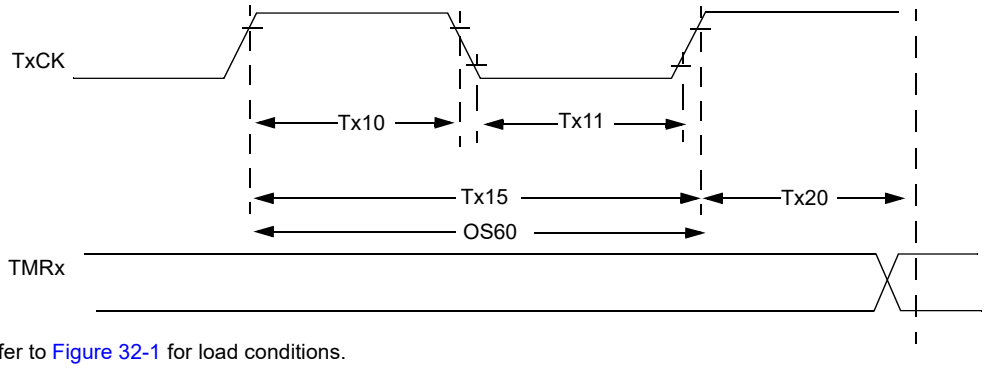

**TABLE 32-22: RESETS TIMING**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period<br>Internal Voltage Regulator Enabled | — | 400 | 600 | µs | -40°C to +85°C |
| SY02 | TSYSDLY | System Delay Period:<br>Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched. | — | 1 µs + 8 SYSCLK cycles | — | — | -40°C to +85°C |
| SY20 | TMCLR | $\overline{\text{MCLR}}$ Pulse Width (low) | — | 2 | — | µs | -40°C to +85°C |
| SY30 | TBOR | BOR Pulse Width (low) | — | 1 | — | µs | -40°C to +85°C |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

**FIGURE 32-6: TIMER1, 2, 3, 4, 5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | — | ns | Must also meet parameter TA15 |
| | | | Asynchronous, with prescaler | 10 | — | — | ns | — |
| TA15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of 25 ns or 2 TPB)/N] + 30 ns | — | — | ns | VDD > 2.7V |
| | | | | [(Greater of 25 ns or 2 TPB)/N] + 50 ns | — | — | ns | VDD < 2.7V |
| | | | Asynchronous, with prescaler | 20 | — | — | ns | VDD > 2.7V **(Note 3)** |
| | | | | 50 | — | — | ns | VDD < 2.7V **(Note 3)** |
| OS60 | FT1 | SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>)) | | 32 | — | 100 | kHz | — |
| TA20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | — | 1 | TPB | — |

**Note 1:** Timer1 is a Type A.

**2:** This parameter is characterized, but not tested in manufacturing.

**3:** N = Prescale Value (1, 8, 64, 256).


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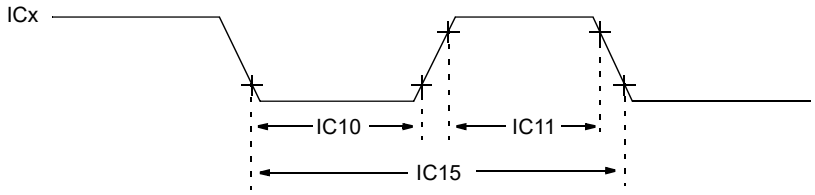
**TABLE 32-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | | **Min.** | **Max.** | **Units** | **Conditions** | |
| TB10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | N = prescale value (1, 2, 4, 8, 16, 32, 64, 256) |
| TB11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | |
| TB15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of [(25 ns or 2 TPB)/N] + 30 ns | — | ns | VDD > 2.7V | |
| | | | | [(Greater of [(25 ns or 2 TPB)/N] + 50 ns | — | ns | VDD < 2.7V | |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TPB | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS**



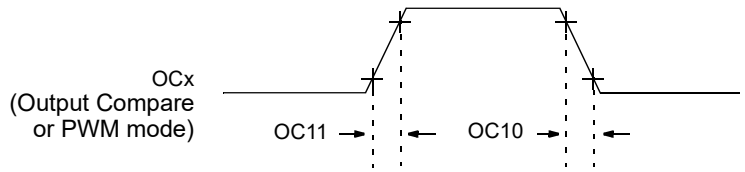

**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TccL | ICx Input Low Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | N = prescale value (1, 4, 16) |
| IC11 | TccH | ICx Input High Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | |
| IC15 | TccP | ICx Input Period | [(25 ns or 2 TPB)/N] + 50 ns | — | ns | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| OC10 | TccF | OCx Output Fall Time | — | — | — | ns | See parameter DO32 |
| OC11 | TccR | OCx Output Rise Time | — | — | — | ns | See parameter DO31 |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.


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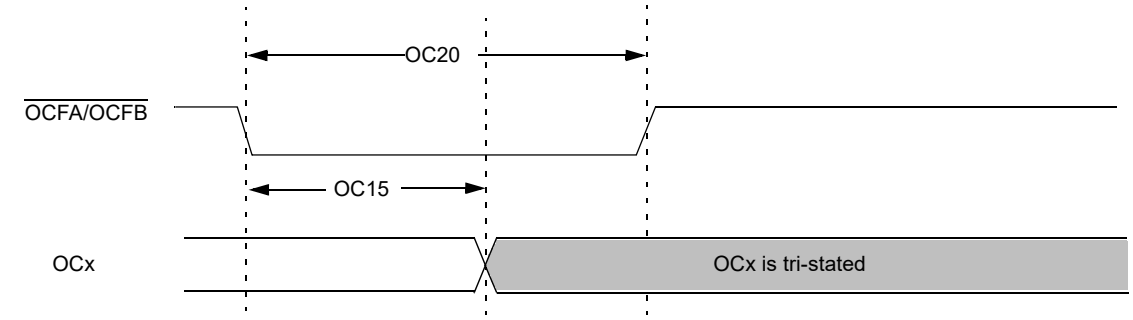
**FIGURE 32-9: OCx/PWM MODULE TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

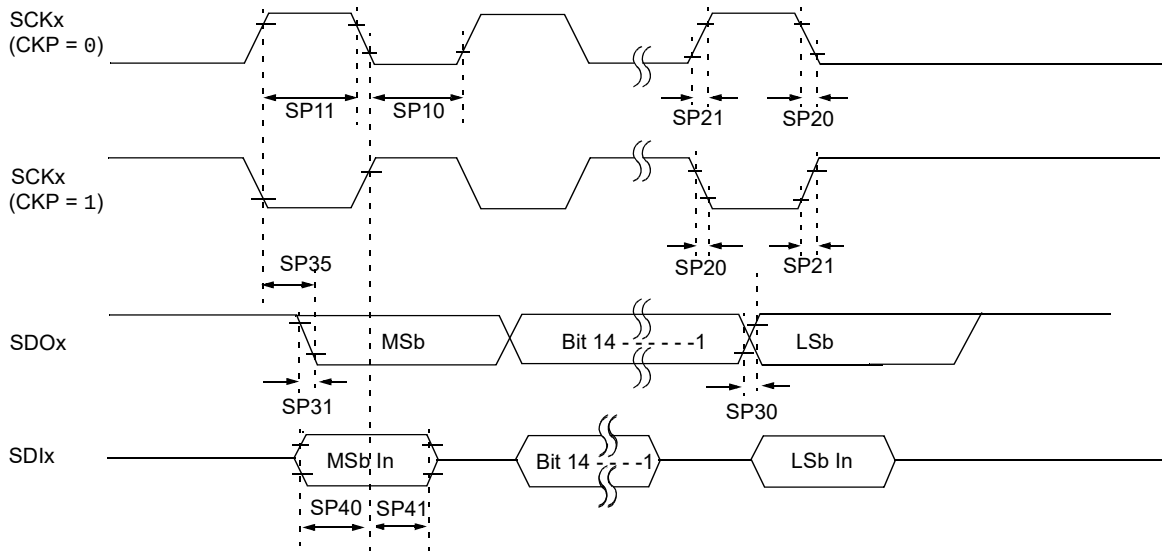
**TABLE 32-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics(1)** | **Min** | **Typical(2)** | **Max** | **Units** | **Conditions** |
| OC15 | TFD | Fault Input to PWM I/O Change | — | — | 50 | ns | — |
| OC20 | TFLT | Fault Input Pulse Width | 50 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 32-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(3) | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time(3) | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.


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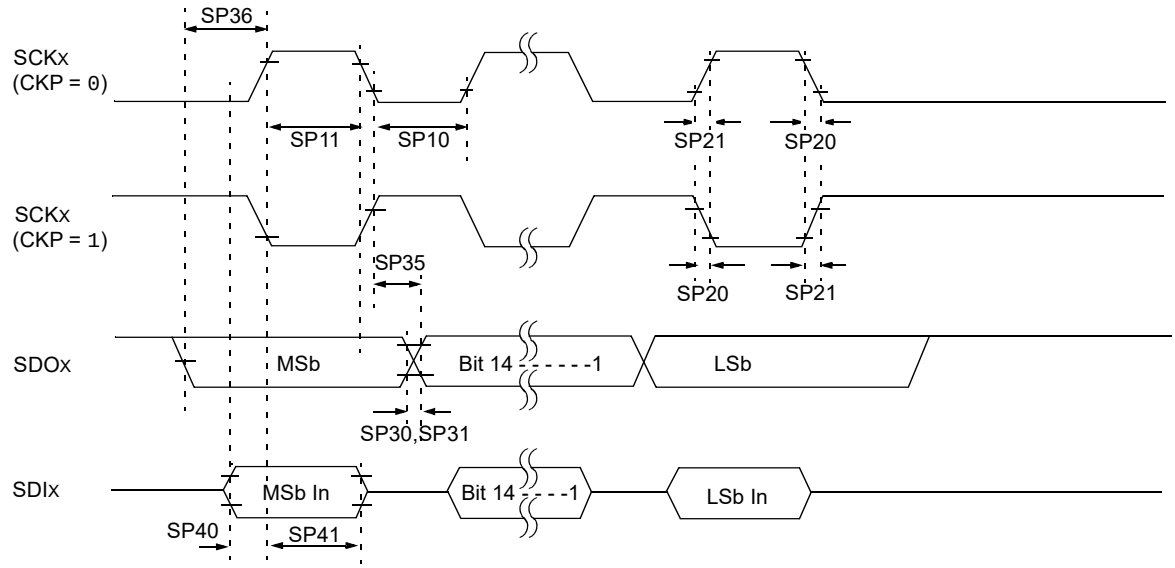
**FIGURE 32-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | TscL | SCKx Output Low Time(3) | Tsck/2 | — | — | ns | — |
| SP11 | TscH | SCKx Output High Time(3) | Tsck/2 | — | — | ns | — |
| SP20 | TscF | SCKx Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 15 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 15 | — | — | ns | VDD > 2.7V |
| | | | 20 | — | — | ns | VDD < 2.7V |

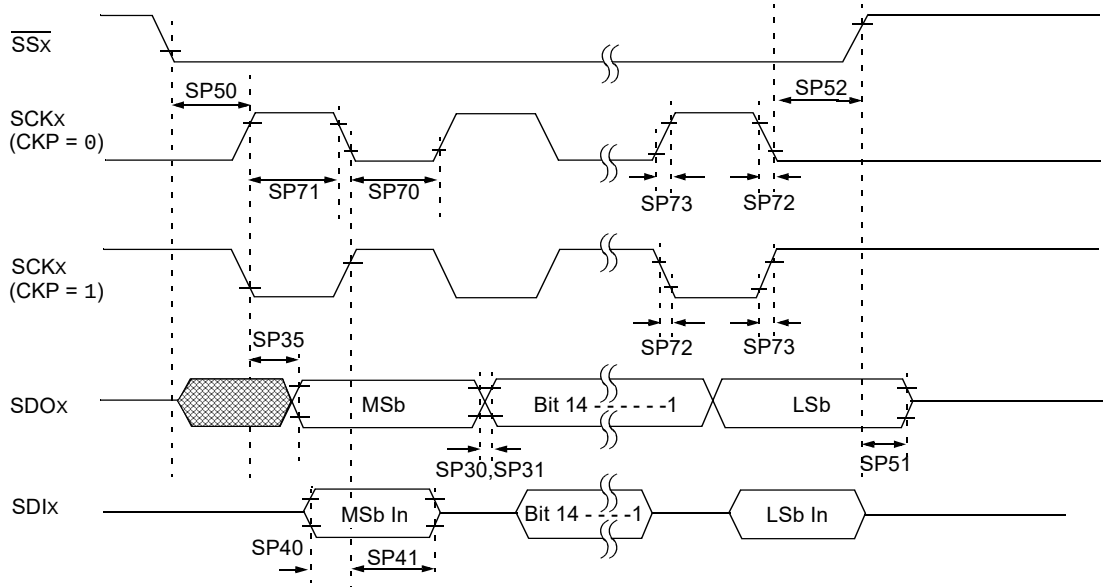
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 32-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time(3) | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time(3) | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See parameter DO32 |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | VDD > 2.7V |
| | | | — | — | 20 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input | 175 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance(3) | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH TscL2ssH | $\overline{SSx}$ after SCKx Edge | Tsck + 20 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.


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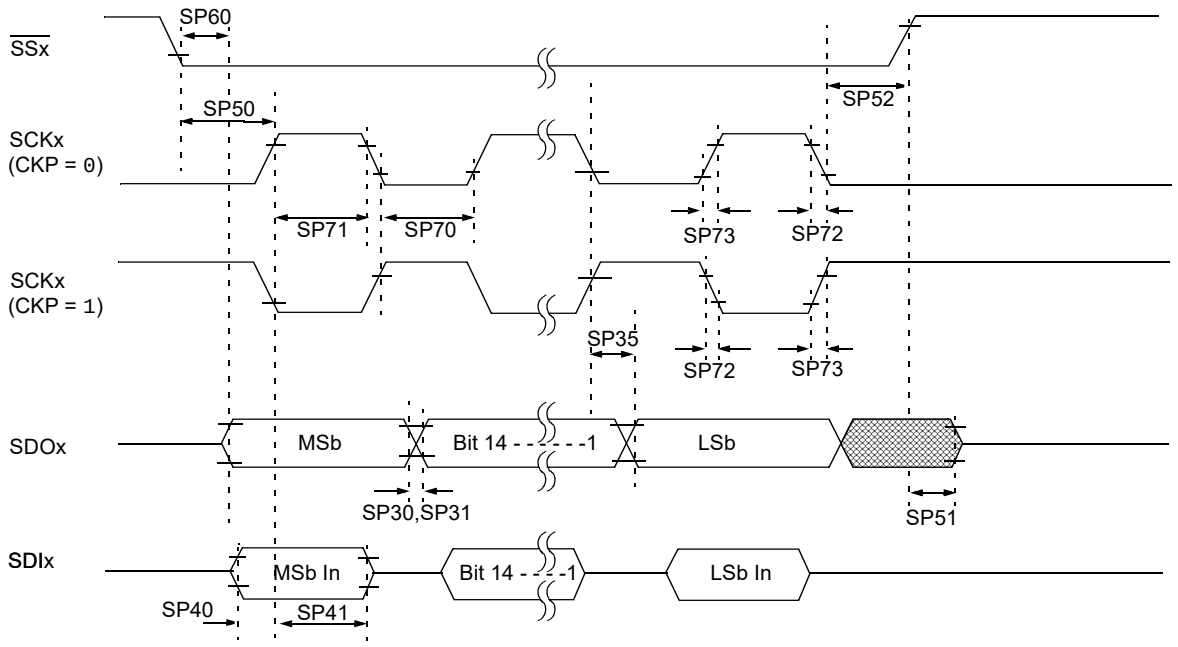
**FIGURE 32-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time(3) | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time(3) | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | 175 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**TABLE 32-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance(4) | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH<br>TscL2ssH | $\overline{SSx}$ ↑ after SCKx Edge | Tsck + 20 | — | — | ns | — |
| SP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 25 | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.


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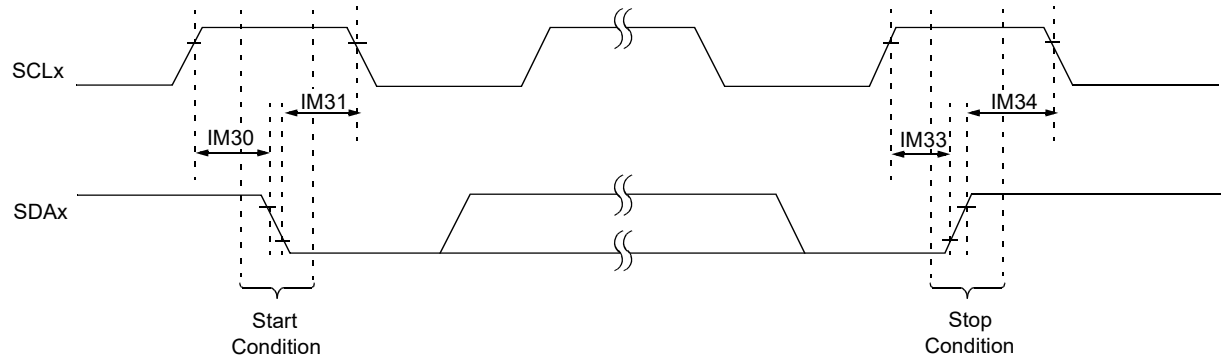
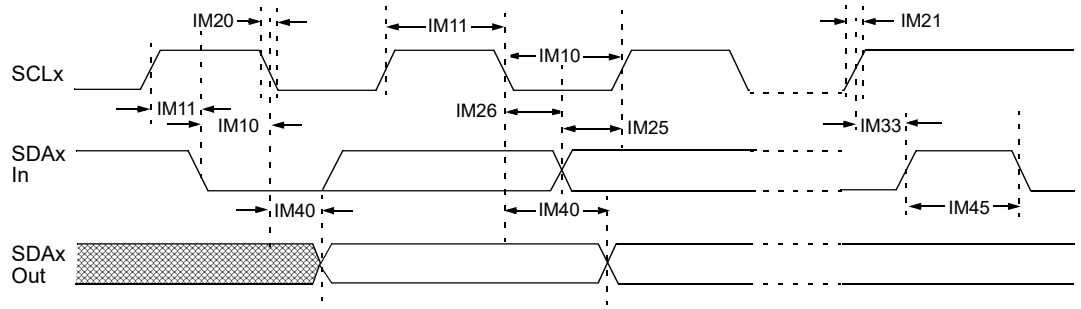
**FIGURE 32-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | µs | — |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | µs | — |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | µs | — |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(2) | 100 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | — |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(2) | 0 | 0.3 | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | ns | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | ns | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | ns | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TPB * (BRG + 2) | — | ns | — |
| | | | 400 kHz mode | TPB * (BRG + 2) | — | ns | |
| | | | 1 MHz mode(2) | TPB * (BRG + 2) | — | ns | |
| IM40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | — |
| | | | 400 kHz mode | — | 1000 | ns | — |
| | | | 1 MHz mode(2) | — | 350 | ns | — |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(2) | 0.5 | — | µs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |
| IM51 | TPGD | Pulse Gobbler Delay(3) | | 52 | 312 | ns | — |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (only for 1 MHz mode).

**3:** The typical value for this parameter is 104 ns.


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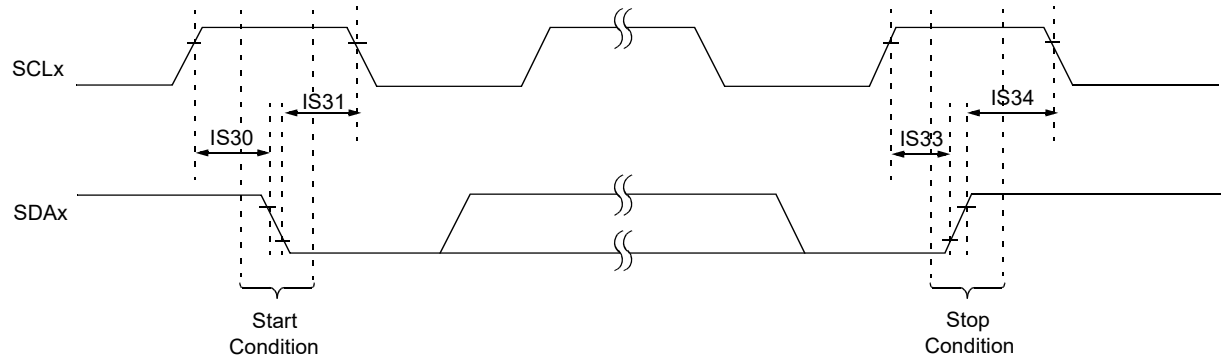
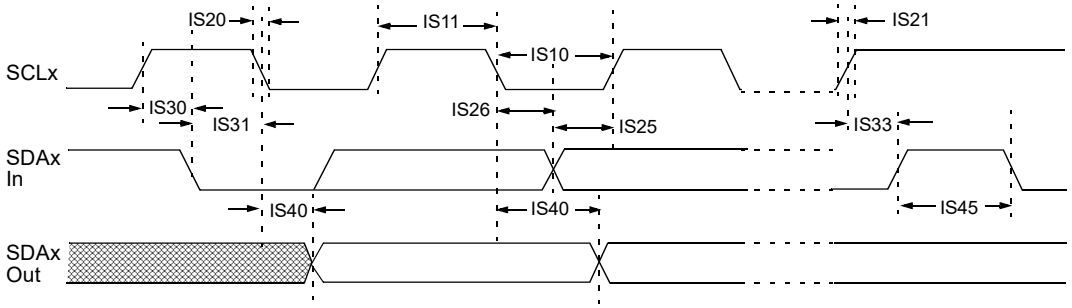
**FIGURE 32-16: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 32-1 for load conditions.

**FIGURE 32-17: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**




**Note:** Refer to Figure 32-1 for load conditions.

**TABLE 32-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 1.3 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | μs | — |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | μs | PBCLK must operate at a minimum of 800 kHz |
| | | | 400 kHz mode | 0.6 | — | μs | PBCLK must operate at a minimum of 3.2 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | μs | — |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | — |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(1) | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | — |
| | | | 400 kHz mode | 0 | 0.9 | μs | |
| | | | 1 MHz mode(1) | 0 | 0.3 | μs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4700 | — | ns | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | — | ns | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4000 | — | ns | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | — | ns | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 600 | — | ns | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4000 | — | ns | — |
| | | | 400 kHz mode | 600 | — | ns | |
| | | | 1 MHz mode(1) | 250 | | ns | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | — |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode(1) | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | μs | The amount of time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | μs | |
| | | | 1 MHz mode(1) | 0.5 | — | μs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | — |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (only for 1 MHz mode).


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**FIGURE 32-18: CAN MODULE I/O TIMING CHARACTERISTICS**

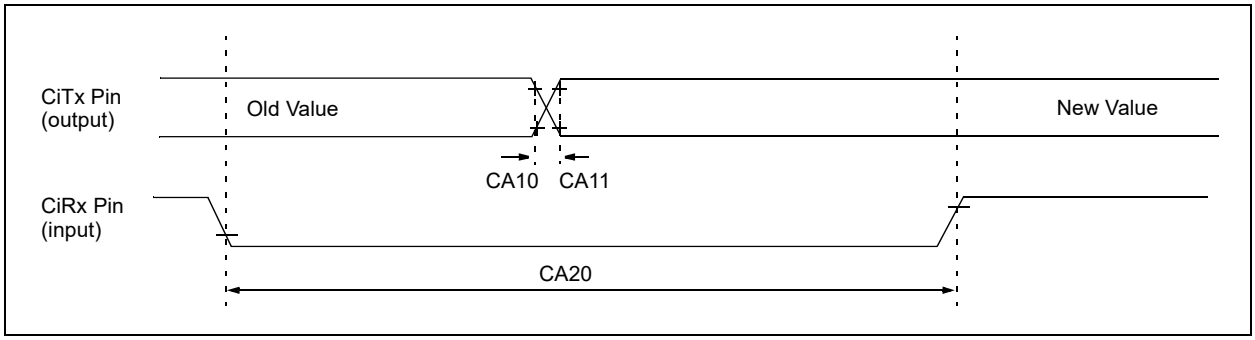


**TABLE 32-34: CAN MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| CA10 | TioF | Port Output Fall Time | — | — | — | ns | See parameter DO32 |
| CA11 | TioR | Port Output Rise Time | — | — | — | ns | See parameter DO31 |
| CA20 | Tcwf | Pulse Width to Trigger CAN Wake-up Filter | 700 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**TABLE 32-35: ETHERNET MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | Standard Operating Conditions (see Note 1): 2.9V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Characteristic** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **MIIM Timing Requirements** | | | | | | |
| ET1 | MDC Duty Cycle | 40 | — | 60 | % | — |
| ET2 | MDC Period | 400 | — | — | ns | — |
| ET3 | MDIO Output Setup and Hold | 10 | — | 10 | ns | See Figure 32-19 |
| ET4 | MDIO Input Setup and Hold | 0 | — | 300 | ns | See Figure 32-20 |
| **MII Timing Requirements** | | | | | | |
| ET5 | TX Clock Frequency | — | 25 | — | MHz | — |
| ET6 | TX Clock Duty Cycle | 35 | — | 65 | % | — |
| ET7 | ETXDx, ETEN, ETXERR Output Delay | 0 | — | 25 | ns | See Figure 32-21 |
| ET8 | RX Clock Frequency | — | 25 | — | MHz | — |
| ET9 | RX Clock Duty Cycle | 35 | — | 65 | % | — |
| ET10 | ERXDx, ERXDV, ERXERR Setup and Hold | 10 | — | 30 | ns | See Figure 32-22 |
| **RMII Timing Requirements** | | | | | | |
| ET11 | Reference Clock Frequency | — | 50 | — | MHz | — |
| ET12 | Reference Clock Duty Cycle | 35 | — | 65 | % | — |
| ET13 | ETXDx, ETEN, Setup and Hold | 2 | — | 4 | ns | — |
| ET14 | ERXDx, ERXDV, ERXERR Setup and Hold | 2 | — | 4 | ns | — |

**Note 1:** The Ethernet module is functional at VBORMIN < VDD < 2.9V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**FIGURE 32-19: MDIO SOURCED BY THE PIC32 DEVICE**

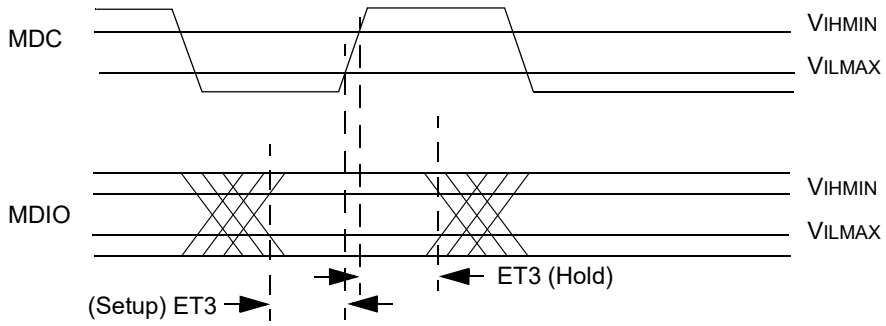


**FIGURE 32-20: MDIO SOURCED BY THE PHY**

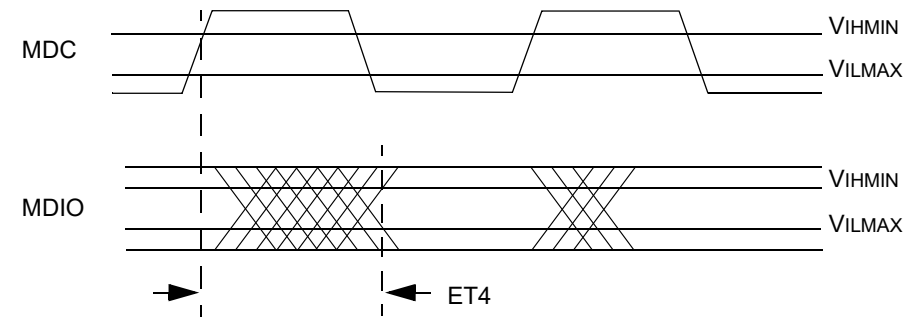



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**FIGURE 32-21: TRANSMIT SIGNAL TIMING RELATIONSHIPS AT THE MII**

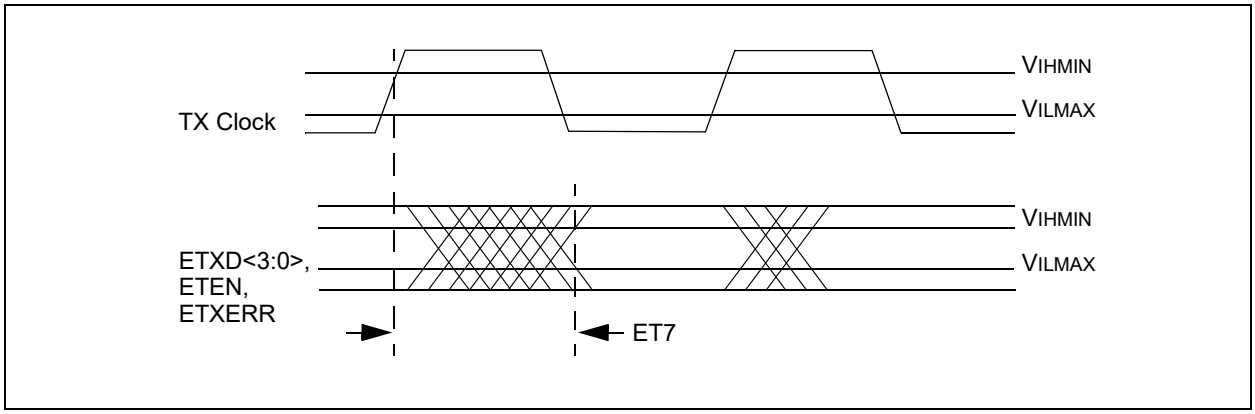


**FIGURE 32-22: RECEIVE SIGNAL TIMING RELATIONSHIPS AT THE MII**

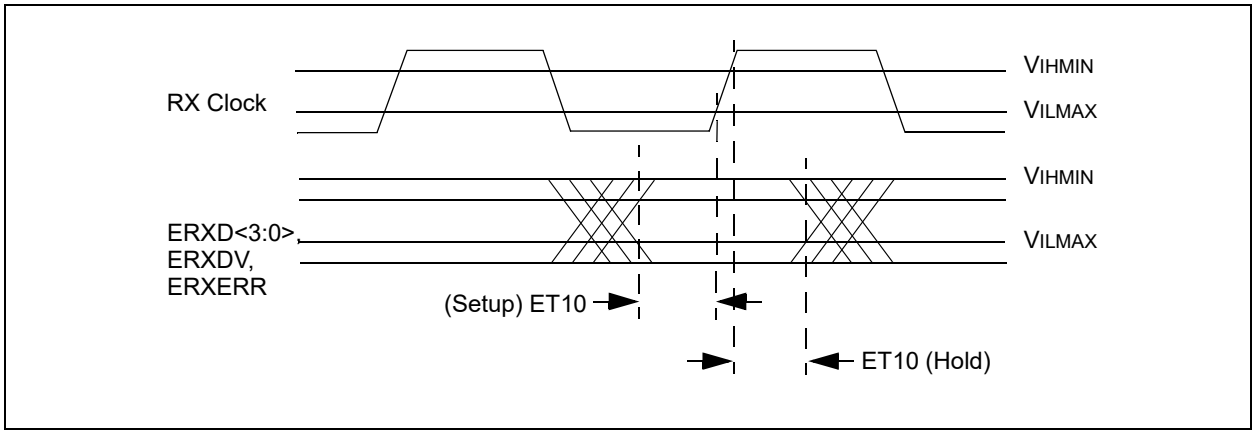

**TABLE 32-36: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of VDD – 0.3 or 2.5 | — | Lesser of VDD + 0.3 or 3.6 | V | — |
| AD02 | AVSS | Module VSS Supply | VSS | — | VSS + 0.3 | V | — |
| **Reference Inputs** | | | | | | | |
| AD05<br>AD05a | VREFH | Reference Voltage High | AVSS + 2.0<br>2.5 | —<br>— | AVDD<br>3.6 | V<br>V | **(Note 1)**<br>VREFH = AVDD **(Note 3)** |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | VREFH – 2.0 | V | **(Note 1)** |
| AD07 | VREF | Absolute Reference Voltage (VREFH – VREFL) | 2.0 | — | AVDD | V | **(Note 3)** |
| AD08<br>AD08a | IREF | Current Drain | —<br>— | 250<br>— | 400<br>3 | μA<br>μA | ADC operating<br>ADC off |
| **Analog Input** | | | | | | | |
| AD12 | VINH-VINL | Full-Scale Input Span | VREFL | — | VREFH | V | — |
| AD13 | VINL | Absolute VINL Input Voltage | AVSS – 0.3 | — | AVDD/2 | V | — |
| AD14 | VIN | Absolute Input Voltage | AVSS – 0.3 | — | AVDD + 0.3 | V | — |
| AD15 | | Leakage Current | — | ±0.001 | ±0.610 | μA | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V<br>Source Impedance = 10 kΩ |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | — | 5K | Ω | **(Note 1)** |
| **ADC Accuracy – Measurements with External VREF+/VREF-** | | | | | | | |
| AD20c | Nr | Resolution | 10 data bits | | | bits | — |
| AD21c | INL | Integral Nonlinearity | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V |
| AD22c | DNL | Differential Nonlinearity | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V<br>**(Note 2)** |
| AD23c | GERR | Gain Error | > -1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V,<br>AVDD = VREFH = 3.3V |
| AD24c | EOFF | Offset Error | > -1 | — | < 1 | LSb | VINL = AVSS = 0V,<br>AVDD = 3.3V |
| AD25c | — | Monotonicity | — | — | — | — | Guaranteed |

**Note 1:** These parameters are not characterized or tested in manufacturing.

**2:** With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

**4:** Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.


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**TABLE 32-36: ADC MODULE SPECIFICATIONS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 5): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy – Measurements with Internal VREF+/VREF-** | | | | | | | |
| AD20d | Nr | Resolution | 10 data bits | | | bits | **(Note 3)** |
| AD21d | INL | Integral Nonlinearity | > -1 | — | < 1 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD22d | DNL | Differential Nonlinearity | > -1 | — | < 1 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Notes 2,3)** |
| AD23d | GERR | Gain Error | > -4 | — | < 4 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD24d | EOFF | Offset Error | > -2 | — | < 2 | LSb | VINL = AVSS = 0V, AVDD = 2.5V to 3.6V **(Note 3)** |
| AD25d | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance** | | | | | | | |
| AD31b | SINAD | Signal to Noise and Distortion | 55 | 58.5 | — | dB | **(Notes 3,4)** |
| AD34b | ENOB | Effective Number of Bits | 9.0 | 9.5 | — | bits | **(Notes 3,4)** |

**Note 1:** These parameters are not characterized or tested in manufacturing.

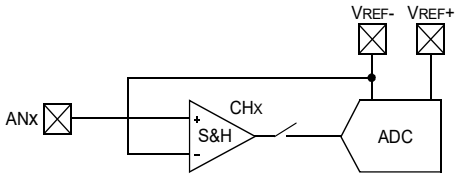
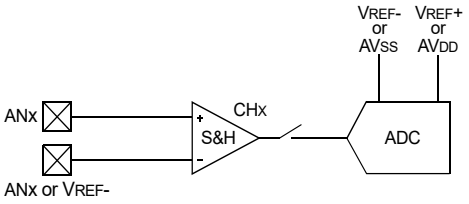
**2:** With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

**4:** Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**TABLE 32-37: 10-BIT ADC CONVERSION RATE PARAMETERS**

| **Standard Operating Conditions (see Note 3): 2.5V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | | |
|---|---|---|---|---|---|
| **ADC Speed(2)** | **TAD Minimum** | **Sampling Time Minimum** | **RS Maximum** | **VDD** | **ADC Channels Configuration** |
| 1 Msps to 400 ksps(1) | 65 ns | 132 ns | 500Ω | 3.0V to 3.6V |  |
| Up to 400 ksps | 200 ns | 200 ns | 5.0 kΩ | 2.5V to 3.6V |  |

**Note 1:** External VREF- and VREF+ pins must be used for correct operation.

**2:** These parameters are characterized, but not tested in manufacturing.

**3:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.


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**TABLE 32-38: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 4): 2.5V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | Analog-to-Digital Clock Period(2) | 65 | — | — | ns | See Table 32-37 |
| **Conversion Rate** | | | | | | | |
| AD55 | TCONV | Conversion Time | — | 12 TAD | — | — | — |
| AD56 | FCNV | Throughput Rate (Sampling Speed) | — | — | 1000 | ksps | AVDD = 3.0V to 3.6V |
| | | | — | — | 400 | ksps | AVDD = 2.5V to 3.6V |
| AD57 | TSAMP | Sample Time | 1 TAD | — | — | — | TSAMP must be ≥ 132 ns |
| **Timing Parameters** | | | | | | | |
| AD60 | TPCS | Conversion Start from Sample Trigger(3) | — | 1.0 TAD | — | — | Auto-Convert Trigger (SSRC<2:0> = 111) not selected |
| AD61 | TPSS | Sample Start from Setting Sample (SAMP) bit | 0.5 TAD | — | 1.5 TAD | — | — |
| AD62 | TCSS | Conversion Completion to Sample Start (ASAM = 1)(3) | — | 0.5 TAD | — | — | — |
| AD63 | TDPU | Time to Stabilize Analog Stage from Analog-to-Digital Off to Analog-to-Digital On(3) | — | — | 2 | μs | — |

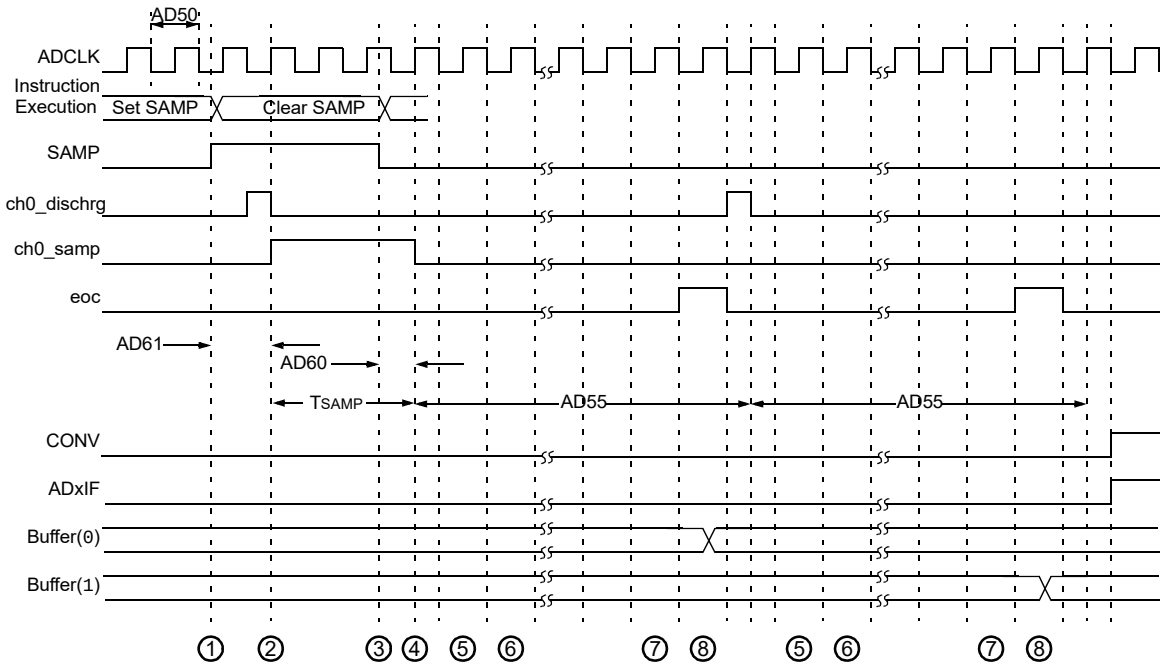
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

**3:** Characterized by design but not tested.

**4:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

**FIGURE 32-23: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)**




(1) – Software sets ADxCON. SAMP to start sampling.

(2) – Sampling starts after discharge period. TSAMP is described in Section 17. “10-bit A/D Converter” (DS60001104) of the *“PIC32 Family Reference Manual”*.

(3) – Software clears ADxCON. SAMP to start conversion.

(4) – Sampling ends, conversion sequence starts.

(5) – Convert bit 9.

(6) – Convert bit 8.

(7) – Convert bit 0.

(8) – One TAD for end of conversion.


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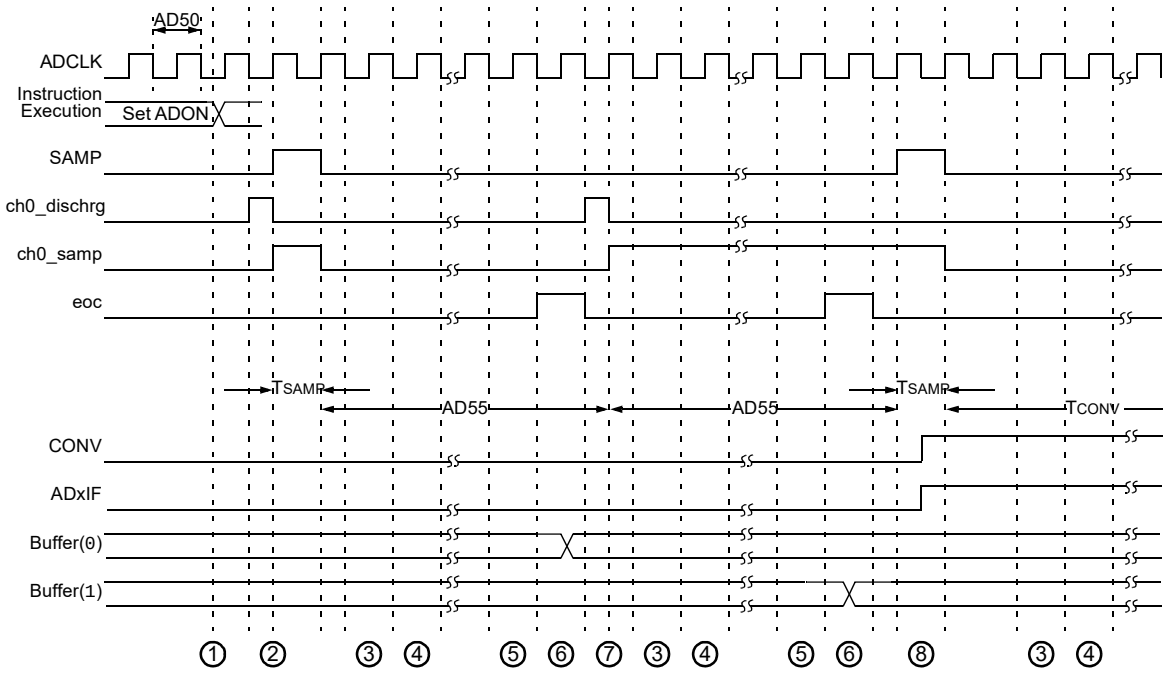
**FIGURE 32-24: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)**




(1) – Software sets ADxCON. ADON to start AD operation.

(2) – Sampling starts after discharge period.
TSAMP is described in Section 17. "10-bit A/D Converter" (DS60001104) of the *"PIC32 Family Reference Manual*.

(3) – Convert bit 9.

(4) – Convert bit 8.

(5) – Convert bit 0.

(6) – One TAD for end of conversion.

(7) – Begin conversion of next channel.

(8) – Sample for time specified by SAMC<4:0>.

**FIGURE 32-25: PARALLEL SLAVE PORT TIMING**

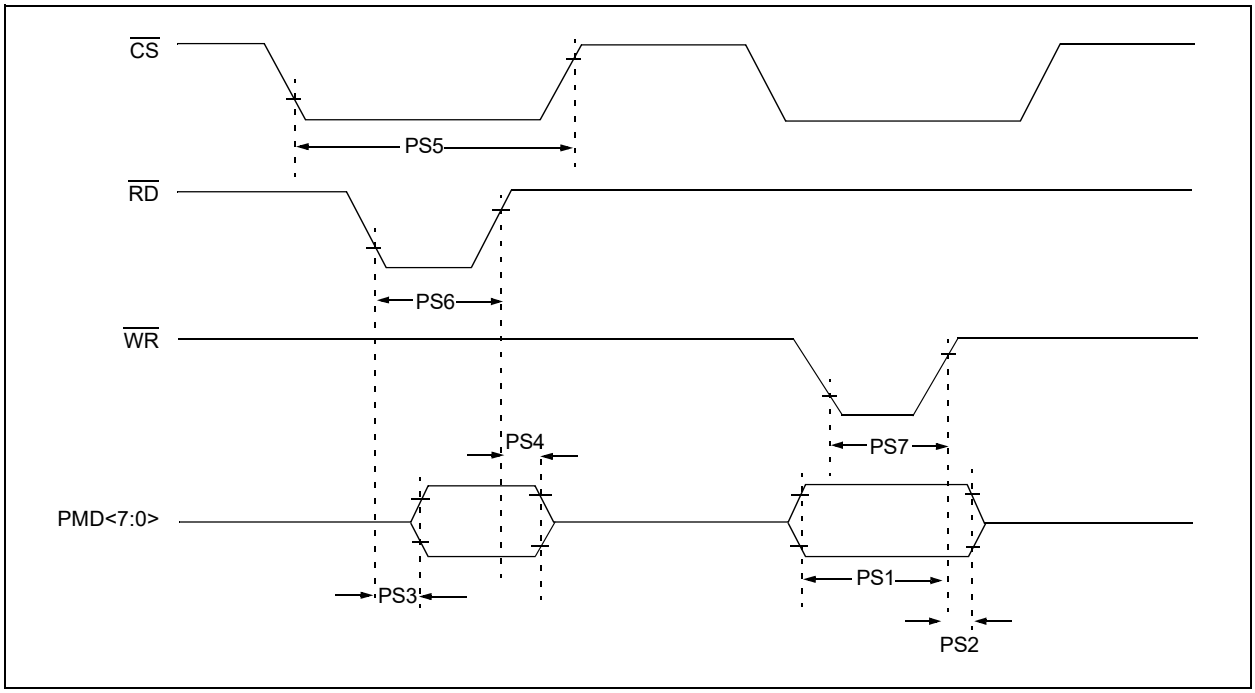



**TABLE 32-39: PARALLEL SLAVE PORT REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| PS1 | TdtV2wrH | Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time) | 20 | — | — | ns | — |
| PS2 | TwrH2dtI | $\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time) | 40 | — | — | ns | — |
| PS3 | TrdL2dtV | $\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid | — | — | 60 | ns | — |
| PS4 | TrdH2dtI | $\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid | 0 | — | 10 | ns | — |
| PS5 | Tcs | $\overline{CS}$ Active Time | TPB + 40 | — | — | ns | — |
| PS6 | TWR | $\overline{WR}$ Active Time | TPB + 25 | — | — | ns | — |
| PS7 | TRD | $\overline{RD}$ Active Time | TPB + 25 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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**FIGURE 32-26: PARALLEL MASTER PORT READ TIMING DIAGRAM**

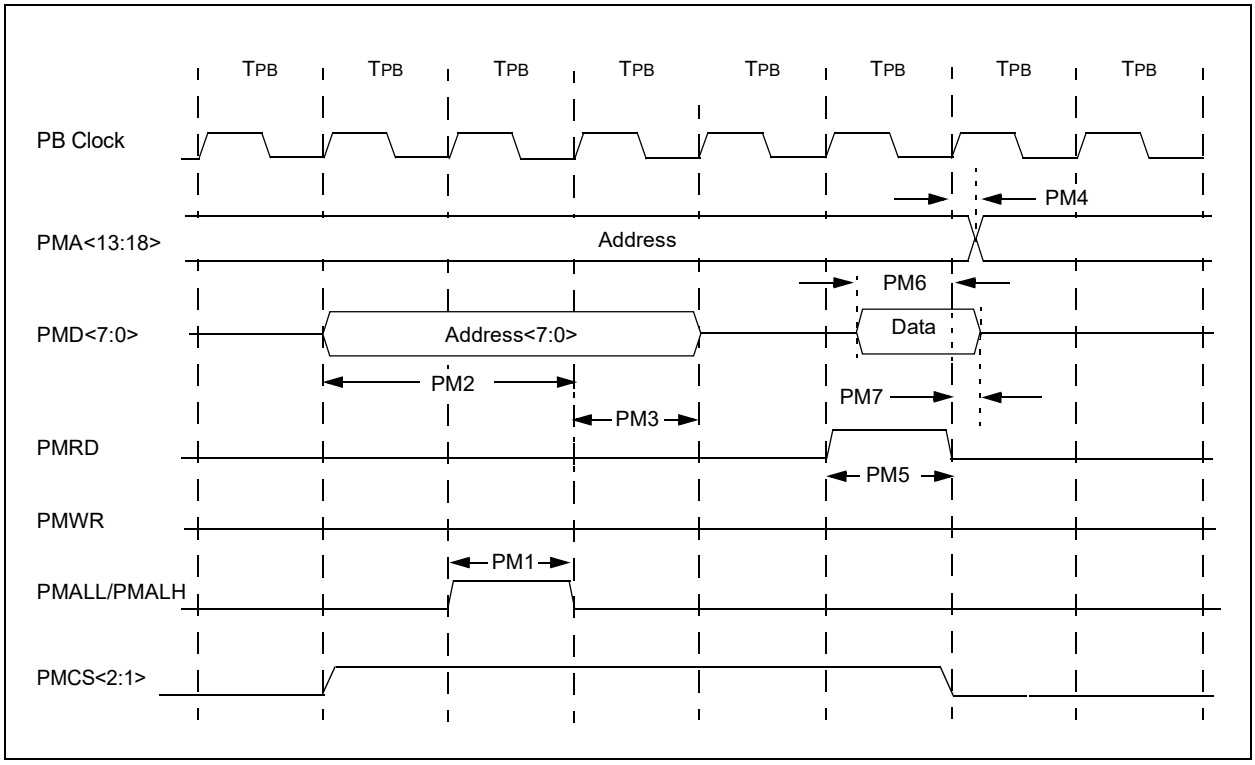


**TABLE 32-40: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| PM1 | TLAT | PMALL/PMALH Pulse Width | — | 1 TPB | — | — | — |
| PM2 | TADSU | Address Out Valid to PMALL/ PMALH Invalid (address setup time) | — | 2 TPB | — | — | — |
| PM3 | TADHOLD | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | — | 1 TPB | — | — | — |
| PM4 | TAHOLD | PMRD Inactive to Address Out Invalid (address hold time) | 5 | — | — | ns | — |
| PM5 | TRD | PMRD Pulse Width | — | 1 TPB | — | — | — |
| PM6 | TDSU | PMRD or PMENB Active to Data In Valid (data setup time) | 15 | — | — | ns | — |
| PM7 | TDHOLD | PMRD or PMENB Inactive to Data In Invalid (data hold time) | 1 TPBCLK | — | — | ns | PMP PBCLK |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-27: PARALLEL MASTER PORT WRITE TIMING DIAGRAM**

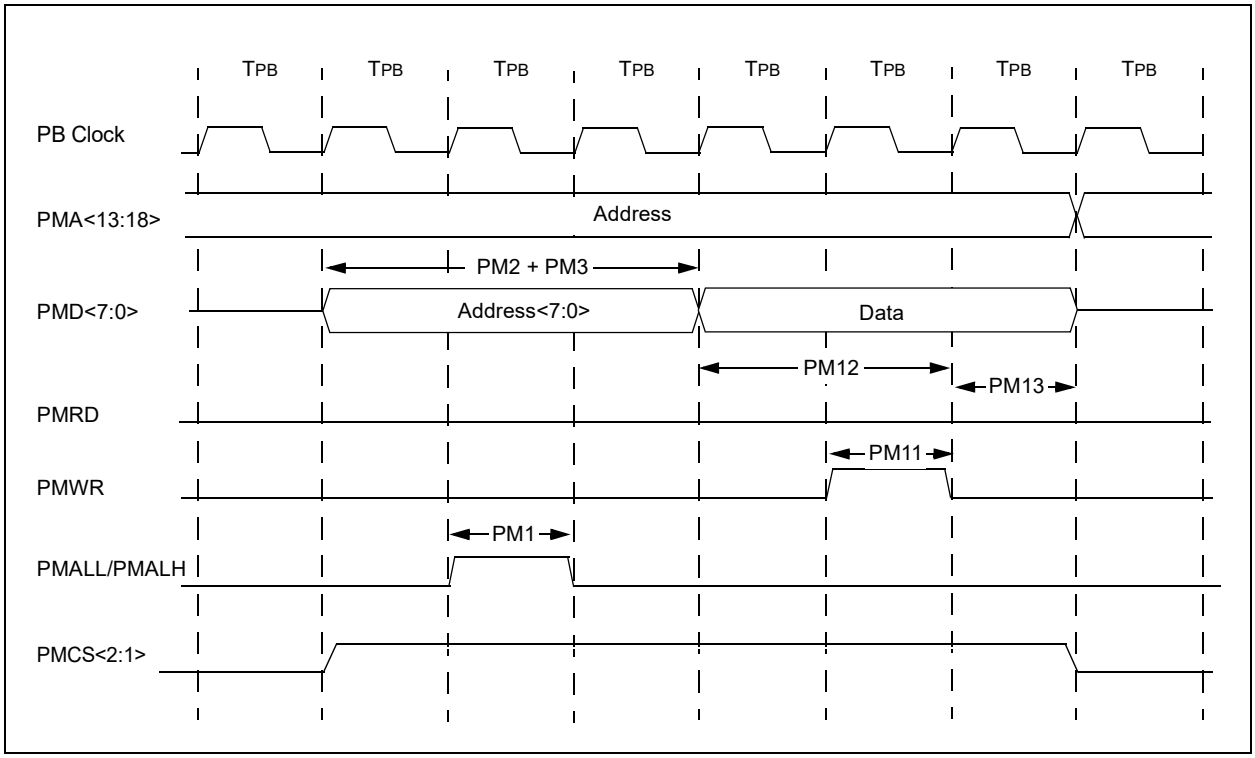


**TABLE 32-41: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| PM11 | TWR | PMWR Pulse Width | — | 1 TPB | — | — | — |
| PM12 | TDVSU | Data Out Valid before PMWR or PMENB goes Inactive (data setup time) | — | 2 TPB | — | — | — |
| PM13 | TDVHOLD | PMWR or PMEMB Invalid to Data Out Invalid (data hold time) | — | 1 TPB | — | — | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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**TABLE 32-42: USB OTG ELECTRICAL SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical** | **Max.** | **Units** | **Conditions** |
| USB313 | VUSB3V3 | USB Voltage | 3.0 | — | 3.6 | V | Voltage on VUSB3V3 must be in this range for proper USB operation |
| USB315 | VILUSB | Input Low Voltage for USB Buffer | — | — | 0.8 | V | — |
| USB316 | VIHUSB | Input High Voltage for USB Buffer | 2.0 | — | — | V | — |
| USB318 | VDIFS | Differential Input Sensitivity | — | — | 0.2 | V | The difference between D+ and D- must exceed this value while VCM is met |
| USB319 | VCM | Differential Common Mode Range | 0.8 | — | 2.5 | V | — |
| USB320 | ZOUT | Driver Output Impedance | 28.0 | — | 44.0 | Ω | — |
| USB321 | VOL | Voltage Output Low | 0.0 | — | 0.3 | V | 1.425 kΩ load connected to VUSB3V3 |
| USB322 | VOH | Voltage Output High | 2.8 | — | 3.6 | V | 14.25 kΩ load connected to ground |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 32-28: EJTAG TIMING CHARACTERISTICS**

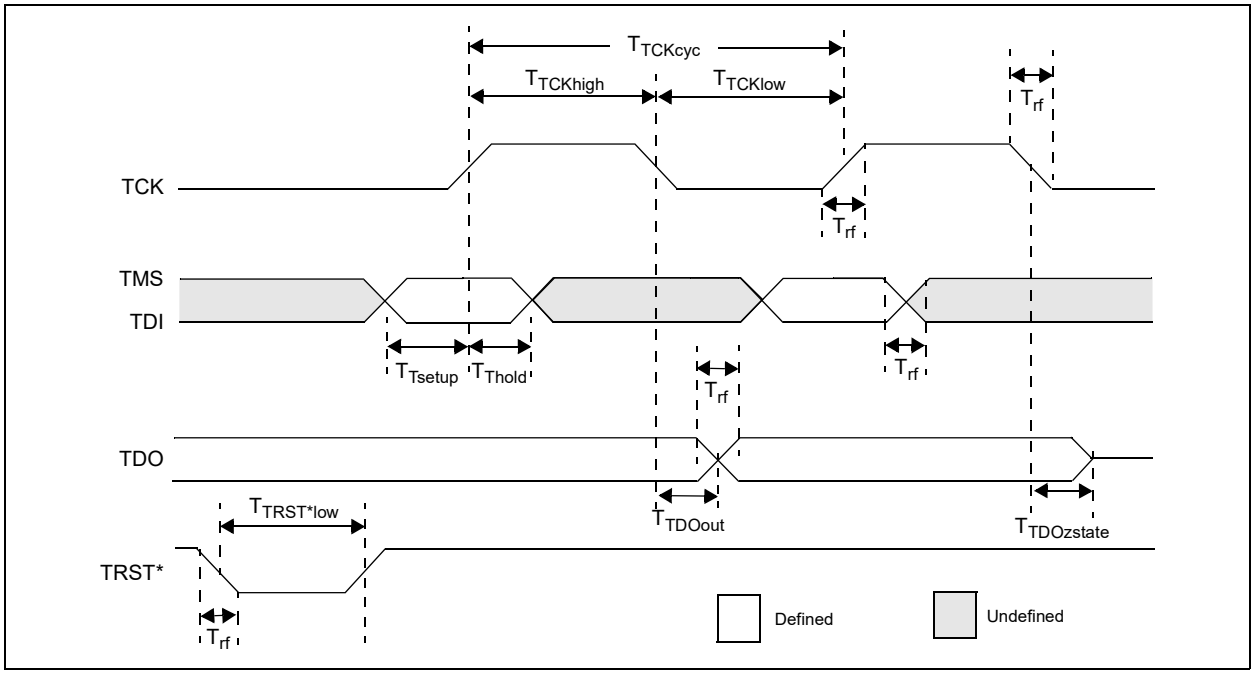


**TABLE 32-43: EJTAG TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-Temp | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Description(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| EJ1 | TTCKCYC | TCK Cycle Time | 25 | — | ns | — |
| EJ2 | TTCKHIGH | TCK High Time | 10 | — | ns | — |
| EJ3 | TTCKLOW | TCK Low Time | 10 | — | ns | — |
| EJ4 | TTSETUP | TAP Signals Setup Time Before Rising TCK | 5 | — | ns | — |
| EJ5 | TTHOLD | TAP Signals Hold Time After Rising TCK | 3 | — | ns | — |
| EJ6 | TTDOOUT | TDO Output Delay Time from Falling TCK | — | 5 | ns | — |
| EJ7 | TTDOZSTATE | TDO 3-State Delay Time from Falling TCK | — | 5 | ns | — |
| EJ8 | TTRSTLOW | TRST Low Time | 25 | — | ns | — |
| EJ9 | TRF | TAP Signals Rise/Fall Time, All Input and Output | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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## 33.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 33-1: VOH – 4x DRIVER PINS**

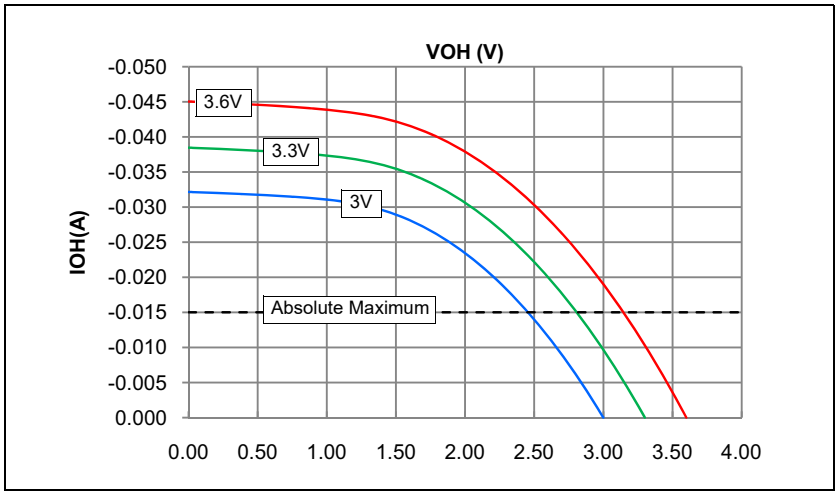



**FIGURE 33-2: VOH – 8x DRIVER PINS**

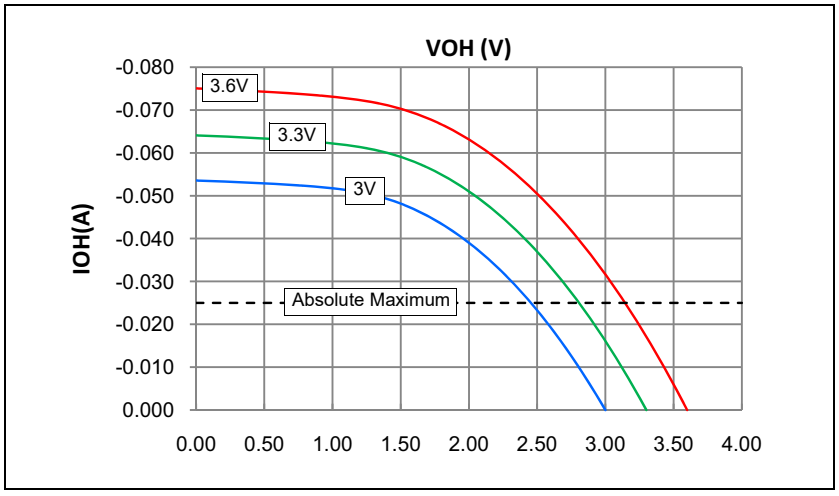



**FIGURE 33-3: VOL – 4x DRIVER PINS**

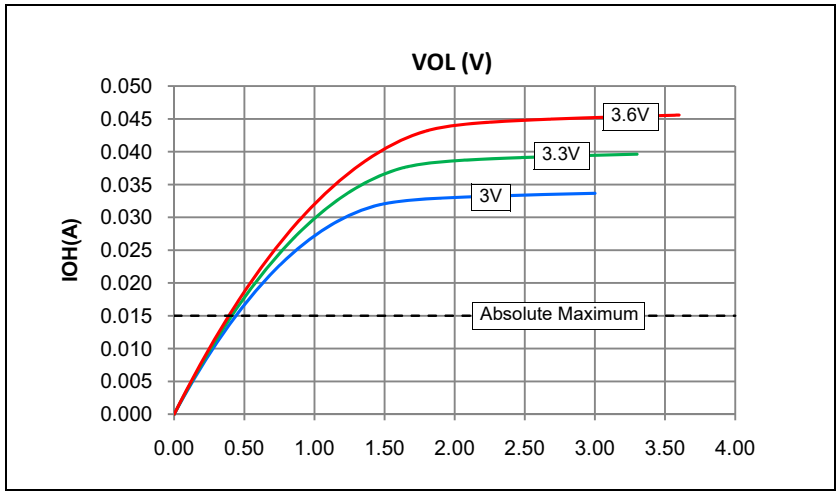
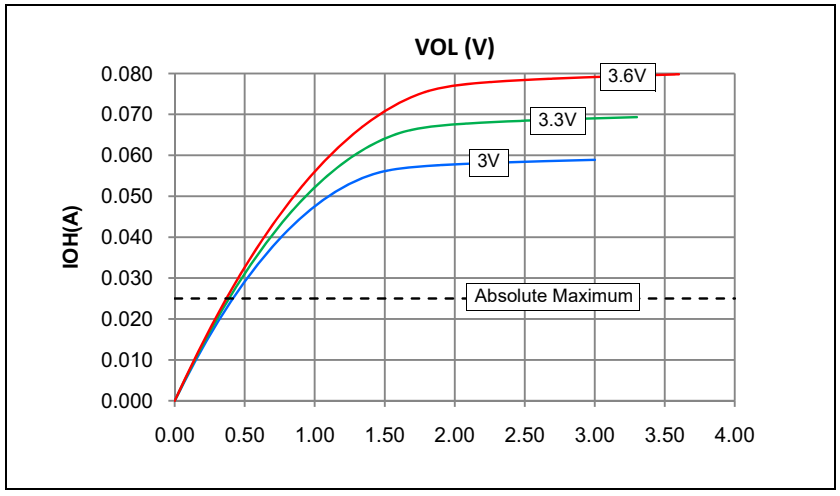



**FIGURE 33-4: VOL – 8x DRIVER PINS**



**NOTES:**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## 34.0 PACKAGING INFORMATION

### 34.1 Package Marking Information

64-Lead TQFP (10x10x1 mm)

Example

100-Lead TQFP (14x14x1 mm)

Example

100-Lead TQFP (12x12x1 mm)

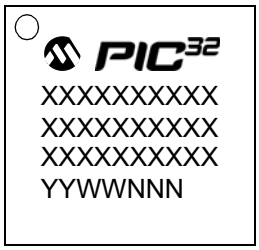
Example

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

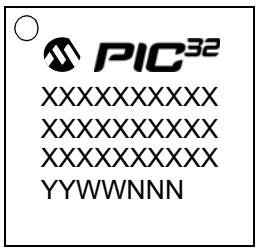
### 34.1 Package Marking Information (Continued)

64-Lead QFN (9x9x0.9 mm)

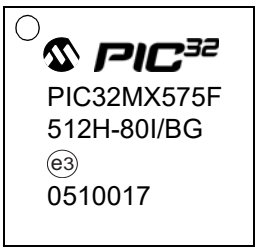



Example

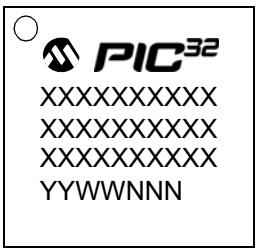
121-Lead TFBGA (10x10x1.1 mm)




Example




124-Lead VTLA (9x9x0.9 mm)




Example

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.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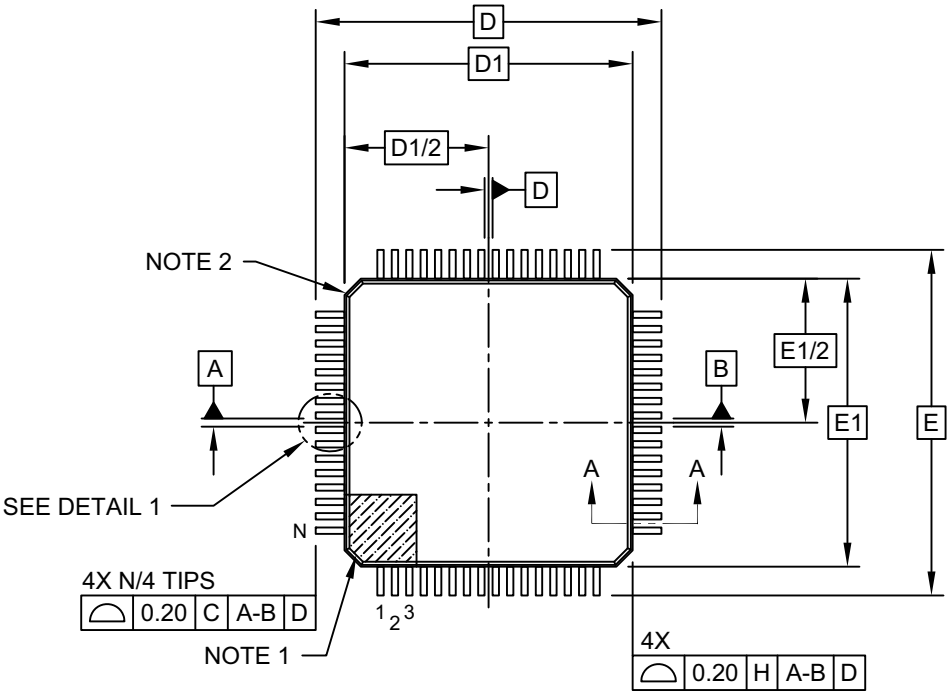
## 34.2 Package Details

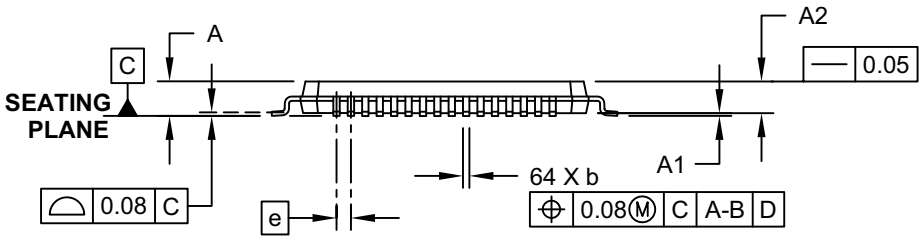
The following sections give the technical details of the packages.

### 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW

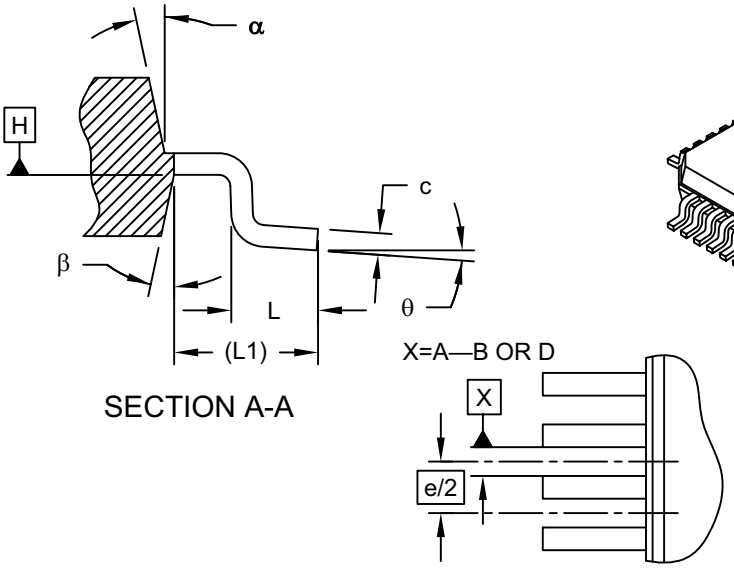


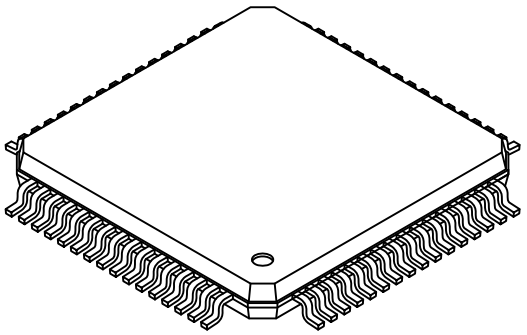

SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

### 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2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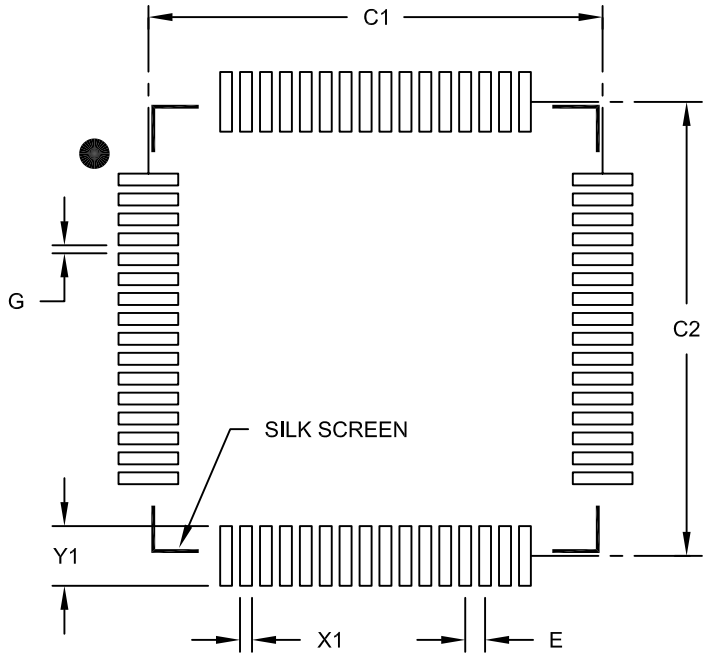
64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

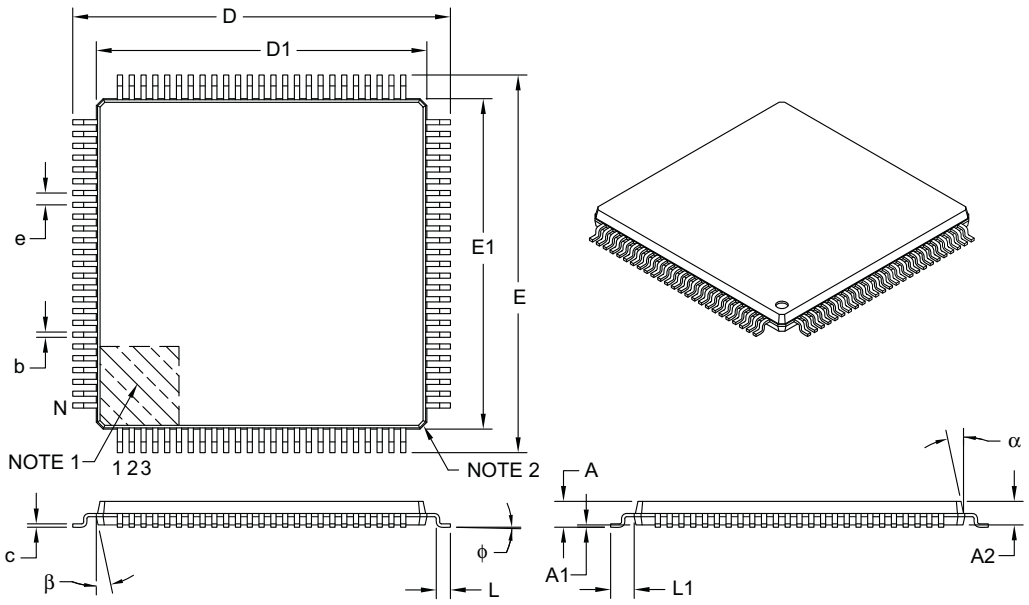
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2085B

### 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 16.00 BSC | |
| Overall Length | D | | 16.00 BSC | |
| Molded Package Width | E1 | | 14.00 BSC | |
| Molded Package Length | D1 | | 14.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B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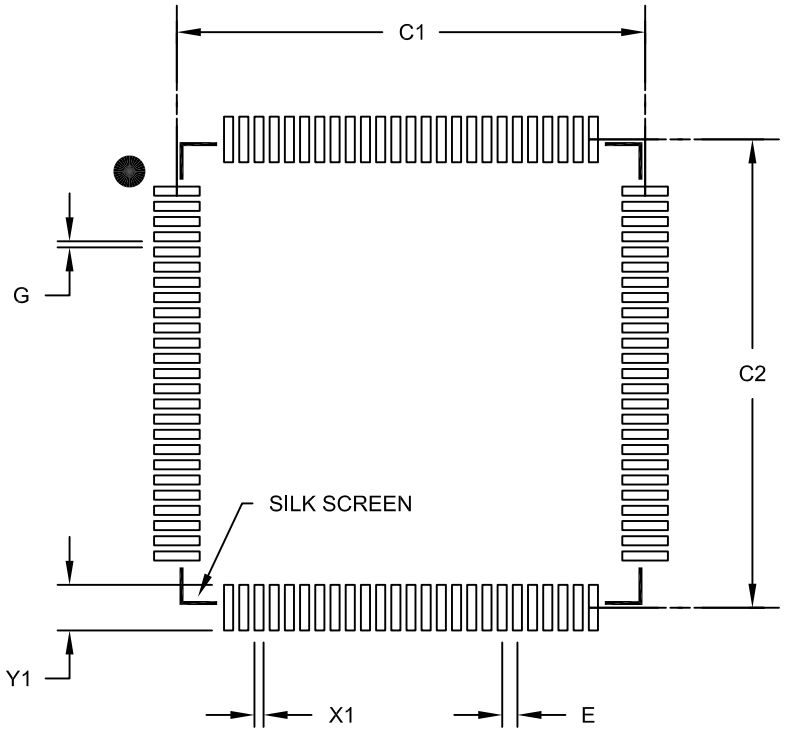
100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 15.40 | |
| Contact Pad Spacing | C2 | | 15.40 | |
| Contact Pad Width (X100) | X1 | | | 0.30 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

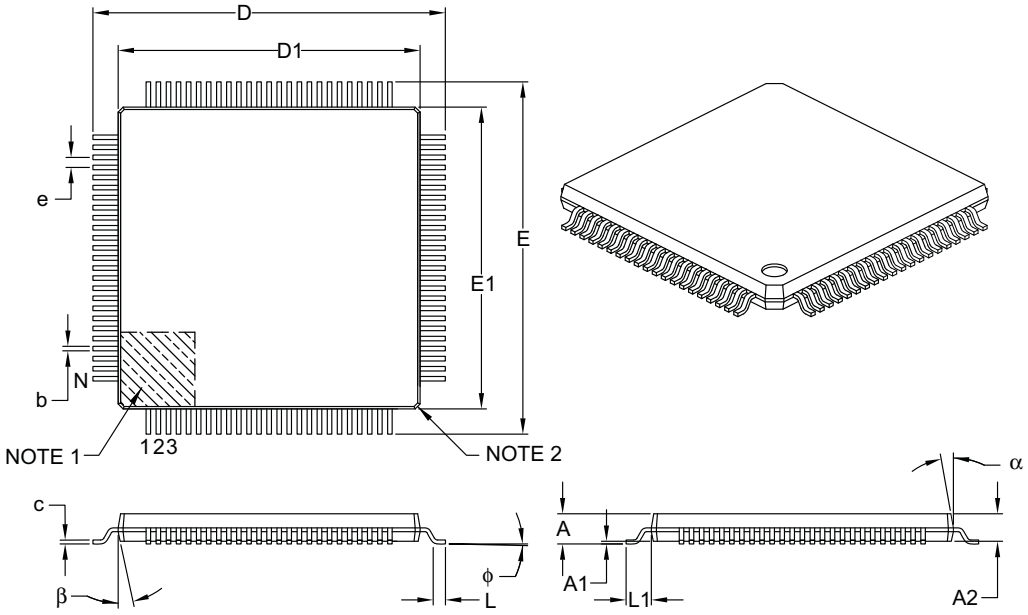
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

### 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 100 | |
| Lead Pitch | e | | 0.40 BSC | |
| Overall Height | A | – | – | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | – | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 14.00 BSC | |
| Overall Length | D | | 14.00 BSC | |
| Molded Package Width | E1 | | 12.00 BSC | |
| Molded Package Length | D1 | | 12.00 BSC | |
| Lead Thickness | c | 0.09 | – | 0.20 |
| Lead Width | b | 0.13 | 0.18 | 0.23 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B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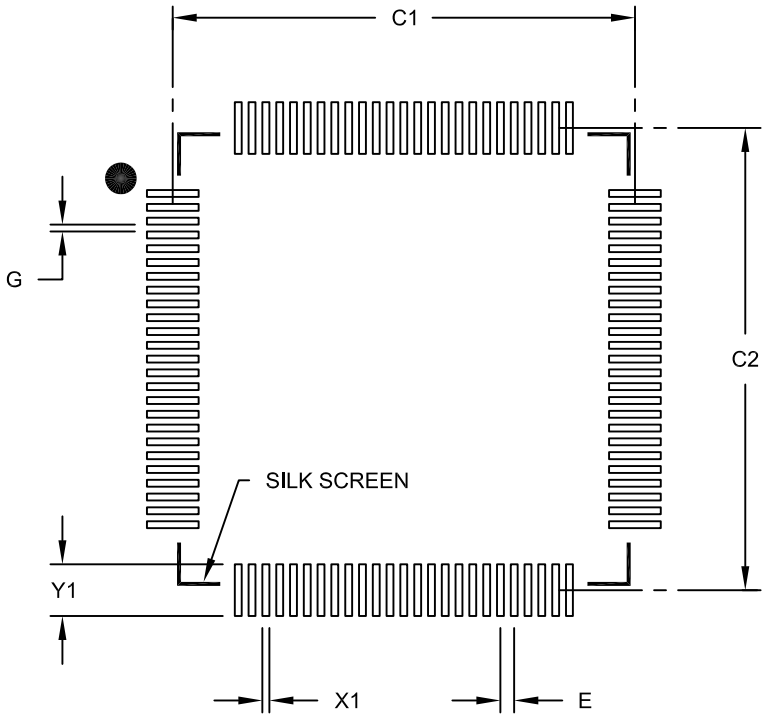
100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Contact Pad Spacing | C1 | | 13.40 | |
| Contact Pad Spacing | C2 | | 13.40 | |
| Contact Pad Width (X100) | X1 | | | 0.20 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

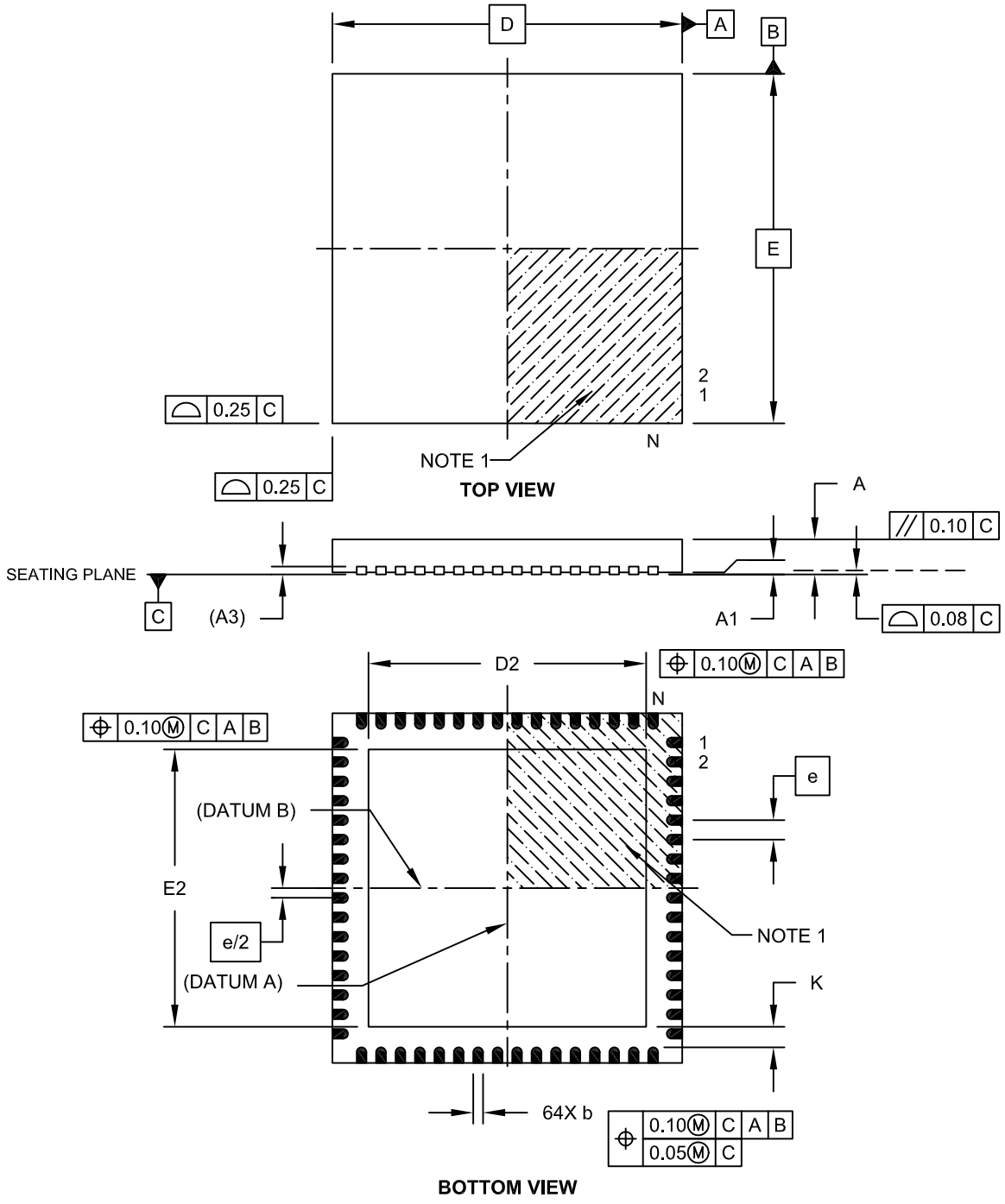
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-149C Sheet 1 of 2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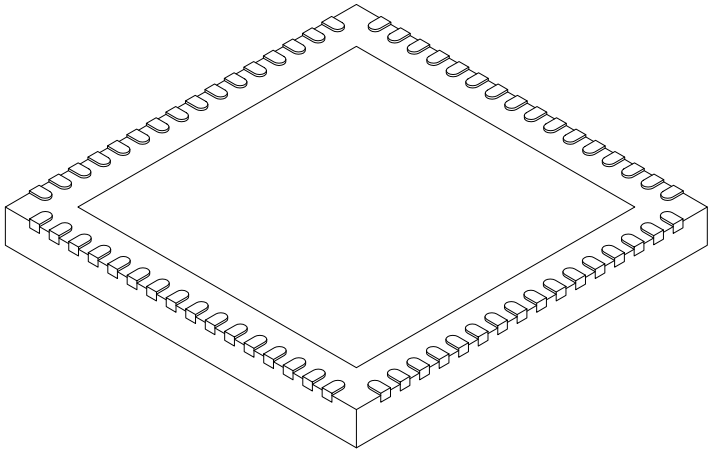
**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]**
**With 7.15 x 7.15 Exposed Pad [QFN]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 7.05 | 7.15 | 7.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 7.05 | 7.15 | 7.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

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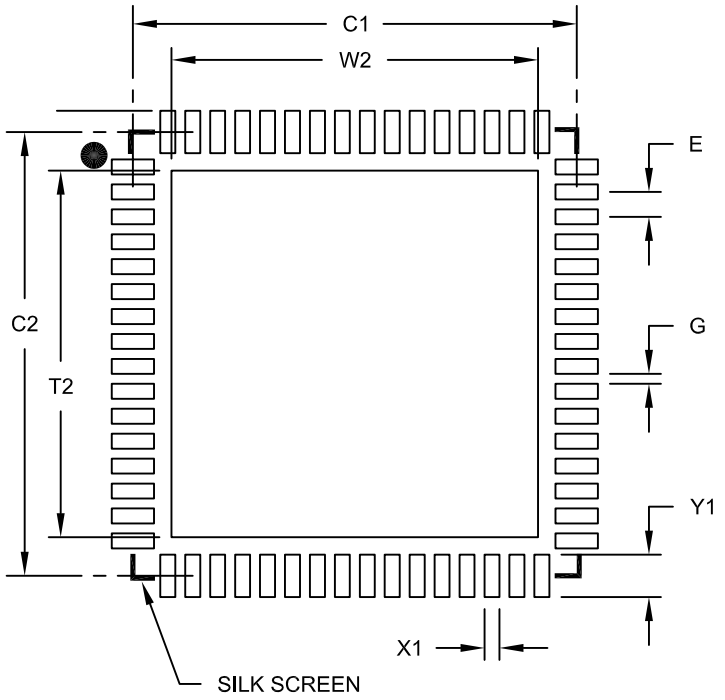
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 7.35 |
| Optional Center Pad Length | T2 | | | 7.35 |
| Contact Pad Spacing | C1 | | 8.90 | |
| Contact Pad Spacing | C2 | | 8.90 | |
| Contact Pad Width (X64) | X1 | | | 0.30 |
| Contact Pad Length (X64) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A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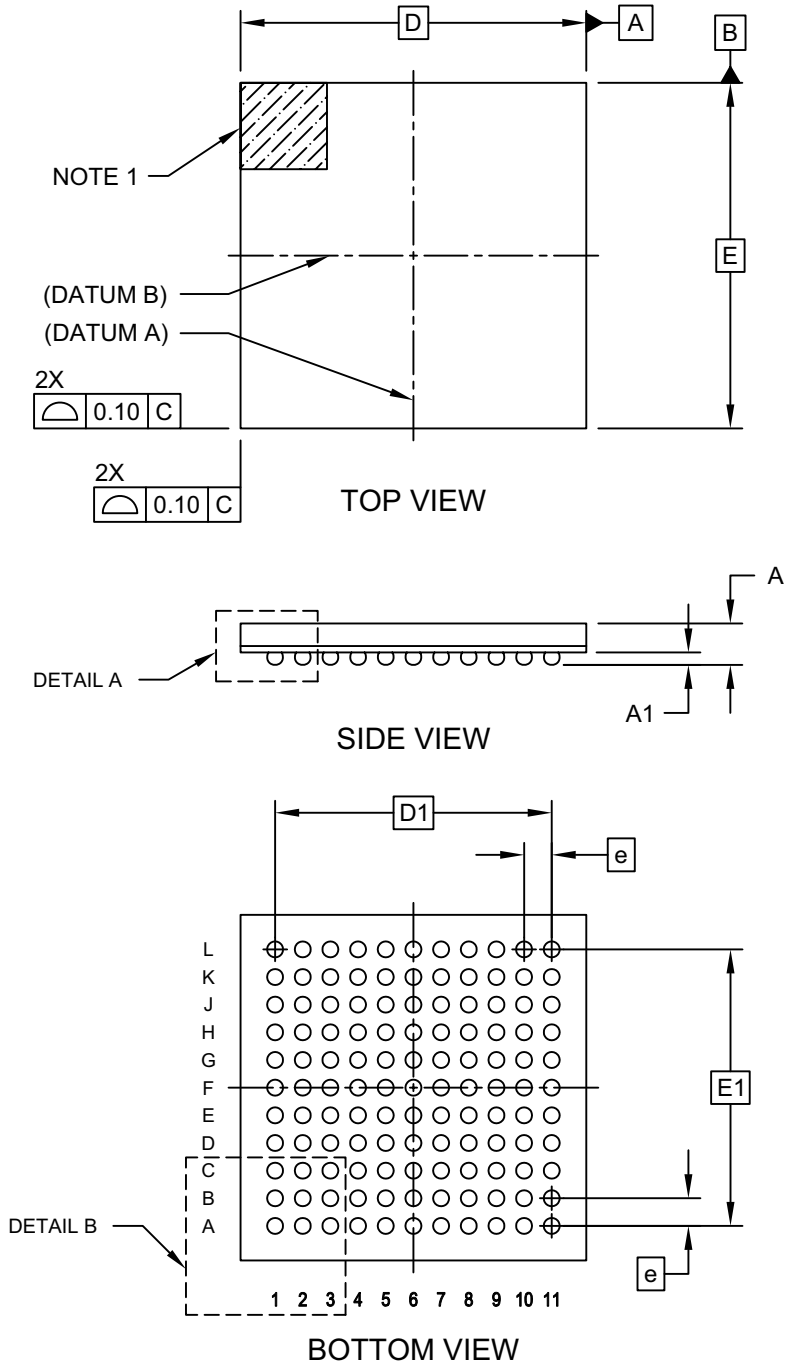
**121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]**

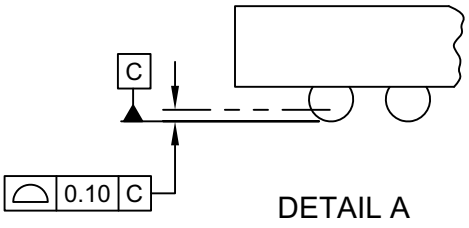
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



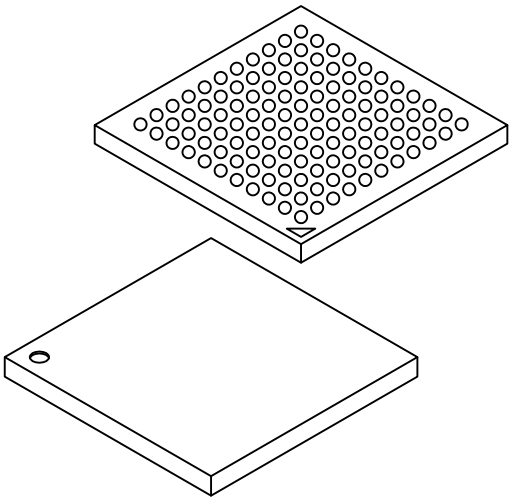

Microchip Technology Drawing C04-148 Rev F Sheet 1 of 2

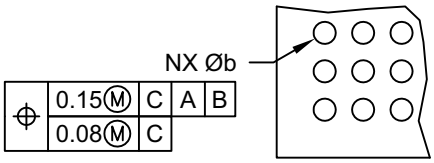
### 121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




DETAIL A






DETAIL B

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Contacts | N | | 121 | |
| Contact Pitch | e | | 0.80 BSC | |
| Overall Height | A | 1.00 | 1.10 | 1.20 |
| Ball Height | A1 | 0.25 | 0.30 | 0.35 |
| Overall Width | E | | 10.00 BSC | |
| Array Width | E1 | | 8.00 BSC | |
| Overall Length | D | | 10.00 BSC | |
| Array Length | D1 | | 8.00 BSC | |
| Contact Diameter | b | 0.35 | 0.40 | 0.45 |

Notes:

1. Ball A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
3. The outer rows and colums of balls are located with respect to datums A and B.
4. Ball interface to package body: 0.37mm nominal diameter.

Microchip Technology Drawing C04-148 Rev F Sheet 2 of 2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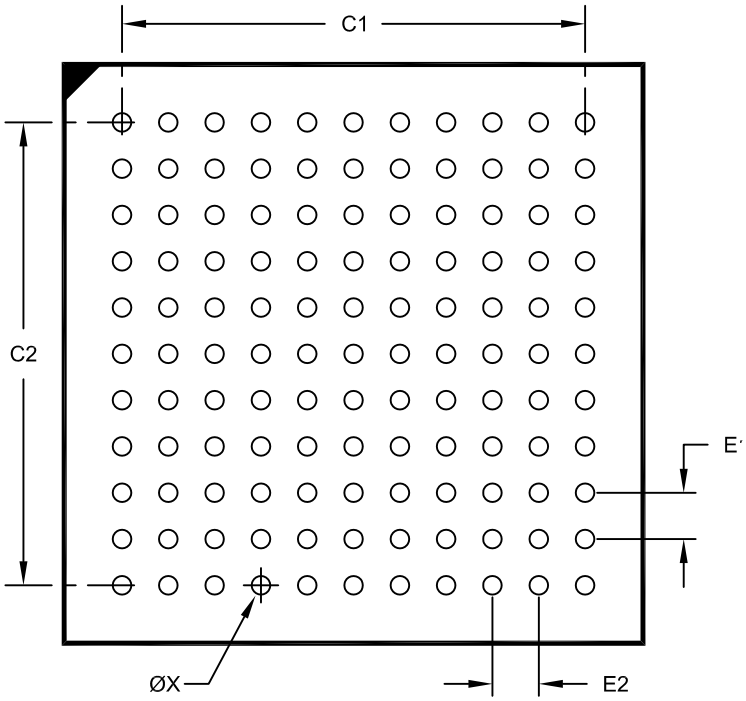
## 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E1 | | 0.80 BSC | |
| Contact Pitch | E2 | | 0.80 BSC | |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Diameter (X121) | X | | | 0.32 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D

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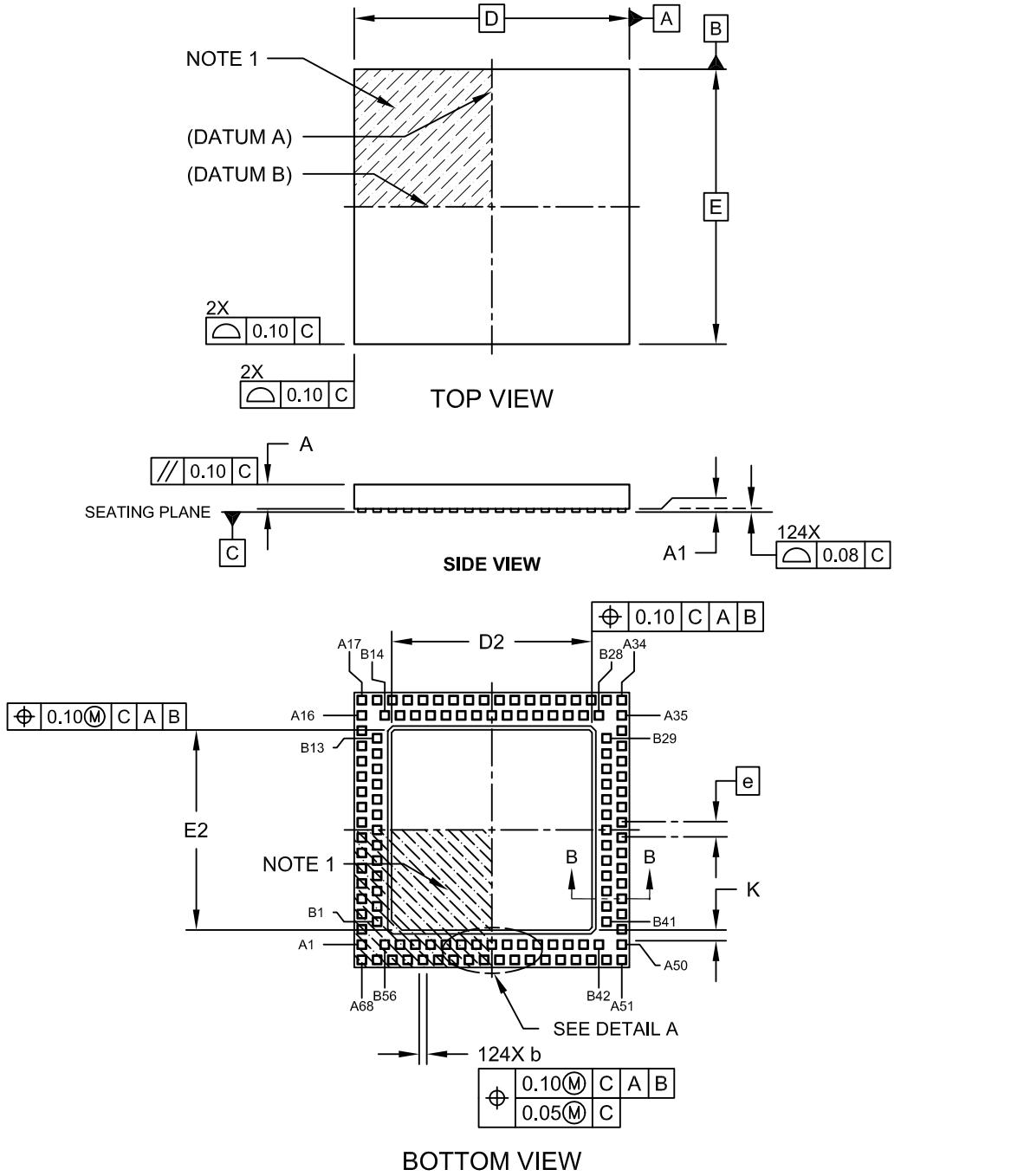
### 124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-193A Sheet 1 of 2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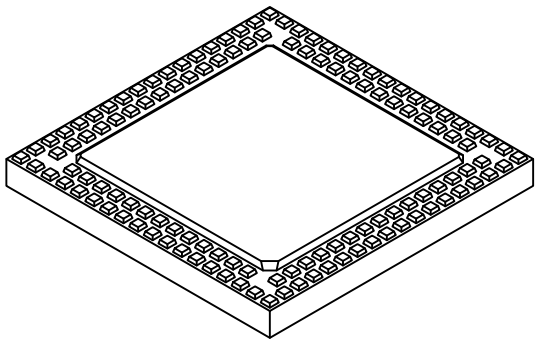
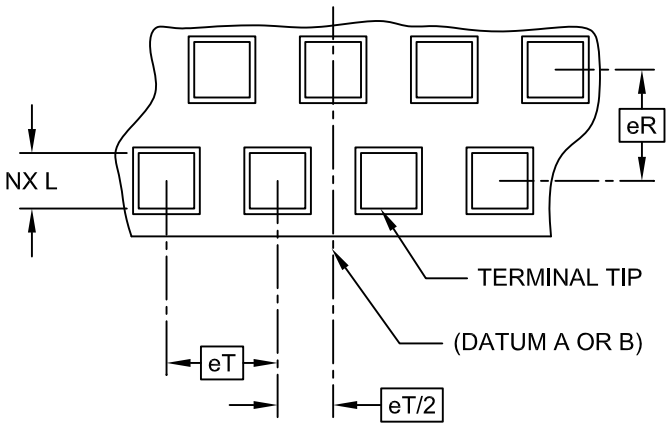
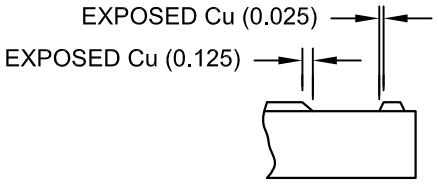
## 124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging






DETAIL A




SECTION B-B

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 124 | |
| Pitch | eT | | 0.50 BSC | |
| Pitch (Inner to outer terminal ring) | eR | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | - | 0.05 |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 6.40 | 6.55 | 6.70 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 6.40 | 6.55 | 6.70 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

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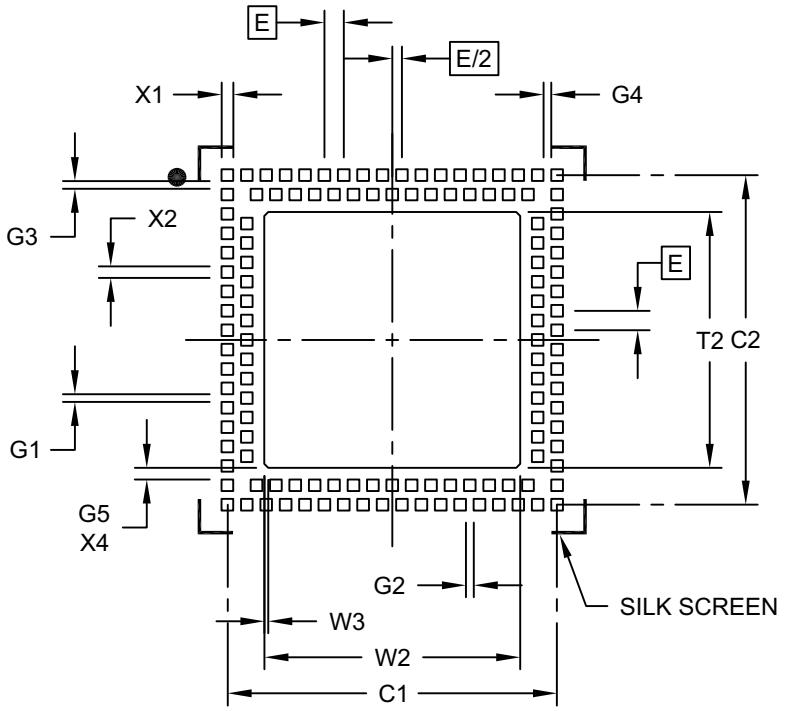
### 124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Pad Clearance | G1 | 0.20 | | |
| Pad Clearance | G2 | 0.20 | | |
| Pad Clearance | G3 | 0.20 | | |
| Pad Clearance | G4 | 0.20 | | |
| Contact to Center Pad Clearance (X4) | G5 | 0.30 | | |
| Optional Center Pad Width | T2 | | | 6.60 |
| Optional Center Pad Length | W2 | | | 6.60 |
| Optional Center Pad Chamfer (X4) | W3 | | 0.10 | |
| Contact Pad Spacing | C1 | | 8.50 | |
| Contact Pad Spacing | C2 | | 8.50 | |
| Contact Pad Width (X124) | X1 | | | 0.30 |
| Contact Pad Length (X124) | X2 | | | 0.30 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A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# APPENDIX A: MIGRATING FROM PIC32MX3XX/4XX TO PIC32MX5XX/6XX/7XX DEVICES

This appendix provides an overview of considerations for migrating from PIC32MX3XX/4XX devices to the PIC32MX5XX/6XX/7XX family of devices. The code developed for the PIC32MX3XX/4XX devices can be ported to the PIC32MX5XX/6XX/7XX devices after making the appropriate changes outlined below.

## A.1 DMA

PIC32MX5XX/6XX/7XX devices do not support stopping DMA transfers in Idle mode.

## A.2 Interrupts

PIC32MX5XX/6XX/7XX devices have persistent interrupts for some of the peripheral modules. This means that the interrupt condition for these peripherals must be cleared before the interrupt flag can be cleared.

For example, to clear a UART receive interrupt, the user application must first read the UART Receive register to clear the interrupt condition and then clear the associated UxIF flag to clear the pending UART interrupt. In other words, the UxIF flag cannot be cleared by software until the UART Receive register is read.

Table A-1 outlines the peripherals and associated interrupts that are implemented differently on PIC32MX5XX/6XX/7XX versus PIC32MX3XX/4XX devices.

In addition, on the SPI module, the IRQ numbers for the receive done interrupts were changed from 25 to 24 and the transfer done interrupts were changed from 24 to 25.

**TABLE A-1: PIC32MX3XX/4XX VERSUS PIC32MX5XX/6XX/7XX INTERRUPT IMPLEMENTATION DIFFERENCES**

| Module | Interrupt Implementation |
|---|---|
| Input Capture | To clear an interrupt source, read the Buffer Result (ICxBUF) register to obtain the number of capture results in the buffer that are below the interrupt threshold (specified by ICI<1:0> bits). |
| SPI | Receive and transmit interrupts are controlled by the SRXISEL<1:0> and STXISEL<1:0> bits, respectively. To clear an interrupt source, data must be written to, or read from, the SPIxBUF register to obtain the number of data to receive/transmit below the level specified by the SRXISEL<1:0> and STXISEL<1:0> bits. |
| UART | TX interrupt will be generated as soon as the UART module is enabled.<br>Receive and transmit interrupts are controlled by the URXISEL<1:0> and UTXISEL<1:0> bits, respectively. To clear an interrupt source, data must be read from, or written to, the UxRXREG or UxTXREG registers to obtain the number of data to receive/transmit below the level specified by the URXISEL<1:0> and UTXISEL<1:0> bits. |
| ADC | All samples must be read from the result registers (ADC1BUFx) to clear the interrupt source. |
| PMP | To clear an interrupt source, read the Parallel Master Port Data Input/Output (PMDIN/PMDOUT) register. |

# APPENDIX B: REVISION HISTORY

## Revision A (August 2009)

This is the initial released version of this document.

## Revision B (November 2009)

The revision includes the following global update:

Added Note 2 to the shaded table that appears at the beginning of each chapter. This new note provides information regarding the availability of registers and their associated bits.

Other major changes are referenced by their respective chapter/section in Table B-1.

**TABLE B-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"** | Added the following devices:<br>- PIC32MX575F256L<br>- PIC32MX695F512L<br>- PIC32MX695F512H<br>The 100-pin TQFP pin diagrams have been updated to reflect the current pin name locations (see the **"Pin Diagrams"** section).<br>Added the 121-pin Ball Grid Array (XBGA) pin diagram.<br>Updated Table 1: "PIC32 USB and CAN – Features"<br>Added the following tables:<br>- Table 4: "Pin Names: PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L, PIC32MX575F256L and PIC32MX575F512L Devices"<br>- Table 5: "Pin Names: PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices"<br>- Table 6: "Pin Names: PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices"<br>Updated the following pins as 5V tolerant:<br>- 64-pin QFN: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)<br>- 64-pin TQFP: Pin 36 (D-/RG3) and Pin 37 (D+/RG2)<br>- 100-pin TQFP: Pin 56 (D-/RG3) and Pin 57 (D+/RG2) |
| **1.0 "Guidelines for Getting Started with 32-bit Microcontrollers"** | Removed the last sentence of **1.3.1 "Internal Regulator Mode"**.<br>Removed Section 2.3.2 "External Regulator Mode" |


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**TABLE B-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **4.0 "Memory Organization"** | Updated all register tables to include the Virtual Address and All Resets columns.<br>Updated the title of Figure 4-4 to include the PIC32MX575F256L device.<br>Updated the title of Figure 4-6 to include the PIC32MX695F512L and PIC32MX695F512H devices. Also changed PIC32MX795F512L to PIC32MX795F512**H**.<br>Updated the title of Table 4-3 to include the PIC32MX695F512H device.<br>Updated the title of Table 4-5 to include the PIC32MX575F5256L device.<br>Updated the title of Table 4-6 to include the PIC32MX695F512L device.<br>Reversed the order of Table 4-11 and Table 4-12.<br>Reversed the order of Table 4-14 and Table 4-15.<br>Updated the title of Table 4-15 to include the PIC32MX575F256L and PIC32MX695F512L devices.<br>Updated the title of Table 4-45 to include the PIC32MX575F256L device.<br>Updated the title of Table 4-47 to include the PIC32MX695F512H and PIC32MX695F512L devices. |
| **1.0 "I/O Ports"** | Updated the second paragraph of **1.1.2 "Digital Inputs"** and removed Table 12-1. |
| **22.0 "10-bit Analog-to-Digital Converter (ADC)"** | Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2). |
| **1.0 "Special Features"** | Removed references to the ENVREG pin in **1.3 "On-Chip Voltage Regulator"**.<br>Updated the first sentence of **1.3.1 "On-Chip Regulator and POR"** and **1.3.2 "On-Chip Regulator and BOR"**.<br>Updated the Connections for the On-Chip Regulator (see Figure 1-2). |
| **1.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings and added Note 3.<br>Added Thermal Packaging Characteristics for the 121-pin XBGA package (see Table 1-3).<br>Updated the Operating Current ($I_{DD}$) DC Characteristics (see Table 1-5).<br>Updated the Idle Current ($I_{IDLE}$) DC Characteristics (see Table 1-6).<br>Updated the Power-Down Current ($I_{PD}$) DC Characteristics (see Table 1-7).<br>Removed Note 1 from the Program Flash Memory Wait State Characteristics (see Table 1-12).<br>Updated the SPIx Module Slave Mode (CKE = 1) Timing Characteristics, changing SP52 to SP35 between the MSb and Bit 14 on SDOx (see Figure 1-13). |
| **1.0 "Packaging Information"** | Added the 121-pin XBGA package marking information and package details. |
| **"Product Identification System"** | Added the definition for BG (121-lead 10x10x1.1 mm, XBGA).<br>Added the definition for Speed. |

### Revision C (February 2010)

The revision includes the following updates, as described in Table B-2:

**TABLE B-2: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"** | Added the following devices:<br>• PIC32MX675F256H<br>• PIC32MX775F256H<br>• PIC32MX775F512H<br>• PIC32MX675F256L<br>• PIC32MX775F256L<br>• PIC32MX775F512L<br>Added the following pins:<br>• EREFCLK<br>• ECRSDV<br>• AEREFCLK<br>• AECRSDV<br>Added the EREFCLK and ECRSDV pins to Table 5 and Table 6. |
| **1.0 "Device Overview"** | Updated the pin number pinout I/O descriptions for the following pin names in Table 1-1:<br>• SCL3 • SCL5 • RTCC • C1OUT<br>• SDA3 • SDA5 • CVREF- • C2IN-<br>• SCL2 • TMS • CVREF+ • C2IN+<br>• SDA2 • TCK • CVREFOUT • C2OUT<br>• SCL4 • TDI • C1IN- • PMA0<br>• SDA4 • TDO • C1IN+ • PMA1<br>Added the following pins to the Pinout I/O Descriptions table (Table 1-1):<br>• EREFCLK<br>• ECRSDV<br>• AEREFCLK<br>• AECRSDV |
| **4.0 "Memory Organization"** | Added new devices and updated the virtual and physical memory map values in Figure 4-4.<br>Added new devices to Figure 4-5.<br>Added new devices to the following register maps:<br>• Table 4-3, Table 4-4, Table 4-6 and Table 4-7 (Interrupt Register Maps)<br>• Table 4-12 (I2C2 Register Map)<br>• Table 4-15 (SPI1 Register Map)<br>• Table 4-24 through Table 4-35 (PORTA-PORTG Register Maps)<br>• Table 4-36 and Table 4-37 (Change Notice and Pull-up Register Maps)<br>• Table 4-45 (CAN1 Register Map)<br>• Table 4-46 (CAN2 Register Map)<br>• Table 4-47 (Ethernet Controller Register Map)<br>Changed the bits named POSCMD to POSCMOD in Table 4-42 (Device Configuration Word Summary). |
| **1.0 "Special Features"** | Changed all references of POSCMD to POSCMOD in the Device Configuration Word 1 register (see Register 1-2). |
| **Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/6XX/7XX Devices"** | Added the new section Appendix . |


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## Revision D (May 2010)

The revision includes the following updates, as described in Table B-3:

**TABLE B-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers"** | Updated the initial Flash memory range to 64K.<br>Updated the initial SRAM memory range to 16K.<br>Added the following devices (see Table 1, Table 2, Table 3 and the Pin Diagrams):<br>• PIC32MX534F064H<br>• PIC32MX564F064H<br>• PIC32MX664F064H<br>• PIC32MX564F128H<br>• PIC32MX664F128H<br>• PIC32MX764F128H<br>• PIC32MX534F064L<br>• PIC32MX564F064L<br>• PIC32MX664F064L<br>• PIC32MX564F128L<br>• PIC32MX664F128L<br>• PIC32MX764F128L |
| **4.0 "Memory Organization"** | Added new Memory Maps (Figure 4-1, Figure 4-2 and Figure 4-3).<br>The bit named I2CSIF was changed to I2C1SIF and the bit named I2CBIF was changed to I2C1BIF in the Interrupt Register Map tables (Table 4-2, Table 4-3, Table 4-4, Table 4-5, Table 4-6 and Table 4-7)<br>Added the following devices to the Interrupt Register Map (Table 4-2):<br>• PIC32MX534F064H<br>• PIC32MX564F064H<br>• PIC32MX564F128H<br>Added the following devices to the Interrupt Register Map (Table 4-3):<br>• PIC32MX664F064H<br>• PIC32MX664F128H<br>Added the following device to the Interrupt Register Map (Table 4-4):<br>• PIC32MX764F128H<br>Added the following devices to the Interrupt Register Map (Table 4-5):<br>• PIC32MX534F064L<br>• PIC32MX564F064L<br>• PIC32MX564F128L<br>Added the following devices to the Interrupt Register Map (Table 4-6):<br>• PIC32MX664F064L<br>• PIC32MX664F128L<br>Added the following device to the Interrupt Register Map (Table 4-7):<br>• PIC32MX764F128L |

**TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **4.0 "Memory Organization" (Continued)** | Made the following bit name changes in the I2C1, I2C3, I2C4 and I2C5 Register Map (Table 4-11):<br>• I2C3BRG SFR: I2C1BRG was changed to I2C3BRG<br>• I2C4BRG SFR: I2C1BRG was changed to I2C4BRG<br>• I2C5BRG SFR: I2C1BRG was changed to I2C5BRG<br>• I2C4TRN SFR: I2CT1DATA was changed to I2CT2ADATA<br>• I2C4RCV SFR: I2CR2DATA was changed to I2CR2ADATA<br>• I2C5TRN SFR: I2CT1DATA was changed to I2CT3ADATA<br>• I2C5RCV SFR: I2CR1DATA was changed to I2CR3ADATA<br>Added the RTSMD bit and UEN<1:0> bits to the UART1A, UART1B, UART2A, UART2B, UART3A and UART3B Register Map (Table 4-13)<br>Added the SIDL bit to the DMA Global Register Map (Table 4-17).<br>Changed the CM bit to CMR in the System Control Register Map (Table 4-23).<br>Added the following devices to the I2C2, SPI1, PORTA, PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-12, Table 4-14, Table 4-24, Table 4-27, Table 4-29, Table 4-31, Table 4-33, Table 4-35 and Table 4-36):<br>• PIC32MX534F064L<br>• PIC32MX564F064L<br>• PIC32MX564F128L<br>• PIC32MX664F064L<br>• PIC32MX664F128L<br>• PIC32MX764F128L<br>Added the following devices to the PORTC, PORTD, PORTE, PORTF, PORTG, Change Notice and Pull-up Register Maps (Table 4-26, Table 4-28, Table 4-30, Table 4-32, Table 4-34 and Table 4-37):<br>• PIC32MX534F064H<br>• PIC32MX564F064H<br>• PIC32MX564F128H<br>• PIC32MX664F064H<br>• PIC32MX664F128H<br>• PIC32MX764F128H<br>Added the following devices to the CAN1 Register Map (Table 4-45):<br>• PIC32MX534F064H<br>• PIC32MX564F064H<br>• PIC32MX564F128H<br>• PIC32MX764F128H<br>• PIC32MX534F064L<br>• PIC32MX564F064L<br>• PIC32MX564F128L<br>• PIC32MX764F128L<br>Added the following devices to the Ethernet Controller Register Map (Table 4-47):<br>• PIC32MX664F064H<br>• PIC32MX664F128H<br>• PIC32MX764F128H<br>• PIC32MX664F064L<br>• PIC32MX664F128L<br>• PIC32MX764F128L |


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**TABLE B-3: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **1.0 "Electrical Characteristics"** | Updated the Typical and Maximum DC Characteristics: Operating Current (IDD) in Table 1-5.<br>Updated the Typical and Maximum DC Characteristics: Idle Current (IIDLE) in Table 1-6.<br>Updated the Typical and Maximum DC Characteristics: Power-Down Current (IPD) in Table 1-7.<br>Added DC Characteristics: Program Memory parameters D130a and D132a in Table 1-11.<br>Added the Internal Voltage Reference parameter (D305) to the Comparator Specifications in Table 1-13. |

### Revision E (July 2010)

Minor corrections were incorporated throughout the document.

### Revision F (December 2010)

The revision includes the following global update:

VCAP/VDDCORE has been changed to: VCAP/VCORE

Other major changes are referenced by their respective chapter/section in Table B-4:

**TABLE B-4: SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers** | Removed the following Analog Feature: FV tolerant input pins (digital pins only)<br>Updated the term LIN 1.2 support as LIN support for the peripheral feature: Six UART modules with: RS-232, RS-485, and LIN support |
| **1.0 “Device Overview”** | Updated the value of 64-pin QFN/TQFP pin number for the following pin names: PMA0, PMA1 and ECRSDV |
| **4.0 “Memory Organization”** | The following register map tables were updated:<br>• Table 4-2:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT<br>- Changed bits 25/9/-24/8 to U5IS<1:0> in IPC12<br>- Added note 2<br>• Table 4-3 through Table 4-7:<br>- Changed bits 24/8-24/10 to SRIPL<2:0> in INTSTAT<br>- Changed bits 25/9-24/8 to U5IS<1:0> in IPC12<br>• Table 4-3:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Added note 2<br>• Table 4-4:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8 to I2C5BIE in IEC1<br>- Added note 2 references<br>• Table 4-5:<br>- Changed bits 24/8 to I2C5BIF in IFS1<br>- Changed bits 24/8 to I2C5BIE in IEC1<br>- Added note 2 references<br>• Table 4-6:<br>- Changed bit 24/8 to I2C5BIF in IFS1<br>- Updated the bit value of bit 24/8 as I2C5BIE for the IEC1 register.<br>- Added note 2<br>• Table 4-7:<br>- Changed bit 25/9 to I2C5SIF in IFS1<br>- Changed bit 24/8 as I2C5BIF in IFS1<br>- Changed bit 25/9 as I2C5SIE in IEC1<br>- Changed bit 24/8 as I2C5BIE in IEC1<br>- Added note 2 references<br>• Added note 2 to Table 4-8<br>• Updated the All Resets values for the following registers in Table 4-11: I2C3CON, I2C4CON, I2C5CON and I2C1CON.<br>• Updated the All Resets values for the I2C2CON register in Table 4-12 |


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**TABLE B-4: SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **4.0 "Memory Organization"** (Continued) | • Table 4-13:<br>- Changed register U4RG to U1BRG<br>- Changed register U5RG to U3BRG<br>- Changed register U6RG to U2BRG<br>• Table 4-14:<br>- Updated the All Resets values for the following registers: SPI3STAT, SPI2STAT and SPI4STAT<br>• Table 4-15: Updated the All Resets values for the SPI1STAT register<br>• Table 4-17: Added note 2<br>• Table 4-19: Added note 2<br>• Table 4-20: Updated the All Resets values for the CM1CON and CM2CON registers<br>• Table 4-21:<br>- Updated the All Resets values as `0000` for the CVRCON register<br>- Updated note 2<br>• Table 4-38: Updated the All Resets values for the PMSTAT register<br>• Table 4-40: Updated the All Resets values for the CHECON and CHETAG registers<br>• Table 4-42: Updated the bit value of bit 29/13 as '—' for the DEVCFG3 register<br>• Table 4-44:<br>- Updated the note references in the entire table<br>- Changed existing note 1 to note 4<br>- Added notes 1, 2 and 3<br>- Changed bits 23/7 in U1PWRC to UACTPND<br>- Changed register U1DDR to U1ADDR<br>- Changed register U4DTP1 to U1BDTP1<br>- Changed register U4DTP2 to U1BDTP2<br>- Changed register U4DTP3 to U1BDTP3<br>• Table 4-45:<br>- Updated the All Resets values for the C1CON and C1VEC registers<br>- Changed bits 30/14 in C1CON to FRZ<br>- Changed bits 27/11 in C1CON to CANBUSY<br>- Changed bits 22/6-16/0 in C1VEC to ICODE<6:0><br>- Changed bits 22/6-16/0 in C1TREC to RERRCNT<7:0><br>- Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0><br>• Table 4-46:<br>- Updated the All Resets values for the C2CON and C2VEC registers<br>- Changed bits 30/14 in C1CON to FRZ<br>- Changed bits 27/11 in C1CON to CANBUSY<br>- Changed bits 22/6-16/0 in C1VEC register to ICODE<6:0><br>- Changed bits 22/6-16/0 in C1TREC register to RERRCNT<7:0><br>- Changed bits 31/15-24/8 in C1TREC to TERRCNT<7:0> |

**TABLE B-4: SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **7.0 "Interrupt Controller"** | • Updated the following Interrupt Sources in Table 7-1:<br>- Changed IC2AM – I2C4 Master Event to: IC4M – I2C4 Master Event<br>- Changed IC3AM – I2C5 Master Event to: IC5M – I2C4 Master Event<br>- Changed U1E – UART1A Error to: U1E – UART1 Error<br>- Changed U4E – UART1B Error to: U4E – UART4 Error<br>- Changed U1RX – UART1A Receiver to: U1RX – UART1 Receiver<br>- Changed U4RX – UART1B Receiver to: U4RX – UART4 Receiver<br>- Changed U1TX – UART1A Transmitter to: U1TX – UART1 Transmitter<br>- Changed U4TX – UART1B Transmitter to: U4TX – UART4 Transmitter<br>- Changed U6E – UART2B Error to: U6E – UART6 Error<br>- Changed U6RX – UART2B Receiver to: U6RX – UART6 Receiver<br>- Changed U6TX – UART2B Transmitter to: U6TX – UART6 Transmitter<br>- Changed U5E – UART3B Error to: U5E – UART5 Error<br>- Changed U5RX – UART3B Receiver to: U5RX – UART5 Receiver<br>- Changed U5TX – UART3B Transmitter to: U5TX – UART5 Transmitter |
| **1.0 "Oscillator Configuration"** | Updated Figure 1-1 |
| **1.0 "Output Compare"** | Updated Figure 1-1 |
| **1.0 "Ethernet Controller"** | Added a note on using the Ethernet controller pins (see note above Table 1-3) |
| **1.0 "Comparator Voltage Reference ($CV_{REF}$)"** | Updated the note in Figure 1-1 |
| **1.0 "Special Features"** | Updated the bit description for bit 10 in Register 1-2<br>Added notes 1 and 2 to Register 1-4 |
| **1.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings:<br>• Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD}$ < 2.3V - 0.3V to +3.6V was updated<br>• Voltage on $V_{BUS}$ with respect to $V_{SS}$ - 0.3V to +5.5V was added<br>Updated the maximum value of DC16 as 2.1 in Table 1-4<br>Updated the Typical values for the following parameters: DC20b, DC20c, DC21c, DC22c and DC23c (see Table 1-5)<br>Updated Table 1-11:<br>• Removed the following DC Characteristics: Programming temperature 0°C ≤ TA ≤ +70°C (25°C recommended)<br>• Updated the Minimum value for the Parameter number D131 as 2.3<br>• Removed the Conditions for the following Parameter numbers: D130, D131, D132, D135, D136 and D137<br>• Updated the condition for the parameter number D130a and D132a<br>Updated the Minimum, Typical and Maximum values for parameter D305 in Table 1-13<br>Added note 2 to Table 1-18<br>Updated the Minimum and Maximum values for parameter F20b (see Table 1-19)<br>Updated the following figures:<br>• Figure 1-4<br>• Figure 1-9<br>• Figure 1-22<br>• Figure 1-23 |
| **Appendix A: "Migrating from PIC32MX3XX/4XX to PIC32MX5XX/ 6XX/7XX Devices"** | Removed the A.3 Pin Assignments sub-section. |


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## Revision G (May 2011)

The revision includes the following global updates:

- All references to VDDCORE/VCAP have been changed to: VCORE/VCAP
- Added references to the new V-Temp temperature range: -40ºC to +105ºC

This revision also includes minor typographical and formatting changes throughout the data sheet text. Major updates are referenced by their respective section in Table B-5.

**TABLE B-5: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **High-Performance, USB, CAN and Ethernet 32-bit Flash Microcontrollers** | Removed the shading for all D- and D+ pins in all pin diagrams. |
| **1.0 "Device Overview"** | Updated the VBUS description in Table 1-1. |
| **1.0 "Guidelines for Getting Started with 32-bit Microcontrollers"** | Added **"Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input."**. |
| **4.0 "Memory Organization"** | Added Note 3 to the Interrupt Register Map tables (see Table 4-2 through Table 4-7. |
| **22.0 "10-bit Analog-to-Digital Converter (ADC)"** | Updated the ADC Conversion Clock Period Block Diagram (see Figure 22-2). |
| **1.0 "Comparator Voltage Reference (CVREF)"** | Updated the Comparator Voltage Reference Block Diagram (see Figure 1-1). |
| **1.0 "Special Features"** | Removed the second paragraph from **1.3.1 "On-Chip Regulator and POR"**. |
| **1.0 "Electrical Characteristics"** | Added the new V-Temp temperature range (-40ºC to +105ºC) to the heading of all specification tables.<br><br>Updated the Ambient temperature under bias, updated the Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V, and added Voltage on VBUS with respect to Vss in Absolute Maximum Ratings.<br><br>Added the characteristic, DC5a to Operating MIPS vs. Voltage (see Table 1-1).<br><br>Updated or added the following parameters to the Operating Current (IDD) DC Characteristics: DC20, DC20b, DC23, and DC23b (see Table 1-5).<br><br>Added the following parameters to the Idle Current (IIDLE) DC Characteristics: DC30b, DC33b, DC34c, DC35c, and DC36c (see Table 1-6).<br><br>Added the following parameters to the Power-down Current (IPD) DC Characteristics: DC40g, DC40h, DC40i, and DC41g, (see Table 1-7).<br><br>Added parameter IM51 and Note 3 to the I2Cx Bus Data Timing Requirements (Master Mode) (see Table 1-32).<br><br>Updated the 10-bit ADC Conversion Rate Parameters (see Table 1-37).<br><br>Updated parameter AD57 (TSAMP) in the Analog-to-Digital Conversion Timing Requirements (see Table 1-38). |
| **1.0 "Packaging Information"** | Updated the 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] packing diagram. |
| **Product Identification System** | Added the new V-Temp (V) temperature information. |

## Revision H (March 2013)

This revision includes the following global updates:

- Where applicable, control register tables have been added to the document
- All references to VCORE were removed
- All occurrences of XBGA have been updated to: TFBGA
- All occurrences of VUSB have been updated to: VUSB3V3

This revision also includes minor typographical and formatting changes throughout the data sheet text.

All other significant changes are referenced by their respective section in Table B-6.

**TABLE B-6: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"** | Updated Core features.<br>Added the VTLA to the Packages table.<br>Added Note 5 to the Feature tables (see Table 1, Table 2, and Table 3). |
| **Section 2.0 "Guidelines for Getting Started with 32-bit MCUs"** | The Recommended Minimum Connection was updated (see Figure 2-1). |
| **Section 5.0 "Flash Program Memory"** | A note regarding Flash page size and row size was added. |
| **Section 8.0 "Oscillator Configuration"** | The RP resistor was added and Note 1 was updated in the Oscillator Diagram (see Figure 8-1). |
| **Section 31.0 "Electrical Characteristics"** | Added Note 1 to Operating MIPS vs. Voltage (see Table 31-1).<br>Added the VTLA package to Thermal Packaging Characteristics (see Table 31-3).<br>Added Note 2 to DC Temperature and Voltage Specifications (see Table 31-4).<br>Updated Note 2 in the Operating Current DC Characteristics (see Table 31-5).<br>Updated Note 1 in the Idle Current DC Characteristics (see Table 31-6).<br>Updated Note 1 in the Power-Down Current DC Characteristics (see Table 31-7).<br>Updated the I/O Pin Output Specifications (see Table 31-9).<br>Added Note 2 to the BOR Electrical Characteristics (see Table 31-10).<br>Added Note 3 to the Comparator Specifications (see Table 31-13).<br>Parameter D320 (VCORE) was removed (see Table 31-15).<br>Updated the Minimum value for parameter OS50 (see Table 31-18).<br>Parameter SY01 (TPWRT) was removed (see Table 31-22).<br>Note 1 was added and the conditions for parameters ET3, ET4, ET7, and ET9 were updated in the Ethernet Module Specifications (see Table 31-35).<br>Added Note 6 to the ADC Module Specifications (see Table 31-36).<br>Added Note 3 to the 10-bit ADC Conversion Rate Parameter (see Table 31-37).<br>Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 31-38).<br>The following figures were added:<br>**Figure 31-19: "MDIO Sourced by the PIC32 Device"**<br>**Figure 31-21: "Transmit Signal Timing Relationships at the MII"**<br>**Figure 31-22: "Receive Signal Timing Relationships at the MII"** |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | This new chapter was added. |
| **Section 33.0 "Packaging Information"** | Added the 124-lead VTLA package information (see **Section 33.1 "Package Marking Information"** and **Section 33.2 "Package Details"**). |
| **"Product Identification System"** | Added the TL definition for VTLA packages. |


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## Revision J (September 2016)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-7.

**TABLE B-7: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Graphics Interface, USB, CAN, and Ethernet"** | Updated Communication Interfaces for LIN support to 2.1.<br>Updated Qualification and Class B Support to AEC-Q100 REVH. |
| **2.0 "Guidelines for Getting Started with 32-bit MCUs"** | The Recommended Minimum Connection diagram was updated (see Figure 2-1).<br>The Example of $\overline{\text{MCLR}}$ Pin Connections diagram was updated (see Figure 2-2).<br>**2.12 "EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations"** was added. |
| **4.0 "Memory Organization"** | The SFR Memory Map was added (see Table 4-1). |
| **7.0 "Interrupt Controller"** | The UART interrupt sources were updated in the Interrupt IRQ, Vector, and Bit location table (see Table 7-1). |
| **8.0 "Oscillator Configuration"** | Updated the bit value definitions for the TUN<5:0> bits in the OCSTUN register (see Register 8-2). |
| **15.0 "Watchdog Timer (WDT)"** | The content in this chapter was relocated from the Special Features chapter to its own chapter. |
| **18.0 "Serial Peripheral Interface (SPI)"** | The register map tables were combined (see Table 18-1). |
| **19.0 "Inter-Integrated Circuit ($I^2C$)"** | The register map tables were combined (see Table 19-1).<br>The PMADDR register was updated (see Register 21-3). |
| **21.0 "Parallel Master Port (PMP)"** | The bit value definitions for the ADRMUX<1:0> and CSF<1:0> bits in the PMCON register were updated (see Register 21-1). |
| **29.0 "Special Features"** | Removed the duplicate bit value definition for '010' in the DEVCFG2 register (see Register 29-3).<br>Note 1 was added to the Programming, Debugging, and Trace Ports block diagram (see Figure 29-2).<br>The DDPCON register was relocated (see Register 29-6).<br>The Device ID, Revision, and Configuration Summary was updated (see Table 29-2). |

**TABLE B-7: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **32.0 "Electrical Characteristics"** | Note 4 in the Operating Current specification was updated (see Table 32-5).<br>Note 3 in the Idle Current specification was updated (see Table 32-6).<br>Note 6 references in the Power-Down Current specification were updated (see Table 32-7).<br>The Program Memory parameters, D135, D136, and D137, and Note 4 were updated (see Table 32-11).<br>The Voltage Reference Specifications were updated (see Table 32-14).<br>Parameter DO50 (Cosco) was added to the Capacitive Loading Requirements on Output Pins (see Table 32-16).<br>The EJTAG Timing Characteristics were updated (see Figure 32-28).<br>The maximum value for parameters ET13 and ET14 were updated in the Ethernet Module Specifications (see Table 32-35).<br>Parameter PM7 (TDHOLD) was updated (see Table 32-40). |
| **34.0 "Packaging Information"** | Packaging diagrams were updated. |
| **Product Identification System** | The Speed and Program Memory Size were updated and Note 1 was added. |


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## Revision K (September 2019)

This revision includes typographical and formatting updates throughout the data sheet text. In addition, all SFR Register maps were moved from the Memory chapter to their respective peripheral chapters.

All other major updates are referenced by their respective section in Table B-8.

**TABLE B-8: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **7.0 "Interrupt Controller"** | Updated the U3 and U2 bit names in the following Register Maps:<br>• **TABLE 7-2: "Interrupt Register Map for PIC32MX534F064H, PIC32MX564F064H, PIC32MX564F128H, PIC32MX575F256H and PIC32MX575F512H Devices"**<br>• **TABLE 7-3: "Interrupt Register Map for PIC32MX664F064H, PIC32MX664F128H, PIC32MX675F256H, PIC32MX675F512H and PIC32MX695F512H Devices"**<br>• **TABLE 7-4: "Interrupt Register Map for PIC32MX764F128H, PIC32MX775F256H, PIC32MX775F512H and PIC32MX795F512H Devices"**<br>• **TABLE 7-5: "Interrupt Register Map for PIC32MX534F064L, PIC32MX564F064L, PIC32MX564F128L PIC32MX575F512L and PIC32MX575F256L Devices"**<br>• **TABLE 7-6: "Interrupt Register Map for PIC32MX664F064L, PIC32MX664F128L, PIC32MX675F256L, PIC32MX675F512L and PIC32MX695F512L Devices"**<br>• **TABLE 7-7: "Interrupt Register Map for PIC32MX764F128L, PIC32MX775F256L, PIC32MX775F512L and PIC32MX795F512L Devices"** |
| **18.0 "Serial Peripheral Interface (SPI)"** | Updated the FRMPOL bit description in **Register 18-1: "SPIx CON: SPI Control Register"** |
| **20.0 "Universal Asynchronous Receiver Transmitter (UART)"** | Updated **FIGURE 20-3: "Transmission (8-bit or 9-bit Data)"** |
| **21.0 "Parallel Master Port (PMP)"** | Updated bit 10 for **Register 21-2: "PMMODE: Parallel Port Mode Register"** |

**NOTES:**


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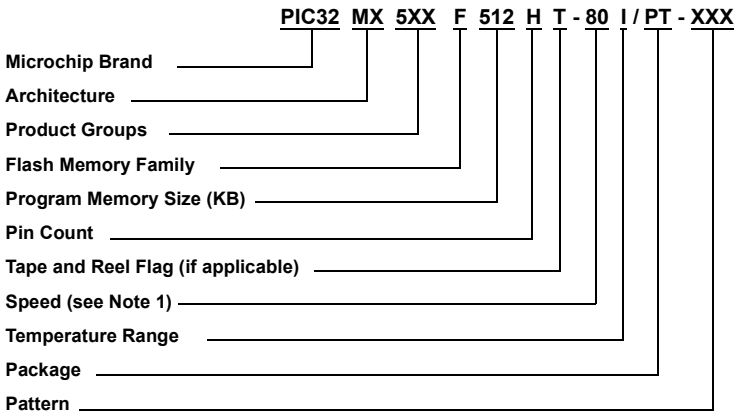


**Example:**

PIC32MX575F256H-80I/PT:
General purpose PIC32,
32-bit RISC MCU,
256 KB program memory,
64-pin, Industrial temperature,
TQFP package.

**Flash Memory Family**

| | |
|---|---|
| Architecture | MX = 32-bit RISC MCU core |
| Product Groups | 5XX = General purpose microcontroller family<br>6XX = General purpose microcontroller family<br>7XX = General purpose microcontroller family |
| Flash Memory Family | F = Flash program memory |
| Program Memory Size | **64 = 64K**<br>**128 = 128K**<br>256 = 256K<br>512 = 512K |
| Pin Count | H = 64-pin<br>L = 100-pin, 121-pin, 124-pin |
| Speed (see **Note 1**) | Blank or 80 = 80 MHz |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>V = -40°C to +105°C (V-Temp) |
| Package | PT = 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)<br>PT = 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)<br>PF = 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack)<br>MR = 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat)<br>BG = 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array)<br>TL = 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array) |
| Pattern | Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)<br>ES = Engineering Sample |

**Note 1: This option is not available for PIC32MX534/564/664/764 devices.**

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