Reference Design:

HFRD-05.0

Rev. 8; 11/08

As of July, 2008 this reference design board is no longer available.

Gerber files and schematics are available upon request.

REFERENCE DESIGN

Multi-Rate (1Gbps – 3.2Gbps) 850nm Small Form Factor Pluggable (SFP) Transceiver

maxim integrated™

Reference Design: Multi-Rate (1Gbps – 3.2Gbps) 850nm SFP Transceiver

Table of Contents

1 Overview

High Frequency Reference Design (HFRD) 5.0 is a complete optical transceiver targeted for the Small Form Factor Pluggable (SFP) Multisource Agreement (MSA) market and other high-speed optical transceiver applications.

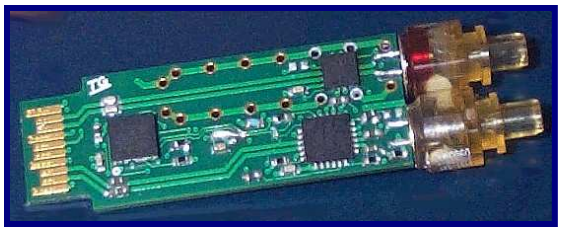
Data rates up to 3.2Gbps are attainable with the high-speed vertical cavity surface-emitting laser (VCSEL), high-speed PIN, the MAX3744 TIA, the MAX3748 limiting amplifier and the high-speed MAX3740 VCSEL driver. Average power and optical modulation amplitude (OMA) are held constant over the full temperature range using the APC loop of the MAX3740 and the Dallas Semiconductor DS1859 dual temperature-controlled digital resistors.

The DS1859 provides digital monitors for bias current, monitor diode current, received power, VCC and temperature. The DS1859 is compatible with SFF 8472 digital diagnostic requirements and has the capability of performing internal calibration.

The HFRD-5.0 transceiver reduces design time for SFP and other optical transmitters by providing the schematics, PC board layout, Gerber files and bill of materials for a complete SFP transceiver. Test data and typical performance from an assembled board are also given to aid in the evaluation of this reference design.

1.1 Features

- Schematics and Bill of Materials Provided
- Gerber Plot Files Available
- Multi-Rate (1Gbps to 3.2Gbps)
- Single +3.3V Power Supply
- SFP Multisource Footprint
- Digital Diagnostic Monitors and Internal Calibration.
- 850nm Wavelength VCSEL
- Temperature Compensation using Variable Digital Resistors with Look-Up Tables and Digital Diagnostics
- Compatible with LC Fiber-Optic Connector
- Assembled and Tested SFP TX Board (RD005-1) and SFP Host Board (RD003-2) are Available for Evaluation



2 Obtaining Additional Information

The RD005-1 SFP transmitter board and RD003-2 SFP host board are no longer available. For more information about the reference design or to request Gerber files or schematics please email to: https://support.maxim-ic.com/ .

3 Reference Design Details

The HFRD-5.0 SFP transceiver reference design (Figure 1) is implemented using a high-speed VCSEL driver (MAX3740), a dual temperature-controlled variable resistor (DS1859) with monitors and internal calibration, a high-speed limiting amplifier with RSSI output (MAX3748) a VCSEL, a ROSA (MAX3744 and PIN photodiode) and an SFP module board (RD005-1). The design is SFP and SFF 8472 MSA compatible, incorporates safety features, and can be internally calibrated. HFRD-5.0 is also multi-rate compatible and can be operated at data rates from 1Gbps to 3.2Gbps. Typical performance results at 4.25Gbps are also provided. See Section 7.7 for more information about 4.25Gbps operation.

3.1 Transmitter Components

3.1.1 MAX3740 Laser Driver

The MAX3740 is a high-speed VCSEL driver for small-form-factor (SFF) and small-form-factor pluggable (SFP) fiber optic LAN transmitters. It contains a bias generator, a laser modulator, and comprehensive safety features. The automatic power control (APC) adjusts the VCSEL bias current to maintain average optical power over changes in temperature and VCSEL properties.

The MAX3740 can switch up to 15mA of VCSEL modulation current and source up to 15mA of bias current. The MAX3740 interfaces with the Dallas DS1859 to meet the SFF-8472 timing and diagnostic requirements and accommodates various VCSEL packages, including low-cost TO-46 and TO-56 headers.

The MAX3740 safety circuitry detects faults that could cause hazardous light levels and disables the VCSEL output. The safety circuits are compliant with SFF and SFP multisource agreements (MSA).

For additional information see the MAX3740 data sheet available on the web at www.maxim-ic.com.

3.1.2 DS1859 Digital Potentiometer

The DS1859 Dual Temperature-Controlled NV Variable Resistor consists of two 50kΩ 256-position variable resistors, a “direct-to-digital” temperature sensor, three external voltage monitors, and one internal voltage monitor for V_{CC}. The DS1859 is compliant with SFF-8472 requirements and provides internal calibration. The device provides temperature compensation to the bias and modulation currents by changing the resistance as a function of temperature using look-up tables.

The variable resistors’ settings are stored in EEPROM memory and can be accessed over the industry standard 2-wire serial bus. The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value to each resistor for every 2°C increment over the –40°C to +102°C range.

The output of temperature, supply voltage and the three monitors is available as a 12bit value (left justified) over the serial bus. Flags for supply voltage and the monitors can be set and read from the device as well.

For additional information see the DS1859 data sheet available on the web at www.maxim-ic.com.

3.1.3 VCSEL

HFRD 5.0 was tested with high-speed VCSELs from Emcore (Part# 8585-3510-A) and Advanced Optical Components (formerly Honeywell) (Part# HFE4191-541). Both VCSELs were packaged in LC connectorized headers and are intended for high-speed communications applications.

Additional information regarding the Emcore VCSEL can be obtained at www.emcore.com.

Additional information regarding the Honeywell VCSEL can be obtained at www.adopco.com or email sales@adopco.com.

3.2 Receiver Components

3.2.1 MAX3748 Limiting Amplifier

The MAX3748 multi-rate limiting amplifier functions as a data quantizer for SONET, Fibre Channel and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides constant-level current-mode logic (CML) output voltages with controlled edge speeds.

A received-signal-strength indicator (RSSI) is available when the MAX3748 is combined with the MAX3744 SFP transimpedance amplifier (TIA) that can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional polarity reversal and an output disable which can be used to implement a squelch of the outputs.

The combination of the MAX3748 and the MAX3744 allows for the simple implementation of the small-form-factor SFF-8472 digital diagnostics specifications using a standard 4-pin TO-46 header using a Maxim-proprietary interface technique (patent pending).

For additional information see the MAX3748 data sheet available on the web at www.maxim-ic.com.

3.2.2 MAX3744 Transimpedance Amplifier

The MAX3744 transimpedance amplifier provides a compact, low-power solution for communication up to 2.7Gbps. It features a 330nA input-referred noise at 2.1GHz bandwidth (BW) with 0.85pF input capacitance.

The MAX3744 operates from a single +3.3V supply and consumes 93mW. The MAX3744 die measures 30-mil x 50-mil and requires no external compensation capacitor. A space-saving filter connection is provided for positive bias to the photodiode through an on-chip 580Ω resistor to V_{CC}.

For additional information see the MAX3744 data sheet available on the web at www.maxim-ic.com.

3.2.3 Receiver Optical Sub-Assembly (ROSA)

The TO-46 ROSA, which includes the MAX3744, a photodiode and other components, is assembled by Honeywell (Part# HFD3180-202). For more information regarding the ROSA, please call Honeywell at 1-866-MY-VCSEL, email VCSEL@honeywell.com or visit their web page (http://www.honeywell.com/vcsel).

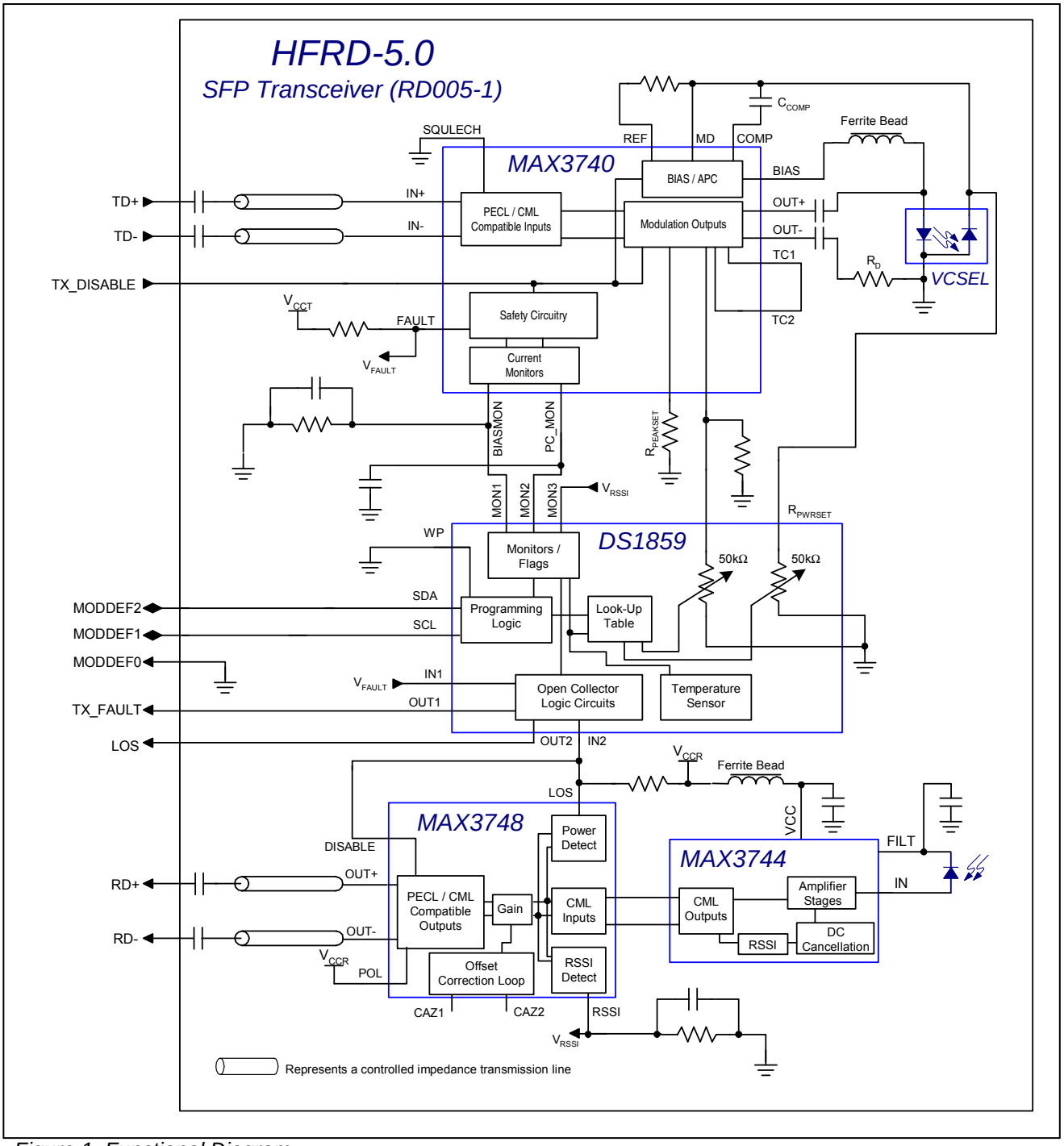


Figure 1. Functional Diagram

4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Ambient Temperature	T_A	Note 1	0		70	°C
Supply Voltage	V_{CC}		3.0	3.3	3.63	V
Data Rate		ETHERNET Patterns (≤ 2^7-1), Note 2	1			Gbps
Differential Input Voltage	V_{ID}		200		2200	mV_{p-p}
TTL Input Voltage (Low)	V_{IL}				1.1	V
TTL Input Voltage (High)	V_{IH}		2.6			V

Note 1: The operating temperature of the MAX3748, MAX3744 and MAX3740 is –40°C to +85°C. The recommend operating temperature of the Emcore VCSEL is 0°C to +85°C (Case Temperature) and 0°C to +70°C (Ambient) for the Honeywell VCSEL. See Section 8.8 for additional information.

Note 2: The maximum guaranteed operating data rate of the MAX3740 and MAX3748 is 3.2Gbps. The MAX3744 maximum guaranteed operating data rate is 2.7Gbps. The performance of the reference design is shown for data rates up to 4.25Gbps. See Section 8.7 for additional information.

5 Typical Design Performance Data

5.1 Transmitter Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V, Average Power = -3dBm to –4.5dBm, Extinction Ratio > 10dB unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Transmitter Only	83	mA
Average Optical Power	P_{AVG}	Measured @ 2.125Gbps (Note 1)	-3.0 to –4.3	dBm
		With TX_DISABLE Asserted	< -50	dBm
Extinction Ratio (Note 1)	E_R	-10°C to +80°C, Data Rate ≤ 2.125Gbps	> 10	dB
		-10°C to +80°C, Data Rate > 2.125Gbps	> 8	
Optical Modulation Amplitude (Note 1)	OMA	@ 1.063Gbps	0.80	mW
		@ 1.25Gbps	0.81	
		@ 2.125Gbps	0.84	
		@ 3.125Gbps	0.80	
Optical Modulation Amplitude Variation		-40°C to +85°C (Note 1, 2)	< 3	%
Optical Rise Time	t_R	20% to 80% (Notes 3, 4)	47	ps
Optical Fall Time	t_F	80% to 20% (Notes 3, 4)	89	ps
Jitter Generation (Total Jitter)	TJ	@ 1.063Gbps (Notes 1, 5)	47	mUI
		@ 1.25Gbps (Notes 1, 5)	60	
		@ 2.125Gbps (Notes 1, 5)	52	

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
		DJ Only @ 3.125Gbps (Notes 1, 6)	72	
		DJ Only @ 4.25Gbps (Notes 1, 6)	98	
Jitter Generation (Random Jitter)	RJ	RMS Random Jitter (Note 3)	0.8	ps_{RMS}
Eye Mask Margin (Notes 1, 7)		@ 1.063Gbps	> 35	%
		@ 1.25Gbps	> 35	
		@ 2.125Gbps	> 35	
		@ 3.125Gbps	> 20	
Center Wavelength			850	nm

Note 1: Measured using a 2^7-1 PRBS input data pattern.
Note 2: Optical Modulation Amplitude variation refers to the obtainable variation using multiple calibration points. Measured at 2.125Gbps on the filtered optical output.
Note 3: Measured using a 2.125Gbps repeating 0011 pattern.
Note 4: Measured using an unfiltered optical output.
Note 5: Total jitter (peak to peak) is measured after acquiring 2000 waveforms. Measurement includes approximately 14ps of total jitter from the test equipment.
Note 6: Deterministic jitter (peak-to-peak) is measured after acquiring 2000 waveforms. Measurement includes approximately 14ps of deterministic jitter (DJ) from the test equipment at data rates > 3Gbps.
Note 7: Mask margin is measured after acquiring 2000 waveforms using standard mask limits at 25˚C. Mask margin is measured at 1.063Gbps and 1.25Gbps using a reference receiver. Mask margin is measured at 2.125Gbps and 3.125Gbps using a 2.3GHz bandwidth O/E converter.

5.2 Receiver Performance Data

(Typical values are measured at T_A = +25°C, V_{CC} = +3.3V, Optical Source is HFRD 5.0 Transmitter)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Power Supply Current		Receiver Only	65	mA
Average Optical Input Power Overload	P_{AVGMAX}		-3	dBm
Receiver Sensitivity Expressed as Optical Modulation Amplitude (OMA) (Note 1, 2)	OMA_{MIN}	Data Rate = 1.063Gbps	7.2	μW_{PK-PK}
		Data Rate = 1.25Gbps	6.5	
		Data Rate = 2.125Gbps	8.3	
		Data Rate = 3.125Gbps	11.7	
		Data Rate = 4.25Gbps	22.1	
Receiver Sensitivity Expressed as Average Power (Note 1)	P_{AVGMIN}	Data Rate = 1.063Gbps	-23.6	dBm
		Data Rate = 1.25Gbps	-24.1	
		Data Rate = 2.125Gbps	-23.0	
		Data Rate = 3.125Gbps	-21.5	
		Data Rate = 4.25Gbps	-18.7	

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Transceiver Sensitivity (Note 3)		No Significant Difference From Receiver Sensitivity		
Loss of Signal (Note 4)	LOS	Assert	-25.2	dBm
		De-Assert	-22.7	
Loss of Signal Hysteresis			2.5	dB

Note 1: Sensitivity is measured using a 2^7-1 PRBS test pattern to a BER of approximately 10^{-12}. An isolated HFRD-05.0 transmitter is used as the optical source for the BER testing.
Note 2: Optical Modulation Amplitude (OMA) is calculated using an extinction ratio of approximately 10dB. The extinction ratio of the input signal at each data rate is measured and used in the calculation.
Note 3: Transceiver sensitivity is measured with data present on the transmitter with the transmitter enabled.
Note 4: Loss of Signal (LOS) is measured using at 2.125Gbps with a 2^7-1 PRBS test pattern.

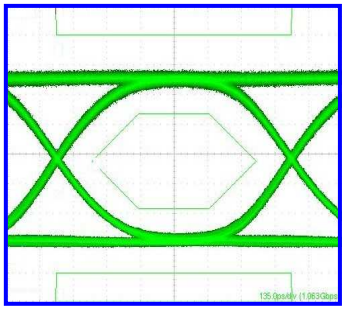
5.3 Transceiver Timing Data

TX_DISABLE Assert Time	t_{OFF}	Time from rising edge of TX_DISABLE to optical power at 5% of steady state.	1.5	µs
TX_DISABLE Negate Time	t_{ON}	Time from falling edge of T_{DIS} to optical power at 95% of steady state when TX_FAULT = 0 before reset.	<200	µs
TX_FAULT Reset Time or Power on Time	t_{INIT}	From power on or negation of TX_FAULT using TX_DISABLE.	60	ms
TX_FAULT Assert Time	t_{FAULT}	Time from fault occurrence to TX_FAULT on, C_{FAULT} < 20pF, R_{FAULT} = 4.7kΩ.	1.4	µs
TX_FAULT Delay Time	t_{FLTDLY}	Time from fault to bias and modulation current at off state limits.	1	µs
LOS Assert Time	T_{LOS}	Time from LOS state to LOS Assert.	< 50	µs
LOS De-Assert Time	T_{LOS}	Time from non-LOS state to LOS De-Assert.	< 50	µs
TX_DISABLE to Reset		Time TX_DISABLE must be held high to reset TX_FAULT.	<1	µs

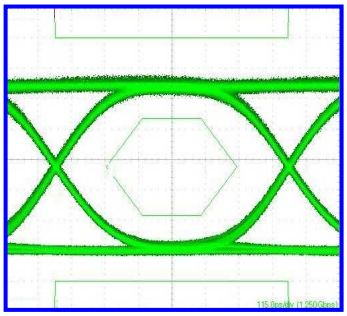
6 Transmitter Characteristic Graphs

(T_A = +25°C, V_{CC} = +3.3V, 2.125Gbps, 2^7-1 PRBS and -3.0 to –4.3dBm average power unless otherwise noted)

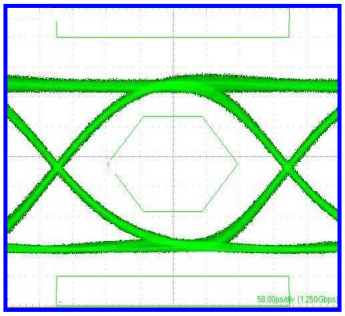
OPTICAL EYE DIAGRAM
(1.063 Gbps, E_R > 10dB,
OMA ≈ 800µW)



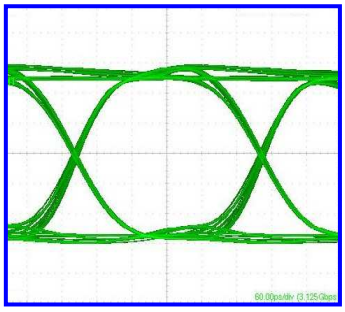
OPTICAL EYE DIAGRAM
(1.25 Gbps, E_R > 10dB,
OMA ≈ 800µW)



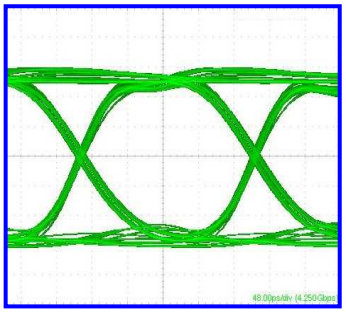
OPTICAL EYE DIAGRAM
(2.5 Gbps, E_R = 10dB,
OMA ≈ 800µW)



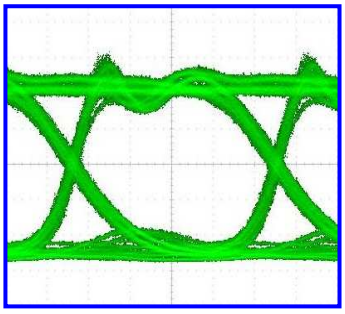
OPTICAL EYE DIAGRAM
(3.125 Gbps, E_R > 8dB,
Math Filter, No RJ)



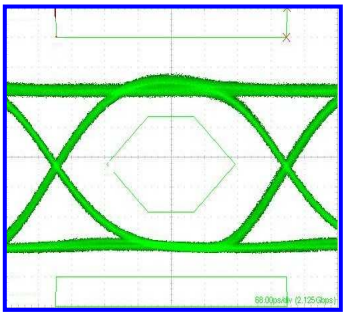
OPTICAL EYE DIAGRAM
(4.25 Gbps, E_R > 8dB,
Math Filter, No RJ)



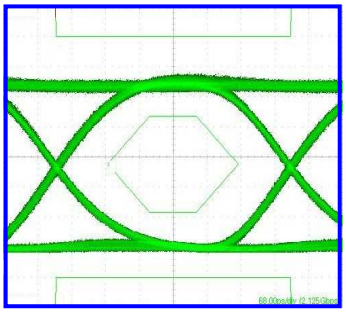
OPTICAL EYE DIAGRAM
(4.25 Gbps, E_R > 8dB,
Unfiltered, 12Ghz O/E)



OPTICAL EYE DIAGRAM
(2.125 Gbps, E_R > 10dB,
Temperature = 0°C)



OPTICAL EYE DIAGRAM
(2.125 Gbps, E_R > 10dB,
Temperature = 25°C)



OPTICAL EYE DIAGRAM
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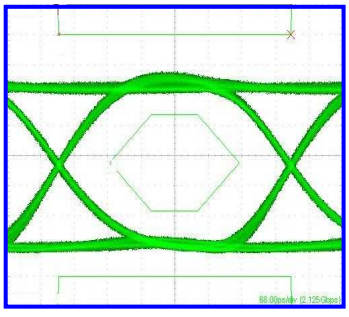
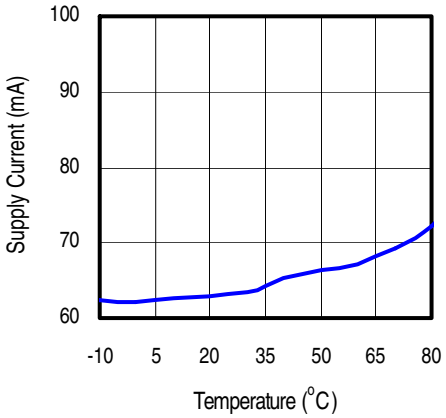
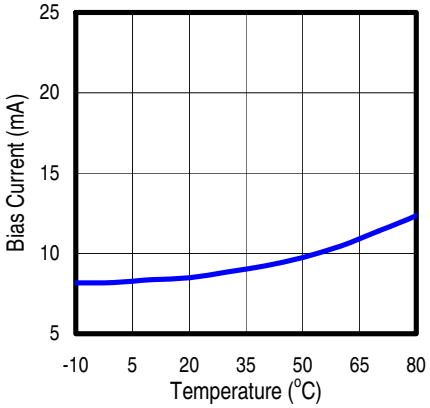
Temperature = 70°C)



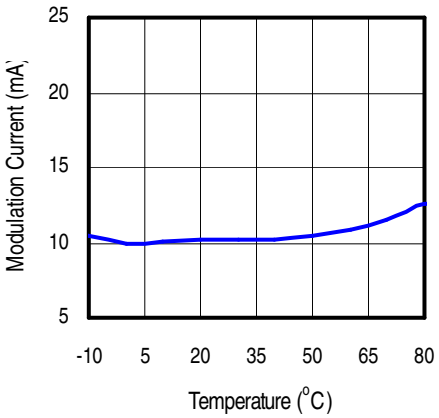
SUPPLY CURRENT vs. TEMPERATURE



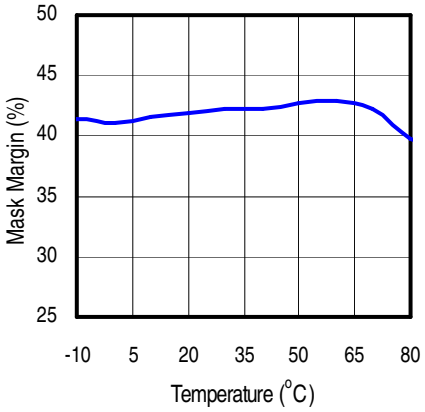
BIAS CURRENT vs. TEMPERATURE



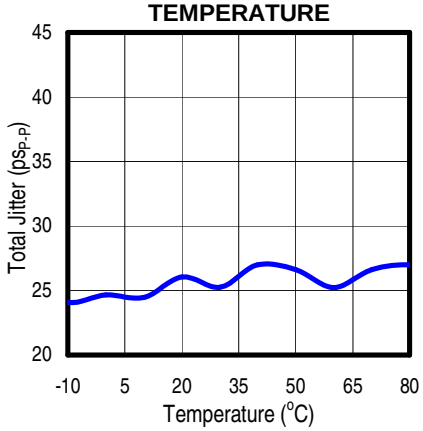
MODULATION CURRENT vs. TEMPERATURE



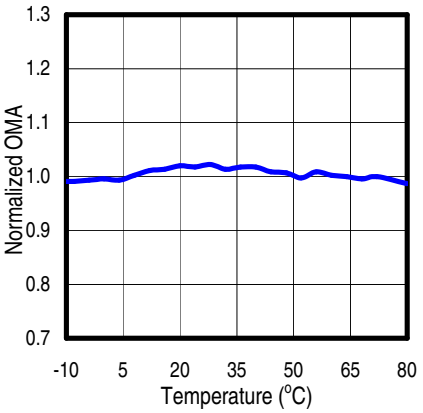
MASK MARGIN vs. TEMPERATURE



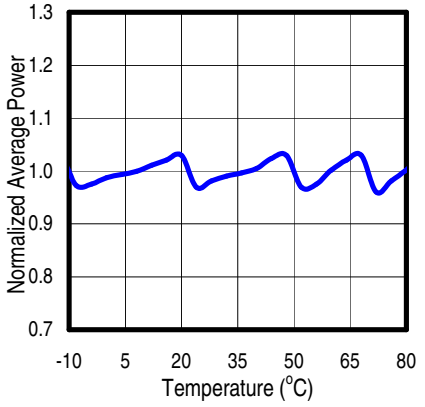
TOTAL JITTER vs. TEMPERATURE



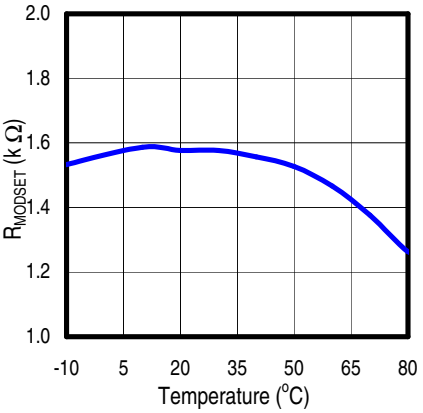
NORMALIZED OMA vs. TEMPERATURE



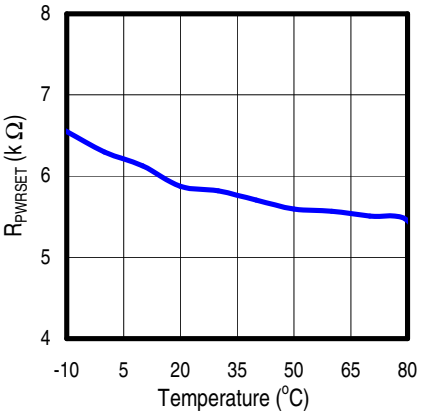
NORMALIZED AVERAGE OPTICAL POWER vs. TEMPERATURE



R_{MODSET} vs. TEMPERATURE



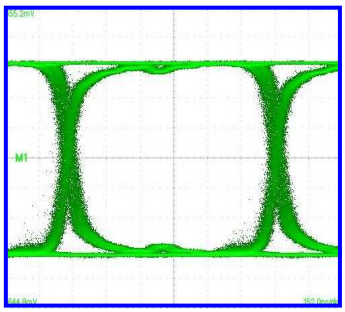
R_{PWRSET} vs. TEMPERATURE



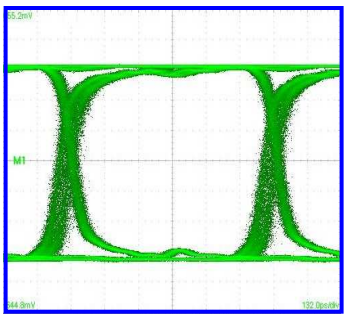
7 Receiver Characteristic Graphs

(T_A = +25°C, V_{CC} = +3.3V, 2.125Gbps, 2^7-1 PRBS, Diagrams taken at received data output SMA connectors of RD003-2 host board.)

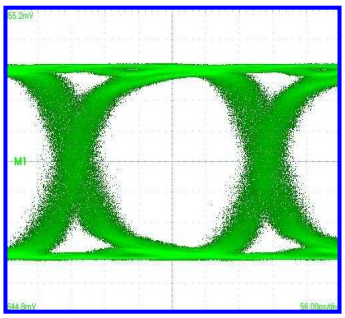
OUTPUT EYE DIAGRAM
(1.063 Gbps, -21.7dBm Optical Input)



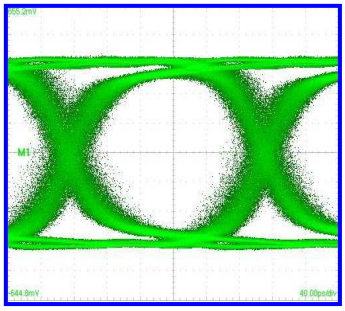
OUTPUT EYE DIAGRAM
(1.25 Gbps, -21.7dBm Optical Input)



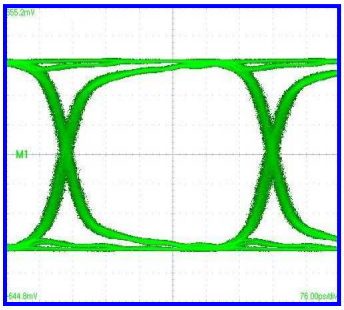
OUTPUT EYE DIAGRAM
(3.125 Gbps, -19.7dBm Optical Input)



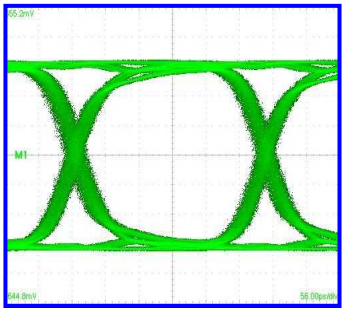
OUTPUT EYE DIAGRAM
(4.25 Gbps, -18.2dBm Optical Input)



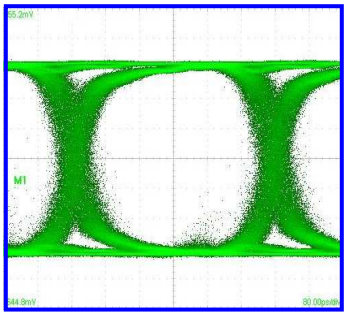
OUTPUT EYE DIAGRAM
(2.125 Gbps, -14.9dBm Optical Input)



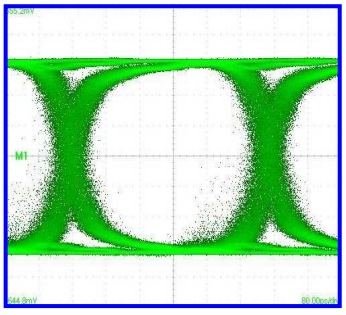
OUTPUT EYE DIAGRAM
(3.125Gbps, -13.5dBm Optical Input)



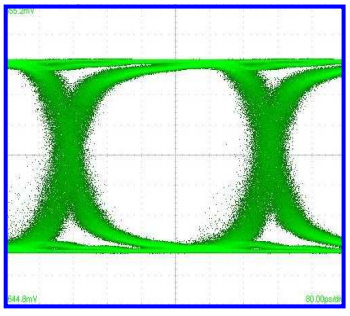
OUTPUT EYE DIAGRAM
(2.125 Gbps, -21.7 Optical Input, Temperature = -10°C)



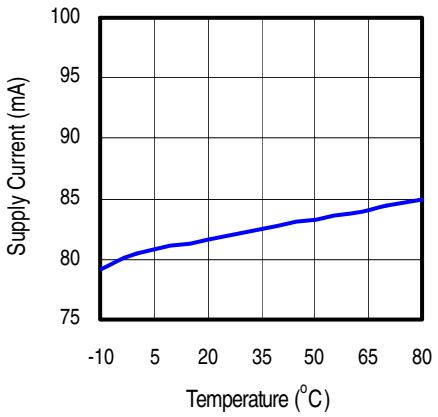
OUTPUT EYE DIAGRAM
(2.125 Gbps, -21.7 Optical Input, Temperature = 25°C)



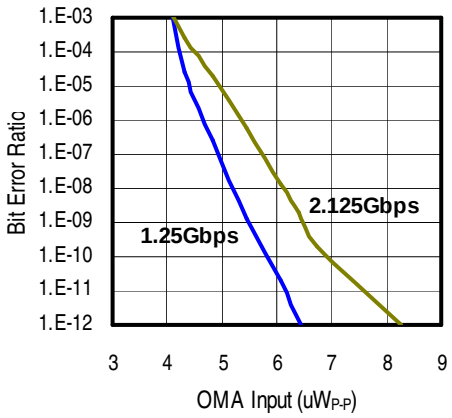
OUTPUT EYE DIAGRAM
(2.125 Gbps, -21.7 Optical Input, Temperature = 70°C)



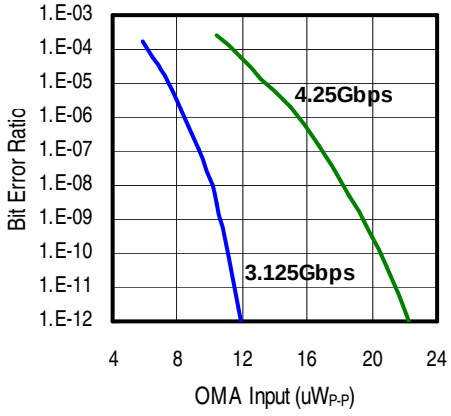
Supply Current vs. Temperature



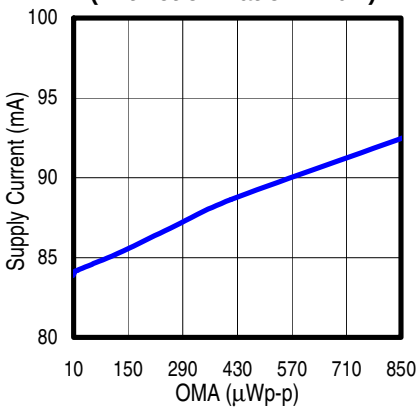
Bit Error Ratio vs. Optical Input



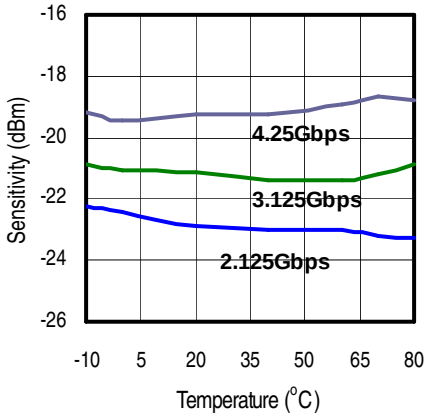
Bit Error Ratio vs. Optical Input



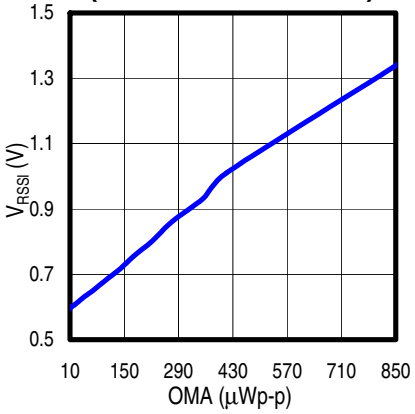
Supply Current vs. OMA Input (Extinction Ratio = 11dB)



Sensitivity vs. Temperature



VRSSI vs. OMA Input (Extinction Ratio = 11dB)



8 Application Information

8.1 Small Form Factor Pluggable (SFP) Transceivers

The RD005-1 transceiver design was specifically engineered to meet the requirements of the Small Form Factor Pluggable (SFP) Transceiver Multisource Agreement (MSA) and the digital diagnostic requirements of SFF-8472 MSA. These MSAs set guidelines for the package outline, pin function and other aspects of the module design. By complying with the standard, modules are mechanically and functionally interchangeable.

8.2 Monitor Outputs

The MAX3740 and MAX3748 have on-chip current monitors for bias and monitor diode current of the VCSEL and the received signal strength of the photodiode.

The bias monitor (BIASMON of the MAX3740) pin generates a ground-referenced voltage across an external resistor connected from the monitor pin to ground that is proportional to the bias current. The relation is given mathematically as:

$$I_{BIAS} = \frac{9 \cdot V_{BIASMON}}{330\Omega}$$

The average power monitor (PWRMON of the MAX3740) generates a ground-referenced voltage across an external resistor that is proportional to both the monitor diode current (I_{PD}) and the average optical power. The relation is given mathematically as:

$$I_{PD} = \frac{V_{PWRMON}}{2 \cdot 300\Omega}$$

The received signal monitor (RSSI of the MAX3748) generates a ground-referenced voltage across an external resistor that is proportional to both the DC photodiode current (I_{PD}) and the average optical input power. See page 12 for a graph of the typical response.

The voltages at the monitor pins ($V_{BIASMON}$, V_{PWRMON} and V_{RSSI}) are sampled by the DS1859 and stored in memory. The values can then be read over the 2-wire bus as a 12bit digitized number. If the voltage at BIASMON or PWRMON exceeds 0.8V (typical), a fault condition will be latched by the MAX3740 and TX_FAULT will assert.

8.3 Programming the DS1859

The DS1859 dual variable resistor is programmed with an industry standard 2-wire interface. The interface I/O pins consist of SDA and SCL (see DS1859 data sheet for more information). These control lines are connected to pad 4 (MOD-DEF2, SDA) and pad 5 (MOD-DEF1, SCL) of the transmitter board. The data can then be programmed into the device through these pins using the connections of a standard SFP evaluation board.

To facilitate the programming of the DS1859, additional materials such as software, DS3900 serial port adapter, cable, and RD003-2 host board can be used. These materials allow easy adjustments to be made to the DS1859 through the 2-wire interface. See *Additional Evaluation Materials* on page 23 for more information.

8.4 Layout Considerations

Differential and single-ended transmission lines are designed on the RD005-1 PC board. Changing the PCB layer profile (see details on page 23) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

8.5 Host Board Requirements

Controlled-impedance transmission lines and good high-frequency design techniques should be used when interfacing to the RD005-1 SFP transceiver board. The host board should provide the necessary power supply filtering. The recommended SFP MSA power supply filter for the transmitter is shown in Figure 2.

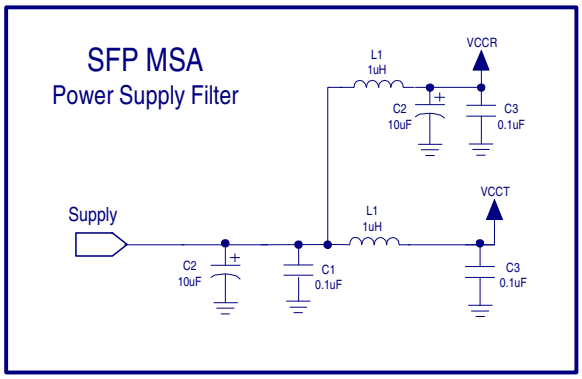


Figure 2. Power Supply Filter

8.6 MSA Compliance, EMI and Safety Issues

Full compliance to the SFP MSA and other performance specifications cannot be guaranteed by Maxim and are therefore the responsibility of the user of this reference design. This reference design is intended to aide SFP module designers and is not intended to take the place of the entire design process. The SFP module designer should evaluate the reference design and modify it as necessary to meet the specification for each particular project. The designer should also carefully consider safety and EMI issues related to the particular application.

8.7 Operating Data Rates

Due to the low frequency cutoff of the APC loop and AC-coupling capacitors on the data inputs and outputs, the optical performance for data rates less than 1Gbps is degraded due to baseline wander when using 2^7-1 PRBS test patterns.

Typical performance of the reference design at data rates up to 4.25Gbps is provided to demonstrate that such high modulation rates can be obtained with this reference design. However, the high-speed parameters in the data sheets of the MAX3740, MAX3748 and MAX3744 are not guaranteed at 4.25Gbps. If operating at data rates above 3.2Gbps (above 2.7Gbps for the MAX3744), the user should carefully characterize the high-speed parameters in order to determine the performance at these data rates.

When operating at 4.25Gbps, the peaking resistor ($R_{PEAKSET}$) of the MAX3740 should be adjusted to improve the falling edge of the VCSEL. The VCSEL bias level should also be optimized to maximize bandwidth and reduce turn-on delay and the associated jitter. The performance of these parameters is related to the extinction ratio setting of the VCSEL. In general, the extinction ratio should be set slightly lower as the operational data rate increases in order to obtain optimal performance.

8.8 Operating Temperature

The operating temperatures of the MAX3748, MAX3744 and MAX3740 are –40°C to +85°C. The recommend operating temperature of the Emcore VCSEL is 0°C to +85°C (Case Temperature) and 0°C to +70°C (Ambient) for the Honeywell VCSEL. Given temperature constraints of the VCSELs, the reference design is recommended for 0°C to +70°C operation.

8.9 Gerber Files

The Gerber files for this reference design are available. Email to: https://support.maxim-ic.com/ Note that modifications will need to be made to the Gerber files before building a board to account for the hand-modified changes that were made to the design. The modifications are shown in the layout files (page 21) and the schematic connections are shown on page 19.

8.10 Improving Receiver Sensitivity

Improved receiver sensitivity can be obtained by providing high frequency isolation between the MAX3748 limiting amplifier and the MAX3744 TIA. By placing a small inductor (3.3nH to 6.8nH) between each of the TIA outputs and the MAX3748 inputs, the sensitivity can be improved by 1 to 1.5dBm. Using inductors larger than 6.8nH will improve the sensitivity further, but at the cost of increased jitter at the limiting amplifier output.

The RD005-1 PCB can be modified to incorporate these changes by cutting the data traces and placing 0402 size inductors as shown in Figure 3.

It is suggested to use multi-layer inductors that have a small DC resistance.

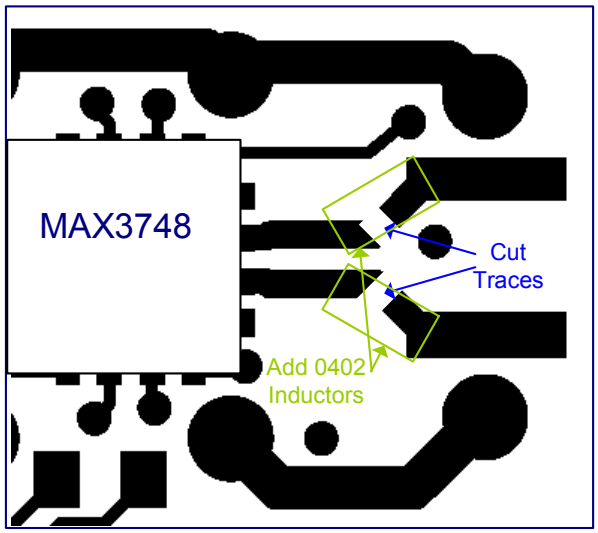


Figure 3. Board Modification

9 Quick Start

RD005-1 can be evaluated in any standard SFP host board. Changes to the settings of the DS1859 can be done through the MOD-DEF2 and MOD-DEF1 pads. The module may be shipped with either the Honeywell or the Emcore VCSEL. By reading memory location 00h from the auxiliary device (device address A0h) of the DS1859, the type of VCSEL can be determined as shown in Table 1.

Table 1. Populated VCSEL

VCSEL	Value @ 00h
Emcore	12h
Honeywell	44h

The module has been pre-programmed prior to shipment to provide an extinction ratio of approximately 11dB and an average power of -4.5dBm to -3.0dBm at 25°C. A typical curve has also been loaded into the memory table for temperature compensation of the VCSEL. The table is generated using typical data from several VCSELs. The average optical power and OMA variation may be larger than that shown in the reference design characteristic graphs unless it is calibrated over temperature using the Dallas DS1859 software.

Precautions must be taken in order to insure safe operation when using a device with a laser diode. Laser light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm or injury as a result of the use of this reference design. The safe operation of this design is the sole responsibility of the user.

To evaluate the RD005-1 transmitter in a standard SFP host board:

1) Connect the RD005-1 to an SFP host board.
2) Attach a 1Gbps to 3.2Gbps differential source to the host board so that data is applied to pads 18 and 19 of the SFP board. Each source should have a peak-to-peak amplitude between 100mV and 1100mV (200mV and 2200mV differential).
3) Connect a multi-mode fiber with an LC-type ferrule to the laser. Do not place mechanical stress on the laser with the fiber cable. Stress by the fiber cable or other sources could damage the laser.
4) Connect the other end of the fiber to a high-speed oscilloscope through an optical-to-electrical converter or an optical plug-in module. The optical-to-electrical conversion device should have a bandwidth sufficiently large for the operational frequency and be able to detect 850nm wavelengths. **Note: The laser supplied with the reference design has a maximum power rating of 5mW. Attenuation may be required if 5mW of optical power exceeds the optical-to-electrical device's input power rating.**
5) Apply a +3.3V power supply to the host board. Set the current limit to 200mA.
6) Verify that TX_DISABLE is deasserted so that the SFP transmitter may operate.

To evaluate the RD005-1 receiver in a standard SFP host board:

7) Connect the RD005-1 to an SFP host board.

8) Attach high-speed SMA coaxial cables to the differential outputs from the host board to the oscilloscope.
9) Connect a multi-mode fiber with an LC-type ferrule to the ROSA. Do not place mechanical stress on the ROSA with the fiber cable. Stress by the fiber cable or other sources could damage the ROSA.
10) Connect the other end of the fiber to a high-speed 850nm optical source through an optical attenuator. If using the transmitter portion of the reference design as the optical source, follow steps 1-7 to setup the transmitter. The output power of the optical source should be less than 0dBm.
11) Apply a +3.3V power supply to the host board. Set the current limit to 200mA.

10 Pad Description

PAD	NAME	FUNCTION
1,17,20	$V_{EE}T$	Transmitter Ground
2	TX_FAULT	Transmitter Fault Indication (open collector)
3	TX_DISABLE	Transmitter Disable
4	MOD-DEF2	Module Definition 2, 2 wire serial ID interface (SDA of the DS1859).
5	MOD-DEF1	Module Definition 1, 2 wire serial ID interface (SCL of the DS1859).
6	MOD-DEF0	Module Definition 0, Connected to $V_{EE}T$.
7	RATE SELECT	N.A. - No Connection
8	LOS	Loss of Signal (open collector)
9, 10, 11, 14	$V_{EE}R$	Receiver Ground
12	RD-	Inv. Receiver Data Out
13	RD+	Receiver Data Out
15	$V_{CC}R$	Receiver Power, +3.3V Supply ±5%
16	$V_{CC}T$	Transmitter Power, +3.3V Supply ±5%
18	TD+	Transmitter Data In
19	TD-	Inv. Transmitter Data In

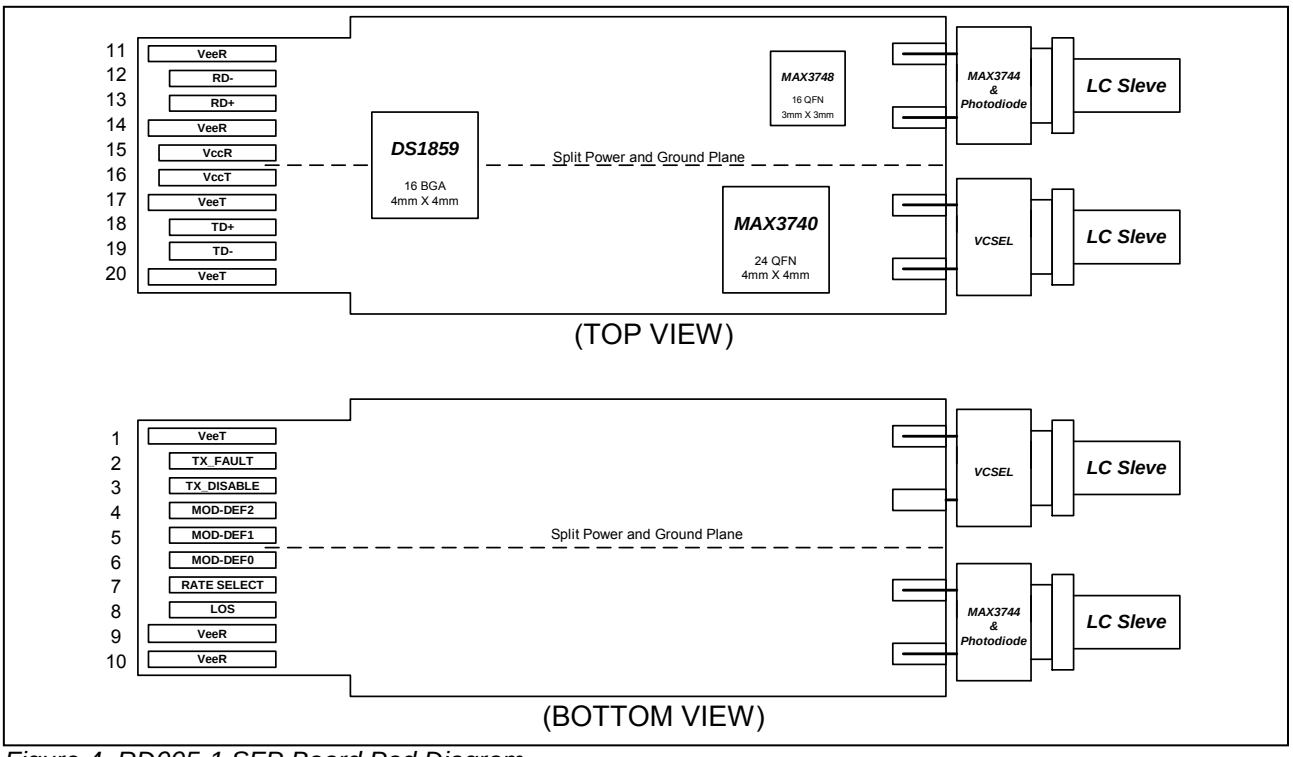


Figure 4. RD005-1 SFP Board Pad Diagram

11 Component List (RD005-1)

DESIGNATION	QTY	DESCRIPTION
C1, C5 – C7, C11, C16, C20, C24	8	0.01uF ± 10% Ceramic Capacitor (0402)
C2, C4, C18, C21 – C23	6	0.1uF ± 10% Ceramic Capacitor (0402)
C12	1	0.047uF ± 10% Ceramic Capacitor (0402)
C13, C26	2	680pF ± 10% Ceramic Capacitor (0402)
C19	1	Open
D1	1	VCSEL Emcore: 8585-3510-A Or Honeywell: HFE4191-541
L1	1	300Ω Ferrite Beads (0402) TDK MMZ1005Y-301
L2-L3	2	600Ω Ferrite Beads (0402) TDK MMZ1005Y-601
R1, R6, R10	3	Open (0402)
R2, R9	2	1.8kΩ ±5% Resistor (0402)
R3, R8, R12, R15, R16	5	0Ω ±5% Resistor (0402)
R4	1	300Ω ±5% Resistor (0402)
R5	1	3.01kΩ ±5% Resistor (0402)
R11, R13	2	10kΩ ±5% Resistor (0402)
R14	1	332Ω ±1% Resistor (0402)
R18	1	20kΩ ±1% Resistor (0402)
R19	1	49.9Ω ±1% Resistor (0402)
R20	1	330Ω ±5% Resistor (0402)
U1	1	MAX3740ETG 24 Pin QFN (Exposed Pad)
U2	1	DS1859B-050 16 Ball BGA
U3	1	MAX3748ETE 16 Pin QFN (Exposed Pad)
None	1	ROSA Assembled by Honeywell
None	1	SFP Transmitter Board (RD005-1)

12 Component List (RD003-2)

DESIGNATION	QTY	DESCRIPTION
C6, C7, C11, C31	4	10uF ±10% Ceramic Capacitor AVX TAJC106K010R
C5	1	Open
C8, C53	2	0.1uF ± 10% Ceramic Capacitor (0603)
C9, C10, C54	3	0.1uF ± 10% Ceramic Capacitor (0402)
D1 – D6	6	LED, red T1 package
J1	1	20 Pin, Right Angle Connector AMP 1367073-1
J2 – J5	4	SMA Edge-Mount Connectors
J6	1	6 Pin, Phone Jack Connector AMP 555077-1
JP1, JP2	2	2x8 Pin Headers, 0.1in centers
JU1, JU2	2	1x2 Pin Headers, 0.1in centers
JU3, JU4	2	1x3 Pin Headers, 0.1in centers
L1, L2, L3, L13	4	1µH Inductor (1008CS) Coilcraft 1008CS-102XKBC
R3 – R7	5	4.7kΩ ±1% Resistor (0603)
R8 – R13	6	300Ω ±5% Resistor (0603)
TP1 – TP7, J9, J10, J37, J38	11	Test Points
U1, U2	2	Dual Inverters Fairchild NC7WZ04P6X
None	1	SFP Host Board (RD003-2)

13 Schematic (RD005-1)

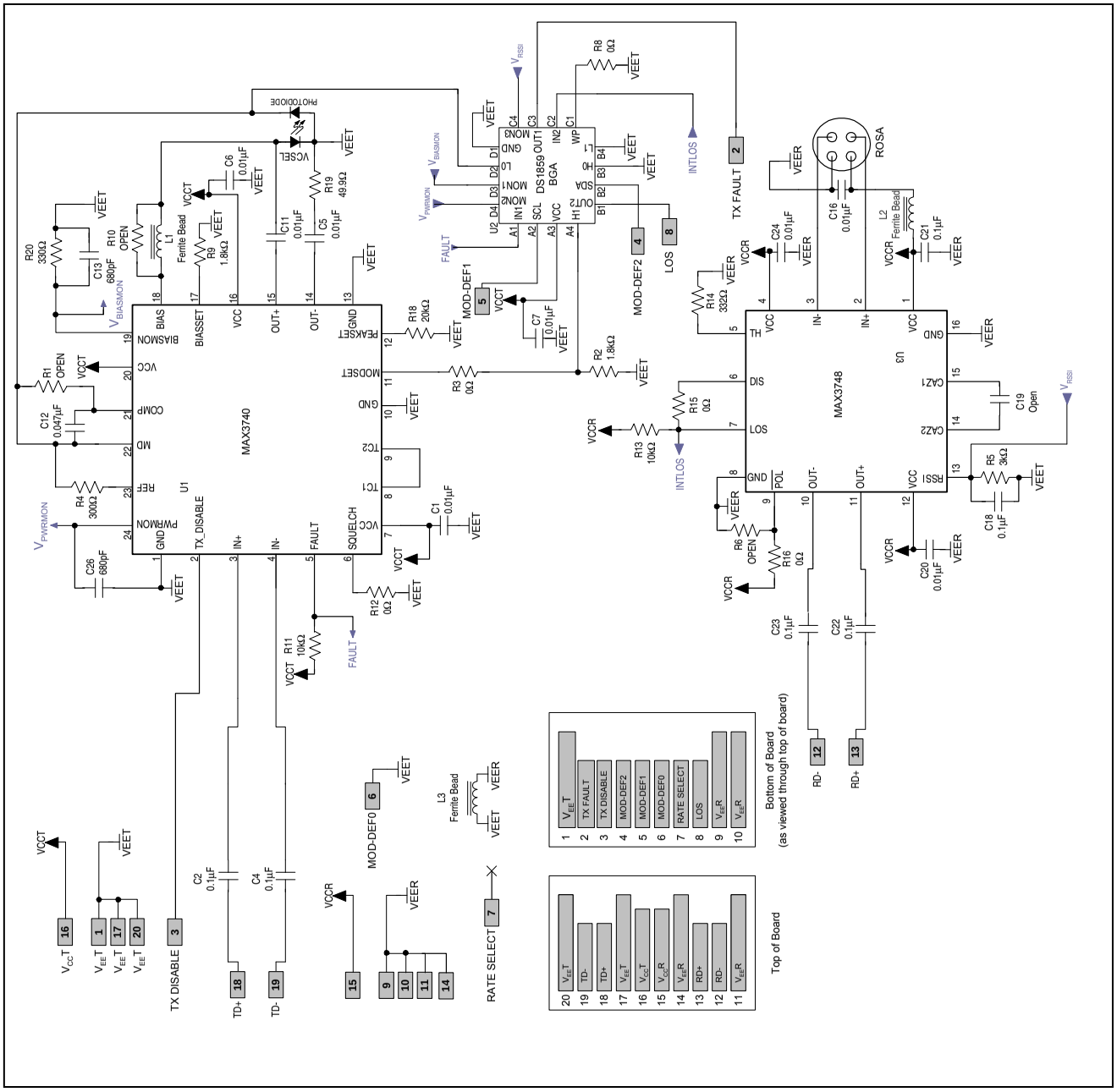


Figure 5. RD005-1 SFP Transmitter Schematic

14 Schematic (RD003-2)

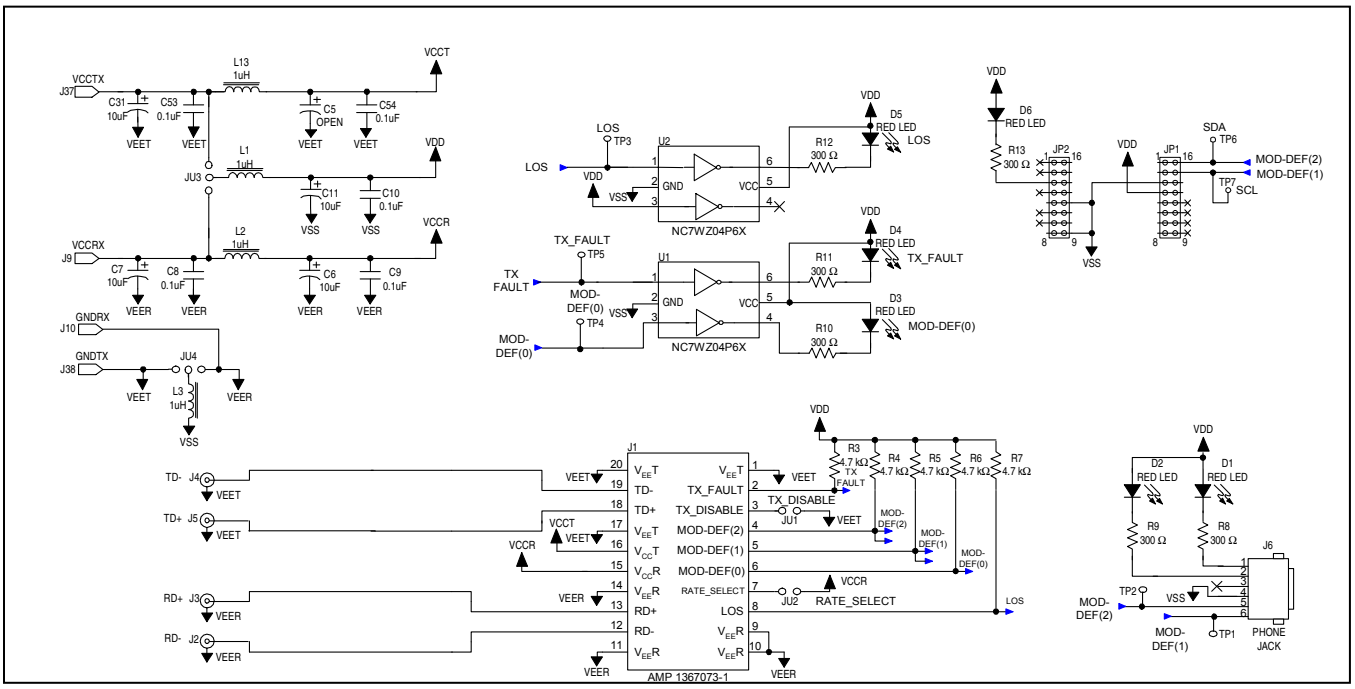


Figure 6. RD003-2 Host Board Schematic

15 Board Dimensions (RD005-1)

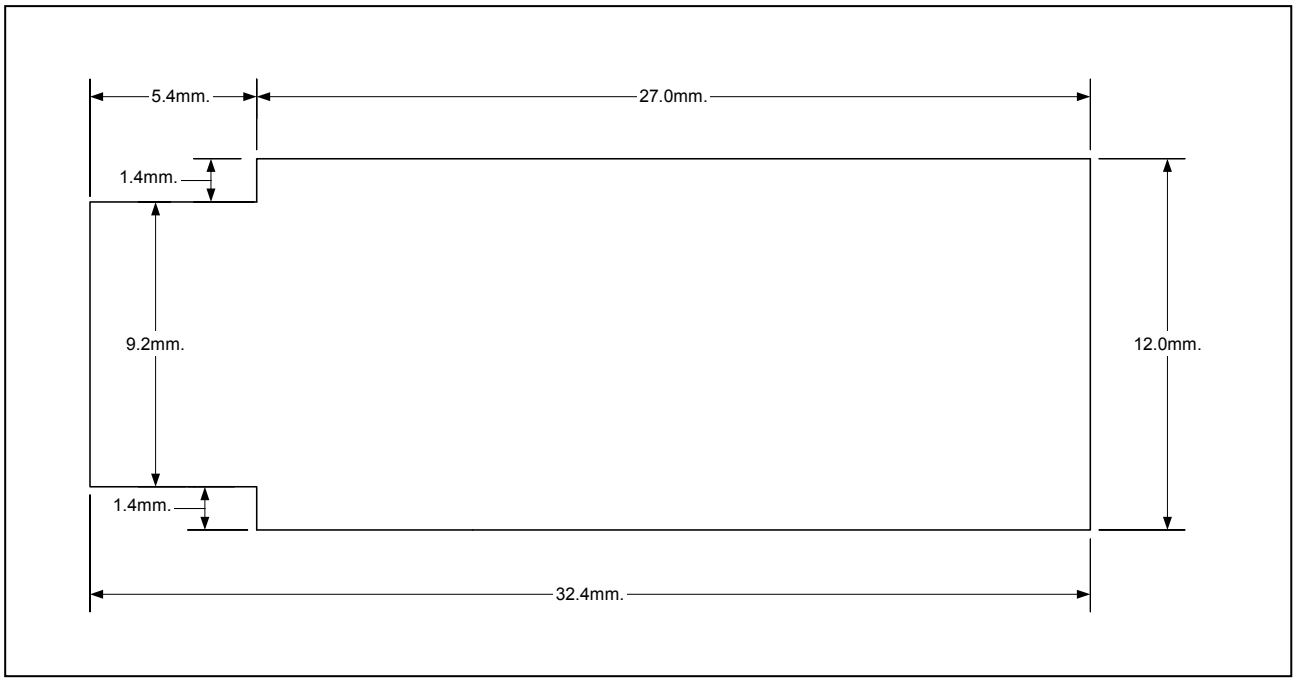


Figure 7. Board Dimensions See SFP MSA for additional dimensions.

16 Board Layout (RD005-1)

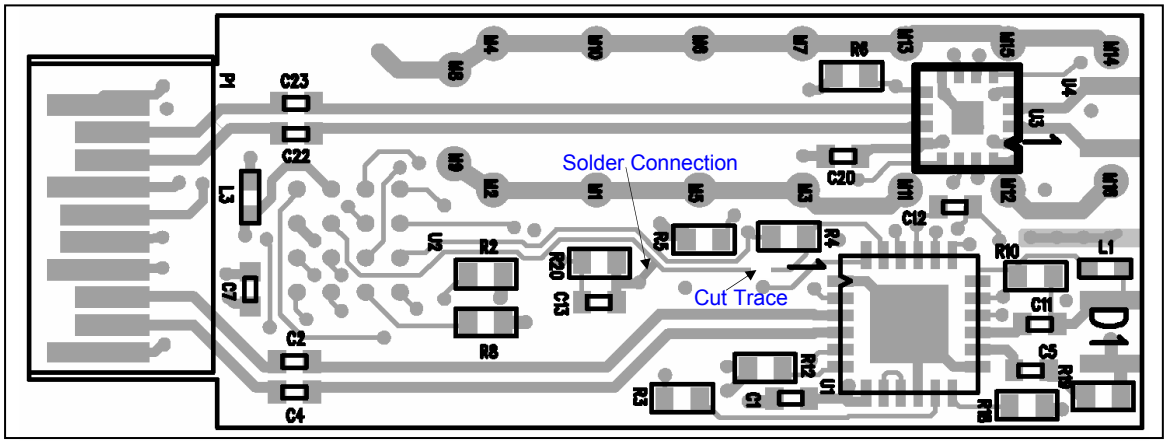


Figure 8. RD005-1 Component Placement Guide – Component Side

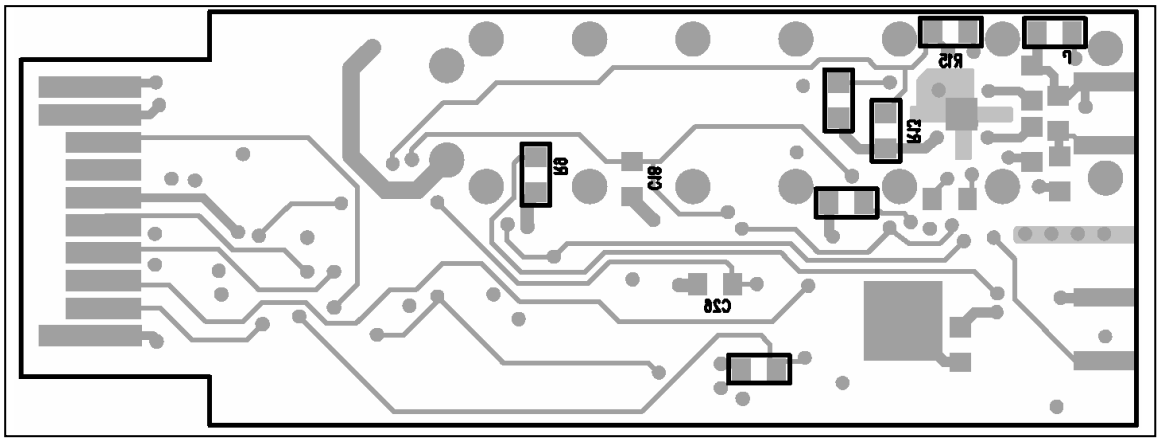


Figure 9. RD005-1 Component Placement Guide – Solder Side

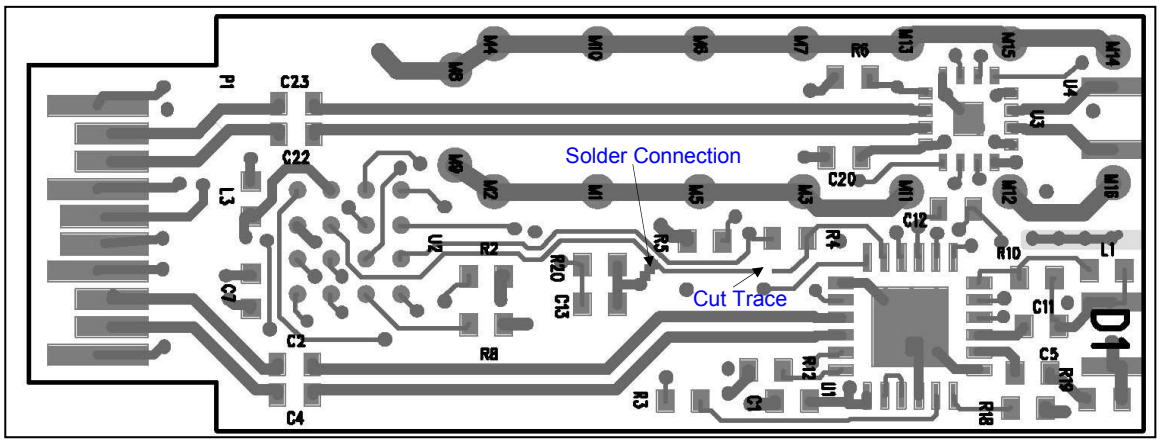


Figure 10. RD005-1 PC Board Layout – Component Side

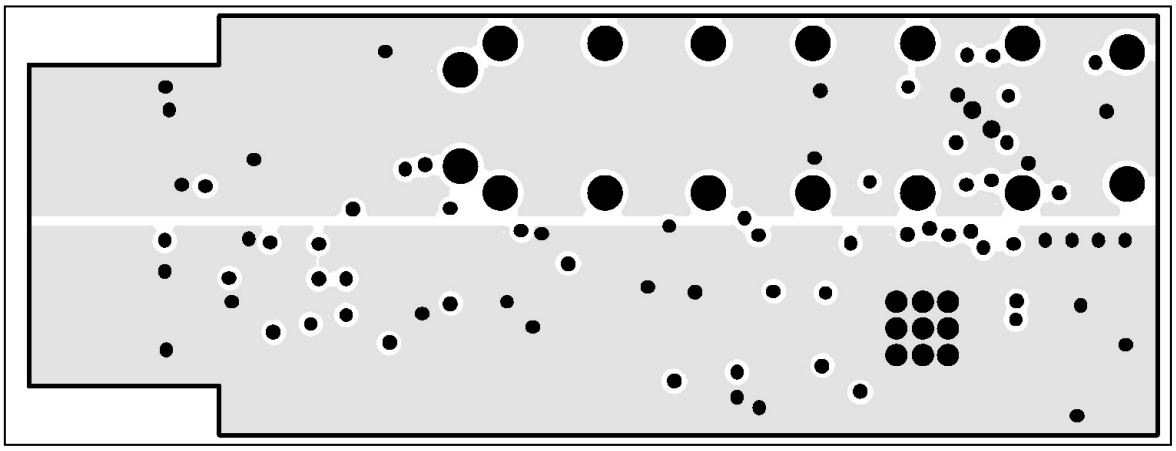


Figure 11. RD005-1 PC Board Layout – Ground Plane

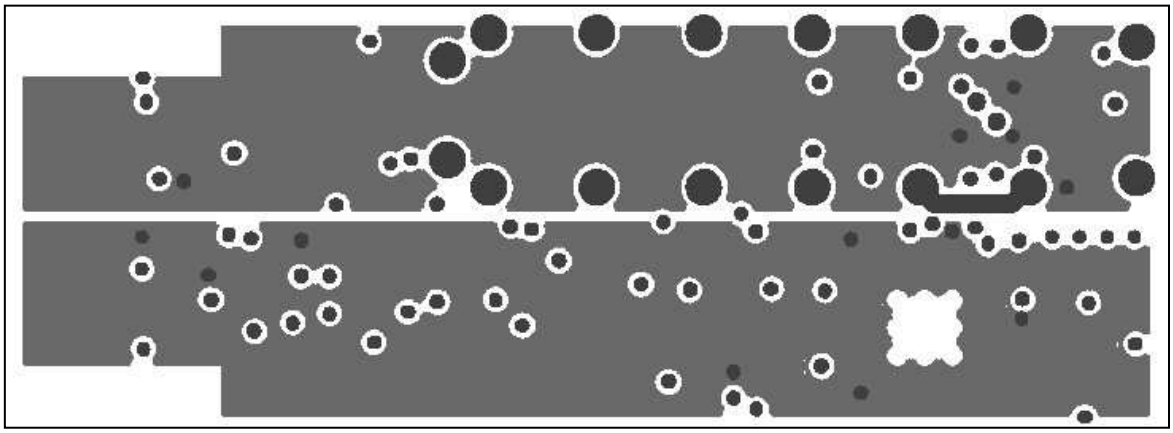


Figure 12. RD005-1 PC Board Layout – Power Plane

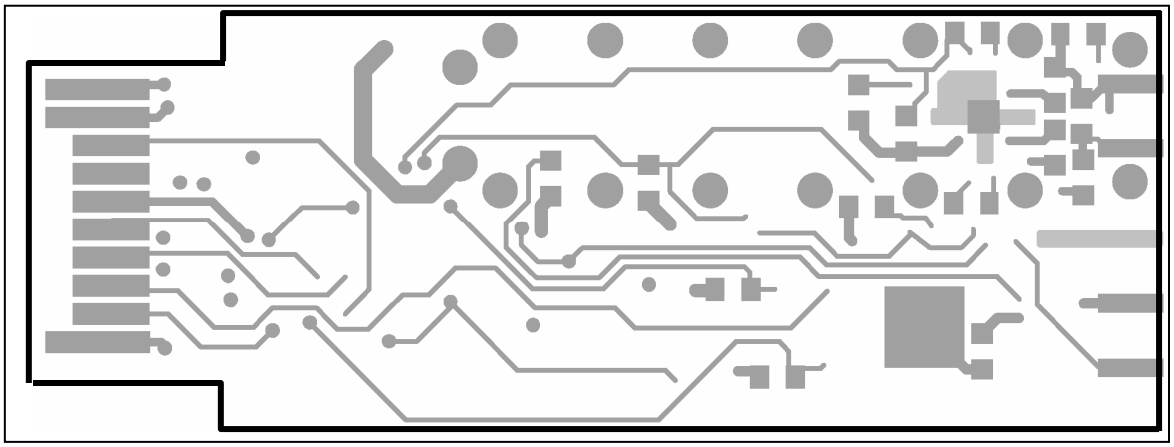


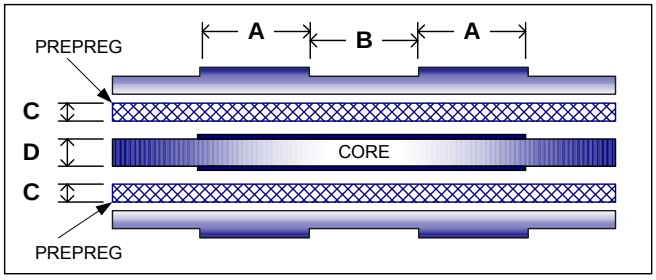
Figure 13. RD005-1 PC Board Layout – Solder Side

17 Layer Profile

The RD005-1 SFP transmitter board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is FR4 with a dielectric constant of ~ 4.7
2. 1oz copper foil

	SINGLE ENDED	COUPLED
A	N.A.	12.5mil
B	>50mil	10mil
C	16mil	16mil
D	As Needed	As Needed



18 Additional Evaluation Materials

The following materials may be needed to program the DS1859.

1. DS1859 Evaluation Software: Software that can be run on a standard PC. The software facilitates the interface to the DS1859 controller IC. Software sends and receives data by communication with the serial port, and the DS3900 serial port adapter.
2. DS3900 Serial Port Adapter: Converts RS232 protocol to 2-wire protocol with appropriate levels. Functions with the software to communicate with the DS1859 controller IC. The DS3900 plugs directly onto the RD003-2 host board.
3. RS232 Cable: Cable with standard DB9 connector that is used to connect the DS3900 serial port adapter to the computer.
4. RD003-2 Reference Design Host Board: Contains plug-in connectors for SFP modules, high-speed data connector (SMA), and 2-wire digital communication connections for the DS3900.

For further information email to: https://support.maxim-ic.com/ .