# EFM32 Gecko
# EFM32LG Errata

This document contains information on the EFM32LG errata. The latest available revision of this device is revision F.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from package marking or electronically.

Errata effective date: November 2019.

# 1. Errata Summary

The table below lists all known errata for the EFM32LG and all unresolved errata in revision F of the EFM32LG.

**Table 1.1. Errata Overview**

| Designator | Title/Problem | Work-around Exists | Exists on Revision: | | | | |
|---|---|---|---|---|---|---|---|
| | | | B | C | D | E | F |
| ADC_E116 | Offset in ADC Temperature Sensor Calibration Data | Yes | — | — | X | — | — |
| ADC_E117 | TIMEBASE not wide enough | Yes | X | X | X | — | — |
| ADC_E118 | Requirements for ADC_CLK > 7 MHz | Yes | X | X | X | X | X |
| AES_E101 | BYTEORDER Does Not Work in Combination with DATASTART/XORSTART | Yes | X | X | X | — | — |
| AES_E102 | AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set | Yes | X | X | X | — | — |
| BURTC_E101 | BURTC LPMODE Entry | No | X | X | X | — | — |
| BURTC_E102 | BURTC_CNT Read Error | Yes | X | X | X | — | — |
| BU_E101 | Backup Power Increased Power Consumtion | Yes | X | — | — | — | — |
| BU_E102 | EM4 GPIO Retention in Backup Mode | No | X | — | — | — | — |
| BU_E104 | EM4 with Backup BODs | No | X | — | — | — | — |
| BU_E105 | LFXO Missing Cycles During IOVDD Ramping | Yes | X | X | X | X | X |
| BU_E106 | Current Leakage in Backup Mode | Yes | — | — | X | — | — |
| CMU_E108 | LFxCLKEN Write | Yes | X | — | — | — | — |
| CMU_E110 | LFXO Phase Shift | No | X | — | — | — | — |
| CMU_E111 | LFXO Configuration Incorrect | Yes | X | X | — | — | — |
| CMU_E112 | LFXO Boost Buffer Current Setting | Yes | — | — | X | — | — |
| CMU_E113 | LFXO Startup at High Temperature | Yes | — | — | X | — | — |
| CMU_E114 | Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK | Yes | X | X | X | X | X |
| CUR_E103 | Increased EM2 Current | No | — | X | — | — | — |
| CUR_E104 | Increased Current on AVDD2 (USB) | Yes | X | X | — | — | — |
| CUR_E105 | Increased Current on AVDD2 (No USB) | Yes | X | X | — | — | — |
| DAC_E109 | DAC Output Drift Over Lifetime | Yes | X | X | X | X | X |
| DI_E101 | Flash Page Size | Yes | X | X | X | — | — |
| DMA_E101 | EM2 with WFE and DMA | Yes | X | X | X | — | — |
| DMA_E102 | 2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel | Yes | X | X | X | X | X |
| EBI_E101 | EBI Masking Functionality | Yes | X | — | — | — | — |
| EBI_E102 | EBI Access Fails | Yes | X | — | — | — | — |
| EBI_E103 | Page Mode Read in D16A16ALE Mode | Yes | X | X | X | — | — |

| Designator | Title/Problem | Work-around Exists | Exists on Revision: | | | | |
|---|---|---|---|---|---|---|---|
| | | | B | C | D | E | F |
| EMU_E105 | Debug Unavailable During DMA Processing from EM2 | Yes | X | — | — | — | — |
| EMU_E107 | Interrupts During EM2 Entry | Yes | X | X | X | X | X |
| EMU_E110 | Potential Hard Fault when Exiting EM2 or EM3 | Yes | — | — | — | X | — |
| ETM_E101 | ETM Trace Clock | Yes | X | — | — | — | — |
| GPIO_E101 | GPIO Wakeup from EM4 | Yes | X | — | — | — | — |
| LCD_E103 | Indeterminate Animation Engine Start-Up | Yes | X | X | X | X | X |
| LCD_E104 | Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO | Yes | X | X | X | X | X |
| LES_E101 | LESENSE and Schmitt Trigger | Yes | X | — | — | — | — |
| LES_E102 | LESENSE and DAC CH1 Configuration | Yes | X | — | — | — | — |
| LES_E103 | AUXHFRCO and LESENSE | Yes | — | — | X | — | — |
| LES_E104 | LFPRESC Can Extend Channel Start-Up Delay | Yes | X | X | X | X | X |
| OPA_E101 | OPAMP 2 Startup Rampup | No | X | — | — | — | — |
| PCNT_E102 | PCNT Pulse Width Filtering Does Not Work | No | X | X | X | X | X |
| PRS_E101 | Edge Detect on GPIO/ACMP | No | X | X | X | — | — |
| RMU_E101 | POR Calibration Initialization Issue | Yes | — | — | — | X | — |
| RMU_E102 | Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers | Yes | — | — | X | X | — |
| RMU_E103 | Reset May Fail to Trigger During Supply Voltage Brownouts | Yes | — | — | X | X | — |
| TIMER_E103 | Capture/Compare Output is Unreliable with RSSCOIST Enabled | No | X | X | X | X | X |
| USART_E112 | USART AUTOTX Continues to Transmit Even With Full RX Buffer | No | X | X | X | — | — |
| USART_E113 | IrDA Modulation and Transmission of PRS Input Data | Yes | X | X | X | X | X |
| USB_E101 | USB DMA Transfers with Prescaled HFCLK | Yes | X | — | — | — | — |
| USB_E102 | USB Datalines | No | X | — | — | — | — |
| USB_E103 | HNP Sequence Fails if A-Device Connects After 3.4 ms | No | X | X | X | X | X |
| USB_E104 | USB A-Device Delays the HNP Switch Back Process | No | X | X | X | X | X |
| USB_E105 | B-Device as Host Driving K-J Pairs During Reset | No | X | X | X | X | X |
| USB_E106 | USB Interrupts | Yes | X | — | — | — | — |
| USB_E107 | Entry to EM4 Causes Temporary Leakage from VREGO | No | X | X | — | — | — |
| USB_E108 | Floating DM/DP Pins Cause Leakage when USB is Disabled | Yes | X | X | — | — | — |

| Designator | Title/Problem | Work-around Exists | Exists on Revision: | | | | |
|---|---|---|---|---|---|---|---|
| | | | B | C | D | E | F |
| USB_E109 | Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1 | Yes | X | X | X | X | X |
| USB_E110 | Unexpected USB_HCx_INT.CHHLTD Interrupt | Yes | X | X | X | X | X |

# 2. Current Errata Descriptions

## 2.1 ADC_E118 — Requirements for ADC_CLK > 7 MHz

| ***Description of Errata*** |
|---|
| If operating the ADC_CLK at frequencies greater than 7 MHz, the ADC_BIASPROG register default value of 0x747 may not be sufficient to achieve the published missing codes performance specification. |
| ***Affected Conditions / Impacts*** |
| Devices operating the ADC_CLK at frequencies greater than 7 MHz while using the default ADC_BIASPROG value of 0x747 may experience performance outside data sheet limits. |
| ***Workaround*** |
| For systems requiring an ADC_CLK rate > 7 MHz, it may be necessary to increase the ADC's bias current components via the COMPBIAS, BIASPROG, and/or HALFBIAS bit fields in the ADC_BIASPROG register depending on a given application's ADC performance requirements. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

## 2.2 BU_E105 — LFXO Missing Cycles During IOVDD Ramping

| ***Description of Errata*** |
|---|
| LFXO missing cycles during IOVDD ramping when used in combination with Backup mode. |
| ***Affected Conditions / Impacts*** |
| When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock. |
| ***Workaround*** |
| Set PRESC in BURTC_CTRL to greater than 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

## 2.3 CMU_E114 — Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK

| ***Description of Errata*** |
|---|
| Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK. |
| ***Affected Conditions / Impacts*** |
| If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2. |
| ***Workaround*** |
| Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.4 DAC_E109 — DAC Output Drift Over Lifetime

| *Description of Errata* |
|---|
| The voltage output of the DAC might drift over time. |
| ***Affected Conditions / Impacts*** |
| When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur. |
| ***Workaround*** |
| Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.5 DMA_E102 — 2D Copy Corrupted by Ping-Pong or Scatter-Gather Operation on Another Channel

| *Description of Errata* |
|---|
| When performing a 2D copy (rectangular copy) on one DMA channel, more data than is specified is occasionally transferred from the source buffer if another channel is being used in ping-pong or scatter-gather mode. |
| ***Affected Conditions / Impacts*** |
| The incorrect number of bytes is transferred during the 2D copy when there is corruption caused by concurrent ping-pong or scatter-gather operation. This would be most noticeable when 2D copy is used for moving a graphic image to a display but could cause problems in other use cases. |
| ***Workaround*** |
| Do not allow ping-pong or scatter-gather mode DMA transfers to occur concurrently with a 2D copy. If both types operations are required, interleave them such that the 2D copy is complete before enabling a channel in ping-pong or scatter-gather mode or vice versa. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.6 EMU_E107 — Interrupts During EM2 Entry

| *Description of Errata* |
|---|
| An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag. |
| ***Affected Conditions / Impacts*** |
| During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI is issued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0. |
| ***Workaround*** |
| Before entering EM2, disable all high frequency peripheral interrupts in the core. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.7 LCD_E103 — Indeterminate Animation Engine Start-Up

| *Description of Errata* |
|---|
| The LCD controller animation engine starts counting based on when the writes to LCD_AREGA and LCD_AREGB occur in relation to the clock for the animation frame counter. Because the animation engine cannot know when the writes occur, it is not possible to know whether the A or B register will shift first, which can result in one of the registers shifting twice before the other shifts once. |
| ***Affected Conditions / Impacts*** |
| Animations that require specific sequencing may not start in the correct state such that frames are not displayed in the correct order. |
| ***Workaround*** |
| If animation sequences must be seen in a specific order, consider handling this in software instead of using the animation engine. If the purpose of the animation is to denote ongoing activity, use segments that can be cycled in a generic fashion such that the output achieves the desired effect without depending on a specific frame order. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.8 LCD_E104 — Increased Current Draw when VLCD > VDDIO and LCD Pins are Used for GPIO

| *Description of Errata* |
|---|
| A leakage path to IOVDD exists when the LCD controller is configured to use the internally boosted or external power supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is due to PMOS transistors in the LCD pin logic having their source/bulk terminals connected to the highest VDD (thus the LCD power supply when external/boost mode is used) while their gates are connected to IOVDD. |
| ***Affected Conditions / Impacts*** |
| Use of LCD pins for GPIO results in increased current draw when the LCD controller is configured to use the internally boosted or external supply (LCD_DISPCTRL_VLCDSEL = VEXTBOOST) and VLCD > VDDIO. This is particularly noticeable when the device is operating in EM2 as the LCD to IOVDD supply leakage can amount to tens of microamps. While the GPIO functionality of the LCD pins is not impaired, for certain applications, the increased current draw can be undesirable. |
| ***Workaround*** |
| Do not use LCD pins for GPIO functionality if the LCD controller is configured to use an external power supply or boost mode, and the resulting VLCD can be greater than the IOVDD supply. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.9 LES_E104 — LFPRESC Can Extend Channel Start-Up Delay

| *Description of Errata* |
|---|
| Setting LESENSE_TIMCTRL_LFPRESC to a value other than DIV1 may delay channel start-up longer than the number of $LFACLK_{LESENSE}$ clock cycles specified by LESENSE_TIMCTRL_STARTDLY. |
| ***Affected Conditions / Impacts*** |
| Delaying channel start-up delays the subsequent excitation and measurement phases and may have an impact on the data returned by the LESENSE. |
| ***Workaround*** |
| If a channel start-up delay is used (LESENSE_TIMCTRL_STARTDLY > 0), LESENSE_TIMCTRL_LFPRESC must be set to DIV1. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.10 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

| ***Description of Errata*** |
|---|
| PCNT pulse width filtering does not work. |
| ***Affected Conditions / Impacts*** |
| The PCNT pulse width filter does not work as intended. |
| ***Workaround*** |
| Do not use the pulse width filter, i.e., ensure FILT = 0 in PCNTn_CTRL. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.11 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

| ***Description of Errata*** |
|---|
| The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled. |
| ***Affected Conditions / Impacts*** |
| When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable. |
| ***Workaround*** |
| Do not use a prescaled clock, i.e., ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.12 USART_E113 — IrDA Modulation and Transmission of PRS Input Data

| ***Description of Errata*** |
|---|
| If the USART IrDA modulator is configured to accept input from a PRS channel, the incoming data stream will not be transmitted because the required clock from the baud rate generator is never enabled. |
| ***Affected Conditions / Impacts*** |
| It is not possible for the USART IrDA modulator to directly transmit data from a source other than the USART's own transmitter. The USART_IRCTRL_IRPRSEN bit should remain at its reset state of 0. |
| ***Workaround*** |
| Assuming the data to be sent via the PRS is also data that could be received by the EFM32/EFR32 USART, then the data can be received using the USART's PRS RX feature (USART_INPUT_RXPRS = 1), stored in RAM (e.g., using DMA), and then transmitted with IrDA mode enabled. In cases where IrDA operation is transmit-only, the PRS RX data can be received on the same USART doing the transmission. If IrDA operation is bidirectional, then another USART must be used to receive the PRS data.<br><br>If the data to be sent is in some other format (e.g., pulses from a timer output), then there is no direct way to transmit it using the IrDA modulator. It would be necessary to capture the data in some other way and reformat it as serial data timed according to the clock generated by the USART. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.13 USB_E103 — HNP Sequence Fails if A-Device Connects After 3.4 ms

| ***Description of Errata*** |
|---|
| HNP Sequence fails if A-Device connects after 3.4 ms. |
| ***Affected Conditions / Impacts*** |
| The B-Device core only waits for up to 3.4 ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4 ms. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.14 USB_E104 — USB A-Device Delays the HNP Switch Back Process

| ***Description of Errata*** |
|---|
| The D+ line disconnects after 200 ms, delaying the HNP switch back process. |
| ***Affected Conditions / Impacts*** |
| The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.15 USB_E105 — B-Device as Host Driving K-J Pairs During Reset

| ***Description of Errata*** |
|---|
| The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode. |
| ***Affected Conditions / Impacts*** |
| If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.16 USB_E109 — Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1

| ***Description of Errata*** |
|---|
| A Host-initiated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt. |
| ***Affected Conditions / Impacts*** |
| When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect, will not result in a SessReq interrupt. |
| ***Workaround*** |
| If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

### 2.17 USB_E110 — Unexpected USB_HCx_INT.CHHLTD Interrupt

| ***Description of Errata*** |
|---|
| In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set. |
| ***Affected Conditions / Impacts*** |
| In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR, USB_HCx_INT.DATATGLERR, or USB_HCx_INT.XFERCOMPL interrupts enabled. |
| ***Workaround*** |
| If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt. |
| ***Resolution*** |
| There is currently no resolution for this issue. |

# 3. Resolved Errata Descriptions

This section contains previous errata for EFM32LG devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

### 3.1 ADC_E116 — Offset in ADC Temperature Sensor Calibration Data

| ***Description of Errata*** |
|---|
| The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset. |
| ***Affected Conditions / Impacts*** |
| For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset. |
| ***Workaround*** |
| For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.2 ADC_E117 — TIMEBASE not wide enough

| ***Description of Errata*** |
|---|
| For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough. |
| ***Affected Conditions / Impacts*** |
| For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz. |
| ***Workaround*** |
| If an ADC clock above 32 MHz is required, the acquistion time should be increased to also account for too short warmup-time. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.3 AES_E101 — BYTEORDER Does Not Work in Combination with DATASTART/XORSTART

| ***Description of Errata*** |
|---|
| When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XOR-START. |
| ***Affected Conditions / Impacts*** |
| If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order. |
| ***Workaround*** |
| Do not use BYTEORDER in combination with DATASTART or XORSTART. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.4 AES_E102 — AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set

| ***Description of Errata*** |
|---|
| When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late. |
| ***Affected Conditions / Impacts*** |
| If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption. |
| ***Workaround*** |
| If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.5 BURTC_E101 — BURTC LPMODE Entry

| ***Description of Errata*** |
|---|
| Entering LPMODE with LPCOMP=7 causes counter error. |
| ***Affected Conditions / Impacts*** |
| A counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates. |
| ***Workaround*** |
| Avoid using LPMODE with LPCOMP=7. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.6 BURTC_E102 — BURTC_CNT Read Error

| ***Description of Errata*** |
|---|
| Software reads from BURTC_CNT might fail when LPMODE is activated. |
| ***Affected Conditions / Impacts*** |
| When LPMODE is active (i.e., BURTC_STATUS_LPMODEACT is high), software reads might result in the wrong value being read from BURTC_CNT. |
| ***Workaround*** |
| Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.7 BU_E101 — Backup Power Increased Power Consumtion

| ***Description of Errata*** |
|---|
| Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN. |
| ***Affected Conditions / Impacts*** |
| Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN. |
| ***Workaround*** |
| Avoid having VDD_DREG in between 0.3 BU_VIN to 0.7 BU_VIN. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.8 BU_E102 — EM4 GPIO Retention in Backup Mode

| ***Description of Errata*** |
|---|
| EM4 GPIO retention not shut off in backup mode. |
| ***Affected Conditions / Impacts*** |
| With GPIO retention enabled, GPIO pins will still drive in backup mode. |
| ***Workaround*** |
| Do not use EM4 GPIO retention in combination with backup mode. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.9 BU_E104 — EM4 with Backup BODs

| ***Description of Errata*** |
|---|
| EM4 with backup BODs does not trigger reset. |
| ***Affected Conditions / Impacts*** |
| EM4 with backup BODs does not trigger reset. |
| ***Workaround*** |
| Avoid using backup BODs when entering EM4. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.10 BU_E106 — Current Leakage in Backup Mode

| ***Description of Errata*** |
|---|
| In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD. |
| ***Affected Conditions / Impacts*** |
| In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD. |
| ***Workaround*** |
| To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage starts by configuring the threshold in EMU_BUACT. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.11 CMU_E108 — LFxCLKEN Write

| ***Description of Errata*** |
|---|
| First write to LFxCLKEN can be missed. |
| ***Affected Conditions / Impacts*** |
| For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN may cause the write to miss its effect. |
| ***Workaround*** |
| For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.12 CMU_E110 — LFXO Phase Shift

| ***Description of Errata*** |
|---|
| Transients on pin D8 cause LFXO phase shift. |
| ***Affected Conditions / Impacts*** |
| Transients on pin D8 can give a temporary phase shift on LFXO. Frequency is unchanged. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.13 CMU_E111 — LFXO Configuration Incorrect

| ***Description of Errata*** |
| --- |
| For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect. |
| ***Affected Conditions / Impacts*** |
| For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect. |
| ***Workaround*** |
| On devices with PROD_REV < 15, change LFXOBUFCUR to 1 and LFXOBOOST to 0. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.14 CMU_E112 — LFXO Boost Buffer Current Setting

| ***Description of Errata*** |
| --- |
| LFXO boost buffer current must be disabled. |
| ***Affected Conditions / Impacts*** |
| LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set. |
| ***Workaround*** |
| Do not set LFXOBUFCUR in CMU_CTRL. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.15 CMU_E113 — LFXO Startup at High Temperature

| ***Description of Errata*** |
| --- |
| LFXO does not start at high temperature with default configuration. |
| ***Affected Conditions / Impacts*** |
| For devices with PROD_REV ≥ 16, the LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration. |
| ***Workaround*** |
| Make this line of code part of your startup code, typically in the start of `main()`:<br>`*((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) \| (1<<4);`<br>Version v5.1.1 of the Gecko SDK will include this workaround for all affected device revisions. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.16 CUR_E103 — Increased EM2 Current

| *Description of Errata* |
|---|
| Increased consumption in EM2. |
| ***Affected Conditions / Impacts*** |
| Current consumption in EM2 and EM3 has two stable states, the normal state (1200 nA and 900 nA for EM2 and EM3 respectively) and an error state. In the error state, the current consumption in EM2 and EM3 is typically 4.5 µA at 25 °C (manufacturing test limit is set to 7 µA) but will increase with increased temperature. At 85 °C, the error state EM2 and EM3 current consumption is typically 25 µA. It is unpredictable which state the device will go into on EM2/EM3 entry and it can also change state during operation. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.17 CUR_E104 — Increased Current on AVDD2 (USB)

| *Description of Errata* |
|---|
| On devices with USB, there can be increased current on AVDD2 related to VREGO. |
| ***Affected Conditions / Impacts*** |
| When VREGO is floating or 0 V, a leakage can appear on AVDD2. This leakage is typically less than 10 µA, but can also rise to around 300 µA. |
| ***Workaround*** |
| Make sure VREGO is always defined high when there is power on AVDD2. For bus-powered devices this is always the case, but for devices where the power on VREGO can be lost during operation, e.g., a USB device where the USB phy is powered from VBUS when a master is attached, a 5 MΩ to VDD can help keep VREGO defined. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.18 CUR_E105 — Increased Current on AVDD2 (No USB)

| *Description of Errata* |
|---|
| On devices without USB, an increased current on AVDD2 can appear due to a floating internal node. This leakage is typically less than 10 µA, but can also rise to around 300 µA. The leakage is present in all energy modes. |
| ***Affected Conditions / Impacts*** |
| An increased current on AVDD2 can appear due to a floating internal node. This leakage is typically less than 10 µA, but can also rise to around 300 µA. The leakage is present in all energy modes. |
| ***Workaround*** |
| To reduce this leakage to a few hundred nanoamps, set MODE10 and MODE11 in GPIO->P[5].MODEH to GPIO_P_MODEH_MODE10_PUSHPULL and GPIO_P_MODEH_MODE11_PUSHPULL respectively, and make sure bits 10 and 11 in GPIO->P[5].DOUT are set. To ensure GPIO->P[5] bits 10 and 11 stay set in EM4, set EM4RET in GPIO_CTRL to turn on GPIO retention before entering EM4. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.19 DI_E101 — Flash Page Size

| *Description of Errata* |
|---|
| The MEM_INFO_PAGE_SIZE value stored in the Device Information (DI) Page is incorrect. |
| ***Affected Conditions / Impacts*** |
| For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect. |
| ***Workaround*** |
| Use fixed flash page size of 4 kB. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.20 DMA_E101 — EM2 with WFE and DMA

| *Description of Errata* |
|---|
| WFE does not work for the DMA in EM2. |
| ***Affected Conditions / Impacts*** |
| In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system. |
| ***Workaround*** |
| Use WFI (Wait for Interrupt) or EM1 instead. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.21 EBI_E101 — EBI Masking Functionality

| *Description of Errata* |
|---|
| EBI masking functionality is not limited to bank selected for TFT. |
| ***Affected Conditions / Impacts*** |
| EBI masking functionality is not limited to the bank selected for TFT (by BANKSEL field in EBI_TFTCTRL). When masking is enabled, a mask match can be generated and suppress writes to any bank. |
| ***Workaround*** |
| Disable masking when doing writes that should not be affected. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.22 EBI_E102 — EBI Access Fails

| *Description of Errata* |
|---|
| Certain EBI accesses via the Cortex and Debug interface do not work. |
| ***Affected Conditions / Impacts*** |
| Any access from the Cortex to the EBI not aligned to its size does not work. Also, only word accesses from the debug interface works. |
| ***Workaround*** |
| Make sure all accesses via the Cortex are aligned to its size, and that all debug accesses are word accesses. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.23 EBI_E103 — Page Mode Read in D16A16ALE Mode

| *Description of Errata* |
|---|
| Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses. |
| ***Affected Conditions / Impacts*** |
| Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA. |
| ***Workaround*** |
| To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.24 EMU_E105 — Debug Unavailable During DMA Processing from EM2

| *Description of Errata* |
|---|
| The debugger cannot access the system processing DMA request from EM2. |
| ***Affected Conditions / Impacts*** |
| DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access. |
| ***Workaround*** |
| Make sure DMA requests triggered from EM2 are handled. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.25 EMU_E110 — Potential Hard Fault when Exiting EM2 or EM3

| ***Description of Errata*** |
|---|
| The flash is powered down in EM2 and EM3 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2 or EM3, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 or EM3 that is potentially erroneous. |
| ***Affected Conditions / Impacts*** |
| When exiting EM2 or EM3, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source. |
| ***Workaround*** |
| To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 or EM3 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL:<br><br>https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2017/05/09/emu_e110_-_potential-i2Pn |
| ***Resolution*** |
| This issue has been resolved. Devices with a date code greater than or equal to 1742 will not have this issue. |

### 3.26 ETM_E101 — ETM Trace Clock

| ***Description of Errata*** |
|---|
| ETM Trace Clock needs to be delayed. |
| ***Affected Conditions / Impacts*** |
| ETM trace clock is out of phase making the data transition occur at the same time as the ETM trace clock transitions. |
| ***Workaround*** |
| ETM trace clock needs to be delayed between 10 ns and 1/4 of the trace clock period. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.27 GPIO_E101 — GPIO Wakeup from EM4

| ***Description of Errata*** |
|---|
| On GPIO wakeup from EM4, all cause bits for high-polarity wakeup pins are set. |
| ***Affected Conditions / Impacts*** |
| All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup. |
| ***Workaround*** |
| Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.28 LES_E101 — LESENSE and Schmitt Trigger

| ***Description of Errata*** |
|---|
| Schmitt trigger cannot be disabled on pins used for sensor excitation |
| ***Affected Conditions / Impacts*** |
| When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable amount of current. |
| ***Workaround*** |
| Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.29 LES_E102 — LESENSE and DAC CH1 Configuration

| ***Description of Errata*** |
|---|
| LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE. |
| ***Affected Conditions / Impacts*** |
| LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE. |
| ***Workaround*** |
| Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.30 LES_E103 — AUXHFRCO and LESENSE

| ***Description of Errata*** |
|---|
| LESENSE will not work properly at low AUXHFRCO frequencies. |
| ***Affected Conditions / Impacts*** |
| LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band. |
| ***Workaround*** |
| Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.31 OPA_E101 — OPAMP 2 Startup Rampup

| *Description of Errata* |
|---|
| When OPA2 is started, the output ramp-up is constant independent of bias setting. |
| ***Affected Conditions / Impacts*** |
| When OPA2 is started the output ramp-up is constant independent of bias setting. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.32 PRS_E101 — Edge Detect on GPIO/ACMP

| *Description of Errata* |
|---|
| Edge detect on peripherals with asynchronous edges might be missed. |
| ***Affected Conditions / Impacts*** |
| When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC, edges can be missed. |
| ***Workaround*** |
| Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.33 RMU_E101 — POR Calibration Initialization Issue

| ***Description of Errata*** |
|---|
| Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values. |
| ***Affected Conditions / Impacts*** |
| The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround.<br><br>Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B):<br><br>A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself.<br><br>B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET.<br><br>A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event. |
| ***Workaround*** |
| Additional information including a software workaround is available from the following KB article URL:<br><br>https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2015/10/09/rmu_e101_-_por_calib-cEpZ |
| ***Resolution*** |
| This issue has been resolved. Devices with a date code and PROD_REV greater than or equal to 1539 and 0x96 respectively will not have this issue. |

### 3.34 RMU_E102 — Regulator Output May Be 0 V After Supply Falls to Intermediate Voltage and Recovers

| ***Description of Errata*** |
|---|
| Output of the on-chip regulator (DECOUPLE pin) may be approximately 0 V, and the device will not respond to a pin reset. |
| ***Affected Conditions / Impacts*** |
| The device supply voltage is specified as 1.98 V minimum. For certain supply waveforms, similar to disconnecting a battery, allowing the supply to decay to approximately 0.9 V (and stopping the decay at approximately 0.9 V), then reconnecting the battery, the output of the regulator (DECOUPLE pin) may be approximately 0 V. In this state, code will not execute, and the device will not respond to a pin reset. More information on this issue can be found at the following KB article URL:<br><br>https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e102_por_bodres-AQh7 |
| ***Workaround*** |
| Hold the RESETn pin logic low, starting before the supply is disconnected, and keep RESETn pin logic low until the supply reaches a valid voltage. If the DECOUPLE pin measures approximately 0 V, power cycle the supplies by pulling them all the way to 0 V before connecting supplies again. |
| ***Resolution*** |
| This issue is resolved in revision F devices. |

### 3.35 RMU_E103 — Reset May Fail to Trigger During Supply Voltage Brownouts

| *Description of Errata* |
|---|
| Reset may fail to trigger when the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range. |
| ***Affected Conditions / Impacts*** |
| If the device supplies (AVDD_0, AVDD_2, VDD_DREG) fall to a voltage in the 1.25 - 1.45 V range, the device may fail to reset, allowing code execution while the supply voltage remains in the 1.25 - 1.45 V range. More information on this issue can be found at the following KB article URL:<br><br>https://www.silabs.com/community/mcu/32-bit/knowledge-base.entry.html/2019/01/09/rmu_e103_por_bodres-N3MD |
| ***Workaround*** |
| Hold the RESETn pin in logic low, starting before the device supplies fall below 1.6 V, and keep the RESETn pin logic low until the device supplies reach a valid voltage again. |
| ***Resolution*** |
| This issue is resolved in revision F devices. |

### 3.36 USART_E112 — USART AUTOTX Continues to Transmit Even With Full RX Buffer

| *Description of Errata* |
|---|
| USART AUTOTX continues to transmit even with full RX buffer. |
| ***Affected Conditions / Impacts*** |
| When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision E devices. |

### 3.37 USB_E101 — USB DMA Transfers with Prescaled HFCLK

| *Description of Errata* |
|---|
| USB DMA transfers to flash fail when prescaling HFCLK. |
| ***Affected Conditions / Impacts*** |
| USB DMA transfers to flash may fail when prescaling HFCLK. |
| ***Workaround*** |
| Do not prescale HFCLK when using USB-DMA transfers to read from flash. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.38 USB_E102 — USB Datalines

| *Description of Errata* |
|---|
| USB datalines rise and fall time are slightly outside specification. |
| ***Affected Conditions / Impacts*** |
| USB datalines rise and fall time are slightly outside specification under worst case conditions. They may fail USB certification eye test depending on PCB layout. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.39 USB_E106 — USB Interrupts

| *Description of Errata* |
|---|
| USB interrupts have changed from being level triggered to edge triggered. |
| ***Affected Conditions / Impacts*** |
| USB interrupts are now trigggered by signal edge rather then signal level. |
| ***Workaround*** |
| Make sure to handle edge triggered interrupts, rather then signal level interrupts. |
| ***Resolution*** |
| This issue is resolved in revision C devices. |

### 3.40 USB_E107 — Entry to EM4 Causes Temporary Leakage from VREGO

| *Description of Errata* |
|---|
| Entry to EM4 causes temporary leakage from VREGO. |
| ***Affected Conditions / Impacts*** |
| On transition from EM0 to EM4, a current leakage from VREGO of up to 1 mA lasting a few seconds can occur. |
| ***Workaround*** |
| No known workaround. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

### 3.41 USB_E108 — Floating DM/DP Pins Cause Leakage when USB is Disabled

| ***Description of Errata*** |
|---|
| Floating DM/DP pins cause leakage when USB is disabled. |
| ***Affected Conditions / Impacts*** |
| When the USB_DM or USB_DP pins are floating while the USB PHY is disabled, a current in the order of a couple hundred µA may leak from USB_VREGO to VSS. This will not be an issue if there is no voltage applied to USB_VREGO, either externally or through the USB regulator. |
| ***Workaround*** |
| If there is no intention to use the USB module, e.g., the USB PHY is disabled, but there is still a voltage on USB_VREGO, make sure the USB_DM and USB_DP pins are defined. This can be done using GPIO or by defining them externally. |
| ***Resolution*** |
| This issue is resolved in revision D devices. |

# 4. Revision History

**Revision 1.40**

November, 2019

- Updated to product revision F.
- Added ADC_E118 and LES_E104.
- Resolved RMU_E102 and RMU_E103.
- Migrated to new errata document format.

**Revision 1.30**

January, 2019

- Added DMA_E102, LCD_E103, LCD_E104, RMU_E102, RMU_E103, and USART_E113.
- Resolved EMU_E110 and updated language to refer to both EM2 and EM3.
- Removed ADC_E101, CMU_E103, CMU_E104, CMU_E105, MSC_E101, and USART_E101 from revision history. These errata have never been present on Leopard Gecko.
- RMU_E101 workaround URL updated.

**Revision 1.20**

April, 2017

- Added EMU_E110.
- Updated errata formatting.
- Merged all errata documents for EFM32LG devices into one document.
- Merged errata history and errata into one document.

**Revision 1.10**

October, 2015

- Added DAC_E109, EMU_E107, PCNT_E102, RMU_E101, and TIMER_E103.

**Revision 1.00**

October, 2014

- Initial release for EFM32LG360 and EFM32LG900 devices.

**Revision 0.70**

June, 2014

- Updated to product revision E.
- Removed errata that are not applicable to revision E.

**Revision 0.60**

August, 2013

- Added ADC_E117, AES_E102, USB_E109, and USB_E110.
- Updated disclaimer, trademark and contact information.

**Revision 0.50**

July, 2013

- Added AES_E101, BURTC_E102, CMU_E114, and DMA_E101.
- Updated errata naming convention.

**Revision 0.40**

June, 2012

- Added DI_E101.

**Revision 0.30**

April, 2012

- Added BU_E106 and LES_E103.

**Revision 0.20**

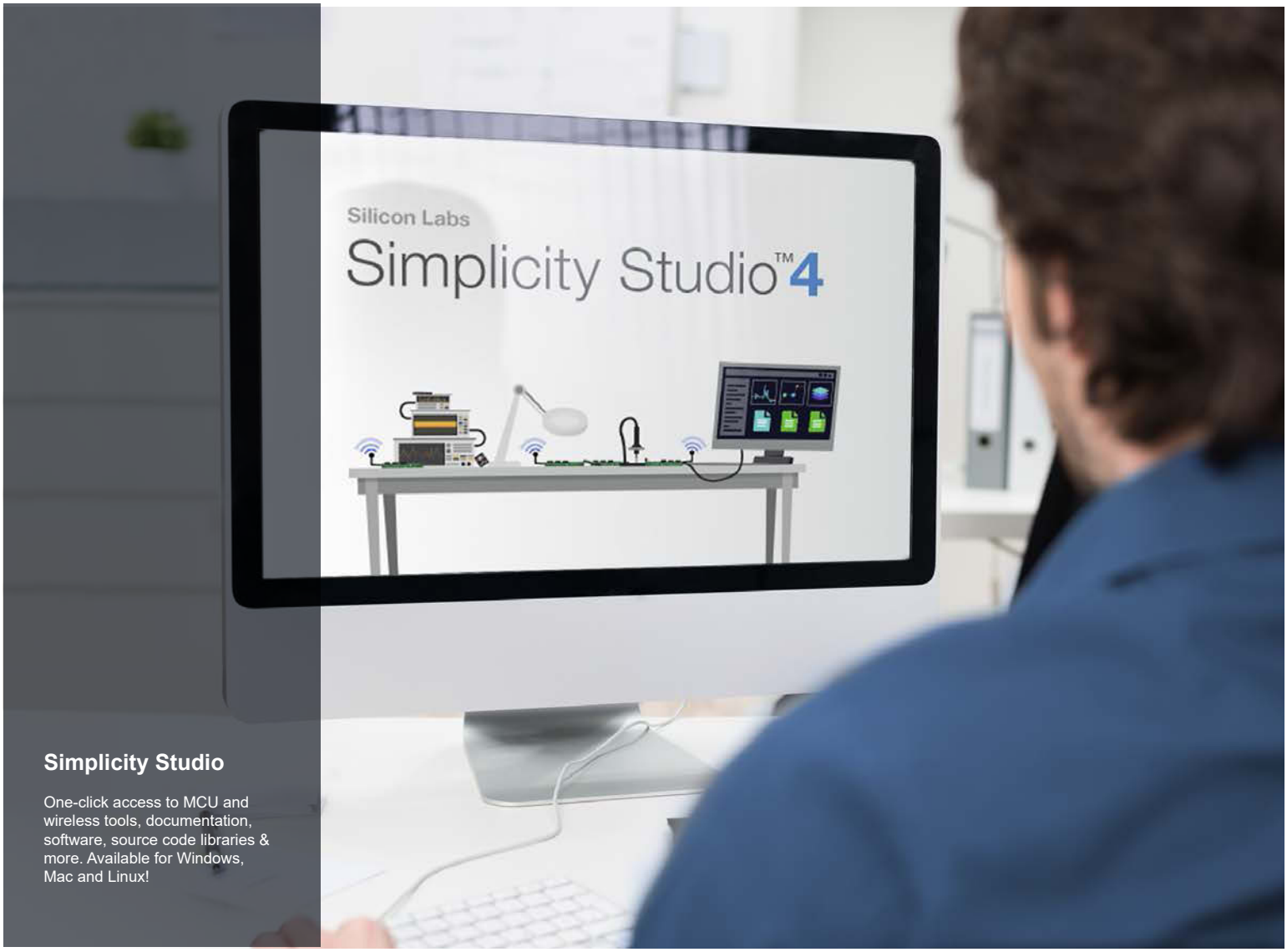
January, 2012

- Added CUR_E103, CUR_E104, CUR_E105, USB_E107, and USB_E108.
- Updated PRS_E101.
- Removed Erratas not valid for chip revision.

**Revision 0.10**

November, 2011

- Initial preliminary release.

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