Silicon Carbide Schottky Diode

650 V, 10 A

FFSD1065A

Description

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

Features

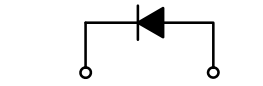
- Max Junction Temperature 175°C
- Avalanche Rated 64 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant

Applications

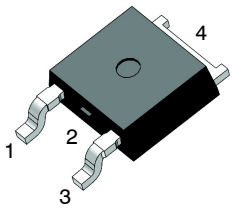
- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

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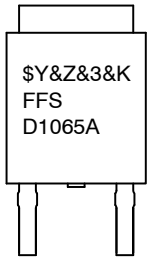


Schottky Diode



DPAK3 (TO−252, 3 LD)
CASE 369AS

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FFSD1065A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Rating	Parameter	FFSD1065A	Unit
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
E_{AS}	Single Pulse Avalanche Energy (Note 1)		64	mJ
I_F	Continuous Rectified Forward Current @ T_C < 158°C		10	A
	Continuous Rectified Forward Current @ T_C < 135°C		18	
$I_{F,MAX}$	Non−Repetitive Peak Forward Surge Current	T_C = 25°C, 10 μs	760	A
		T_C = 150°C, 10 μs	740	A
$I_{F,SM}$	Non−Repetitive Forward Surge Current	Half−Sine Pulse, tp = 8.3 ms	56	A
$I_{F,RM}$	Repetitive Forward Surge Current	Half−Sine Pulse, tp = 8.3 ms	34	A
Ptot	Power Dissipation	T_C = 25°C	150	W
		T_C = 150°C	25	W
T_J. T_{STG}	Operating and Storage Temperature Range		−55 to + 175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
V_F	Forward Voltage	I_F = 10 A, T_C = 25°C	–	1.50	1.75	V
		I_F = 10 A, T_C = 125°C	–	1.6	2.0	
		I_F = 10 A, T_C = 175°C	–	1.72	2.4	
I_R	Reverse Current	V_R = 650 V, T_C = 25°C	–	–	200	μA
		V_R = 650 V, T_C = 125°C	–	–	400	
		V_R = 650 V, T_C = 175°C	–	–	600	
Q_C	Total Capacitive Charge	V = 400 V	–	34	–	nC
C	Total Capacitance	V_R = 1 V, f = 100 kHz	–	575	–	pF
		V_R = 200 V, f = 100 kHz	–	62	–	
		V_R = 400 V, f = 100 kHz	–	47	–	

1. E_{AS} of 64 mJ is based on starting T_J = 25°C; L = 0.5 mH, I_{AS} = 16 A, V = 50 V.

ORDERING INFORMATION

Device	Marking	Package	Reel Size†	Tape Width	Quantity
FFSD1065A	FFSD1065A	DPAK3	13″	N/A	2500

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

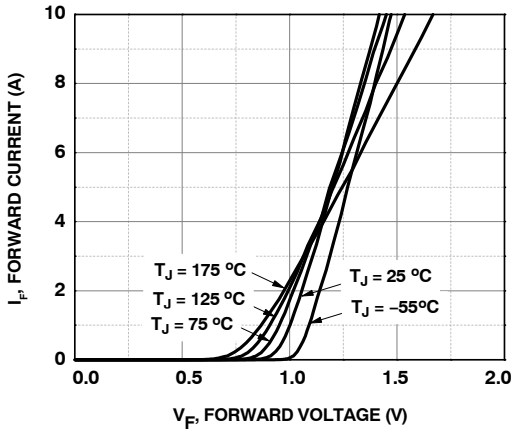


Figure 1. Forward Characteristics

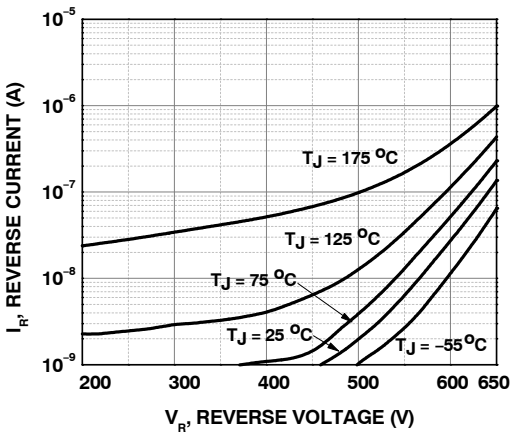


Figure 2. Reverse Characteristics

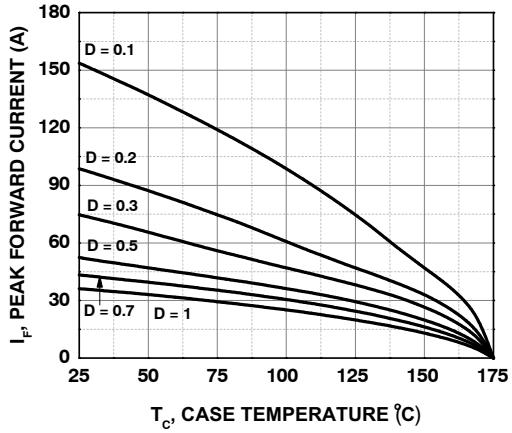


Figure 3. Current Derating

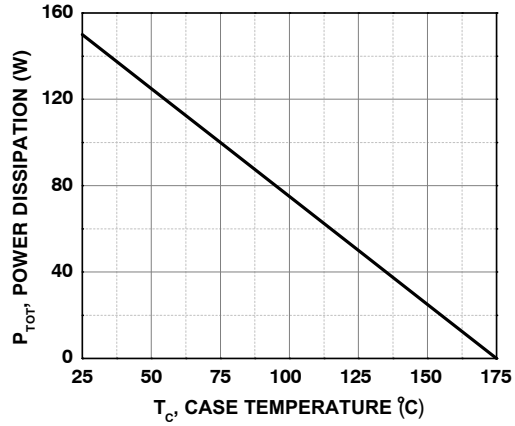


Figure 4. Power Derating

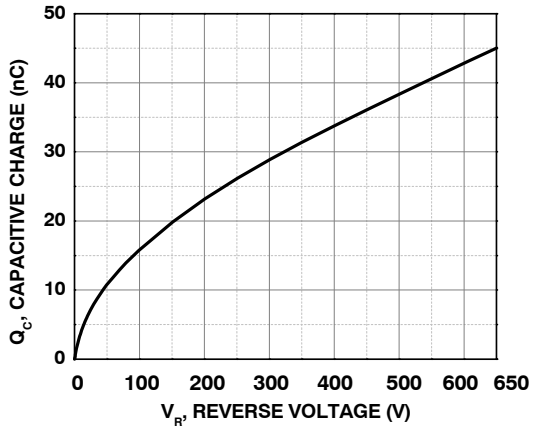


Figure 5. Capacitive Charge vs. Reverse Voltage

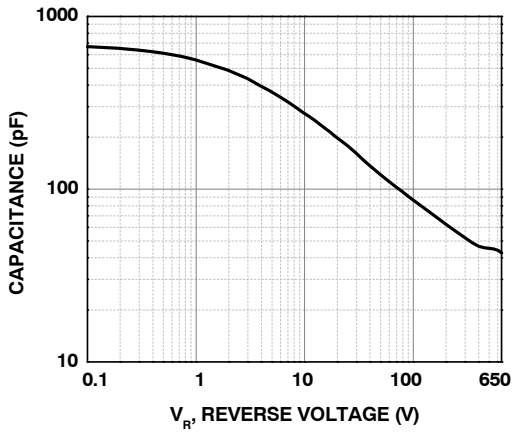


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

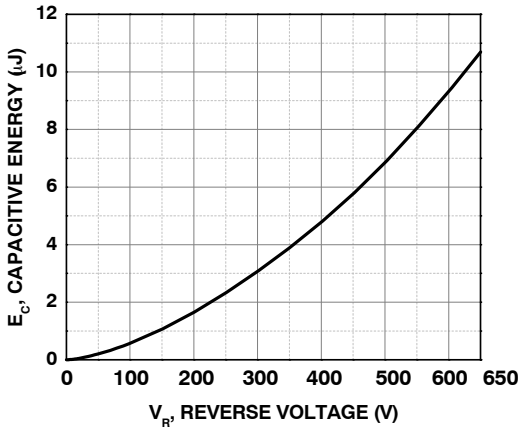


Figure 7. Capacitance Stored Energy

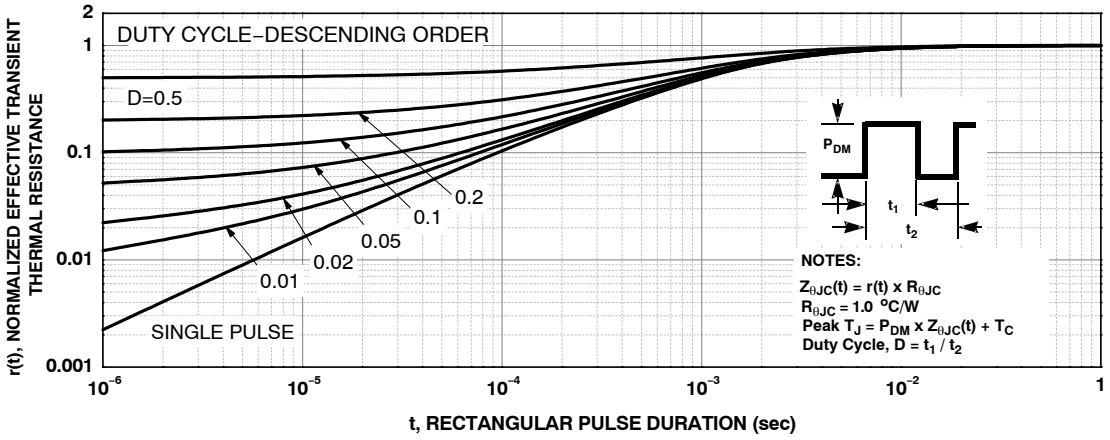


Figure 8. Junction−to−Case Transient Thermal Response Curve

TEST CIRCUIT AND WAVEFORMS

L = 0.5 mH
R < 0.1 Ω
V_{DD} = 50 V
EAVL = 1/2LI2 [$V_{R(AVL)}$ / ($V_{R(AVL)}$ − V_{DD})]
Q1 = IGBT (BV_{CES} > DUT $V_{R(AVL)}$)

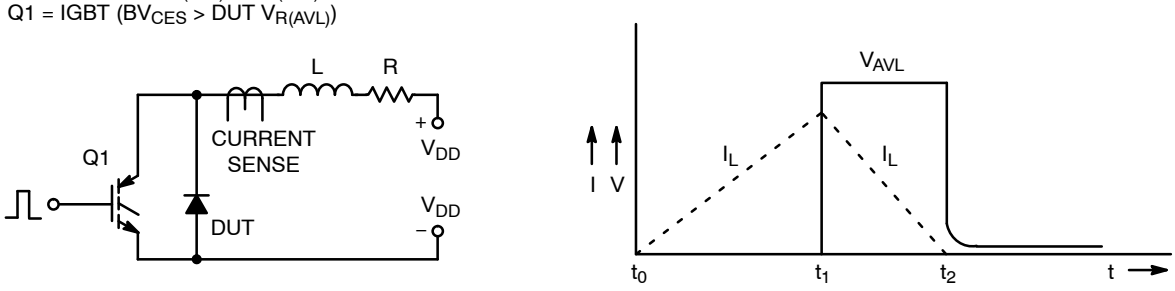
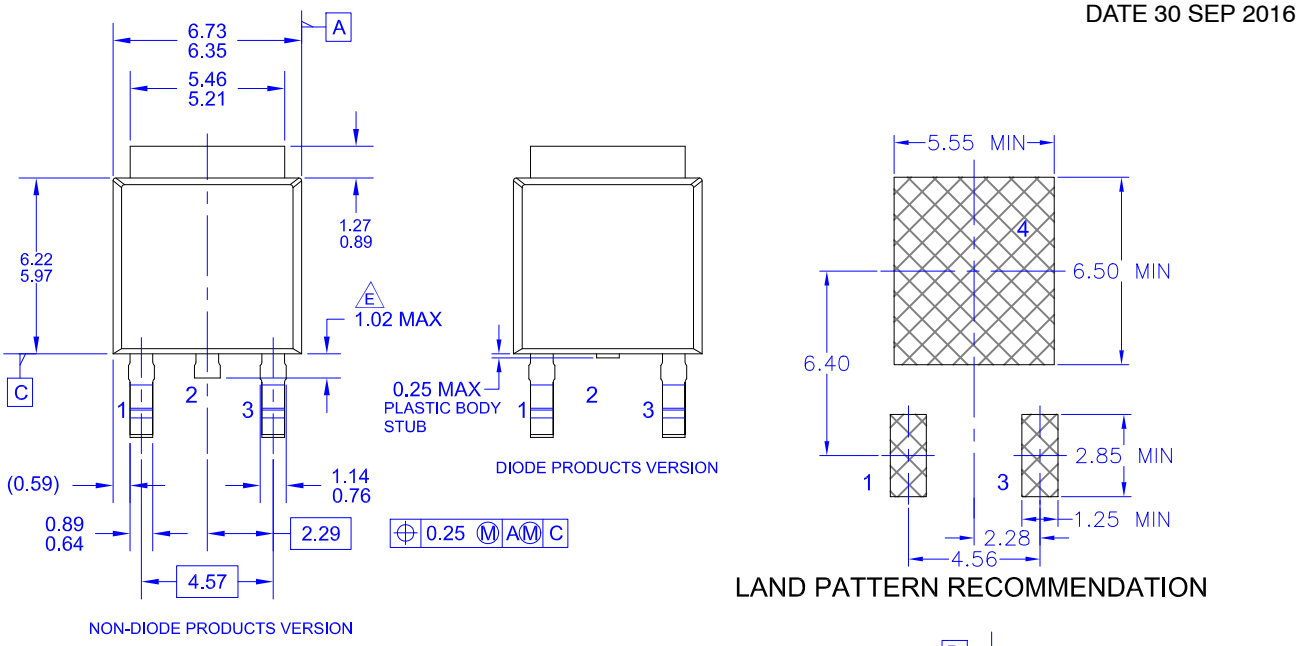
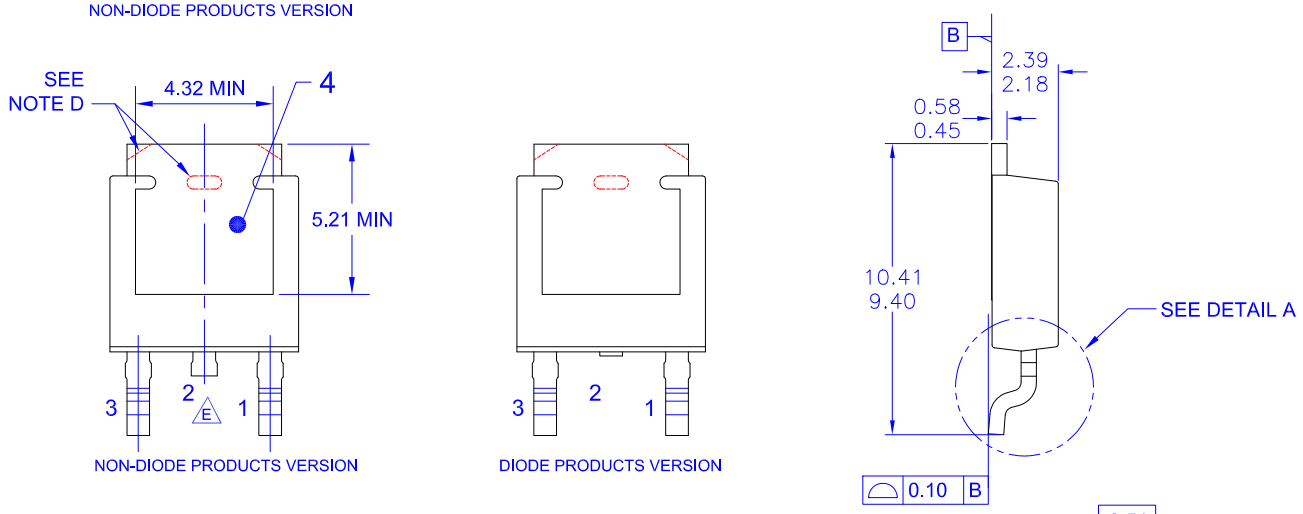


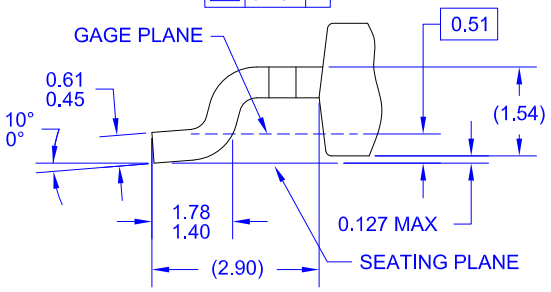
Figure 9. Unclamped Inductive Switching Test Circuit & Waveform

DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

DATE 30 SEP 2016







NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

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