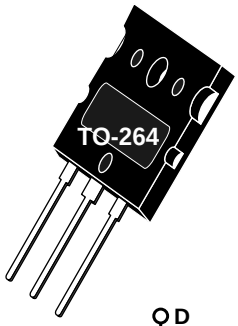
APT5010LVFR

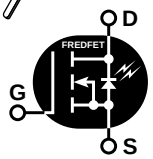
500V 47A 0.100Ω

POWER MOS V® FREDFET



Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- **Fast Recovery Body Diode**
- **100% Avalanche Tested**
- **Lower Leakage**
- **Popular TO-264 Package**
- **Faster Switching**



MAXIMUM RATINGS All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT5010LVFR	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ T_C = 25°C	47	Amps
I_{DM}	Pulsed Drain Current ①	188	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ T_C = 25°C	520	Watts
	Linear Derating Factor	4.16	W/°C
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① (Repetitive and Non-Repetitive)	47	Amps
E_{AR}	Repetitive Avalanche Energy ①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ④	2500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250μA)	500			Volts
$I_{D(on)}$	On State Drain Current ② (V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max, V_{GS} = 10V)	47			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ② (V_{GS} = 10V, 0.5 $I_{D[Cont.]}$)			0.100	Ohms
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = V_{DSS}, V_{GS} = 0V)			250	μA
	Zero Gate Voltage Drain Current (V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125°C)			1000	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 2.5mA)	2		4	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - http://www.advancedpower.com

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050-5546 Rev C

DYNAMIC CHARACTERISTICS

APT5010LVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 0V		7400	8900	pF
C_{oss}	Output Capacitance	V_{DS} = 25V		1000	1400	
C_{rss}	Reverse Transfer Capacitance	f = 1 MHz		380	570	
Q_g	Total Gate Charge ③	V_{GS} = 10V		312	470	nC
Q_{gs}	Gate-Source Charge	V_{DD} = 0.5 V_{DSS}		50	75	
Q_{gd}	Gate-Drain ("Miller") Charge	I_D = I_D [Cont.] @ 25°C		127	190	
$t_d(on)$	Turn-on Delay Time	V_{GS} = 15V		14	30	ns
t_r	Rise Time	V_{DD} = 0.5 V_{DSS}		16	32	
$t_d(off)$	Turn-off Delay Time	I_D = I_D [Cont.] @ 25°C		54	80	
t_f	Fall Time	R_G = 0.6Ω		5	10	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions		MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)				47	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)				188	
V_{SD}	Diode Forward Voltage ② (V_{GS} = 0V, I_S = -I_D [Cont.])				1.3	Volts
$^{dv}/_{dt}$	Peak Diode Recovery $^{dv}/_{dt}$ ⑤				5	V/ns
t_{rr}	Reverse Recovery Time (I_S = -I_D [Cont.], $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C			250	ns
		T_j = 125°C			500	
Q_{rr}	Reverse Recovery Charge (I_S = -I_D [Cont.], $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C		1.6		µC
		T_j = 125°C		5.5		
I_{RRM}	Peak Recovery Current (I_S = -I_D [Cont.], $^{di}/_{dt}$ = 100A/µs)	T_j = 25°C		15		Amps
		T_j = 125°C		27		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.24	°C/W
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 µS, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 2.26mH, R_G = 25Ω, Peak I_L = 47A

⑤ $I_S \le -I_D$ [Cont.], $^{di}/_{dt}$ = 100A/µs, $V_{DD} \le V_{DSS}$, $T_j \le 150°C$, R_G = 2.0Ω, V_R = 200V.

APT Reserves the right to change, without notice, the specifications and information contained herein.

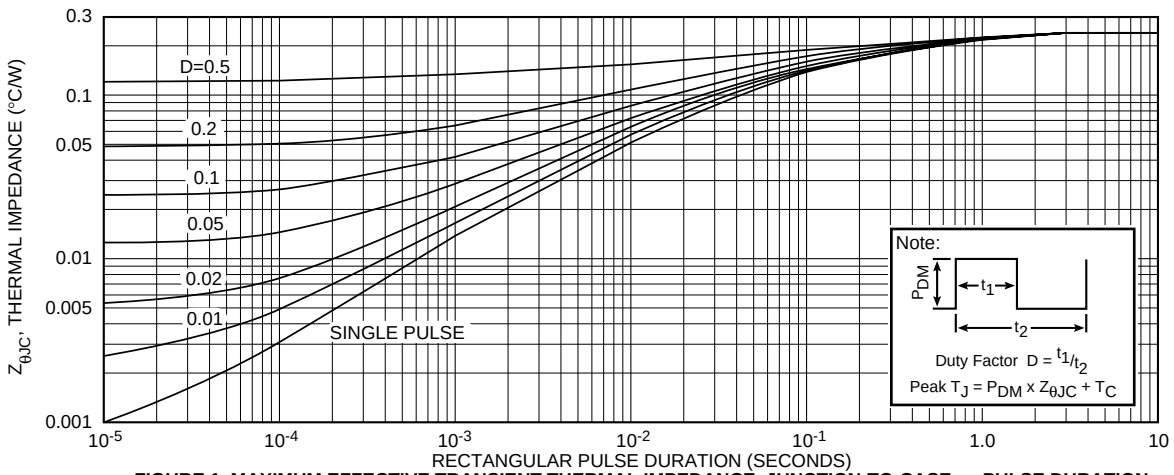


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

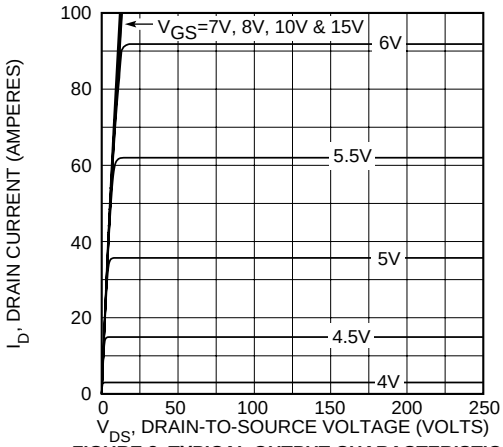


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

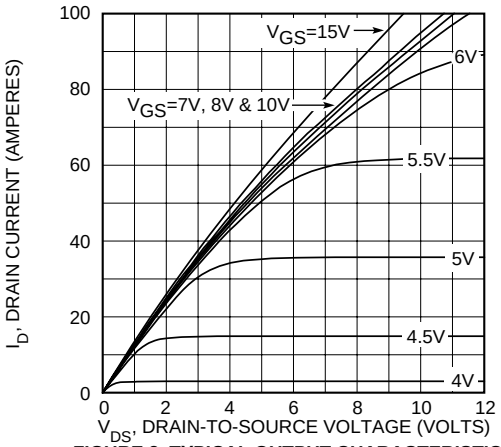


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

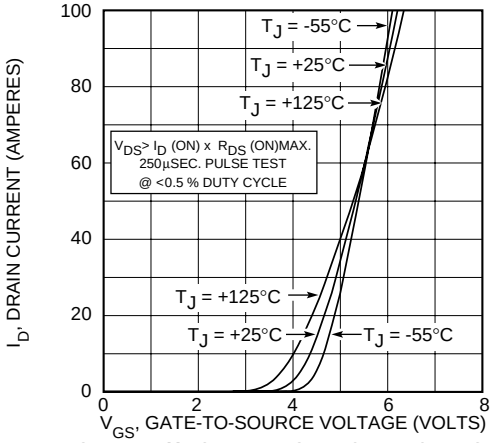


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

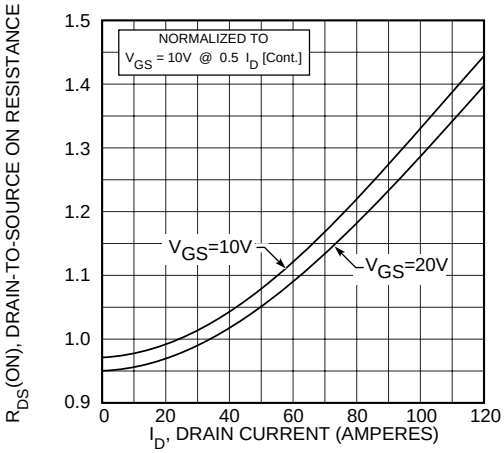


FIGURE 5, R_{DS}(ON) vs DRAIN CURRENT

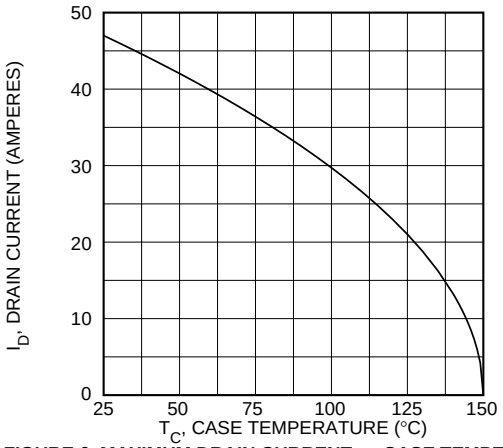


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

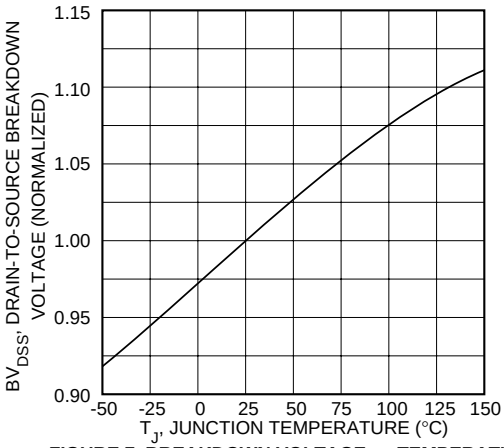


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

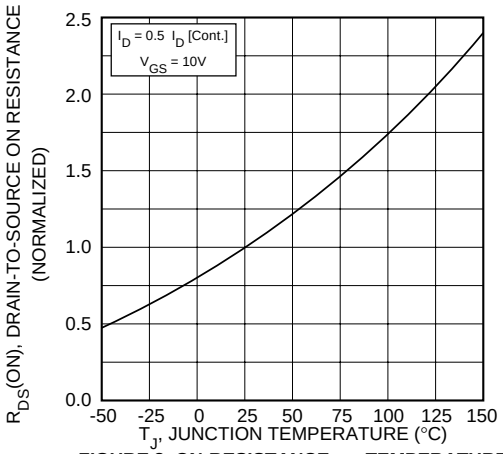


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

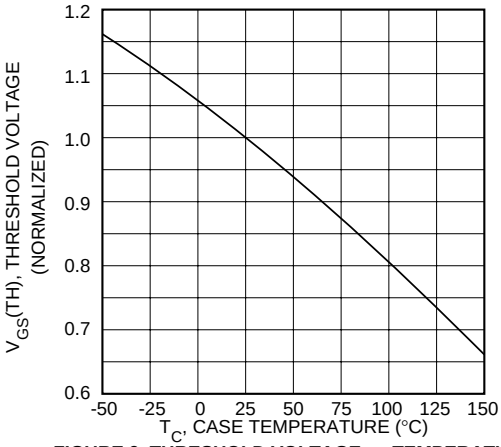


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

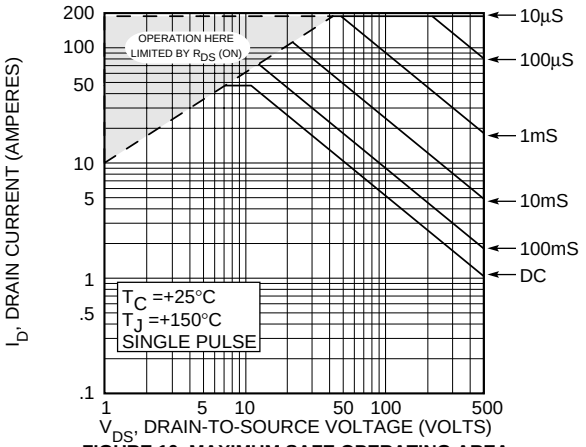


FIGURE 10, MAXIMUM SAFE OPERATING AREA

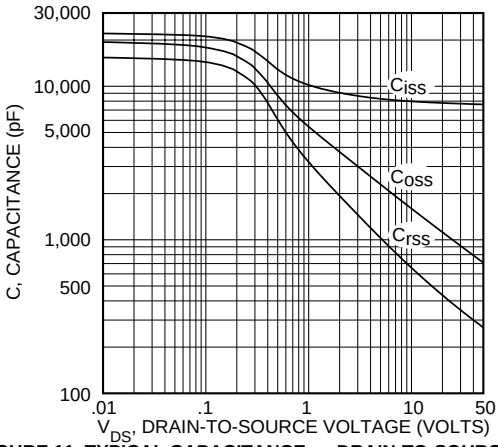


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

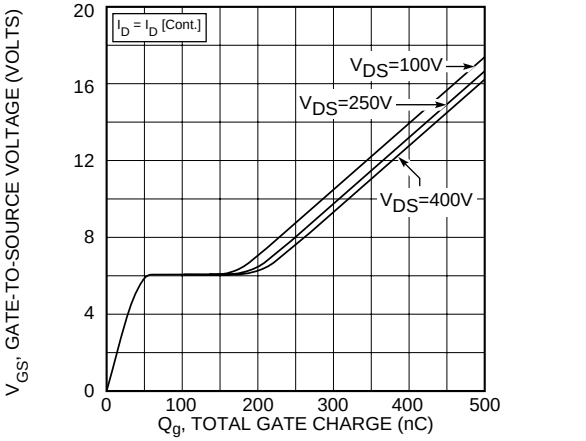


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

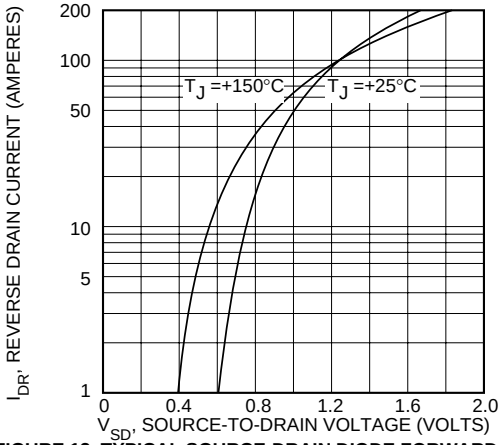
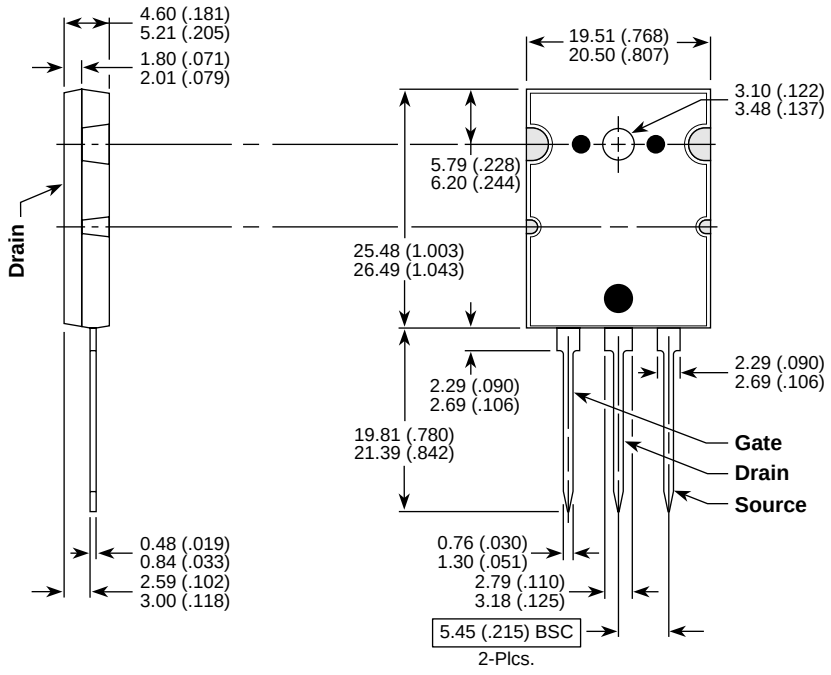


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-264 Package Outline



Dimensions in Millimeters and (Inches)

APT's devices are covered by one or more of the following U.S.patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058