TPS54561-Q1 4.5-V to 60-V Input, 5-A, Step-Down DC-DC Converter With Eco-mode™

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification H1C
  - Device CDM ESD Classification C5
- High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control
- 87-mΩ High-Side MOSFET
- 152-µA Operating Quiescent Current and 2-µA Shutdown Current
- 100-kHz to 2.5-MHz Switching Frequency
- Synchronizes to External Clock
- Low-Dropout Operation at Light Loads With Integrated BOOT Recharge FET
- Adjustable UVLO Voltage and Hysteresis
- Power-Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Soft-Start and Sequencing
- 0.8-V 1% Internal Voltage Reference
- 10-Pin WSON With Thermal Pad Package
- –40°C to 150°C T_J Operating Range
- Create a Custom Design using the TPS54561-Q1 with the WEBENCH® Power Designer

2 Applications

- Vehicle Accessories: GPS (see SLVA412), Entertainment
- USB Dedicated Charging Ports and Battery Chargers (see SLVA464)
- 12-V and 24-V Automotive Power Systems

3 Description

The TPS54561-Q1 device is a 60-V, 5-A, step-down regulator with an integrated high-side MOSFET. The device survives load dump pulses up to 65 V per ISO7637. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode and 152-µA supply current enables high efficiency at light loads. Pulling the enable pin low reduces shutdown supply current to 2 µA .

Undervoltage lockout has an internal 4.3-V setting. Use of an external resistor divider at the EN pin can increase the setting. The soft-start pin controls the output-voltage start-up ramp and also configures sequencing or tracking. An open-drain power-good signal indicates the output is within 93% to 106% of its nominal voltage.

A wide adjustable switching-frequency range allows optimization for either efficiency or external component size. Cycle-by-cycle current limit, frequency foldback, and thermal shutdown protect the device during an overload condition.

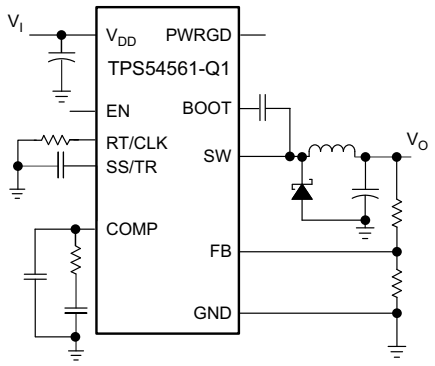
The TPS54561-Q1 is available in a 10-pin, 4-mm × 4-mm WSON package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54561-Q1	WSON (10)	4.00 mm × 4.00 mm

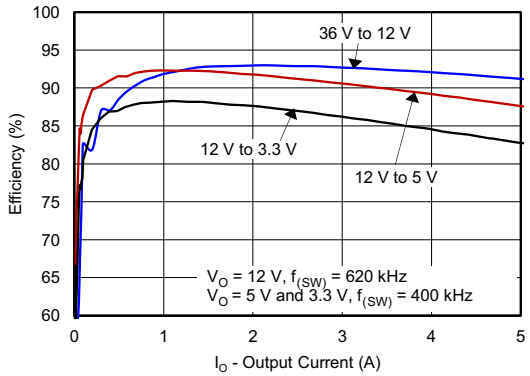
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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Efficiency vs Load Current



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4 Revision History

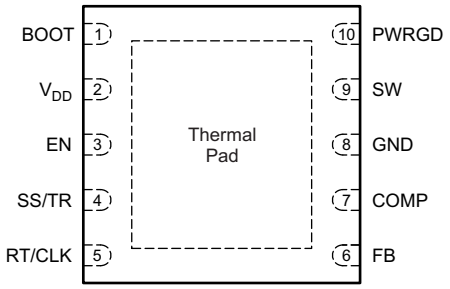
Changes from Original (September 2014) to Revision A **Page**

- Changed package SON To: WSON in the Features and throughout the data sheet ... 1
- Added the WEBENCH information in the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Added SW, 5-ns transient to the *Absolute Maximum Ratings* ... 4
- Moved Storage temperature range to the *Absolute Maximum Ratings* ... 4
- Changed the *Handling Ratings* table to the *ESD Ratings* ... 4
- Changed Equation 10 and Equation 11 ... 19
- Changed Equation 30 ... 30
- Changed Equation 33 ... 30
- Moved *Power Dissipation Estimate* to the *Detailed Design Procedure* section ... 35
- Moved the location of the *Safe Operating Area* ... 37
- Moved *Inverting Power Supply* and *Split-Rail Power Supply* to the *Application Information* section ... 41

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5 Pin Configuration and Functions

DPR Package
10-Pin WSON
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	The device requires a bootstrap capacitor between BOOT and SW. If the voltage on this capacitor is below the minimum required voltage to operate the high-side MOSFET, the gate driver switches off until the bootstrap capacitor recharges.
COMP	7	O	Error amplifier output, and input to the output switch-current comparator (PWM comparator). Connect frequency compensation components to this pin.
EN	3	I	Enable pin, with internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the *Enable and Adjust Undervoltage Lockout* section.
FB	6	I	Inverting input of the transconductance (g_m) error amplifier.
GND	8	—	Ground
PWRGD	10	O	Power-good is an open-drain output that asserts if the output voltage is low because of thermal shutdown, dropout, overvoltage, or EN shutdown.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. When pulled above the PLL upper threshold, a mode change occurs, and the pin becomes a synchronization input. This change disables the internal amplifier, and the pin is a high-impedance clock input to the internal PLL. Stopping the clocking edges re-enables the internal amplifier, and the operating mode returns to resistor programmed mode.
SS/TR	4	I	Soft-start and tracking input pin. An external capacitor connected to this pin sets the output rise time. A voltage on this pin overrides the internal reference, which allows use of the pin for tracking and sequencing.
SW	9	I	The source of the internal high-side power MOSFET, and switching node of the converter.
V_{DD}	2	I	Input supply pin with 4.5-V to 60-V operating range.
Thermal pad	—	—	To ensure proper operation, electrically connect the GND pin to the copper pad under the IC on the printed circuit board.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage	V_{DD}	–0.3	65	V
	EN	–0.3	8.4	
	FB	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	BOOT-SW	–0.3	8	V
	SW	–0.6	65	
	SW, 5-ns transient	–7	65	
	SW, 10-ns transient	–2	65	
Operating junction temperature		-40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Rec–65ommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC-Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply input voltage	4.5	60	V
V_O	Output voltage	0.8	58.8	V
I_O	Output current	0	5	A
T_J	Junction temperature	–40	150	°C

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6.4 Thermal Information

THERMAL METRIC[1][2]		TPS54561-Q1 DPR 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	35.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Determination of the power rating at a specific ambient temperature must be at the maximum junction temperature of 150°C. This is the point where distortion starts to increase substantially. See the power dissipation estimate in the *Power Dissipation Estimate* section of this data sheet for more information.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{DD} = 4.5 to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (V_{DD} PIN)						
	Operating input voltage		4.5		60	V
	Internal undervoltage lockout threshold	V_{DD} rising	4.1	4.3	4.48	V
	Internal undervoltage lockout threshold hysteresis			325		mV
	Shutdown supply current	$V_{(EN)}$ = 0 V, T_A = 25°C, 4.5 V ≤ V_{DD} ≤ 60 V		2.25	4.5	µA
	Operating: nonswitching supply current	$V_{(FB)}$ = 0.9 V, T_A = 25°C		152	200	
ENABLE AND UVLO (EN PIN)						
$V_{(EN)th}$	Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
	Input current	Enable threshold + 50 mV		–4.6		µA
		Enable threshold – 50 mV	–0.58	–1.2	-1.8	
$I_{(HYS)}$	Hysteresis current		–2.2	–3.4	-4.5	µA
VOLTAGE REFERENCE						
V_{ref}	Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET						
	On-resistance	V_{DD} = 12 V, $V_{(BOOT-SW)}$ = 6 V		87	185	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
$g_{m(ea)}$	Error-amplifier transconductance	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		350		µS
	Error-amplifier transconductance (g_m) during soft-start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, $V_{(FB)}$ = 0.4 V		78		µS
$A_{(OL)}$	Error-amplifier open-loop dc gain	$V_{(FB)}$ = 0.8 V		10 000		V/V
	Minimum unity-gain bandwidth			2500		kHz
	Error-amplifier source and sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
$g_{m(ps)}$	COMP to SW current transconductance			17		S
CURRENT LIMIT						
	Current limit threshold	All V_{DD} and temperatures, open loop[1]	6.3	7.5	8.8	A
		All temperatures, V_{DD} = 12 V, open loop[1]	6.3	7.5	8.3	
		V_{DD} = 12 V, T_A = 25°C, open loop[1]	7.1	7.5	7.9	
THERMAL SHUTDOWN						
	Thermal shutdown			176		°C
	Thermal shutdown hysteresis			12		°C

(1) Measure open-loop current limit directly at the SW pin. The current is independent of the inductor value and slope compensation.

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{DD} = 4.5 to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL CLOCK (RT/CLK PIN)						
	RT/CLK high threshold			1.55	2	V
	RT/CLK low threshold		0.5	1.2		V
SOFT-START AND TRACKING (SS/TR PIN)						
$I_{(SS)}$	Charge current	$V_{(SS/TR)}$ = 0.4 V		1.7		µA
	SS/TR-to-FB matching	$V_{(SS/TR)}$ = 0.4 V		42		mV
	SS/TR-to-reference crossover	98% of nominal FB voltage		1.16		V
	SS/TR discharge current (overload)	$V_{(FB)}$ = 0 V, $V_{(SS/TR)}$ = 0.4 V		354		µA
	SS/TR discharge voltage	$V_{(FB)}$ = 0 V		54		mV
POWER GOOD (PWRGD PIN)						
	FB threshold for PWRGD low	FB falling		91%		
	FB threshold for PWRGD high	FB rising		93%		
	FB threshold for PWRGD low	FB rising		108%		
	FB threshold for PWRGD high	FB falling		106%		
	Hysteresis	FB falling		2%		
	Output-high leakage	$V_{(PWRGD)}$ = 5.5 V, T_A = 25°C		10		nA
	On-resistance	$I_{(PWRGD)}$ = 3 mA, $V_{(FB)}$ < 0.79 V		45		Ω
	Minimum input voltage for defined output voltage	$V_{(PWRGD)}$ < 0.5 V, $I_{(PWRGD)}$ = 100 µA		0.9	2	V

6.6 Timing Requirements

		MIN	TYP	MAX	UNIT
RT/CLK					
	Minimum CLK input pulse duration		15		ns

6.7 Switching Characteristics

T_J = –40°C to 150°C, V_{DD} = 4.5 V to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND UVLO (EN PIN)						
	Enable to COMP active	V_{DD} = 12 V, T_A = 25°C		540		µs
CURRENT-LIMIT						
$t_{d(CL)}$	Current limit threshold delay			60		ns
SW						
$t_{(ON)}$	Minimum controllable on-time	V_{DD} = 23.7 V, V_O = 5 V, I_O = 3.5 A, $R_{(RT)}$ = 39.6 kΩ, T_A = 25°C		100		ns
RT/CLK						
	Switching frequency range using RT mode		100		2500	kHz
$f_{(SW)}$	Switching frequency	$R_{(RT)}$ = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with an RT resistor ($R_{(RT)}$) in series		55		ns
	PLL lock-in time	Measured at 500 kHz		78		µs

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6.8 Typical Characteristics

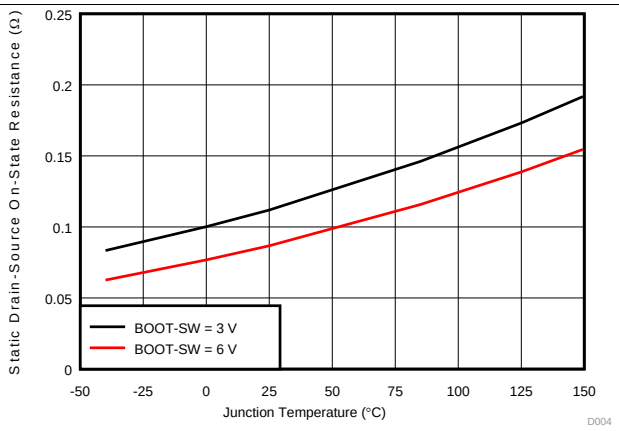
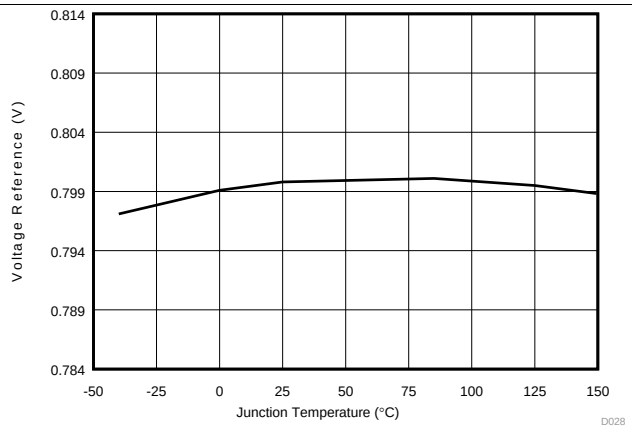
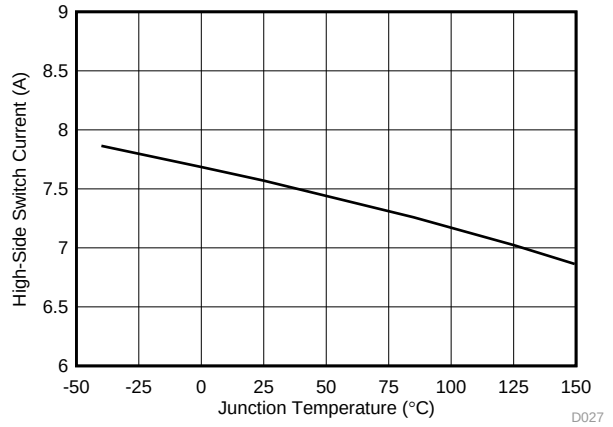


Figure 1. On-Resistance vs Junction Temperature



V_{DD} = 12 V

Figure 2. Voltage Reference vs Junction Temperature



V_{DD} = 12 V

Figure 3. Switch-Current Limit vs Junction Temperature

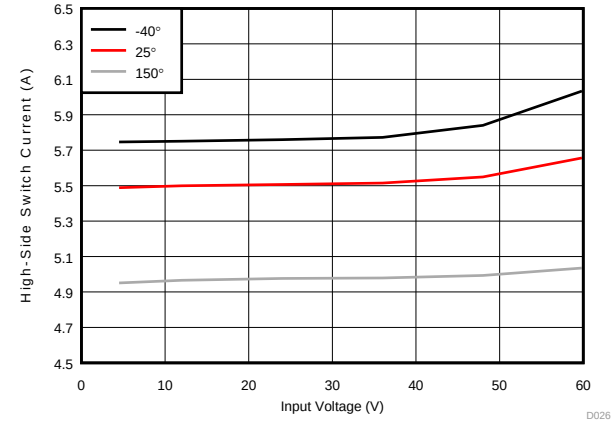
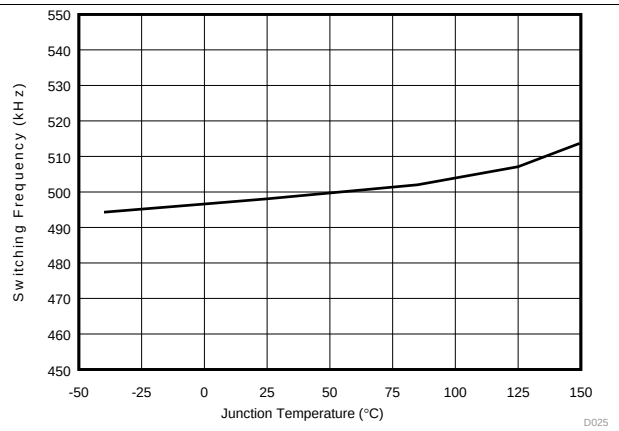


Figure 4. Switch-Current Limit vs Input Voltage



$R_{(RT)}$ = 200 kΩ V_{DD} = 12 V

Figure 5. Switching Frequency vs Junction Temperature

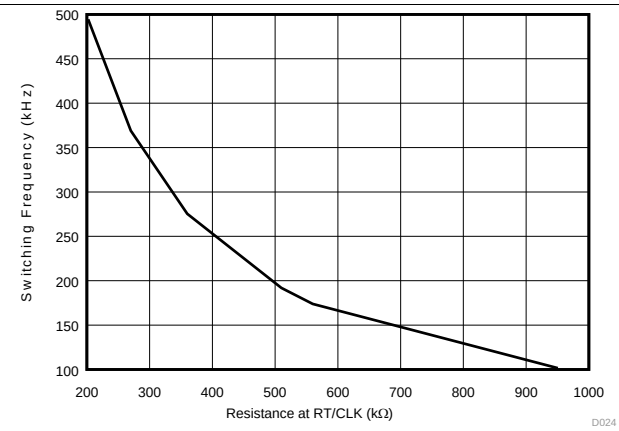


Figure 6. Switching Frequency vs RT/CLK Resistance, Low-Frequency Range

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Typical Characteristics (continued)

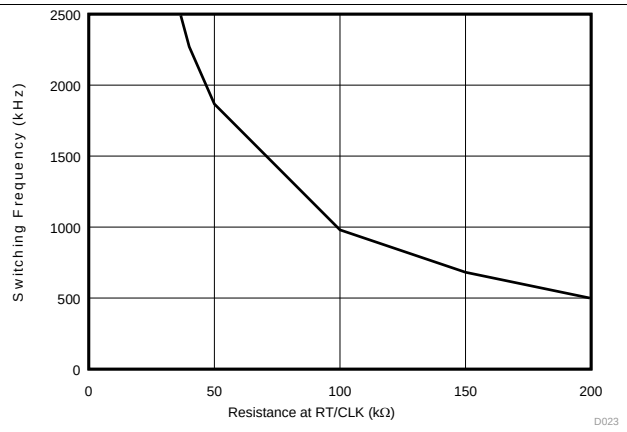
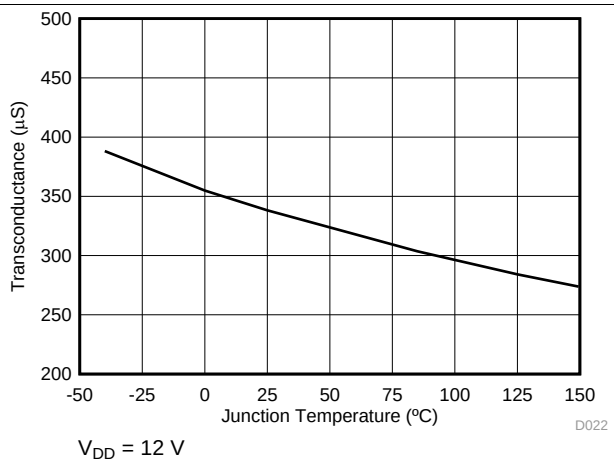
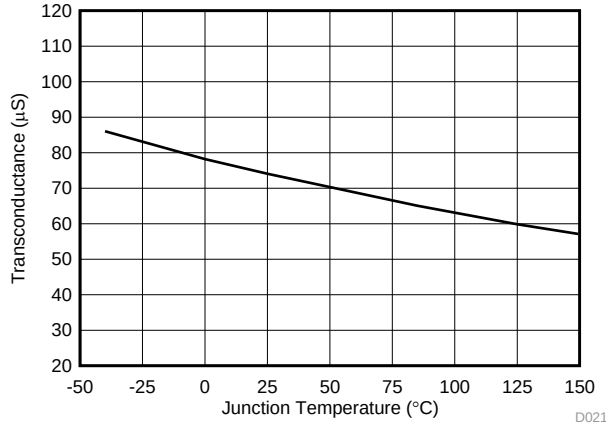


Figure 7. Switching Frequency vs RT/CLK Resistance, High-Frequency Range



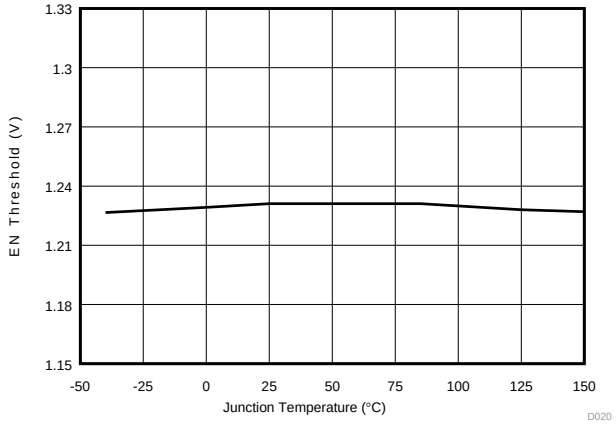
V_{DD} = 12 V

Figure 8. EA Transconductance vs Junction Temperature



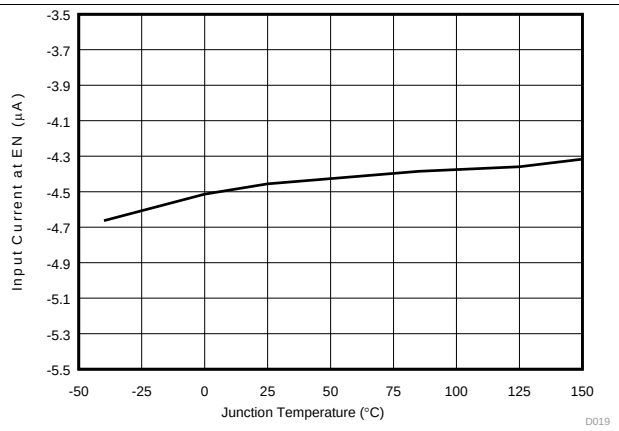
V_{DD} = 12 V

Figure 9. EA Transconductance During Soft-Start vs Junction Temperature



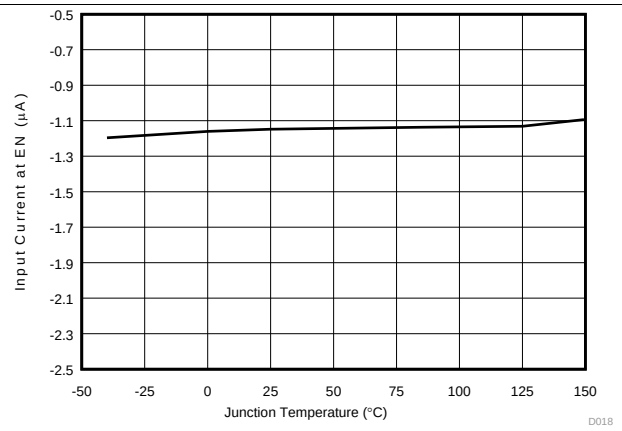
V_{DD} = 12 V

Figure 10. EN Pin Threshold Voltage vs Junction Temperature



V_{DD} = 12 V $V_{(EN)}$ = Threshold + 50 mV

Figure 11. EN Pin Current vs Junction Temperature

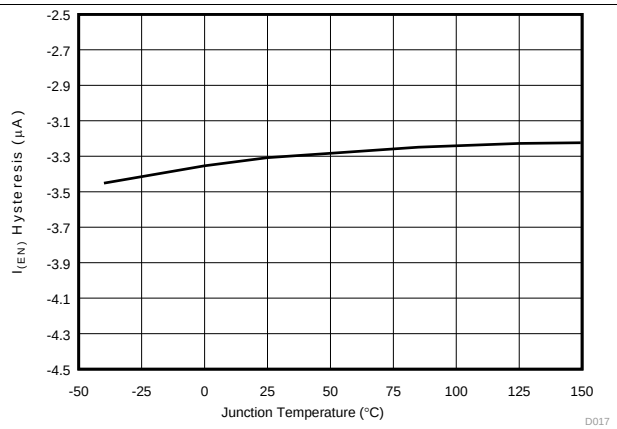


V_{DD} = 12 V $V_{(EN)}$ = Threshold – 50 mV

Figure 12. EN Pin Current vs Junction Temperature

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Typical Characteristics (continued)



V_{DD} = 12 V

Figure 13. EN Pin Current Hysteresis vs Junction Temperature

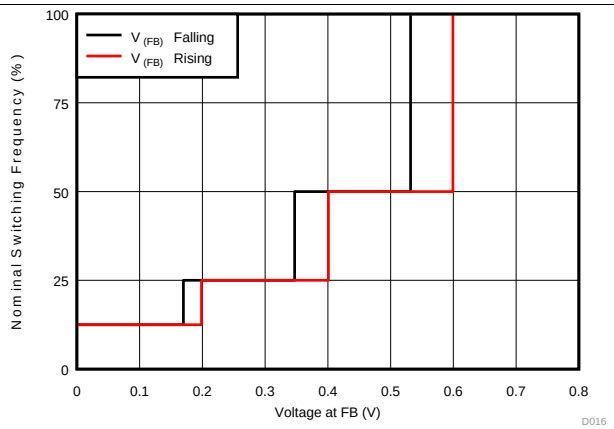
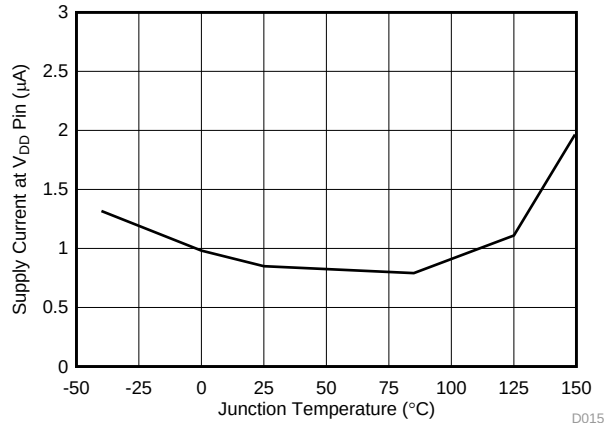
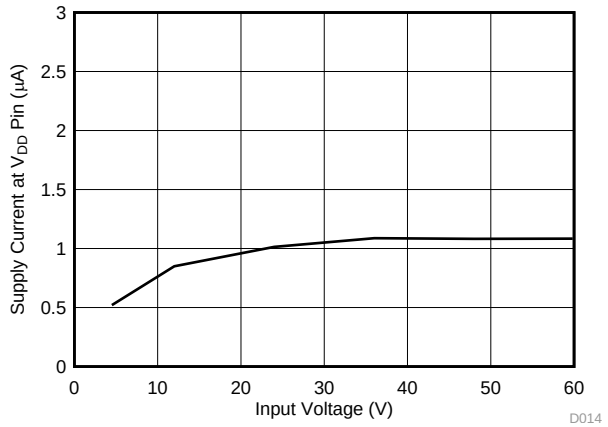


Figure 14. Switching Frequency vs FB



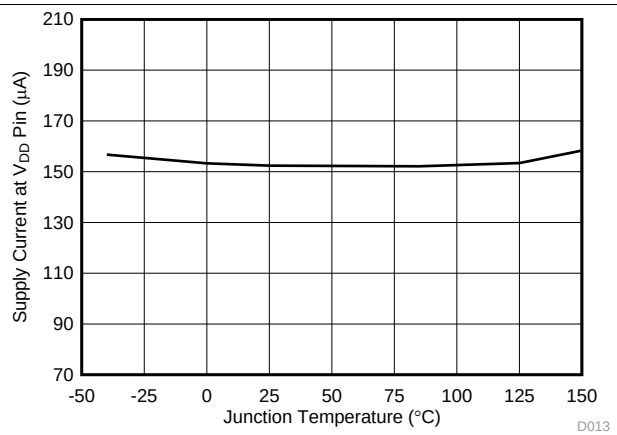
V_{DD} = 12 V

Figure 15. Shutdown Supply Current vs Junction Temperature



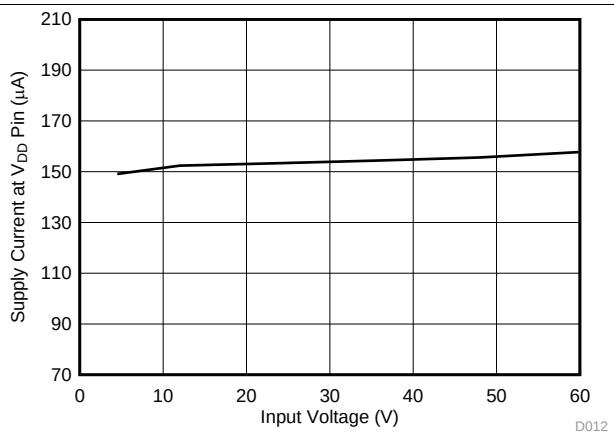
T_J = 25ºC

Figure 16. Shutdown Supply Current vs Input Voltage



V_{DD} = 12 V

Figure 17. $I_{(VDD)}$ Supply Current vs Junction Temperature



T_J = 25ºC

Figure 18. $I_{(VDD)}$ Supply Current vs Input Voltage

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Typical Characteristics (continued)

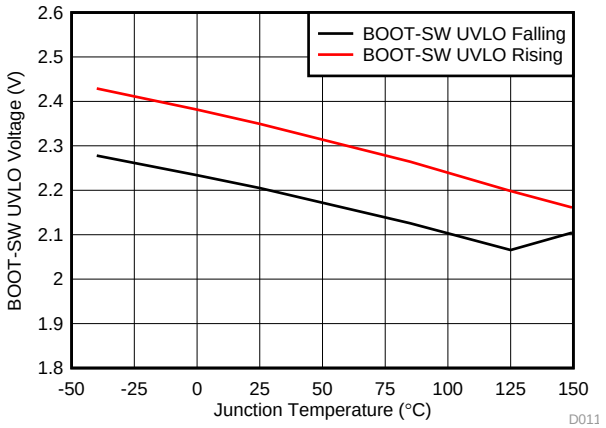


Figure 19. BOOT-SW UVLO vs Junction Temperature

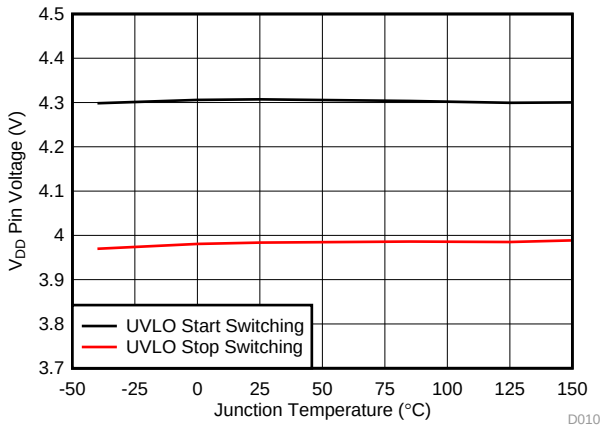
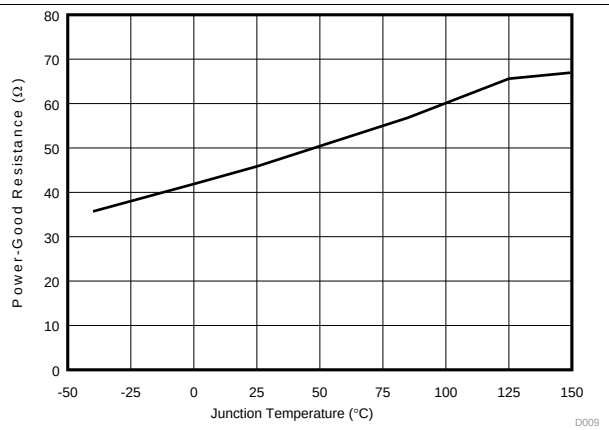
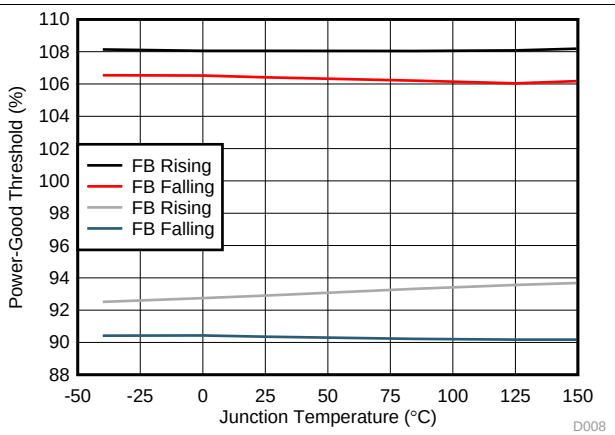


Figure 20. Input Voltage UVLO vs Junction Temperature



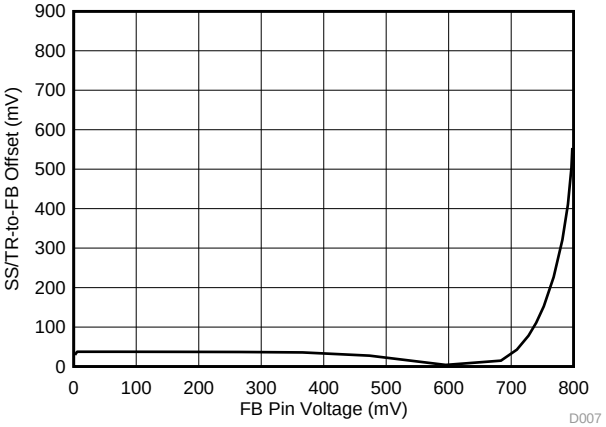
V_{DD} = 12 V

Figure 21. PWRGD On-Resistance vs Junction Temperature



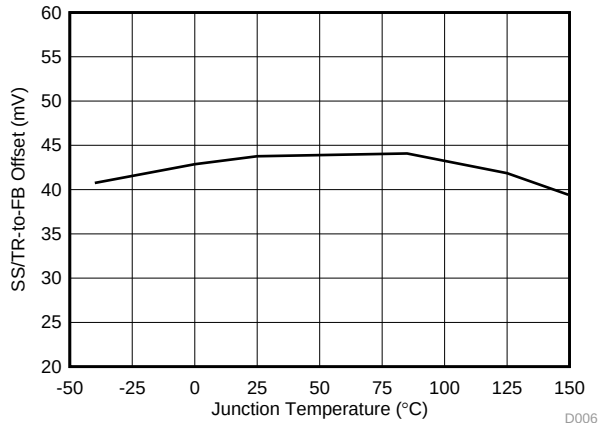
V_{DD} = 12 V

Figure 22. PWRGD Threshold vs Junction Temperature



V_{DD} = 12 V T_J = 25ºC

Figure 23. SS/TR to FB Offset vs FB



V_{DD} = 12 V $V_{(FB)}$ = 0.4 V

Figure 24. SS/TR to FB Offset vs Temperature

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Typical Characteristics (continued)

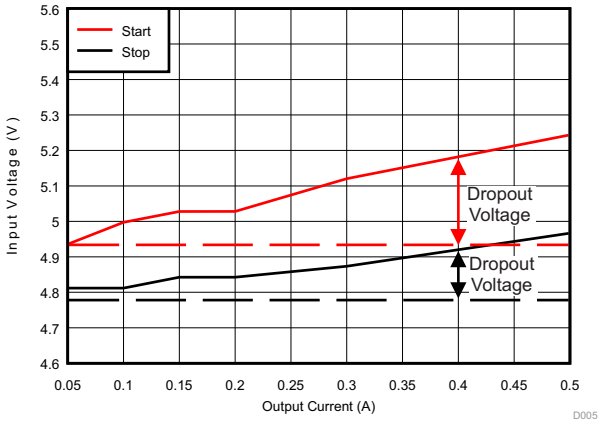


Figure 25. 5-V Start and Stop Voltage (see *Low-Dropout Operation and Bootstrap Voltage (BOOT)*)

7 Detailed Description

7.1 Overview

The TPS54561-Q1 device is a 60-V, 5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The device implements constant-frequency current-mode control, which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The use of a resistor connected to ground from the RT/CLK pin adjusts the switching frequency. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that synchronizes the power-switch turnon to the falling edge of an external clock signal.

The TPS54561-Q1 device has a default input start-up voltage of approximately 4.3 V. The EN pin adjusts the input-voltage undervoltage-lockout (UVLO) threshold with two external resistors. An internal pullup current source enables operation when the EN pin is floating. The operating current is 152 µA under no-load conditions when not switching. With the device disabled, the supply current is 2 µA.

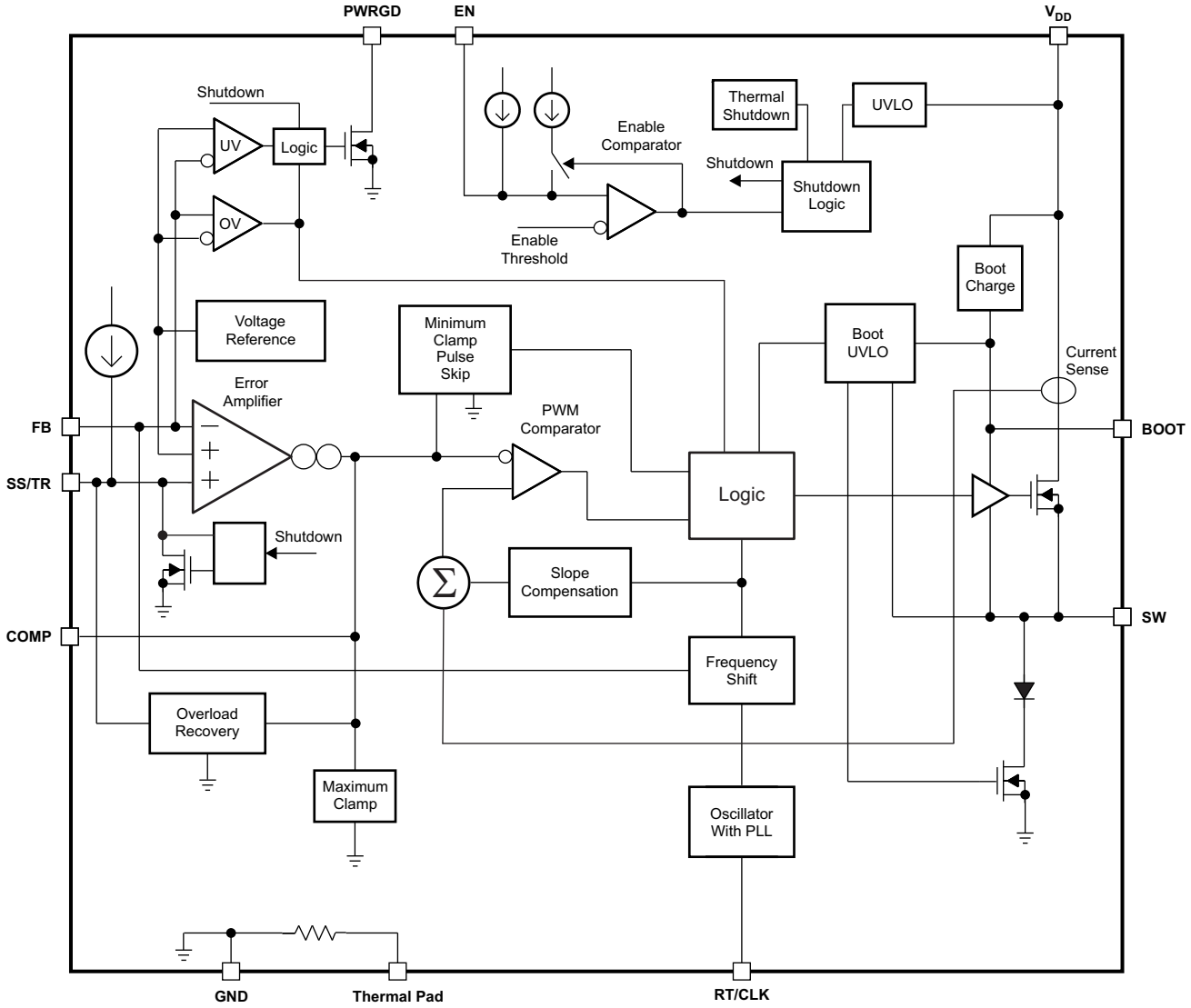
The integrated 87-mΩ high-side MOSFET supports high-efficiency power supply designs capable of delivering 5 A of continuous current to a load. A bootstrap capacitor connected from the BOOT pin to the SW pin supplies the gate-drive bias voltage for the integrated high-side MOSFET. The TPS54561-Q1 device reduces the external component count by integrating the bootstrap recharge diode. A BOOT UVLO circuit monitors the BOOT pin capacitor voltage, and turns off the high-side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54561-Q1 to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is 0.8 V, which equals the internal feedback reference.

An overvoltage protection (OVP) comparator minimizes output overvoltage transients. On activation of the OVP comparator, the high-side MOSFET turns off and remains off until the output voltage is less than 106% of the desired output voltage.

Using the SS/TR (soft-start and tracking) pin minimizes inrush currents or provides power supply sequencing during power-up. Couple a small-value capacitor from the SS/TR pin to the GND pin to adjust the soft-start time. Couple a resistor divider from SS/TR pin to GND pin for critical power-supply sequencing requirements. The device discharges the SS/TR pin before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition. When the overload condition goes away, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up or overcurrent fault conditions to help maintain control of the inductor current.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The TPS54561-Q1 device uses fixed-frequency, peak-current-mode control with adjustable switching frequency. An error amplifier compares the output voltage to an internal voltage reference through an external resistor divider connected to the FB pin. An internal oscillator initiates the turnon of the high-side MOSFET. The error amplifier output at the COMP pin controls the high-side MOSFET current. When the high-side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. Implementation of the pulse-skipping Eco-mode control scheme is through a minimum voltage clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS54561-Q1 adds a compensating ramp to the MOSFET switch-current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The slope compensation does not affect the peak current limit of the high-side switch, which remains constant over the full duty cycle range.

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Feature Description (continued)

7.3.3 Pulse-Skipping Eco-mode Control Scheme

The TPS54561-Q1 device operates in a pulse-skipping Eco-mode control scheme at light load currents to improve efficiency by reducing switching and gate-drive losses. If the output voltage is within regulation and the peak switch current of any switching cycle is below the pulse-skipping current threshold, the device enters pulse-skipping mode. The pulse-skipping current threshold is the peak switch-current level corresponding to a nominal COMP voltage of 600 mV.

When in pulse-skipping mode, the TPS54561-Q1 device clamps the COMP pin voltage to 600 mV and inhibits the high-side MOSFET. Because the device is not switching, the output voltage begins to decay. The voltage control loop responds to the falling output voltage by increasing the COMP pin voltage. The high-side MOSFET enables and switching resumes when the error amplifier lifts COMP above the pulse-skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the pulse-skipping threshold, at which time the device again enters pulse-skipping mode. The internal PLL remains operational when in pulse-skipping mode. When operating at light load currents in pulse-skipping mode, the switching transitions occur synchronously with the external clock signal.

During pulse-skipping operation, the TPS54561-Q1 device senses and controls the peak switch current, not the average load current. Therefore, the load current at which the device enters pulse-skipping mode depends on the output inductor value. The circuit in Figure 46 enters pulse-skipping mode at about 25.3 mA output current. As the load current approaches zero, the device enters the pulse-skipping mode. During the time period when there is no switching the input current falls to the 152-µA quiescent current.

7.3.4 Low-Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54561-Q1 device provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor recharges when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 µF. For stable performance over temperature and voltage, TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher.

When operating with a low voltage difference from input to output, the high-side MOSFET of the TPS54561-Q1 operates at 100% duty cycle as long as the BOOT-to-SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET turns off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low-side MOSFET at high output voltages, the device disables this small low-side MOSFET at 24-V output and re-enables it when the output reaches 21.5 V.

Because the gate-drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET turns off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The main influences on the effective duty cycle of the converter during dropout are the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage, and the printed-circuit-board (PCB) resistance.

Figure 25 shows the start and stop voltages for a typical 5-V output application, and plots the input voltage versus load current. The definition of start voltage is the input voltage required to regulate the output within 1% of nominal voltage. The definition of stop voltage is the input voltage at which the output drops by 5% or where switching stops.

During high-duty-cycle (low dropout) conditions, inductor current ripple increases while the BOOT capacitor recharges, resulting in an increase in output-voltage ripple. Increased ripple occurs when the off-time required to recharge the BOOT capacitor is longer than the high-side off-time associated with cycle-by-cycle PWM control.

At heavy loads, increase the minimum input voltage to ensure a monotonic start-up. For this condition, use Equation 1 to calculate the maximum output voltage for a given minimum input voltage.

$$V_O max = Dmax \times (V_I min - I_O max \times r_{DS(on)} + V_{(d)}) - V_{(d)} + I_O max \times R_{(DC)}$$

where

- Dmax = 0.9
- $V_{(d)}$ = Forward drop of the catch diode
- $R_{(DC)}$ = DC resistance of output inductor

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Feature Description (continued)

- $r_{DS(on)} = 1 / (–0.3 \times V_{(BOOT_SW)}^2 + 3.577 \times V_{(BOOT_SW)} – 4.246)$
- $V_{(BOOT_SW)} = V_{(BOOT)} + V_{(d)}$
- $V_{(BOOT)} = (1.41 \times V_I min – 0.554 – V_{(d)} \times f_{(SW)} – 1.847 \times 10^3 \times I_{(BOOT_SW)}) / (1.41 + f_{(SW)})$
- $I_{(BOOT_SW)} = 100 \times 10^{-6}$ A
- $f_{(SW)}$ = Operating frequency in MHz (1)

7.3.5 Error Amplifier

A transconductance error amplifier controls the TPS54561-Q1 voltage regulation loop. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance ($g_{m(ea)}$) of the error amplifier is 350 µS during normal operation. During soft-start operation, the device reduces the transconductance to 78 µS and references the error amplifier to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor, and capacitor) connect the error-amplifier output COMP pin to the GND pin.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. A resistor divider from the output node to the FB pin sets the output voltage. Divider resistors with a 1% tolerance or better are recommended. Select the low-side resistor, $R_{(LS)}$, for the desired divider current, and use Equation 2 to calculate $R_{(HS)}$. To improve efficiency at light loads, consider using larger-value resistors. However, if the values are too high, the regulator is more susceptible to noise and voltage errors because of the FB input current may become noticeable.

$$R_{(HS)} = R_{(LS)} \times \left(\frac{V_O – 0.8\ V}{0.8\ V} \right) \quad (2)$$

7.3.7 Enable and Adjust Undervoltage Lockout

The V_{DD} pin voltage rising above 4.3 V when the EN pin voltage exceeds the enable threshold of 1.2 V enables the TPS54561-Q1 device. The V_{DD} pin voltage falling below 4 V or the EN pin voltage dropping below 1.2 V disables the TPS54561-Q1 device. The EN pin has an internal pullup current source, $I_{(1)}$, of 1.2 µA that enables operation of the TPS54561-Q1 device when the EN pin floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 26 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, the EN pin sources an additional 3.4 µA of hysteresis current, $I_{(HYS)}$. This additional current facilitates adjustable input voltage UVLO hysteresis. Pulling the EN pin below 1.2 V removes the 3.4-µA $I_{(HYS)}$ current. Use Equation 3 to calculate $R_{(UVLO1)}$ for the desired UVLO hysteresis voltage. Use Equation 4 to calculate $R_{(UVLO2)}$ for the desired V_{DD} start voltage.

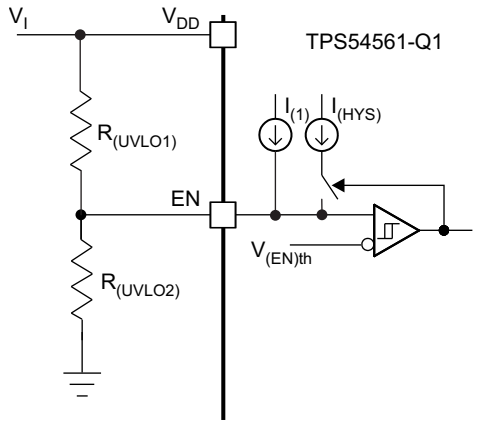
In applications designed to start at relatively low input voltages (for example, from 4.5 V to 9 V) and withstand high input voltages (for example, from 40 V to 60 V), the EN pin may experience a voltage greater than the absolute maximum voltage of 8.4 V during the high-input-voltage condition. To avoid exceeding this voltage when using the EN resistors, a 5.8-V Zener diode that is capable of sinking up to 150 µA internally clamps the EN pin.

$$R_{(UVLO1)} = \left(\frac{V_{(START)} – V_{(STOP)}}{I_{(HYS)}} \right) \quad (3)$$

$$R_{(UVLO2)} = \frac{V_{(EN)th}}{\frac{V_{(START)} – V_{(EN)th}}{R_{(UVLO1)}} + I_{(1)}} \quad (4)$$

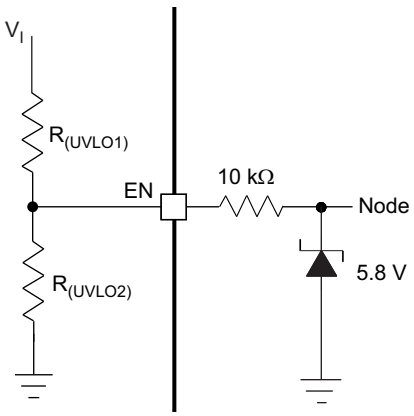
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Feature Description (continued)



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Figure 26. Adjustable Undervoltage Lockout (UVLO)



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Figure 27. Internal Clamp On EN Pin

7.3.8 Soft-Start and Tracking Pin (SS/TR)

The TPS54561-Q1 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft-start time. The TPS54561-Q1 device has an internal pullup current source of 1.7 µA that charges the external soft-start capacitor. Equation 5 shows the calculation for the soft-start time (10% to 90%). The voltage reference (V_{ref}) is 0.8 V and the soft-start current ($I_{(SS)}$) is 1.7 µA. The soft-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$C_{(SS)}\,(nF) = \frac{t_{(SS)}\,(ms) \times I_{(SS)}\,(\mu A)}{V_{ref} \times 0.8} \tag{5}$$

At power up, the TPS54561-Q1 device does not start switching until the voltage in the soft-start pin is less than 54 mV to ensure a proper power up (see Figure 28).

Also, during normal operation, the TPS54561-Q1 stops switching and the SS/TR pin must discharge to 54 mV when one of the following occurs: the V_{DD} pin voltage exceeds the UVLO threshold, the EN pin drops below 1.2 V, or a thermal shutdown event occurs.

The FB voltage follows the SS/TR pin voltage with a 42-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 2.7 V typical, as shown in Figure 28.

Feature Description (continued)

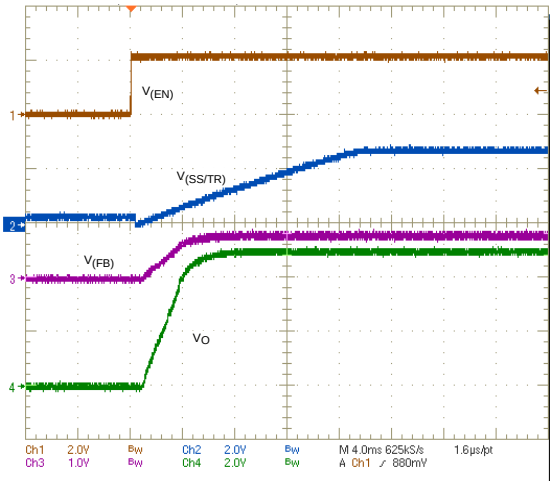
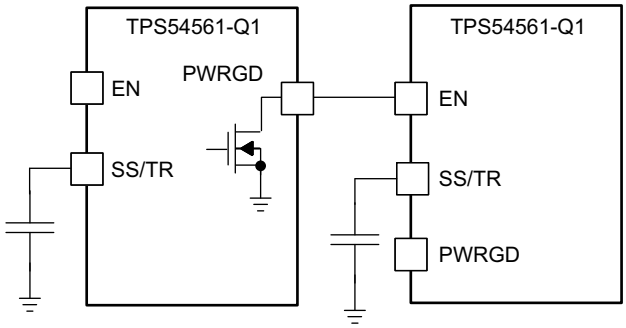


Figure 28. Operation of SS/TR Pin When Starting

7.3.9 Sequencing

A designer can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implementation of the sequential method can be by using an open-drain output of the power-on-reset pin of another device. Figure 29 illustrates the sequential method using two TPS54561-Q1 devices. Connecting the power-good signal of the first TPS54561-Q1 device to the EN pin on the second TPS54561-Q1 device enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms start-up delay. Figure 30 shows the results of Figure 29.



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Figure 29. Schematic for Sequential Start-Up Sequence

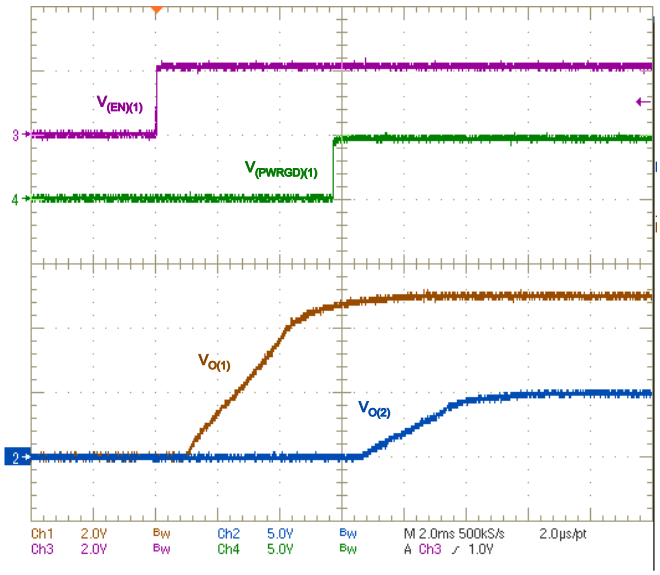
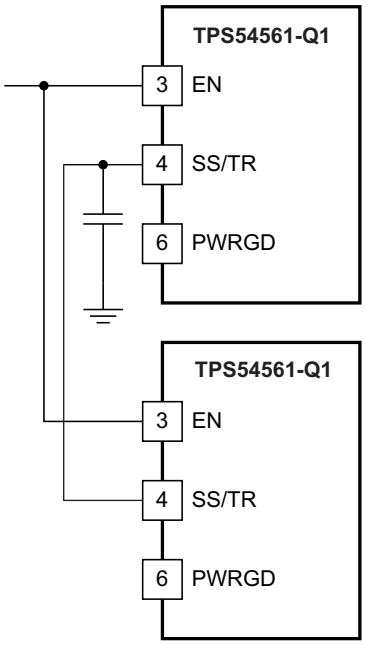


Figure 30. Sequential Start-Up Using EN and PWRGD

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Feature Description (continued)



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Figure 31. Schematic for Ratiometric Start-Up Sequence

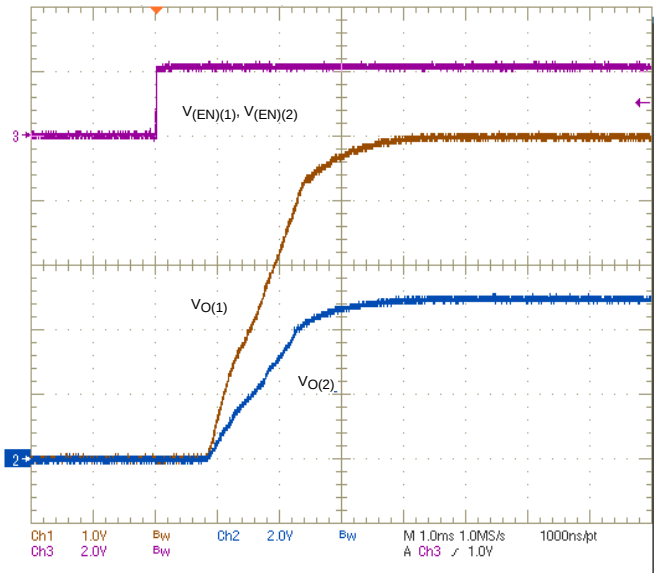
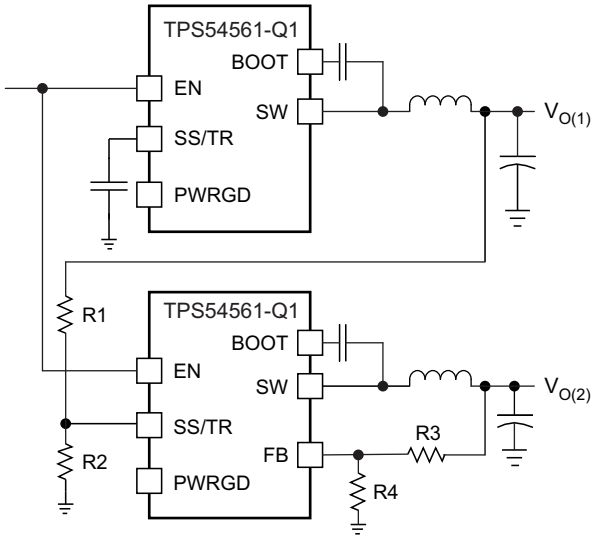


Figure 32. Ratiometric Start-Up Using Coupled SS/TR Pins

Figure 31 shows a method for a ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start capacitor by using Equation 5, double the pullup current source ($I_{(SS)}$). Figure 32 shows the results of Figure 31.



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Figure 33. Schematic for Ratiometric and Simultaneous Start-Up Sequence

One can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in Figure 33 to the output of a power supply that must be tracked, or to another voltage reference source. Using Equation 7 and Equation 8, one can calculate values for the tracking resistors to initiate $V_{O(2)}$ slightly before, after, or at the same time as $V_{O(1)}$. Equation 6 is the voltage difference between $V_{O(1)}$ and $V_{O(2)}$ at 95% of nominal output regulation.

Feature Description (continued)

The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR-to-FB offset ($V_{(SSoffset)}$) in the soft-start circuit and the offset created by the pullup current source ($I_{(SS)}$) and tracking resistors, the equations include $V_{(SSoffset)}$ and $I_{(SS)}$ as variables.

To design a ratiometric start-up in which the $V_{O(2)}$ voltage is slightly greater than the $V_{O(1)}$ voltage when $V_{O(2)}$ reaches regulation, use a negative number in Equation 6 through Equation 8 for ΔV. Equation 6 results in a positive number for applications in which $V_{O(2)}$ is slightly lower than $V_{O(1)}$ when $V_{O(2)}$ reaches its regulation.

Because of the requirement for pulling the SS/TR pin below 54 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors ensures that the device restarts after a fault. Make sure the calculated R1 value from Equation 7 is greater than the value calculated in Equation 9 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, $V_{(SSoffset)}$ becomes larger as the soft-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.5 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$\Delta V = V_{O(1)} - V_{O(2)} \tag{6}$$

at 95% of nominal output regulation.

$$R1 = V_{O(1)} - \frac{V_{O(2)} + \Delta V}{V_{ref}} \times \frac{V_{(SSoffset)}}{I_{(SS)}} \tag{7}$$

$$R2 = \frac{V_{ref} \times R1}{V_{O(2)} + \Delta V - V_{ref}} \tag{8}$$

$$R1 > 2800 \times V_{O(1)} - 180 \times \Delta V \tag{9}$$

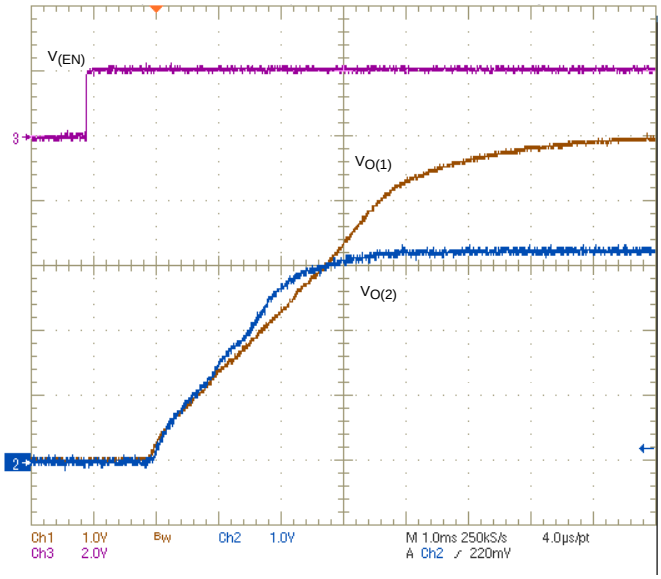


Figure 34. Ratiometric Start-Up With Tracking Resistors – $V_{O(2)}$ Before $V_{O(1)}$

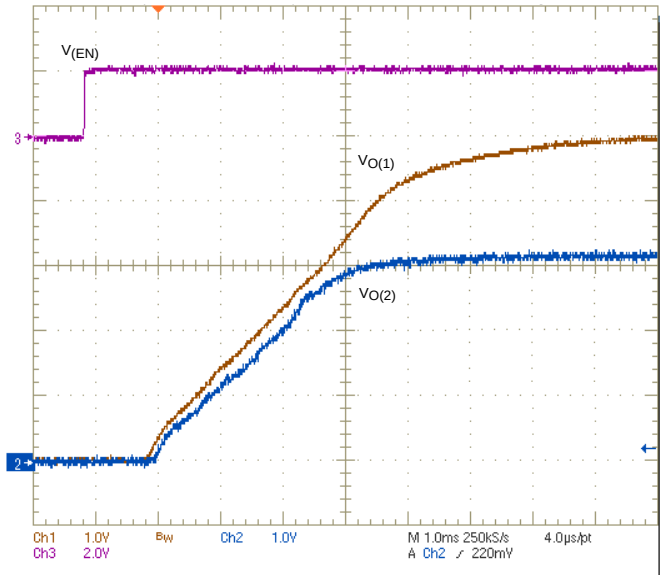


Figure 35. Ratiometric Start-Up With Tracking Resistors – $V_{O(2)}$ After $V_{O(1)}$

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Feature Description (continued)

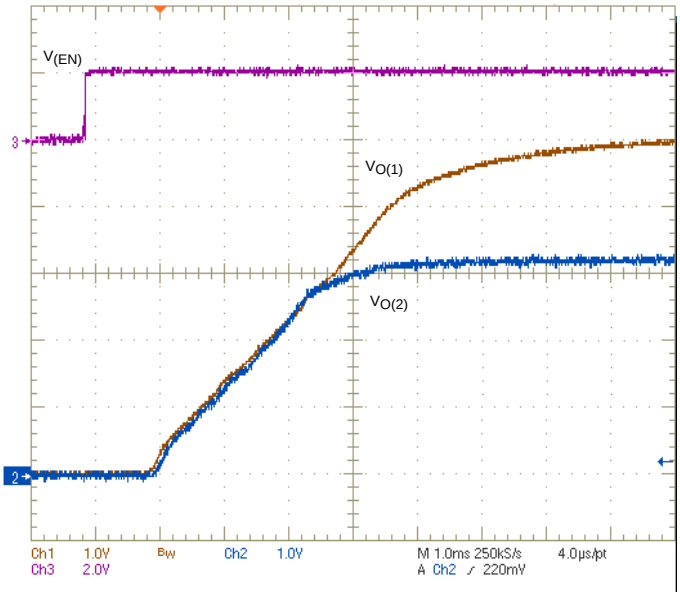


Figure 36. Simultaneous Start-Up With Tracking Resistors

7.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54561-Q1 device is adjustable over a wide range, from 100 kHz to 2500 kHz, by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 10 or Equation 11 or the curves in Figure 6 and Figure 7. To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the conversion efficiency, maximum input voltage, and minimum controllable on-time. The minimum controllable on-time is typically 100 ns, which limits the maximum operating frequency in applications with high input-to-output step-down ratios. The frequency foldback circuit also limits the maximum switching frequency. The next section talks about the maximum switching frequency in detail.

$$R_T\ (k\Omega) = \frac{101756}{f\text{sw}\ (kHz)^{1.008}} \tag{10}$$

$$f\text{sw}\ (kHz) = \frac{92417}{RT\ (k\Omega)^{0.991}} \tag{11}$$

7.3.11 Accurate Current-Limit Operation and Maximum Switching Frequency

The TPS54561-Q1 device implements peak-current-mode control, in which the COMP pin voltage controls the peak current of the high-side MOSFET. A signal proportional to the high-side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The device clamps the error-amplifier output internally at a level which sets the switch-current limit. The TPS54561-Q1 device provides an accurate current-limit threshold with a typical current-limit delay of 60 ns. With smaller inductor values, the delay results in a higher peak inductor current. Figure 37 shows the relationship between the inductor value and the peak inductor current.

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Feature Description (continued)

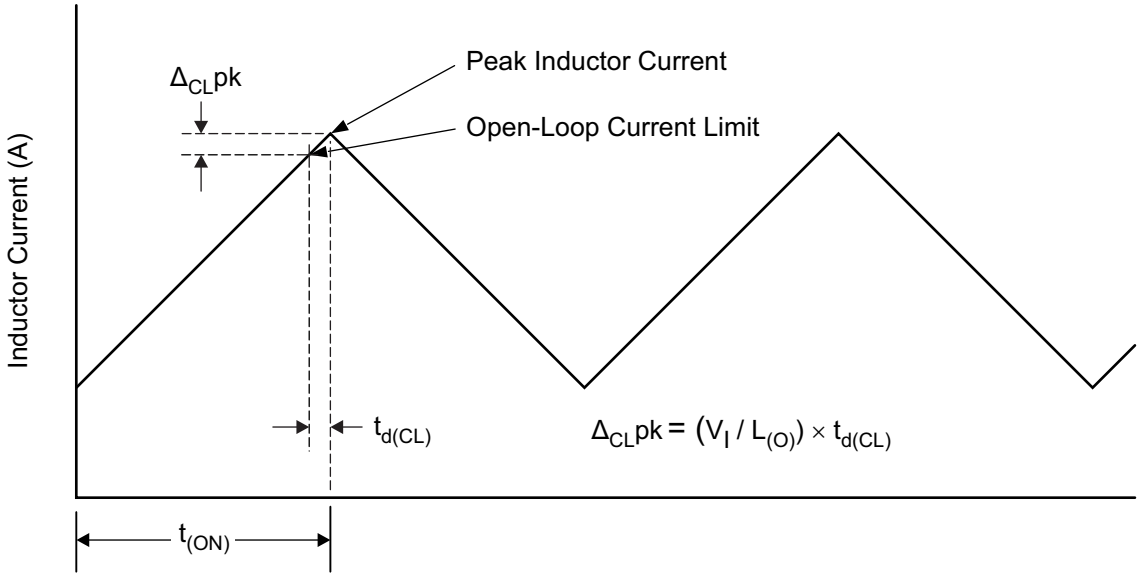


Figure 37. Current Limit Delay

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54561-Q1 device implements frequency foldback. The divisor of the oscillator frequency changes from 1 to 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54561-Q1 device uses digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current may exceed the peak current limit because of the high input voltage and the minimum controllable on-time. When the shorted load forces the output voltage low, the inductor current decreases slowly during the switch off-time. The frequency foldback effectively increases the off-time by increasing the period of the switching cycle, providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which frequency foldback protection can still control the inductor current. Equation 12 calculates the maximum switching frequency at which the inductor current remains under control with V_O forced to $V_{O(SC)}$. The selected operating frequency should not exceed the calculated value.

Equation 13 calculates the maximum switching frequency limitation set by the minimum controllable on-time and the input-to-output step-down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output at maximum input voltage.

$$f_{(SW_shift)} = \frac{f_{(DIV)}}{t_{(ON)}} \times \left(\frac{I_{(CL)} \times R_{(dc)} + V_{O(SC)} + V_{(d)}}{V_I - I_{(CL)} \times r_{DS(on)} + V_{(d)}} \right) \quad (12)$$

$$f_{(SW_skip)}\,max = \frac{1}{t_{(ON)}} \times \left(\frac{I_O \times R_{(dc)} + V_O + V_{(d)}}{V_I - I_O \times r_{DS(on)} + V_{(d)}} \right) \quad (13)$$

where

- $f_{(DIV)}$ is the frequency divisor, which equals (1, 2, 4, or 8)
- $t_{(ON)}$ is the minimum controllable on-time
- $I_{(CL)}$ is the switch current limit
- $R_{(dc)}$ is the inductor resistance
- $V_{O(SC)}$ is the output voltage during output short
- $V_{(d)}$ is the forward voltage drop of the catch diode
- V_I is the maximum input voltage
- $r_{DS(on)}$ is the high-side MOSFET on-resistance

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Feature Description (continued)

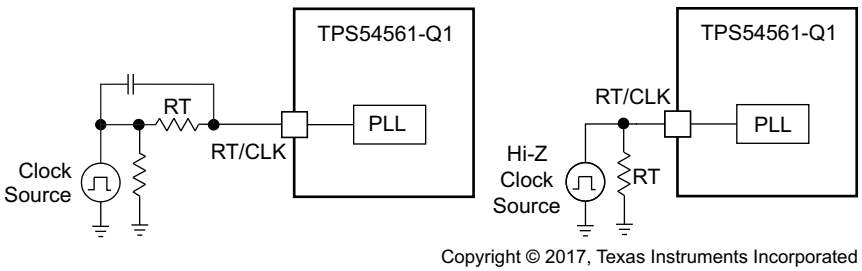
- I_O is the output current
- V_O is the output voltage

7.3.12 Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature, connect a square wave to the RT/CLK pin through either circuit network shown in Figure 38. The square wave applied to the RT/CLK pin must switch lower than 0.5 V, and higher than 2 V, and have a pulse duration greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of SW synchronizes to the falling edge of the RT/CLK pin signal. The design of the external synchronization circuit should be such that the default frequency-set resistor connects from the RT/CLK pin to GND pin when the synchronization signal is off. When using a low-impedance signal source, the connection of the frequency-set resistor is in parallel with an ac-coupling capacitor to a termination resistor (for example, 300 Ω) as shown in Figure 38. The two resistors in series provide the default frequency-setting resistance when the signal source turns off. The sum of the resistance should set the switching frequency close to the external CLK frequency. TI recommends ac-coupling the synchronization signal through a 10-pF ceramic capacitor to the RT/CLK pin.

The first time the input pulls the RT/CLK pin above the PLL high threshold, which has a 2-V maximum value, the TPS54561-Q1 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. Removal of the internal 0.5-V voltage source results, and the RT/CLK pin becomes high-impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor-programmed mode to the PLL mode and locks onto the external clock frequency within 78 µs. During the transition from the PLL mode to the resistor-programmed mode, the switching frequency falls to 150 kHz and then increases or decreases to the resistor-programmed frequency on re-application of the 0.5-V bias voltage to the RT/CLK resistor.

The switching frequency divisor goes from 8 to 4, 2, and 1 as the FB pin voltage ramps from 0 V to 0.8 V. The device implements a digital-frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. Figure 39, Figure 40, and Figure 41 show the device synchronized to an external system clock in continuous-conduction mode (CCM), discontinuous-conduction (DCM) and pulse-skipping mode.



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Figure 38. Synchronizing to a System Clock

Feature Description (continued)

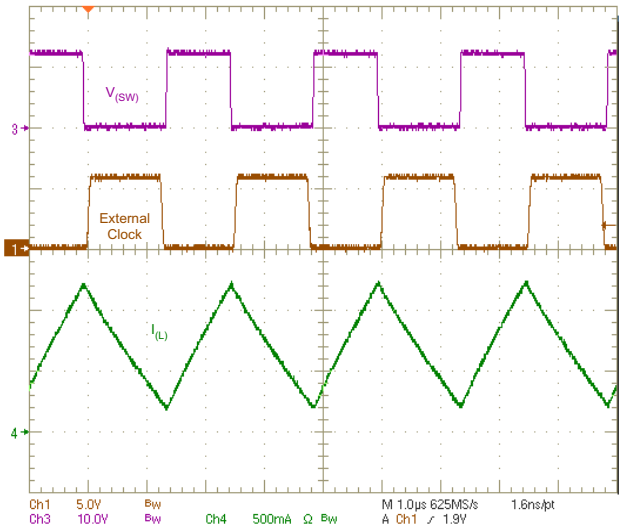


Figure 39. Plot of Synchronizing in CCM

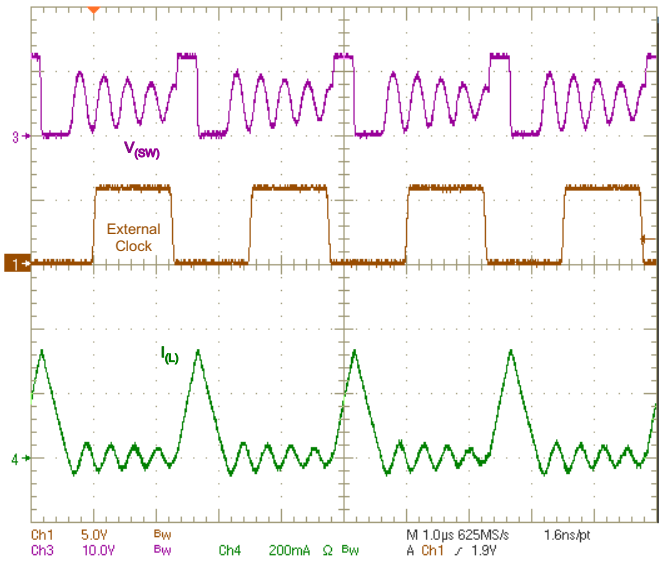


Figure 40. Plot of Synchronizing in DCM

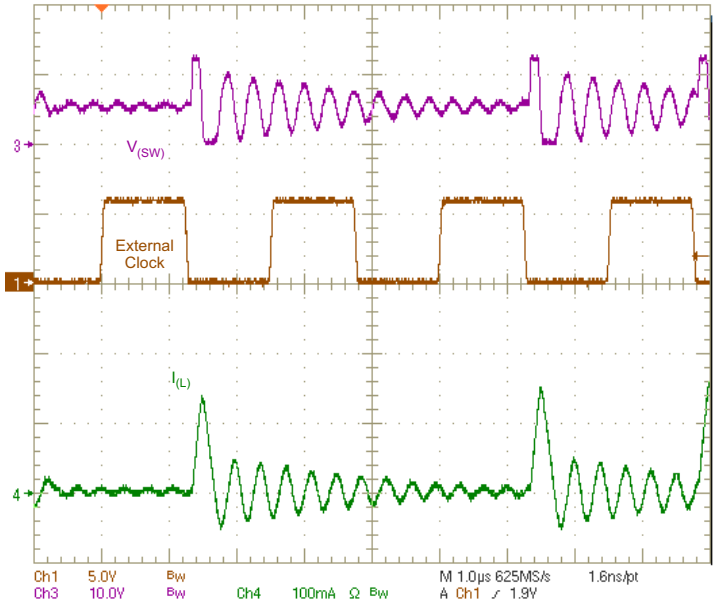


Figure 41. Plot of Synchronizing in Pulse-Skipping Mode

7.3.13 Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. When the FB pin is between 93% and 106% of the internal voltage reference, TPS54561-Q1 device de-asserts the PWRGD pin and this pin floats. TI recommends a pullup resistor of 1 kΩ to a voltage source that is 5.5 V or less. A higher pullup resistance reduces the amount of current drawn from the pullup voltage source when the PWRGD pin is low. A lower pullup resistance reduces the switching noise seen on the PWRGD signal. PWRGD is in a defined state once the V_{DD} pin voltage is greater than 2 V, but with reduced current sinking capability. PWRGD achieves full current-sinking capability as the V_{DD} pin voltage approaches 3 V.

TPS54561-Q1 device pulls the PWRGD pin low when the FB pin voltage is lower than 90% or greater than 108% of the nominal internal reference voltage. Also, the TPS54561-Q1 device pulls the PWRGD pin low after an EN, UVLO, or thermal shutdown fault.

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Feature Description (continued)

7.3.14 Overvoltage Protection

The TPS54561-Q1 incorporates an output overvoltage-protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, on an overload event of the power-supply output, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier increases to a maximum voltage corresponding to the peak current-limit threshold. On removal of the overload condition, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power-supply output voltage can increase faster than the response of the error amplifier output, resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low-value output capacitor by comparing the FB pin voltage to the rising OVP threshold, which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, immediately disabling the high-side MOSFET minimizes output overshoot. When the FB voltage drops below the falling OVP threshold, which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

7.3.15 Thermal Shutdown

The TPS54561-Q1 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high-side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the silicon temperature falls below 164°C, the device reinitiates the power-up sequence controlled by the SS/TR pin.

7.3.16 Small-Signal Model for Loop Response

Figure 42 shows a simplified model for the TPS54561-Q1 control loop, with which the designer can simulate to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a $g_{m(ea)}$ of 350 µS. A user can model the error amplifier using an ideal voltage controlled current source. The resistor, $R_{(OEA)}$, and capacitor, $C_{(OEA)}$, model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting *c/b* provides the small-signal response of the frequency compensation. Plotting *a/b* provides the small-signal response of the overall loop. To evaluate the dynamic loop response, replace the load resistor, $R_{(L)}$, with a current source that has the appropriate load-step amplitude and step rate in a time-domain analysis. This equivalent model is only valid for continuous-conduction-mode (CCM) operation.

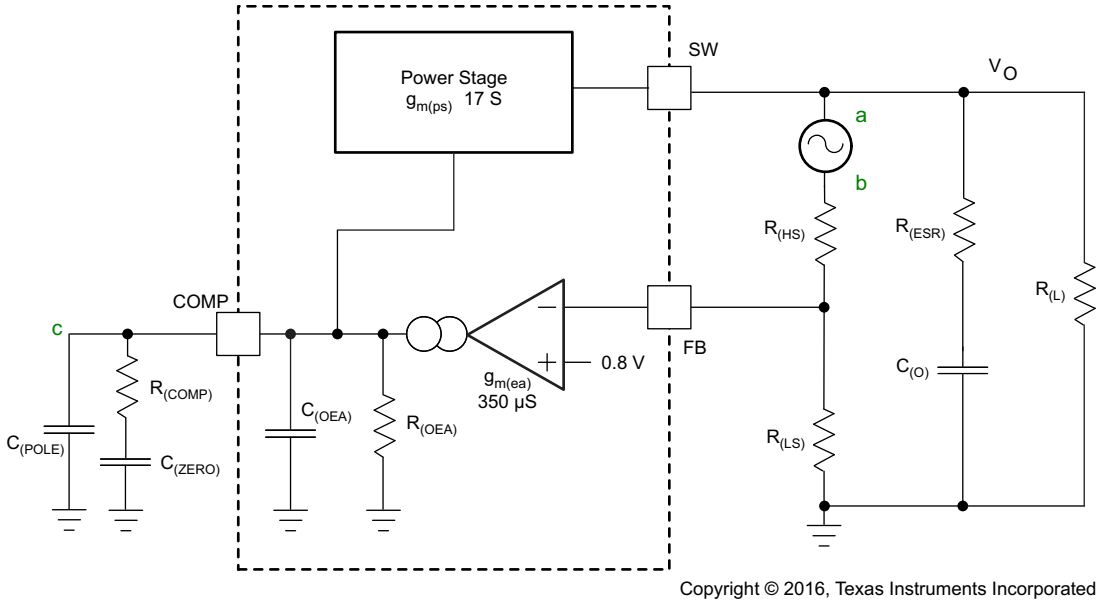


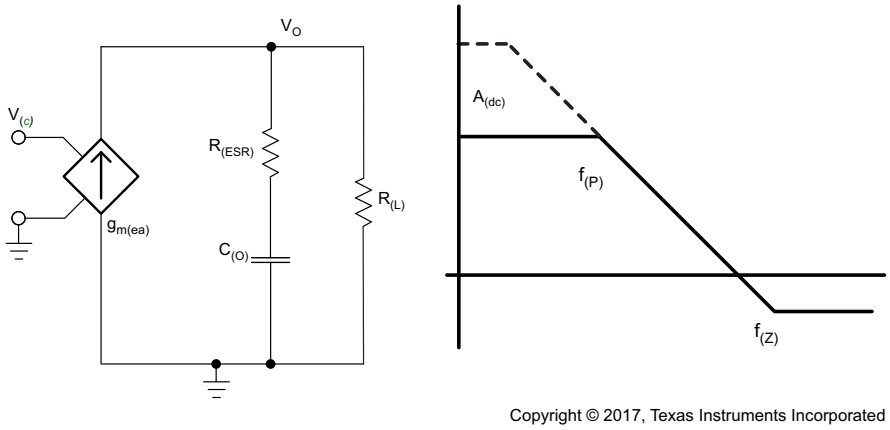
Figure 42. Small-Signal Model for Loop Response

Feature Description (continued)

7.3.17 Simplified Small-Signal Model for Peak-Current-Mode Control

Figure 43 describes a simple small-signal model for use in design of the frequency compensation. A voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor can approximate the TPS54561-Q1 power stage. Equation 14 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 42) is the power stage transconductance, $g_{m(ps)}$. The $g_{m(ps)}$ for the TPS54561-Q1 device is 17 S. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases or decreases, the low-frequency gain decreases or increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The dashed line in the right half of Figure 43 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high-ESR aluminum electrolytic capacitors may reduce the number of frequency compensation components needed to stabilize the overall loop, because the phase margin increases by the ESR zero of the output capacitor (see Equation 17).



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Figure 43. Simplified Small-Signal Model and Frequency Response for Peak-Current-Mode Control

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Feature Description (continued)

$$\frac{V_O}{V_{(C)}} = A_{(dc)} \times \frac{\left(1 + \frac{s}{2\pi \times f_{(Z)}}\right)}{\left(1 + \frac{s}{2\pi \times f_{(P)}}\right)} \quad (14)$$

$$A_{(dc)} = g_{m(ps)} \times R_{(L)} \quad (15)$$

$$f_{(P)} = \frac{1}{C_{(O)} \times R_{(L)} \times 2\pi} \quad (16)$$

$$f_{(Z)} = \frac{1}{C_{(O)} \times R_{(ESR)} \times 2\pi} \quad (17)$$

7.3.18 Small-Signal Model for Frequency Compensation

The TPS54561-Q1 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency-compensation circuits. Figure 44 shows compensation circuits of Type 2A, Type 2B, and Type 1. Implementation of Type 2 circuits is typically in high-bandwidth power-supply designs using low-ESR output capacitors. The Type 1 circuit is good for the power-supply designs using high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 relate the frequency response of the amplifier to the small-signal model in Figure 44. Modeling of the open-loop gain and bandwidth uses $R_{(OEA)}$ and $C_{(OEA)}$, as shown in Figure 44. See the application section for a design example using a Type 2A network with a low-ESR output capacitor.

This data sheet includes Equation 18 through Equation 27 as a reference. An alternative is to use WEBENCH software tools to create a design based on the power-supply requirements.

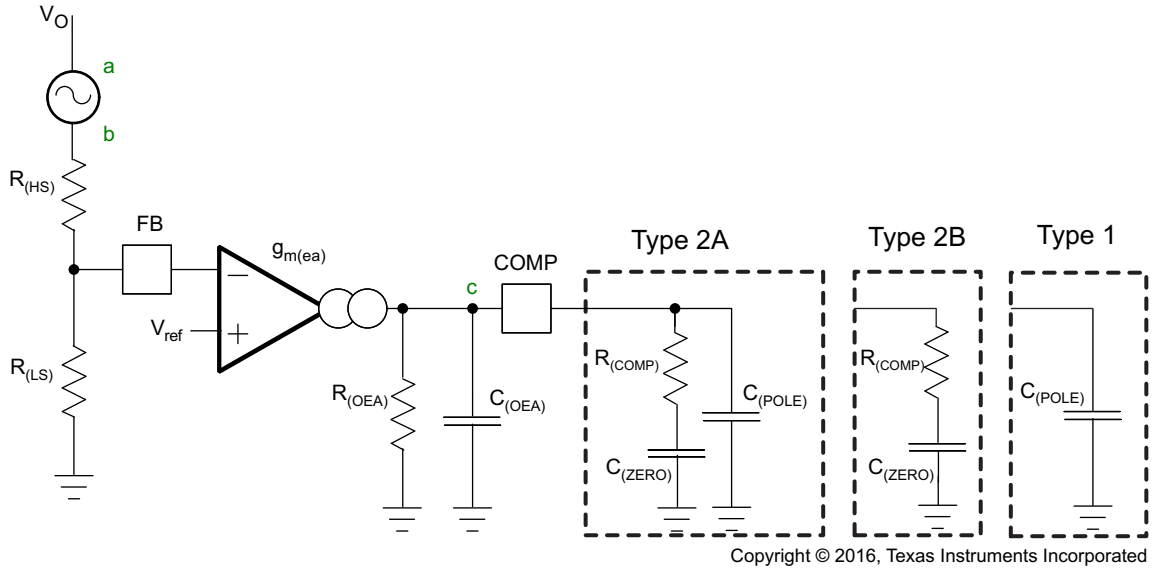


Figure 44. Types of Frequency Compensation

Feature Description (continued)

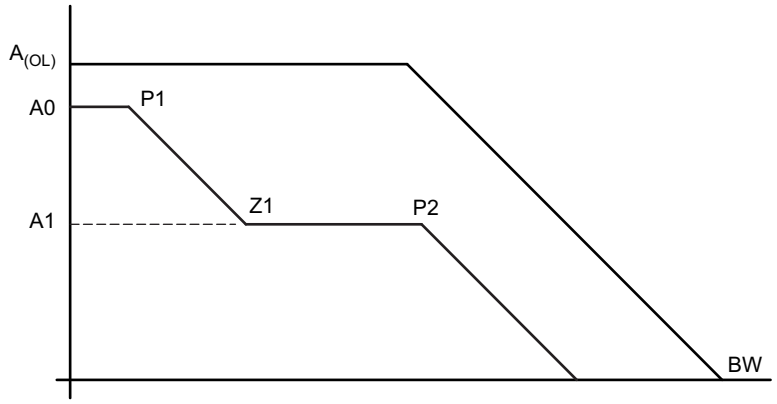


Figure 45. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_{(OEA)} = \frac{A_{(OL)}}{g_{m(ea)}} \quad (18)$$

$$C_{(OEA)} = \frac{g_{m(ea)}}{2\pi \times BW\ (Hz)} \quad (19)$$

$$\frac{V_{(c)}}{V_{(b)}} = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{(Z1)}}\right)}{\left(1 + \frac{s}{2\pi \times f_{(P1)}}\right) \times \left(1 + \frac{s}{2\pi \times f_{(P2)}}\right)} \quad (20)$$

$$A0 = g_{m(ea)} \times R_{(OEA)} \times \frac{R_{(LS)}}{R_{(HS)} + R_{(LS)}} \quad (21)$$

$$A1 = g_{m(ea)} \times R_{(OEA)} \| R_{(COMP)} \times \frac{R_{(LS)}}{R_{(HS)} + R_{(LS)}} \quad (22)$$

$$P1 = \frac{1}{2\pi \times R_{(OEA)} \times C_{(ZERO)}} \quad (23)$$

$$Z1 = \frac{1}{2\pi \times R_{(COMP)} \times C_{(ZERO)}} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R_{(OEA)} \| R_{(COMP)} \times \left(C_{(POLE)} + C_{(OEA)}\right)} \quad \text{Type 2A} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R_{(OEA)} \| R_{(COMP)} \times C_{(OEA)}} \quad \text{Type 2B} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R_{(OEA)} \times \left(C_{(POLE)} + C_{(OEA)}\right)} \quad \text{Type 1} \quad (27)$$

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7.4 Device Functional Modes

7.4.1 Operation With V_I = < 4.5 V (Minimum V_{DD})

TI recommends operating the TPS54561-Q1 device with input voltages above 4.5 V. The typical V_{DD} UVLO threshold is 4.3 V, and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If an external resistor divider pulls the EN pin up to V_{DD} or EN pin is floating, when V_{DD} passes the UVLO threshold the device becomes active. Switching begins, and the soft-start sequence initiates. The TPS54561-Q1 device starts at the soft-start time determined by the external capacitance on the SS/TR pin.

7.4.2 Operation With EN Control

The enable threshold voltage is 1.2 V typical. With EN held below that voltage, the device shuts down and switching stops even if V_{DD} is above its UVLO threshold. The IC quiescent current decreases in this state. After increasing the EN pin voltage above the threshold while V_{DD} is above its UVLO threshold, the device becomes active. Switching resumes and the soft-start sequence begins. The TPS54561-Q1 device starts at the soft-start time determined by the external capacitance at the SS/TR pin.

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8 Application and Implementation

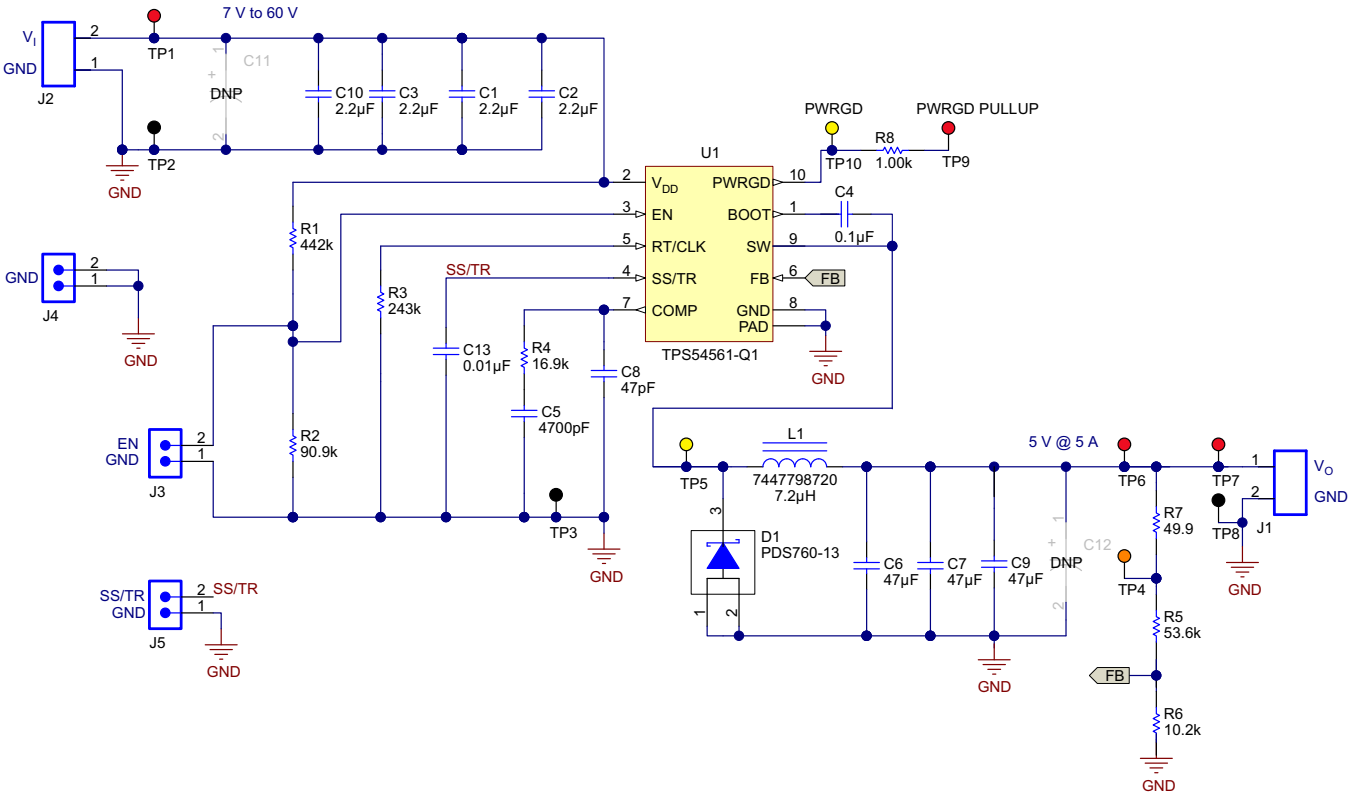
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54561-Q1 device is a 60-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device typically converts a higher dc voltage to a lower dc voltage with a maximum available output current of 5 A. Example applications are: 12-V, 24-V and 48-V industrial, automotive and communication power systems. Use the following design procedure to select component values for the TPS54561-Q1 device. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors. The Excel™ spreadsheet (SLVC452) located on the product page can help on all calculations. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application



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Figure 46. 5-V Output TPS54561-Q1 Design Example

8.2.1 Design Requirements

This guide illustrates the design of a high-frequency switching regulator using ceramic output capacitors. The designer must know a few parameters in order to start the design process. Determination of these requirements is typically at the system level. This example design uses the following known parameters:

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Typical Application (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage (V_O)	5 V
Transient response, 1.25-A to 3.75-A load step	ΔV_O = ±4 %
Maximum output current (I_O)	5 A
Input voltage (V_I)	12 V nominal, 7 V to 60 V
Output voltage ripple ($V_{O(RIPPLE)}$)	0.5% of V_O
Start input voltage (rising V_I)	6.5 V
Stop input voltage (falling V_I)	5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54561-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible because this produces the smallest solution size. High switching frequency allows for lower-value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. Several factors including the minimum controllable on-time of the internal power switch, the input voltage, the output voltage, and the frequency-foldback protection limit the switching frequency that the designer can select.

Use Equation 12 and Equation 13 to calculate the upper limit of the switching frequency for the regulator. Choose the lower-value result from the two equations. Switching frequencies higher than these values result in pulse-skipping or the lack of overcurrent protection during a short circuit.

The typical minimum controllable on-time, $t_{(ON)}$, is 100 ns for the TPS54561-Q1 device. For this example, the output voltage is 5 V and the maximum input voltage is 60 V, which allows for a maximum switch frequency up to 955 kHz to avoid pulse skipping from Equation 28. To ensure overcurrent runaway is not a concern during short circuits, use Equation 29 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 60 V, assuming a diode voltage of 0.7 V, inductor resistance of 11 mΩ, switch resistance of 87 mΩ, a current limit value of 6 A, and short-circuit output voltage of 0.1 V, the maximum switching frequency is 1151 kHz.

For this design, choose a lower switching frequency of 400 kHz to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 10, or the curve in Figure 6, or the curve in Figure 7. Resistor R3 sets the switching frequency shown in Figure 46. For 400-kHz operation, the closest standard value resistor is 243 kΩ.

$$f_{(SW_skip)}max = \frac{1}{100\ ns} \times \left(\frac{5\ A \times 11\ m\Omega + 5\ V + 0.7\ V}{60\ V - 5\ A \times 87\ m\Omega + 0.7\ V} \right) = 955\ kHz \quad (28)$$

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$$f_{(SW_shift)} = \frac{8}{100\ ns} \times \left(\frac{6\ A \times 11\ m\Omega + 0.1\ V + 0.7\ V}{60\ V - 6\ A \times 87\ m\Omega + 0.7\ V} \right) = 1151\ kHz \quad (29)$$

$$R_T\ (k\Omega) = \frac{101756}{400\ (kHz)^{1.008}} = 242\ k\Omega \quad (30)$$

8.2.2.3 Output Inductor Selection ($L_{(O)}$)

To calculate the minimum value of the output inductor, use Equation 31.

$k_{(IND)}$ is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer. However, the designer may use the following guidelines.

For designs using low-ESR output capacitors such as ceramics, a value as high as $k_{(IND)}$ = 0.3 may be desirable. When using higher-ESR output capacitors, $k_{(IND)}$ = 0.2 yields better results. Because the inductor ripple current is part of the current-mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide-input voltage regulator, choosing a relatively large inductor ripple current is best to provide sufficient ripple current with the input voltage at the minimum.

For this design example, $k_{(IND)}$ = 0.3 and the calculated inductor value is 7.6 µH. The nearest standard value is 7.2 µH. It is important not to exceed both the rms current and saturation-current ratings of the inductor. Equation 33 and Equation 34 calculate the rms and peak inductor current. For this design, the rms inductor current is 5.021 A and the peak inductor current is 5.817 A. The chosen inductor has an rms current rating of 6 A and a saturation current rating of 7.9 A.

As the equation set demonstrates, lowering ripple currents reduces the output voltage ripple of the regulator but requires a larger value of inductance. Selecting higher ripple currents increases the output-voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most-conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch-current limit of the TPS54561-Q1 device, which is nominally 7.5 A.

$$L_{(O)}min = \left(\frac{V_I max - V_O}{I_O \times K_{(IND)}} \right) \times \left(\frac{V_O}{V_I max \times f_{(SW)}} \right) = \left(\frac{60\ V - 5\ V}{5\ A \times 0.3} \right) \times \left(\frac{5\ V}{60\ V \times 400\ kHz} \right) = 7.6\ \mu H \quad (31)$$

$$I_{(RIPPLE)} = \frac{V_O \times \left(V_I max - V_O \right)}{V_I max \times L_{(O)} \times f_{(SW)}} = \frac{5\ V \times (60\ V - 5\ V)}{60\ V \times 7.2\ \mu H \times 400\ kHz} = 1.591\ A \quad (32)$$

$$I_{(L)}RMS = \sqrt{\left(I_O\right)^2 + \frac{1}{12} \times \left(\frac{V_O \times \left(V_I max - V_O \right)}{V_I max \times L_{(O)} \times f_{(SW)}} \right)^2} = \sqrt{(5\ A)^2 + \frac{1}{12} \times \left(\frac{5\ V \times (60\ V - 5\ V)}{60\ V \times 7.2\ \mu H \times 400\ kHz} \right)^2} = 5.021\ A \quad (33)$$

$$I_{(L)}peak = I_O + \frac{I_{(RIPPLE)}}{2} = 5.021\ A + \frac{1.591\ A}{2} = 5.817\ A \quad (34)$$

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8.2.2.4 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and the regulator response to a large change in load current. It is necessary to select the output capacitance based on the most-stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for two clock cycles to maintain the output voltage within the specified range. Equation 35 shows the minimum output capacitance necessary, where ΔI_O is the change in output current, $f_{(sw)}$ is the regulator switching frequency, and ΔV_O is the allowable change in the output voltage. For this example, the transient load response specification is 4% change in V_O for a load step from 1.25 A to 3.75 A. Therefore, ΔI_O is 3.75 A – 1.25 A = 2.5 A, and ΔV_O = 4% × 5 V = 0.2 V. Using these numbers gives a minimum capacitance of 62.5 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore. Aluminum electrolytic and tantalum capacitors have higher ESR, and load-step calculations must include the ESR term.

Sizing of the output capacitor must be such as to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator cannot sink current, so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. Figure 51 shows a typical load-step response. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. Sizing of the capacitor must be such as to maintain the desired output voltage during these transient periods. Equation 36 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where $L_{(O)}$ is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_P is the peak output voltage, and $V_{(int)}$ is the initial voltage. For this example, the worst-case load step is from 3.75 A to 1.25 A. The output voltage increases during this load transition, and the stated maximum in our specification is 4% of the output voltage. This makes $V_{(P)}$ = 1.04 × 5 V = 5.2 V. $V_{(int)}$ is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 36 yields a minimum capacitance of 44.1 µF.

Equation 37 calculates the minimum output capacitance needed to meet the output-voltage ripple specification, where $f_{(SW)}$ is the switching frequency, $V_{O(RIPPLE)}$ is the maximum allowable output voltage ripple, and $I_{O(RIPPLE)}$ is the inductor ripple current. Equation 37 yields 19.9 µF.

Equation 38 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 38 indicates the ESR should be less than 15.7 mΩ.

The most stringent criterion for the output capacitor is 62.5 µF, required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature, and dc bias increase this minimum value. For this example, the selection is three 47-µF, 10-V ceramic capacitors with 5 mΩ of ESR. The derated capacitance is 87.4 µF, well above the minimum required capacitance of 62.5 µF.

Capacitors generally have a maximum ripple-current rating. Filtering a ripple current equal to or below that maximum ripple current does not degrade capacitor reliability. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Use Equation 39 to calculate the rms ripple current that the output capacitor must support. For this example, Equation 39 yields 459 mA.

$$C_{(O)} > \frac{2 \times \Delta I_O}{f_{(SW)} \times \Delta V_O} = \frac{2 \times 2.5\ A}{400\ kHz \times 0.2\ V} = 62.5\ \mu F \tag{35}$$

$$C_{(O)} > L_{(O)} \times \frac{\left(\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right)}{\left(\left(V_{(P)}\right)^2 - \left(V_{(int)}\right)^2 \right)} = 7.2\ \mu H \times \frac{\left(3.75\ A^2 - 1.25\ A^2\right)}{\left(5.2\ V^2 - 5\ V^2\right)} = 44.1\ \mu F \tag{36}$$

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$$C_{(O)} > \frac{1}{8 \times f_{(SW)}} \times \frac{1}{\left(\frac{V_{O(RIPPLE)}}{I_{O(RIPPLE)}}\right)} = \frac{1}{8 \times 400\ kHz} \times \frac{1}{\left(\frac{25\ mV}{1.591\ A}\right)} = 19.9\ \mu F \quad (37)$$

$$R_{(ESR)} < \frac{V_{O(RIPPLE)}}{I_{O(RIPPLE)}} = \frac{25\ mV}{1.591\ A} = 15.7\ m\Omega \quad (38)$$

$$I_{(CO)}RMS = \frac{V_O \times \left(V_I min - V_O\right)}{\sqrt{12} \times V_I min \times L_{(O)} \times f_{(SW)}} = \frac{5\ V \times \left(60\ V - 5\ V\right)}{\sqrt{12} \times 60\ V \times 7.2\ \mu H \times 400\ kHz} = 459\ mA \quad (39)$$

8.2.2.5 Catch Diode

The TPS54561-Q1 device requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than maximum input voltage. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode because of the low forward voltage of these diodes. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferable, to allow input voltage transients up to the rated voltage of the TPS54561-Q1 device.

For the example design, select the Schottky diode for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the diode is 0.52 V at 5 A.

One must select the diode with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. Multiplying the output current during the off-time with the forward voltage of the diode can calculate the instantaneous conduction losses of the diode. At higher switching frequencies, take the ac losses of the diode into account. The ac losses of the diode are because of the charging and discharging of the junction capacitance, and also of reverse-recovery charge. Use Equation 40 to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The selected diode has a junction capacitance of 180 pF. Using Equation 40 with the nominal input voltage of 12 V, the total loss in the diode is 1.65 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_{(D)} = \frac{\left(V_I - V_O\right) \times I_O \times V_{(d)}}{V_I} + \frac{C_{(j)} \times f_{(SW)} \times \left(V_I + V_{(d)}\right)^2}{2} =$$

$$\frac{\left(12\ V - 5\ V\right) \times 5\ A \times 0.52\ V}{12\ V} + \frac{180\ pF \times 400\ kHz \times \left(12\ V + 0.52\ V\right)^2}{2} = 1.65\ W \quad (40)$$

8.2.2.6 Input Capacitor

The TPS54561-Q1 device requires a high-quality ceramic type X5R or X7R input decoupling capacitor with at least 3 µF of effective capacitance. Some applications benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance because of dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input current ripple of the TPS54561-Q1 device. Use Equation 41 to calculate the input ripple current.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. Selecting a dielectric material that is more stable over temperature can minimize the capacitance variations because of temperature. The usual selection for capacitors in a switching regulator is X5R or X7R ceramic dielectric, because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The input capacitor selection must also consider the dc bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

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This example design requires a ceramic capacitor with at least a 60-V voltage rating to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V. For this example, use four 2.2-µF, 100-V capacitors in parallel.

The input capacitance value determines the input ripple voltage of the regulator. Use Equation 42 to calculate the input voltage ripple. Using the design example values, I_O = 5 A, $C_{(I)}$ = 8.8 µF, $f_{(sw)}$ = 400 kHz, yields an input voltage ripple of 355 mV and an rms input ripple current of 2.26 A.

$$I_{(CI)}RMS = I_O \times \sqrt{\frac{V_O}{V_I min} \times \left(\frac{V_I min - V_O}{V_I min} \right)} = 5\ A \times \sqrt{\frac{5\ V}{7\ V} \times \left(\frac{7\ V - 5\ V}{7\ V} \right)} = 2.26\ A \quad (41)$$

$$\Delta V_I = \frac{I_O \times 0.25}{C_{(I)} \times f_{(SW)}} = \frac{5\ A \times 0.25}{8.8\ \mu F \times 400\ kHz} = 355\ mV \quad (42)$$

8.2.2.7 Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. Adjustable soft-start is also useful if the output capacitance is large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the output capacitor may make the TPS54561-Q1 device reach the current limit, or the excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

The soft-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Use Equation 43 to find the minimum soft-start time, $t_{(SS)}$, necessary to charge the output capacitor, $C_{(O)}$, from 10% to 90% of the output voltage, V_O, with an typical soft-start current of $I_{(SS)}$. In the example, to charge the effective output capacitance of 87.4 µF up to 5 V with an average current of 1 A requires a 0.3-ms soft-start time.

After selecting the soft-start time, calculate the soft-start capacitor value by using Equation 5. For the example circuit, the soft-start time is not too critical, because the output capacitor value is 3 × 47 µF, which does not require much current to charge to 5 V. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms, which requires a 9.3-nF soft-start capacitor, as calculated by Equation 44. For this design, use the next-larger standard value of 10 nF.

$$t_{(SS)} > \frac{C_{(O)} \times V_O \times 0.8}{I_{(SS)}} \quad (43)$$

$$C13 = \frac{t_{(SS)}\ (ms) \times I_{(SS)}\ (\mu A)}{V_{ref}\ (V) \times 0.8} = \frac{3.5\ ms \times 1.7\ \mu A}{0.8\ V \times 0.8} = 9.3\ nF \quad (44)$$

8.2.2.8 Bootstrap Capacitor Selection

The TPS54561-Q1 device requires a 0.1-µF ceramic capacitor connected between the BOOT and SW pins for proper operation. The recommendation is a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

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8.2.2.9 Undervoltage Lockout Set Point

Using an external voltage divider on the EN pin of the TPS54561-Q1 device can adjust the undervoltage lockout (UVLO). The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down when the input voltage is falling. For the example design, the TPS54561-Q1 device should turn on and start switching once the input voltage increases above 6.5 V (UVLO start). After the regulator starts switching, it should continue to do so until the input voltage falls below 5 V (UVLO stop).

A resistor divider consisting of $R_{(UVLO1)}$ and $R_{(UVLO2)}$ between V_I and ground, and connected to the EN pin, can set programmable UVLO threshold voltage. Equation 3 and Equation 4 calculate the resistance values necessary. For the example application, a 442-kΩ resistor between V_I and EN (R1) and a 90.9-kΩ resistor between EN and ground (R2) are required to produce the 6.5-V start and 5-V stop voltages.

$$R1 = \frac{V_{(START)} - V_{(STOP)}}{I_{(HYS)}} = \frac{6.5\ V - 5\ V}{3.4\ \mu A} = 441.18\ k\Omega \tag{45}$$

$$R2 = \frac{V_{(EN)th}}{\frac{V_{(START)} - V_{(EN)th}}{R_{(UVLO1)}} + I_{(1)}} = \frac{1.2\ V}{\frac{6.5\ V - 1.2\ V}{442\ k\Omega} + 1.2\ \mu A} = 90.97\ k\Omega \tag{46}$$

8.2.2.10 Output Voltage and Feedback Resistor Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, select 10.2 kΩ for R6. Use Equation 2 to calculate R5 as 53.55 kΩ. The nearest standard 1% resistor is 53.6 kΩ. Because of the input current of the FB pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. A value for R6 of less than 800 kΩ satisfies this requirement. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R5 = R6 \times \left(\frac{V_O - 0.8\ V}{0.8\ V} \right) = 10.2\ k\Omega \times \left(\frac{5\ V - 0.8\ V}{0.8\ V} \right) = 53.55\ k\Omega \tag{47}$$

8.2.2.11 Compensation

There are several methods to design compensation for dc-dc regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Ignoring the slope compensation causes the actual crossover frequency to be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole.

To get started, calculate the modulator pole, $f_{(P,mod)}$, and the ESR zero, $f_{(Z,mod)}$ using Equation 48 and Equation 49. For output capacitance $C_{(O)}$, use a derated value of 87.4 µF. Use equations Equation 50 and Equation 51 to estimate a starting point for the crossover frequency, $f_{(CO)}$. For the example design, $f_{(P,mod)}$ is 1821 Hz and $f_{(Z,mod)}$ is 1090 kHz. Equation 50 is the geometric mean of the modulator pole and the ESR zero, and Equation 51 is the geometric mean of modulator pole and half of the switching frequency. Equation 50 yields 44.6 kHz and Equation 51 gives 19.1 kHz. Use the geometric mean value of Equation 50 and Equation 51 for an initial crossover frequency which is 29.2 kHz. For this example, the target crossover frequency is 30 kHz for an improved transient response.

Next, calculate the compensation components. Use of a resistor in series with a capacitor creates a compensating zero. A capacitor in parallel with these two components forms the compensating pole.

$$f_{(P,mod)} = \frac{I_O\ max}{2\pi \times V_O \times C_{(O)}} = \frac{5\ A}{2\pi \times 5\ V \times 87.4\ \mu F} = 1821\ Hz \tag{48}$$

$$f_{(Z,mod)} = \frac{1}{2\pi \times R_{(ESR)} \times C_{(O)}} = \frac{1}{2\pi \times 1.67\ m\Omega \times 87.4\ \mu F} = 1090\ kHz \tag{49}$$

$$f_{(CO1)} = \sqrt{f_{(P,mod)} \times f_{(Z,mod)}} = \sqrt{1821\ Hz \times 1090\ kHz} = 44.6\ kHz \tag{50}$$

$$f_{(CO2)} = \sqrt{f_{(P,mod)} \times \frac{f_{(SW)}}{2}} = \sqrt{1821\ Hz \times \frac{400\ kHz}{2}} = 19.1\ kHz \tag{51}$$

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To determine the compensation resistor, R4, use Equation 52. Assume the power stage transconductance, $g_{m(ps)}$, is 17 S. The output voltage V_O, reference voltage V_{ref}, and amplifier transconductance $g_{m(ea)}$, are 5 V, 0.8 V and 350 µS, respectively. Calculated the value for R4 as 16.84 kΩ, and then select a standard value of 16.9 kΩ. Use Equation 53 to set the compensation zero to the modulator pole frequency. Equation 53 yields 5172 pF for compensating capacitor C5. The selection for this design is 4700 pF.

$$R4 = \left(\frac{2\pi \times f_{(CO)} \times C_{(O)}}{g_{m(ps)}}\right) \times \left(\frac{V_O}{V_{ref} \times g_{m(ea)}}\right) = \left(\frac{2\pi \times 29.2\,kHz \times 87.4\,\mu F}{17\,S}\right) \times \left(\frac{5\,V}{0.8\,V \times 350\,\mu S}\right) = 16.84\,k\Omega \quad (52)$$

$$C5 = \frac{1}{2\pi \times R4 \times f_{(P,mod)}} = \frac{1}{2\pi \times 16.9\,k\Omega \times 1821\,Hz} = 5172\,pF \quad (53)$$

If desired, implement a compensation pole by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 54 and Equation 55 for C8 to set the compensation pole. The selected value of C8 is 47 pF for this example design.

$$C8 = \frac{C_{(O)} \times R_{(ESR)}}{R4} = \frac{87.4\,\mu F \times 1.67\,m\Omega}{16.9\,k\Omega} = 8.64\,pF \quad (54)$$

$$C8 = \frac{1}{\pi \times R4 \times f_{(SW)}} = \frac{1}{\pi \times 16.9\,k\Omega \times 400\,kHz} = 47.1\,pF \quad (55)$$

8.2.2.12 Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the example design enters discontinuous-conduction mode when the output current is less than 408 mA. The power supply enters Eco-mode when the output current is lower than 25.3 mA. The input current draw is 257 µA with no load.

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8.2.2.13 Power Dissipation Estimate

The following formulas show how to estimate the TPS54561-Q1 device power dissipation under continuous conduction mode (CCM) operation. These equations are not suitable if the device operates in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss ($P_{(COND)}$), switching loss ($P_{(SW)}$), gate drive loss ($P_{(G)}$) and supply current loss ($P_{(Q)}$). Example calculations are shown with the 12-V nominal input voltage of the example design.

1. Conduction loss

$$P_{(COND)} = \left(I_O\right)^2 \times r_{DS(on)} \times \left(\frac{V_O}{V_I}\right) = 5\ A^2 \times 87\ m\Omega \times \left(\frac{5\ V}{12\ V}\right) = 0.906\ W$$

where

- I_O is the output current (A)
- $r_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_O is the output voltage (V)
- V_I is the input voltage (V)

(56)

2. Switching loss

$$P_{(SW)} = V_I \times f_{(SW)} \times I_O \times t_r = 12\ V \times 400\ kHz \times 5\ A \times 4.9\ ns = 0.118\ W$$

where

- $f_{(SW)}$ is the switching frequency (Hz)
- t_r is the SW pin voltage rise time, estimated by t_r = V_{DD} (V) × 0.16 (ns/V) + 3 (ns)

(57)

3. Gate drive loss

$$P_{(G)} = V_I \times Q_g \times f_{(SW)} = 12\ V \times 3\ nC \times 400\ kHz = 0.014\ W$$

where

- Q_g is the total gate charge of the internal MOSFET

(58)

4. Quiescent current loss

$$P_{(Q)} = V_I \times I_Q = 12\ V \times 152\ \mu A = 0.0018\ W$$

where

- I_Q is the operating nonswitching supply current

(59)

Therefore,

$$P_{(tot)} = P_{(COND)} + P_{(SW)} + P_{(G)} + P_{(Q)} = 0.906\ W + 0.118\ W + 0.014\ W + 0.0018\ W = 1.040\ W$$

(60)

For given T_A,

$$T_J = T_A + R_{\theta JA} \times P_{(tot)}$$

where

- T_J is the junction temperature (°C)
- T_A is the ambient temperature (°C)
- $R_{\theta JA}$ is the thermal resistance of the package (°C/W)
- $P_{(tot)}$ is the total device power dissipation (W)

(61)

For given $T_J$max = 150°C

$$T_A\,max = T_J\,max - R_{\theta JA} \times P_{(tot)}$$

where

- $T_A$max is maximum ambient temperature (°C)
- $T_J$max is maximum junction temperature (°C)

(62)

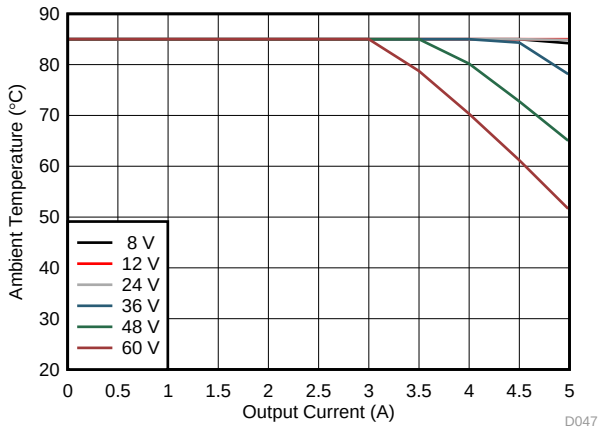
Additional power losses occur in the regulator circuit because of the inductor ac and dc losses, the catch diode and PCB trace resistance. All of these losses impact the overall efficiency of the regulator.

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8.2.3 Safe Operating Area

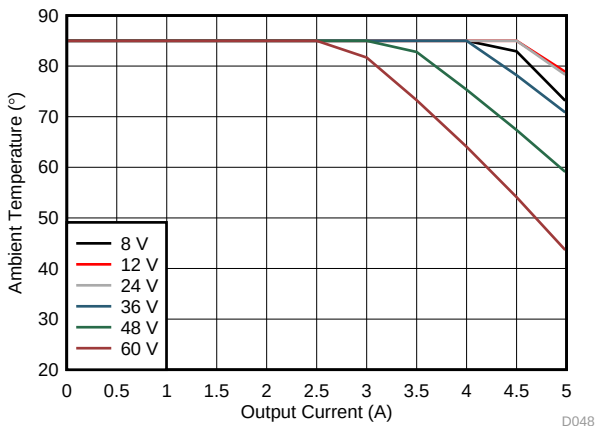
Figure 47 through Figure 50 show the safe operating area (SOA) of the device for 3.3-V, 5-V, and 12-V outputs and varying amounts of forced air flow applications. The temperature derating curves represent the conditions at which the TPS54561-Q1 device, PCB and the output Inductor are at or below the manufacturer's maximum operating temperatures. Figure 47, through Figure 50 doesn't consider the impact from the catch diode thermal performance. For higher reliability, TI uses 125 °C as the temperature limit for TPS54561-Q1 device on Figure 47, through Figure 50. Derating limits apply to devices soldered directly to a double-sided PCB with 2 oz. copper, similar to the board on TPS54561EVM-555 evaluation module.

Pay careful attention to the other components chosen for the design, especially the catch diode. In most applications, the catch diode limits the thermal performance. When operating at high duty cycles or at a higher switching frequency, the thermal performance of the TPS54561-Q1 device can become the limiting factor.



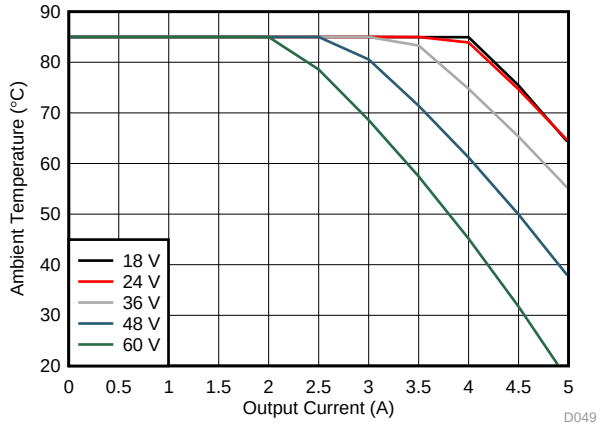
V_O = 3.3 V Natural Convection
$f_{(SW)}$ = 400 kHz

Figure 47. 3.3-V Outputs



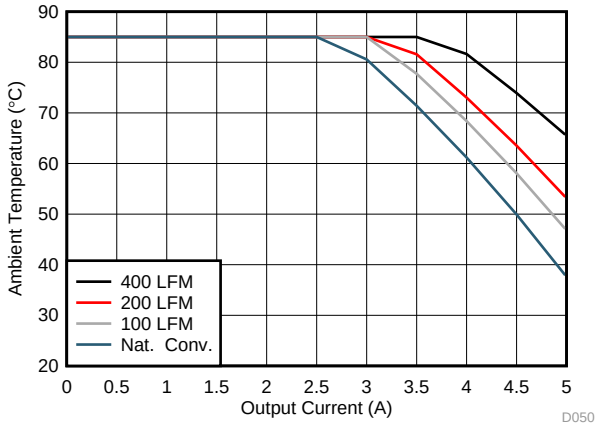
V_O = 5 V Natural Convection
$f_{(SW)}$ = 400 kHz

Figure 48. 5-V Outputs



V_O = 12 V Natural Convection
$f_{(SW)}$ = 600 kHz

Figure 49. 12-V Outputs



V_I = 48 V Air flow direction: L1 to output terminal
V_O = 12 V $f_{(SW)}$ = 600 kHz

Figure 50. Air Flow Conditions

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8.2.4 Application Curves

Acquisition of measurements uses a 12-V input, 5-V output, and 5-A load unless otherwise noted.

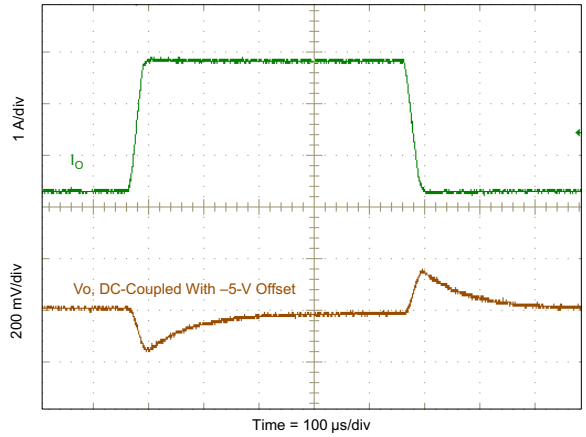


Figure 51. Load Transient Response (1.25-A to 3.75-A Load Step)

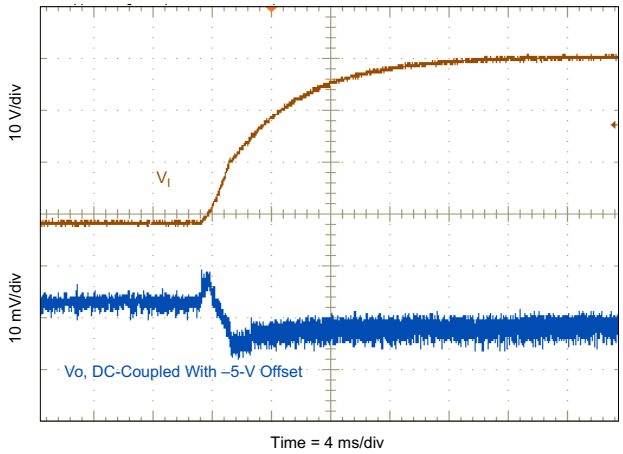
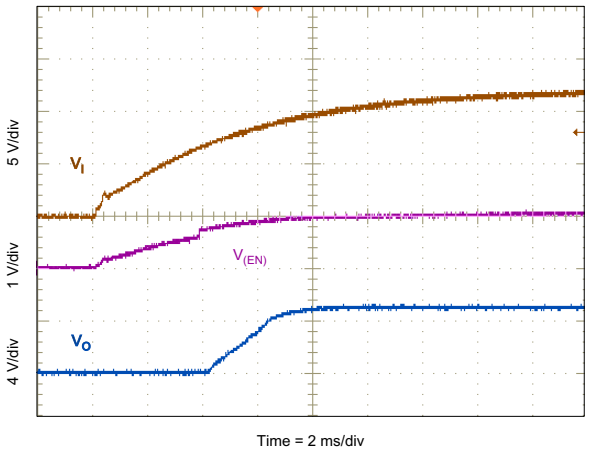
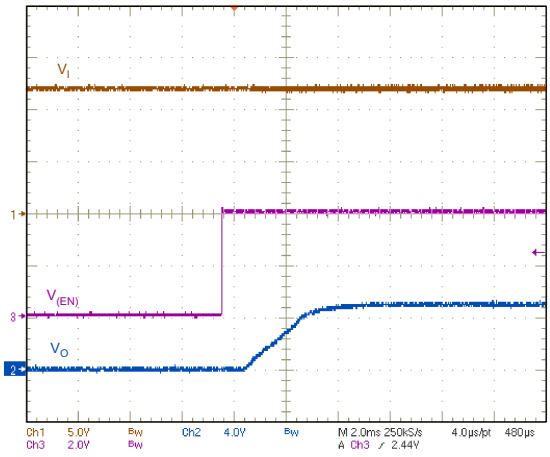


Figure 52. Line Transient (8 V to 40 V)



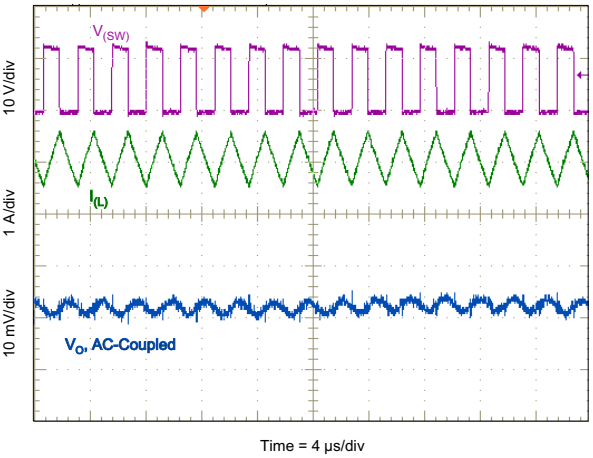
I_O = 5 A

Figure 53. Start-Up With Input Voltage



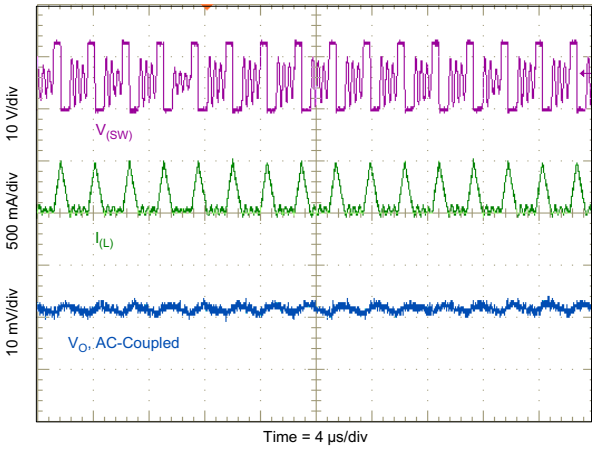
I_O = 5 A

Figure 54. Start-Up With EN



I_O = 5 A

Figure 55. Output Ripple, CCM

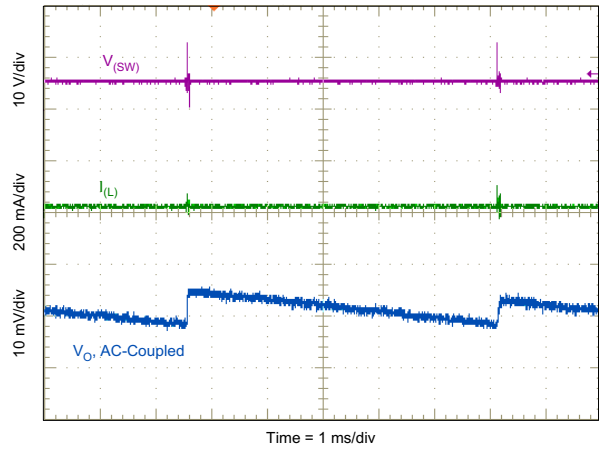


I_O = 100 mA

Figure 56. Output Ripple, DCM

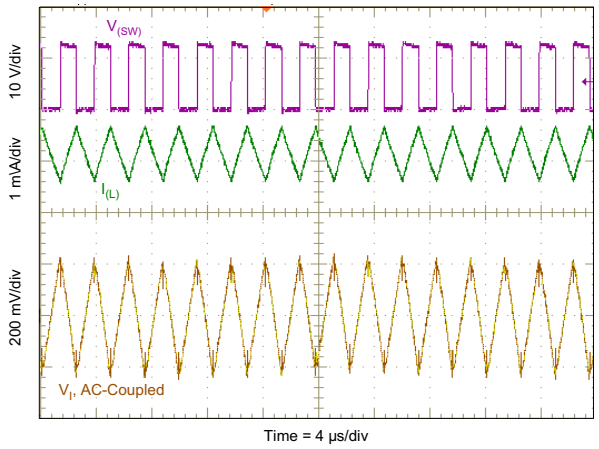
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Acquisition of measurements uses a 12-V input, 5-V output, and 5-A load unless otherwise noted.



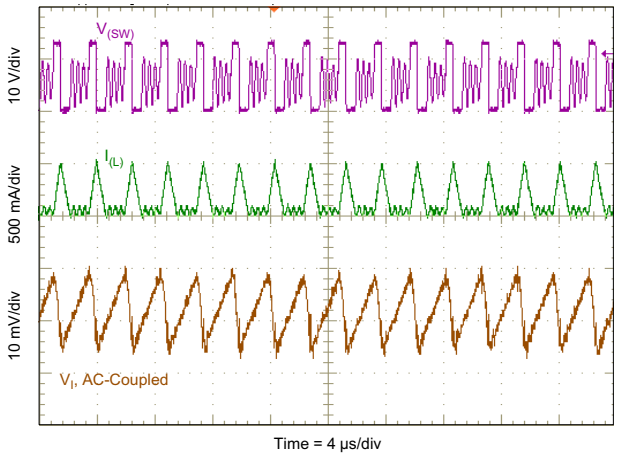
No load

Figure 57. Output Ripple, Eco-mode



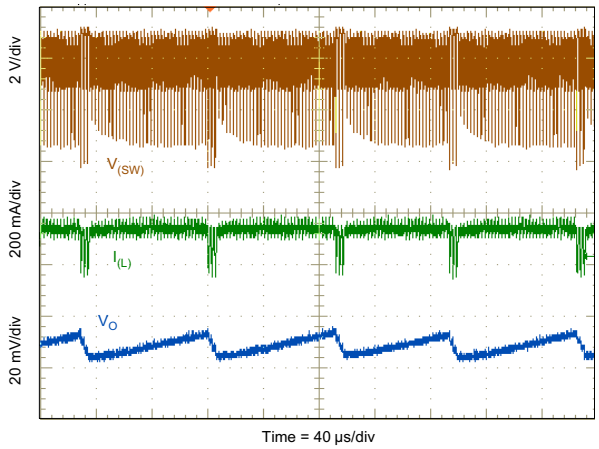
I_O = 5 A

Figure 58. Input Ripple, CCM



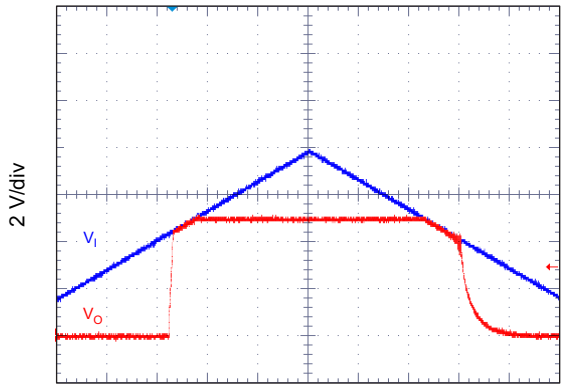
I_O = 100 mA

Figure 59. Input Ripple, DCM



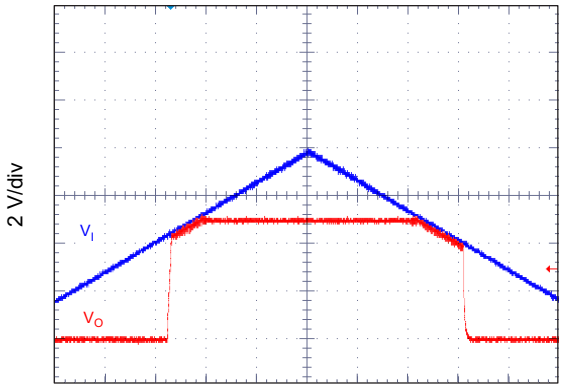
V_I = 5.5 V No load
V_O = 5.0 V EN floating

Figure 60. Low-Dropout Operation, Steady State



I_O = 100 mA EN floating

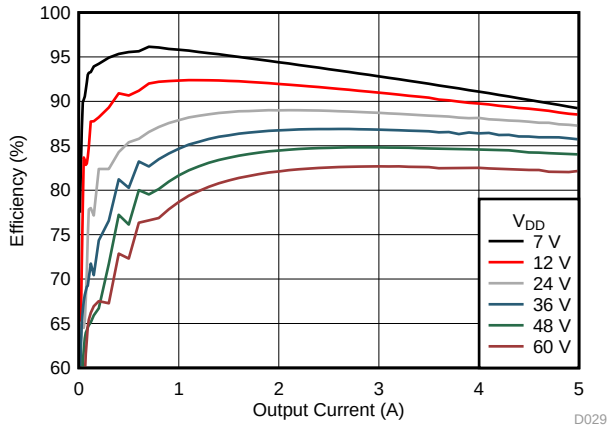
Figure 61. Low-Dropout Operation



I_O = 1 A EN floating

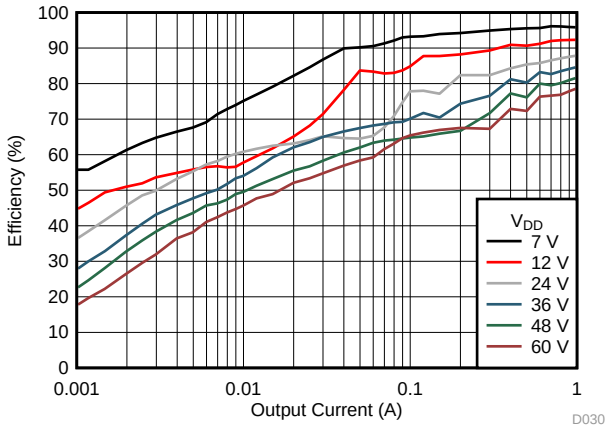
Figure 62. Low-Dropout Operation

Acquisition of measurements uses a 12-V input, 5-V output, and 5-A load unless otherwise noted.



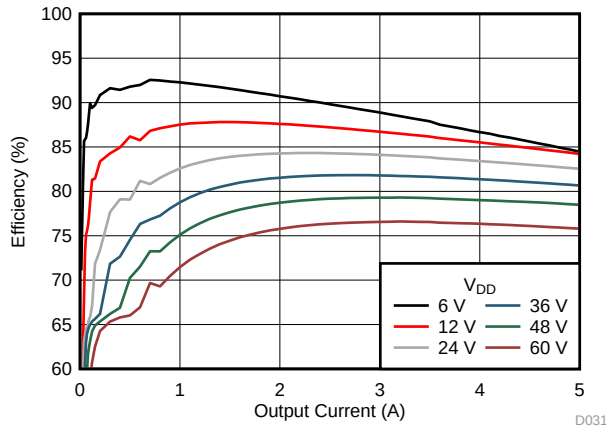
$f_{(SW)}$ = 400 kHz V_O = 5 V

Figure 63. Efficiency vs Load Current



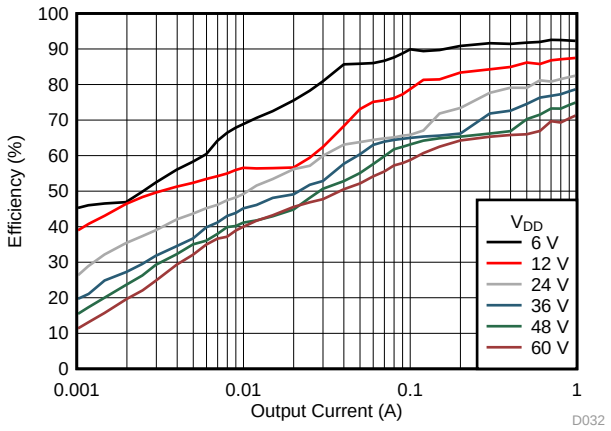
$f_{(SW)}$ = 400 kHz V_O = 5 V

Figure 64. Light-Load Efficiency



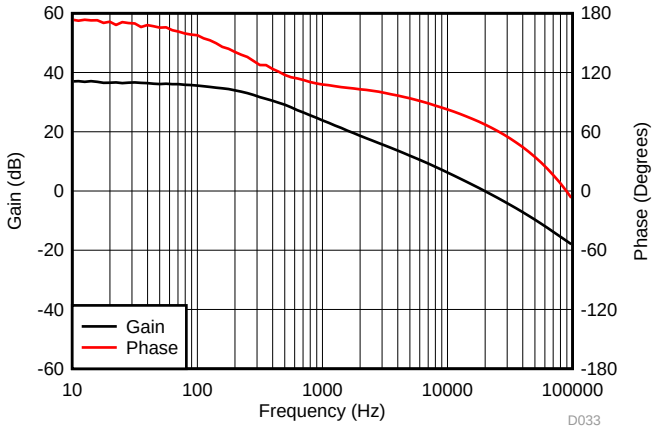
$f_{(SW)}$ = 400 kHz V_O = 3.3 V

Figure 65. Efficiency vs Load Current



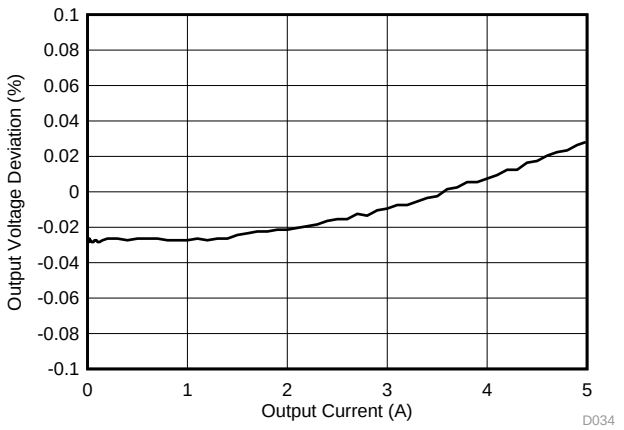
$f_{(SW)}$ = 400 kHz V_O = 3.3 V

Figure 66. Light-Load Efficiency



$f_{(SW)}$ = 400 kHz V_I = 12 V V_O = 5 V
I_O = 5 A

Figure 67. Overall Loop Frequency Response

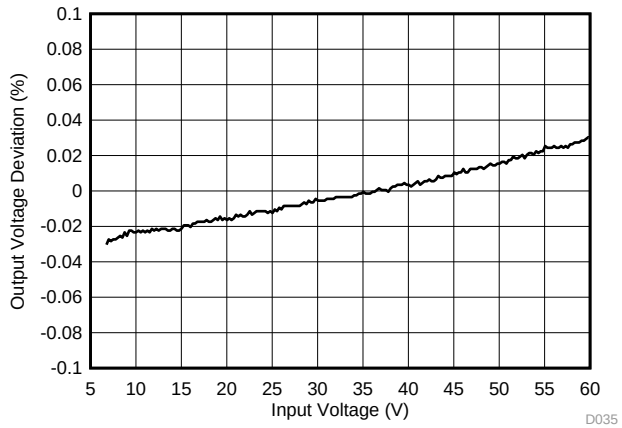


$f_{(SW)}$ = 400 kHz V_I = 12 V V_O = 5 V

Figure 68. Regulation vs Load Current

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Acquisition of measurements uses a 12-V input, 5-V output, and 5-A load unless otherwise noted.



$f_{(SW)}$ = 400 kHz I_O = 2.5 A V_O = 5 V

Figure 69. Regulation vs Input Voltage

8.2.5 Inverting Power Supply

One use of the TPS54561-Q1 is to convert a positive input voltage to a negative output voltage. Ideal applications are amplifiers requiring a negative power supply. For a more-detailed example, see *Create an Inverting Power Supply From a Step-Down Regulator*, application report SLVA317.

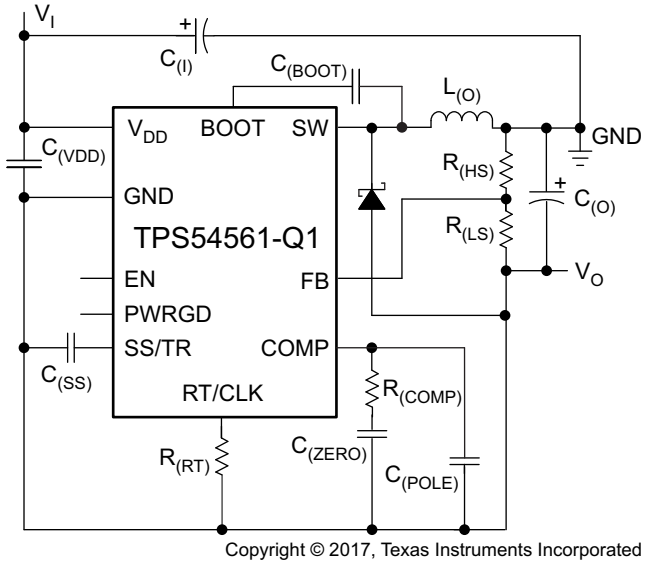


Figure 70. TPS54561-Q1 Inverting Power Supply Based on Application Report SLVA317

Acquisition of measurements uses a 12-V input, 5-V output, and 5-A load unless otherwise noted.

8.2.6 Split-Rail Power Supply

Another use of the TPS54561-Q1 device is to convert a positive input voltage to a split-rail positive- and negative-output voltage by using a coupled inductor. Ideal applications are amplifiers requiring a split-rail positive- and negative-voltage power supply. For a more-detailed example, see *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator*, application report SLVA369.

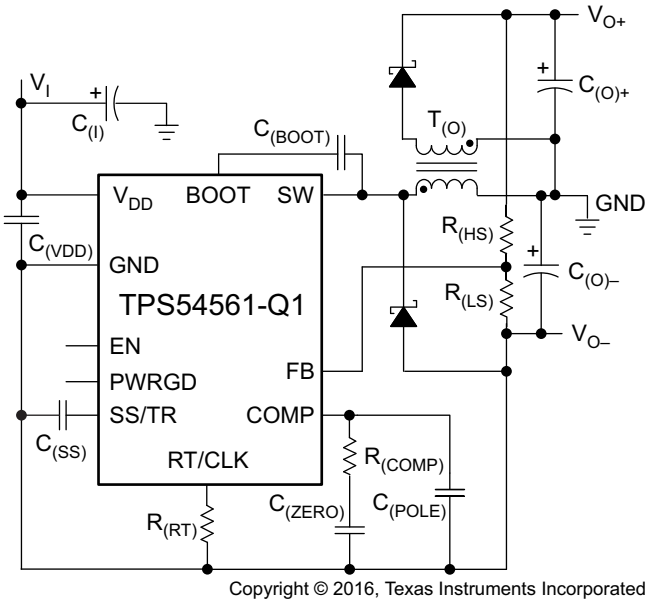


Figure 71. TPS54561-Q1 Split-Rail Power Supply Based on Application Report SLVA369

9 Power Supply Recommendations

The design of the device is for operation from an input voltage supply range between 4.5 V and 60 V. Good regulation of this input supply is essential. If the input supply is more distant than a few inches from the TPS54561-Q1 converter, the circuit may require additional bulk capacitance besides the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

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10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. See Figure 72 for a PCB layout example.

- To reduce parasitic effects, bypass the V_{DD} pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Take care to minimize the loop area formed by the bypass capacitor connections, the V_{DD} pin, and the anode of the catch diode. Route the SW pin to the cathode of the catch diode and to the output inductor. Because the SW connection is the switching node, locate the catch diode and output inductor close to the SW pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling.
- Tie the GND pin directly to the copper pad under the IC for the exposed thermal pad. Connect this copper pad to internal PCB ground planes using multiple vias directly under the IC.
- For operation at full-rated load, the top-side ground area must provide adequate heat dissipating area.
- The RT/CLK pin is sensitive to noise, so locate the RT resistor as close as possible to the IC and route conductors with minimal lengths of trace.
- Figure 72 shows the approximate placement for the additional external components.
- It may be possible to obtain acceptable performance with alternate PCB layouts. However, this layout, meant as a guideline, demonstrably produces good results.

Boxing in the components in the design of Figure 46, the estimated printed-circuit board area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors. To further reduce the area, use a two-sided assembly and replace the 0603-sized passives with a smaller-sized equivalent.

10.2 Layout Example

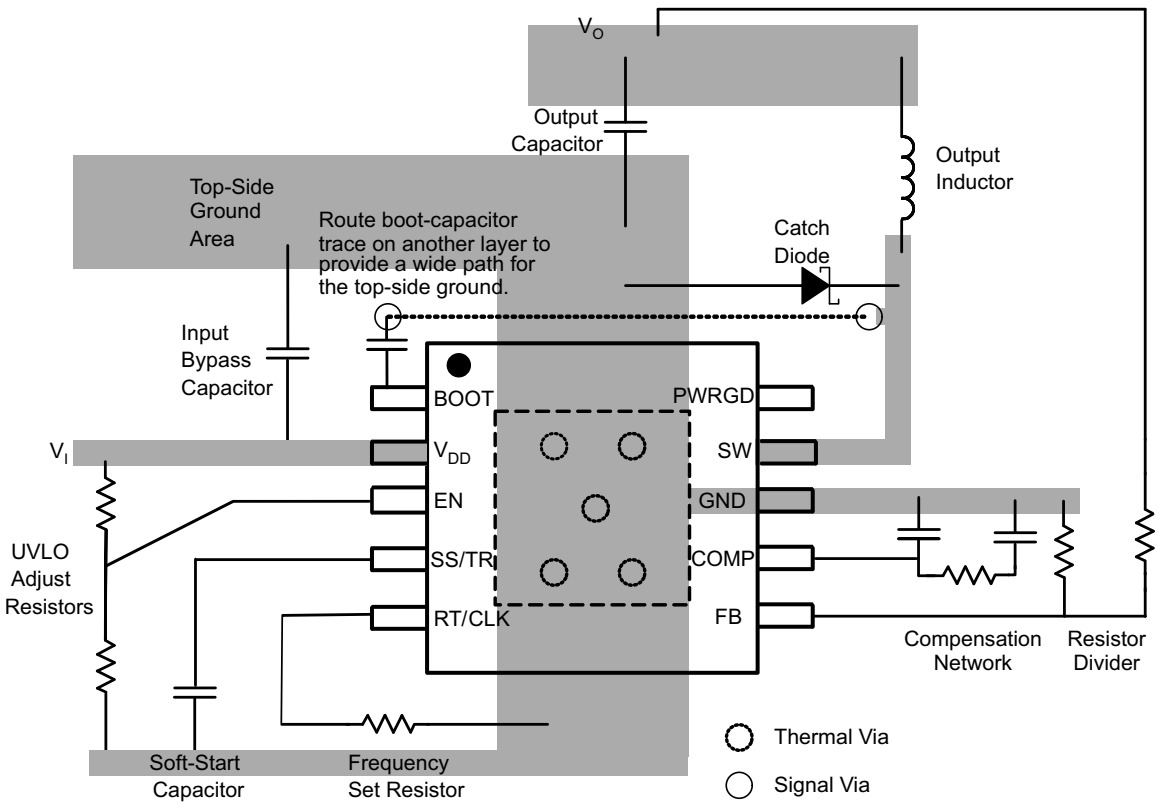


Figure 72. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the TPS54560, TPS54561, and TPS54561-Q1 family Excel design tool, see SLVC452.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Create an Inverting Power Supply From a Step-Down Regulator,* SLVA317
- *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator,* SLVA369
- *Evaluation Module for the TPS54561 Step-Down Converter,* SLVU993
- *Creating a Universal Car Charger for USB Devices From the TPS54240 and TPS2511,* SLVA464

11.2.2 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54561-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54561QDPRRQ1	ACTIVE	WSON	DPR	10	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 54561Q	Samples
TPS54561QDPRTQ1	ACTIVE	WSON	DPR	10	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 54561Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54561-Q1 :

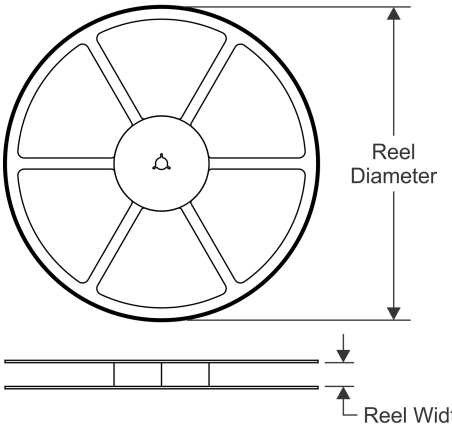
- Catalog: TPS54561

NOTE: Qualified Version Definitions:

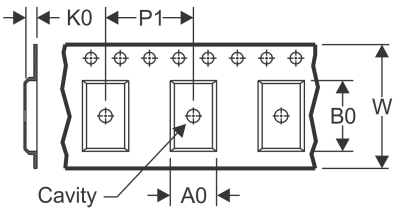
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

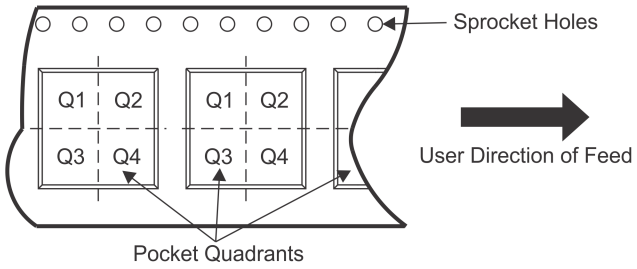


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

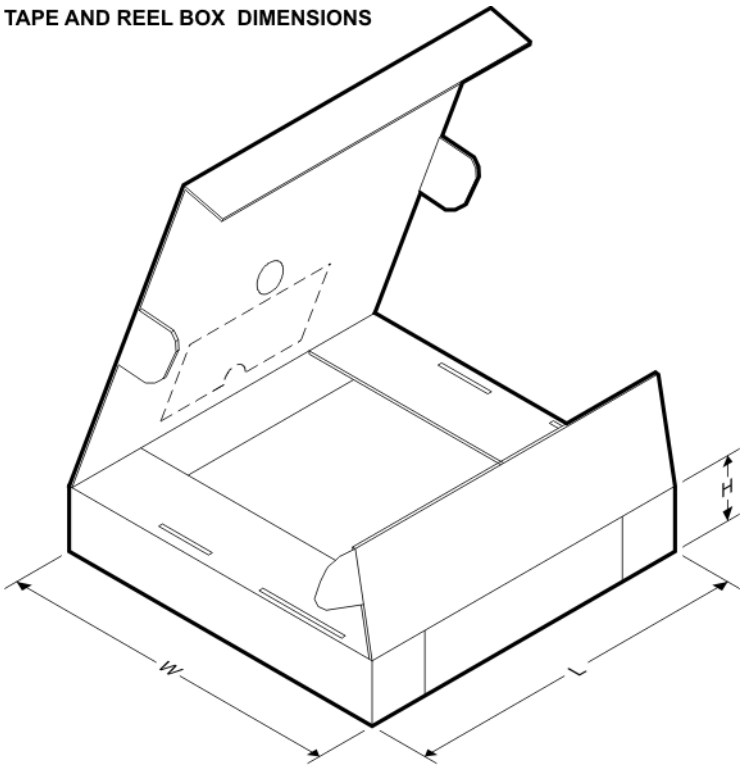
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54561QDPRRQ1	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54561QDPRTQ1	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

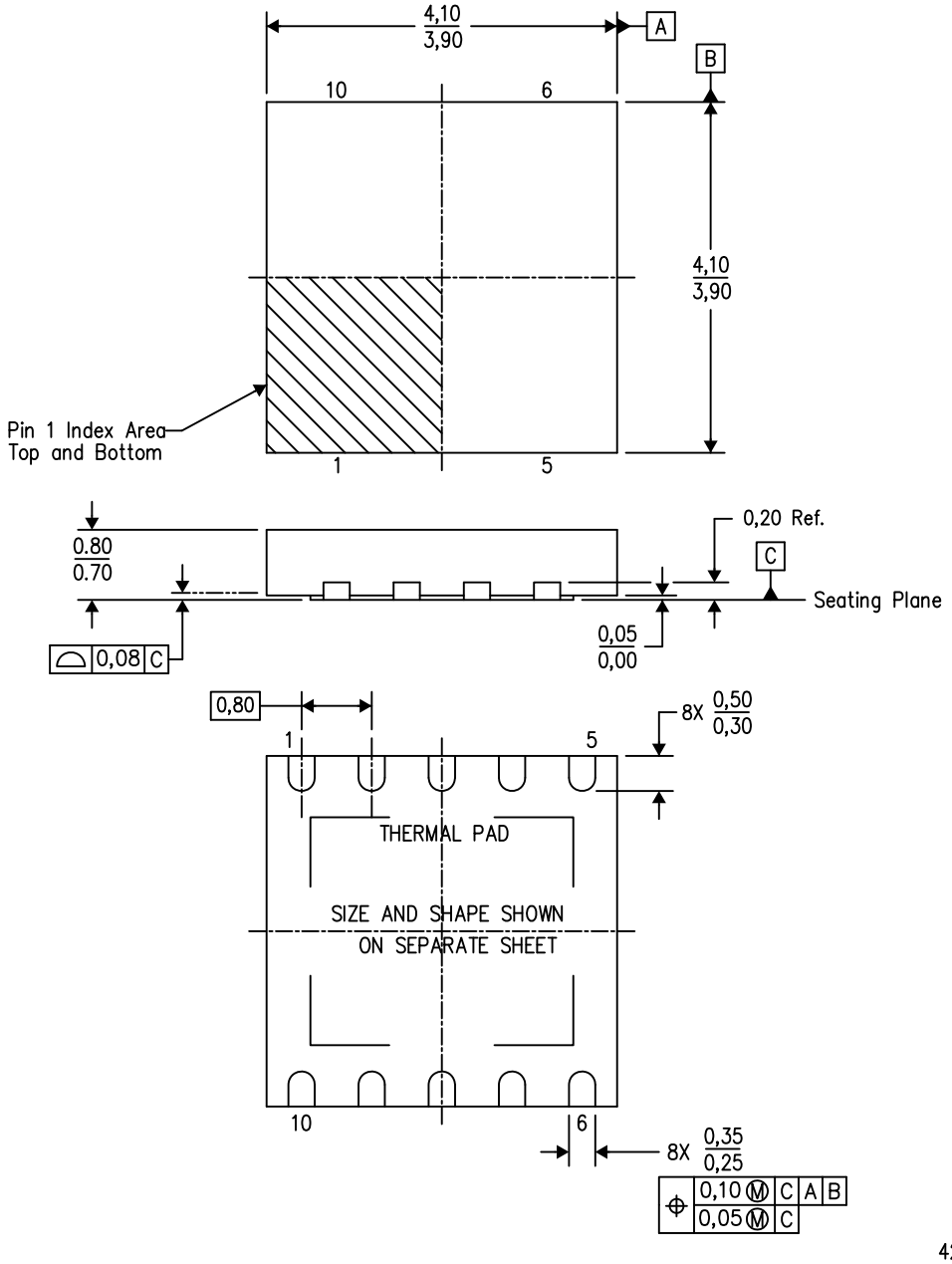
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54561QDPRRQ1	WSON	DPR	10	3000	367.0	367.0	35.0
TPS54561QDPRTQ1	WSON	DPR	10	250	210.0	185.0	35.0

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

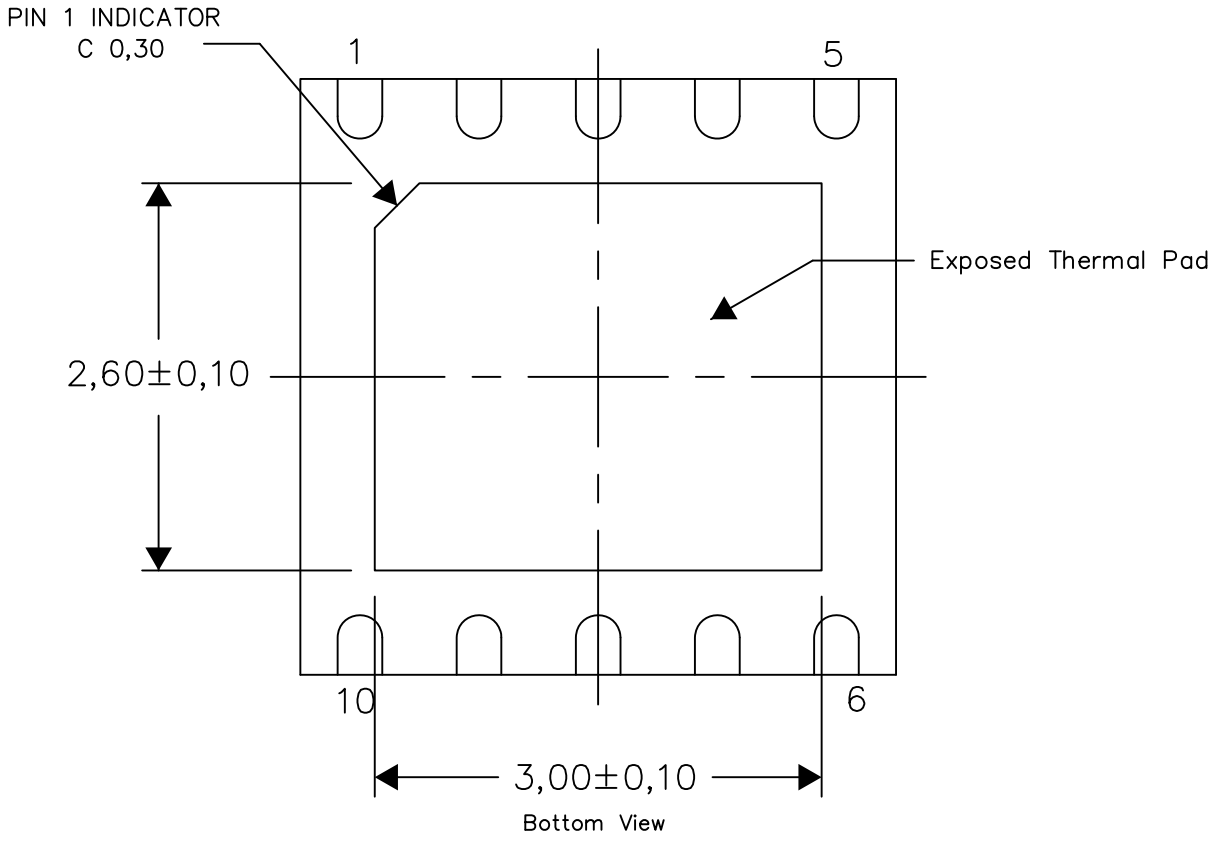
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

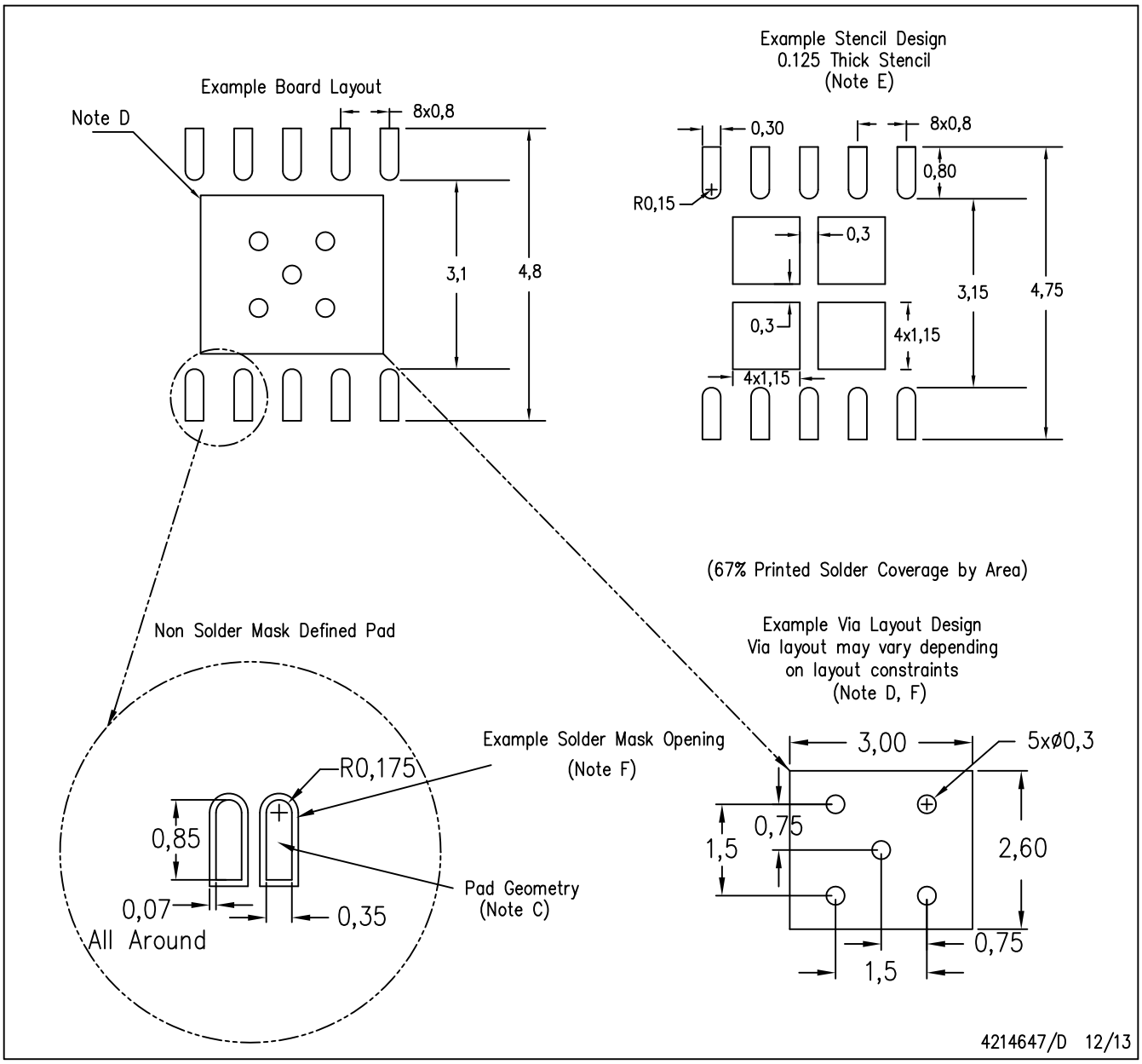


Exposed Thermal Pad Dimensions

4211551/C 12/13

NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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