19-3663; Rev 1; 6/07

Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

General Description

The MAX5077 is a +4.5V to +15V push-pull, current-fed topology driver subsystem with an integrated oscillator used in telecom module power supplies. The device drives two MOSFETs connected to a center-tapped transformer primary providing secondary-side, isolated, negative or positive voltages. The MAX5077 features a programmable accurate integrated oscillator with a synchronizing clock output to synchronize an external PWM regulator. A single external resistor programs the internal oscillator frequency from 50kHz to 1.5MHz.

The MAX5077 incorporates dual MOSFET drivers with ±3A peak drive currents and 50% duty cycle. The MOSFET drivers generate complementary signals to drive external ground-referenced n-channel MOSFETs.

The MAX5077 clock output frequency is programmable by logic inputs to set the clock output to 1x, 2x, or 4x the MOSFET's driver frequency.

The MAX5077 is available in a 14-pin exposed pad TSSOP package and is specified over the -40°C to +125°C operating temperature range.

Applications

Current-Fed Power Supplies

Power-Supply Building Subsystems

Push-Pull Driver Subsystems

Features

- **Dedicated Current-Fed, Push-Pull Driver Subsystem**
- **Oscillator Frequency Programmable from 50kHz to 1.5MHz**
- **Single +4.5V to +15V Supply Voltage Range**
- **±3A Peak Gate-Drive Current**
- **1mA Operating Current at 250kHz with No Capacitive Load**
- **Selectable Synchronizing Clock Frequency for a Preceding PWM Stage**
- **Thermally Enhanced 14-Pin TSSOP**
- **-40°C to +125°C Operating Temperature Range**

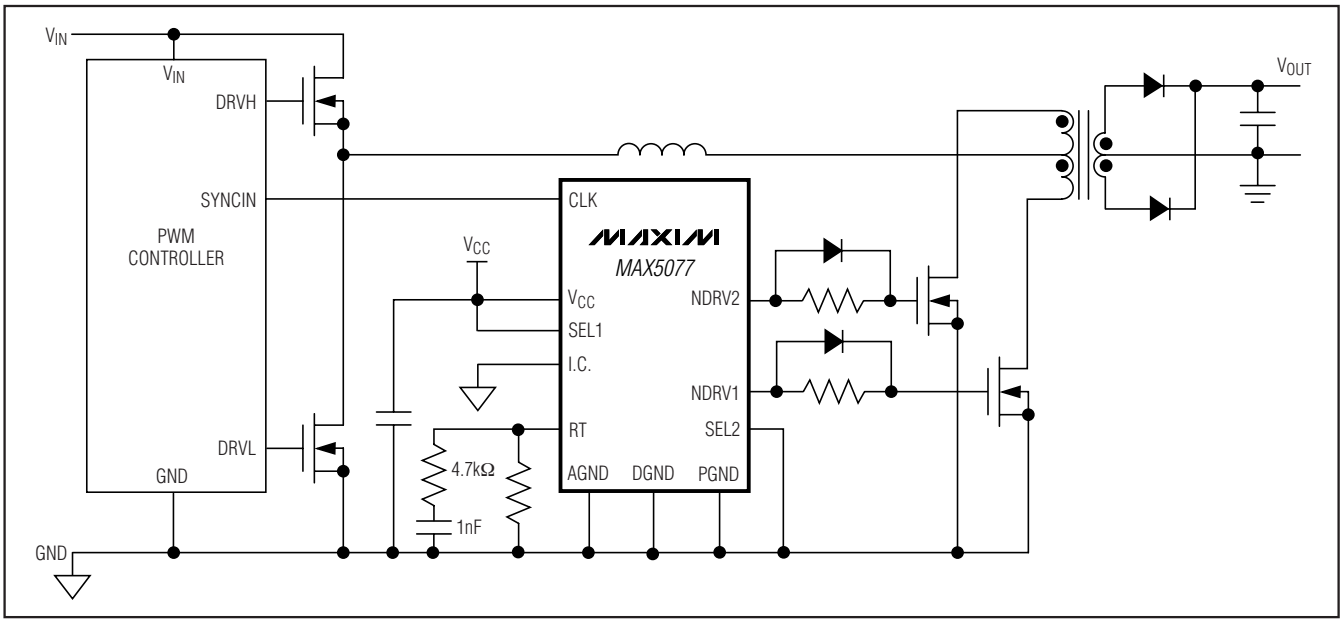
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5077AUD	-40°C to +125°C	14 TSSOP-EP*	U14E-3

**EP = Exposed paddle.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND, DGND, PGND .....-0.3V to +18V
PGND, DGND to AGND .....-0.3V to +0.3V
SEL1, SEL2 to DGND .....-0.3V to +18V
CLK, RT to AGND .....-0.3V to +6V
NDRV1, NDRV2 to PGND .....-0.3V to (V_{CC} + 0.3V)
CLK Current .....±20mA
NDRV1, NDRV2 Peak Current (200ns) .....±5A
NDRV1, NDRV2 Reverse Current (Latchup Current) .....±500mA

Continuous Power Dissipation (T_A = +70°C)
14-Pin TSSOP (derate 20.8mW/°C above +70°C) 1667mW
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, SEL1 = V_{CC}, SEL2 = DGND, R_{RT} = 124kΩ, NDRV1 = NDRV2 = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
Input Voltage Supply Range	V_{CC}			4.5		15.0	V
Static Supply Current	I_{CCST}	SEL2 = SEL1 = DGND, drivers not switching			150	320	µA
Switching Supply Current	I_{CCSW}	SEL2 = DGND, SEL1 = V_{CC}, f_{OSC} = 250kHz			1	3	mA
Undervoltage Lockout	V_{UVLO}	V_{CC} rising		3	3.5	4	V
UVLO Hysteresis					300		mV
OSCILLATOR							
Frequency Range	f_{OSC}	(Note 2)		50		1500	kHz
Accuracy		f_{OSC} = 250kHz, 6V ≤ V_{CC} ≤ 15V (Note 3)		-8		+10	%
Oscillator Jitter					±0.6		%
CLK Output High Voltage		I_{CLK} = 1mA	7V ≤ V_{CC} ≤ 15V	3.9		5.0	V
			4.5V ≤ V_{CC} ≤ 7V	3.35		5.0	
CLK Output Low Voltage		I_{CLK} = -1mA				50	mV
CLK Output Rise Time		C_{CLK} = 30pF			35		ns
CLK Output Fall Time		C_{CLK} = 30pF			10		ns
GATE DRIVERS (NDRV1, NDRV2)							
Output High Voltage	V_{OH}	I_{NDRV1} = I_{NDRV2} = 100mA		V_{CC} - 0.3			V
Output Low Voltage	V_{OL}	I_{NDRV1} = I_{NDRV2} = -100mA				0.3	V
Output Peak Current	I_P	Sourcing and sinking			3		A
Driver Output Impedance		NDRV_ sourcing 100mA			1.8	3	Ω
		NDRV_ sinking 100mA			1.6	2.6	
Latchup Current Protection		Reverse current at NDRV1/NDRV2			400		mA
Rise Time	t_R	C_{LOAD} = 2nF			10		ns
Fall Time	t_F	C_{LOAD} = 2nF			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, SEL1 = V_{CC}, SEL2 = DGND, R_{RT} = 124kΩ, NDRV1 = NDRV2 = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

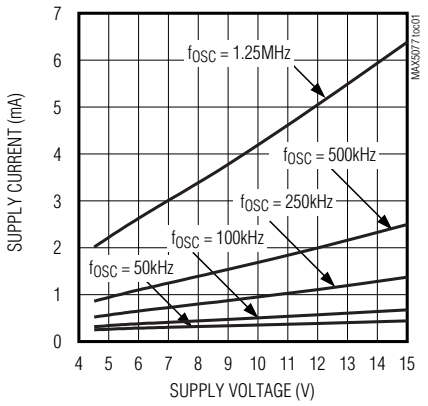
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEL_ INPUTS						
Input Current		0V ≤ $V_{SEL_}$ ≤ V_{CC}			1	µA
Input High Voltage	V_{IH}		3	2.5		V
Input Low Voltage	V_{IL}			2	1.5	V

Note 1: The MAX5077 is 100% tested at T_A = T_J = +125°C. All limits over temperature are guaranteed by design.
Note 2: Use the following formula to calculate the MAX5077 oscillator frequency: $f_{OSC} = 10^{12} / (32 \times R_{RT})$.
Note 3: The accuracy of the oscillator's frequency is lower at frequencies greater than 1MHz.

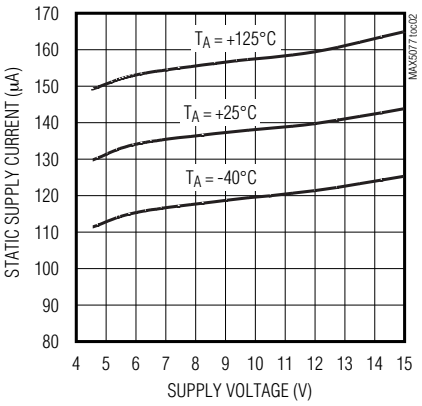
Typical Operating Characteristics

(V_{CC} = +12V, SEL1 = V_{CC}, SEL2 = DGND, R_{RT} = 124kΩ, NDRV1 = NDRV2 = open, CLK = open.)

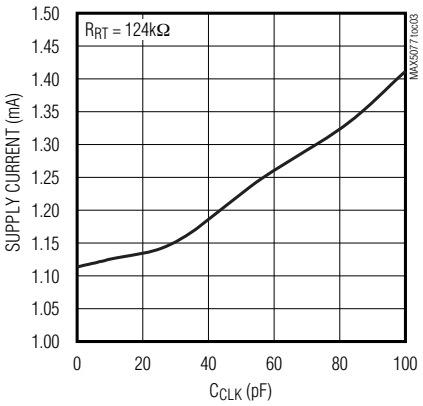
SUPPLY CURRENT vs. SUPPLY VOLTAGE



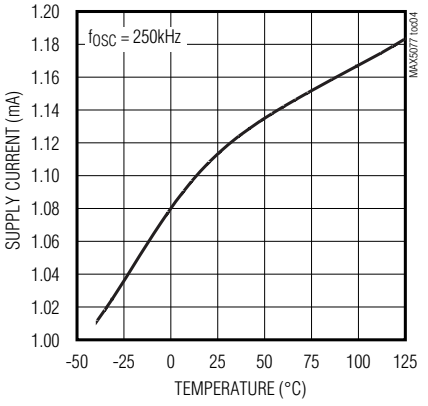
STATIC SUPPLY CURRENT vs. SUPPLY VOLTAGE



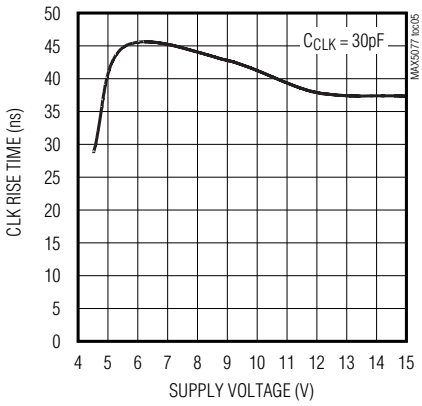
SUPPLY CURRENT vs. C_{CLK}



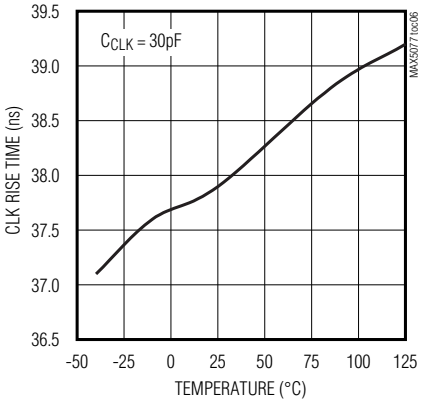
SUPPLY CURRENT vs. TEMPERATURE



CLK RISE TIME vs. SUPPLY VOLTAGE



CLK RISE TIME vs. TEMPERATURE

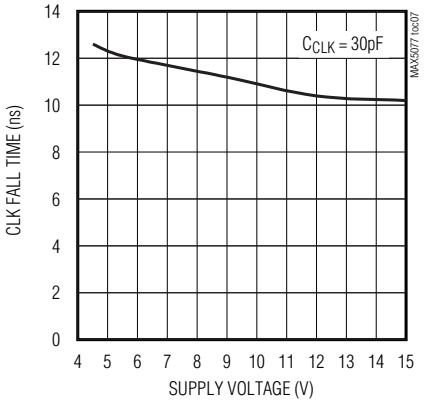


Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

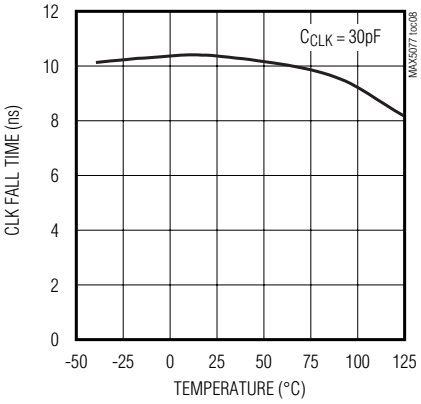
Typical Operating Characteristics (continued)

(V_{CC} = +12V, SEL1 = V_{CC}, SEL2 = DGND, R_{RT} = 124kΩ, NDRV1 = NDRV2 = open, CLK = open.)

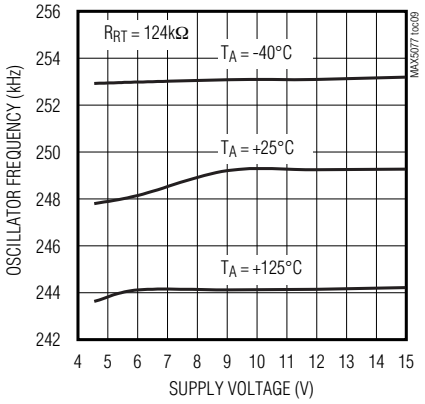
CLK FALL TIME vs. SUPPLY VOLTAGE



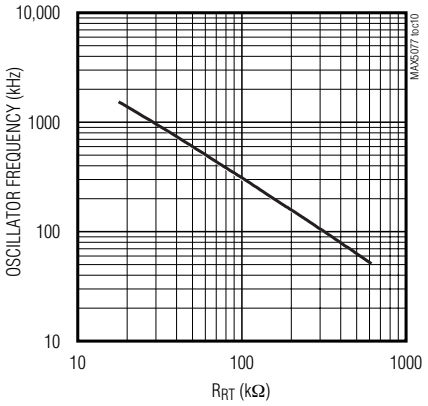
CLK FALL TIME vs. TEMPERATURE



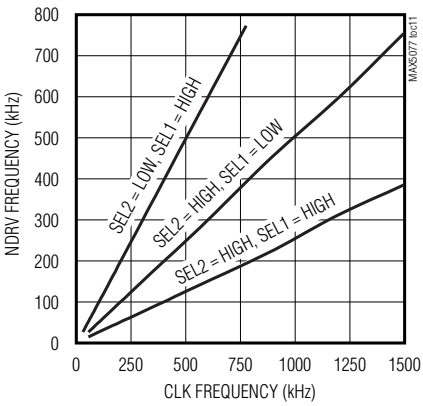
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



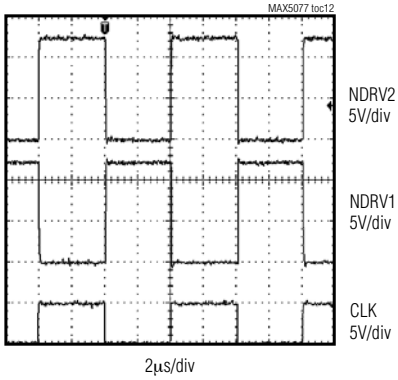
OSCILLATOR FREQUENCY vs. R_{RT}



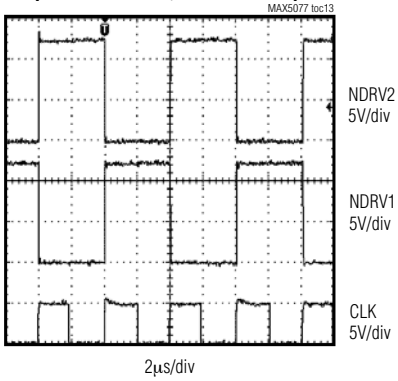
NDRV FREQUENCY vs. CLK FREQUENCY



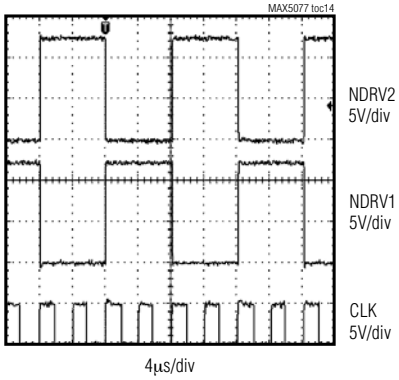
MAX5077 WAVEFORM (f_{CLK}:f_{NDRV} = 1x, R_{RT} = 124kΩ)



MAX5077 WAVEFORM (f_{CLK}:f_{NDRV} = 2x, R_{RT} = 124kΩ)



MAX5077 WAVEFORM (f_{CLK}:f_{NDRV} = 4x, R_{RT} = 124kΩ)



Pin Description

PIN	NAME	FUNCTION
1, 8	N.C.	No Connection. Must be left unconnected.
2	SEL1	CLK Frequency Ratio Select Input. Use SEL1 and SEL2 to set f_{CLK} to $f_{NDRV_}$ frequency ratio (see Table 1).
3	CLK	Synchronizing Clock Output. Clock output with a ±10mA peak current drive that can be used to synchronize an external PWM regulator. CLK/NDRV_ frequency has a 1x, 2x, or 4x ratio (see the *Synchronizing Clock Output* section).
4, 14	I.C.	Connect to ground. Internal function.
5	RT	Oscillator Timing Resistor Connection. Bypass RT with a series of a 4.7kΩ resistor and a 1nF capacitor to AGND. Connect a resistor from RT to AGND to set the internal oscillator frequency.
6	AGND	Analog Ground. Connect AGND to ground plane.
7	DGND	Digital Ground. Connect DGND to ground plane.
9	PGND	Power Ground. Connect to ground plane.
10	NDRV1	Gate Driver 1. Connect NDRV1 to the gate of an external n-channel FET.
11	NDRV2	Gate Driver 2. Connect NDRV2 to the gate of an external n-channel FET.
12	V_{CC}	Power-Supply Input. Bypass V_{CC} to PGND with 0.1µFll1µF ceramic capacitors.
13	SEL2	CLK Frequency Divisor Input. Use SEL1 and SEL2 to set f_{CLK} to $f_{NDRV_}$ frequency ratio (see Table 1).
EP	EP	Exposed Pad. Internally connected to DGND. Connect exposed pad to ground plane.

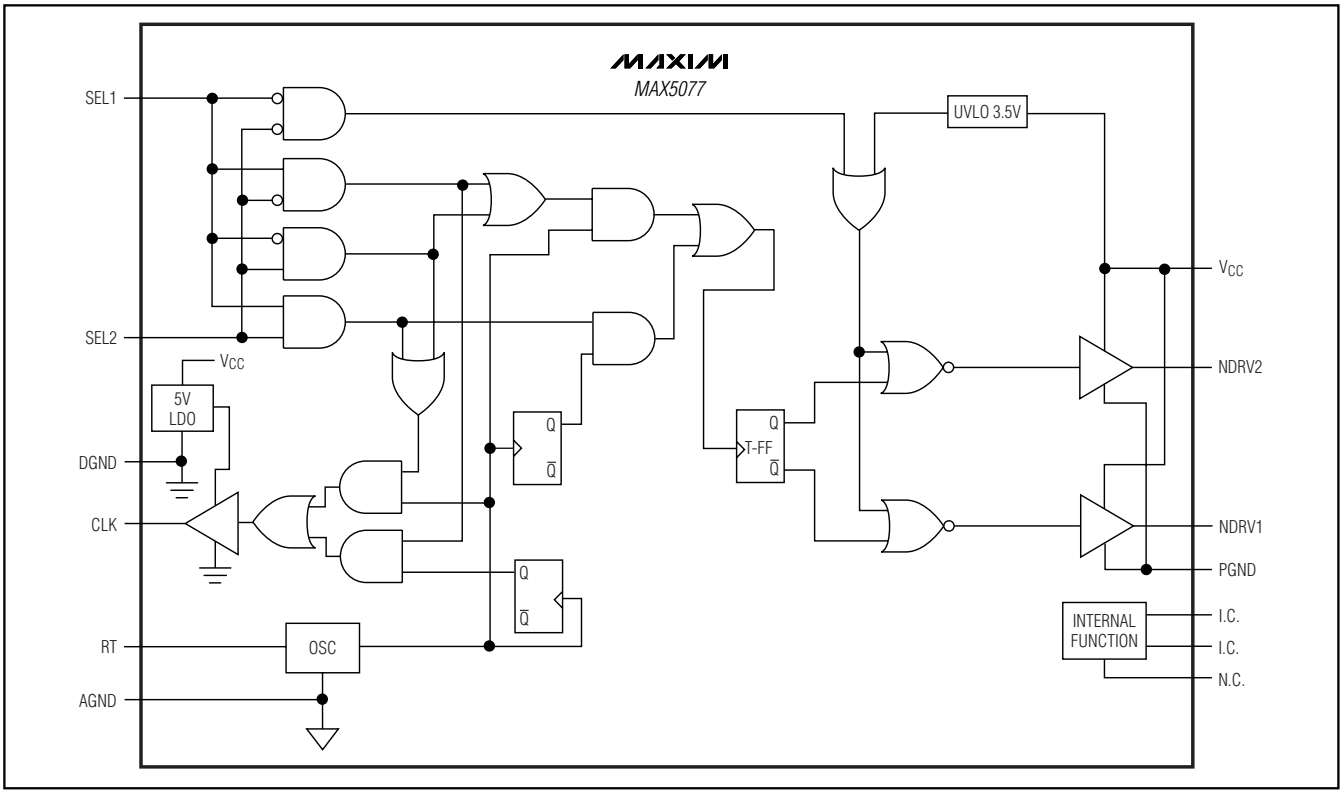


Figure 1. MAX5077 Functional Diagram

Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

Detailed Description

The MAX5077 is a +4.5V to +15V push-pull, current-fed topology driver subsystem with an integrated oscillator for use in 48V module power supplies.

The MAX5077 features a programmable accurate integrated oscillator with a synchronizing clock output that can be used to synchronize an external PWM stage. A single external resistor programs the internal oscillator frequency from 50kHz to 1.5MHz.

The MAX5077 incorporates dual MOSFET drivers with ±3A peak drive currents and a 50% duty cycle. The MOSFET drivers generate complementary signals to drive external ground-referenced n-channel MOSFETs.

The MAX5077 CLK output frequency is programmable through logic inputs that set the f_{CLK}:NDRV_ ratio to 1x, 2x, or 4x.

Internal Oscillator

An external resistor at RT programs the MAX5077's internal oscillator frequency from 50kHz to 1.5MHz. The MAX5077 NDRV1 and NDRV2 switching frequencies are one-half or one-fourth the programmed oscillator frequency with a nominal 50% duty cycle.

Use the following formula to calculate the internal oscillator frequency:

$$f_{OSC} = \frac{10^{12}}{32 \times R_{RT}}$$

where f_{OSC} is the oscillator frequency and R_{RT} is a resistor connected from RT to AGND in ohms.

Place a series combination of a 4.7kΩ resistor and a 1nF capacitor from RT to AGND for stability and to filter out noise.

When the f_{CLK}:$f_{NDRV_}$ ratio is set to 4, the NDRV1 and NDRV2 switching frequency is limited to one-fourth f_{OSC}. When operating the MAX5077 with the f_{CLK}:$f_{NDRV_}$ ratios set to 1 or 2 (see the *Synchronizing Clock Output* section), the NDRV1 and NDRV2 switching frequency is set to one-half f_{OSC}.

Synchronizing Clock Output

The MAX5077 provides a buffered clock output that can be used to synchronize the oscillator input of a PWM controller. CLK is powered from an internal 5V regulator and sources/sinks up to 10mA. Two logic inputs (SEL2, SEL1) select CLK output frequency to 1x, 2x, or 4x with respect to NDRV1 and NDRV2 switching frequency (see Table 1 and Figure 2). Drive SEL2 and SEL1 low to disable NDRV1, NDRV2, and CLK outputs. There is a typical 30ns delay from CLK to NDRV_ output.

Table 1. CLK Output Frequency Selection

SEL2	SEL1	f_{CLK}	$f_{NRDV_}$	f_{CLK} to f_{NDRV} RATIO
Low	Low	NDRV1, NDRV2, and CLK disabled		
Low	High	f_{OSC} / 2	f_{OSC} / 2	1
High	Low	f_{OSC}	f_{OSC} / 2	2
High	High	f_{OSC}	f_{OSC} / 4	4

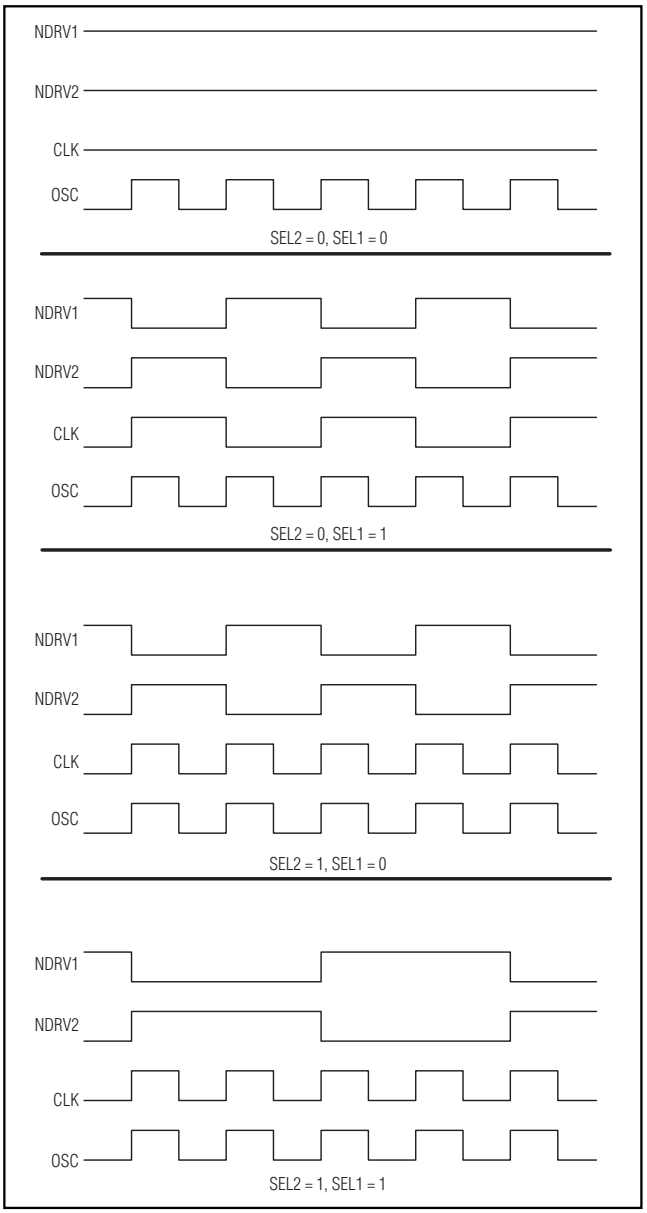


Figure 2. MAX5077 CLK Timing Diagram

Applications Information

Supply Bypassing

Pay careful attention to bypassing and grounding the MAX5077. Peak supply and output currents may exceed 3A when driving large MOSFETs. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same ground-return path. Any series inductance in the V_{CC}, NDRV1, NDRV2, and/or GND paths can cause noise due to the very high di/dt when switching the MAX5077 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{CC} to PGND. Use a ground plane to minimize ground-return resistance and inductance. Place the external MOSFETs as close as possible to the MAX5077 to further minimize board inductance and AC path impedance.

Power Dissipation

Power dissipation of the MAX5077 is a function of the sum of the quiescent current and the output current (either capacitive or resistive load). Maintain the sum of the currents so the maximum power dissipation limit is not exceeded. The power dissipation (P_{DISS}) due to the quiescent switching supply current (I_{CCSW}) can be calculated as:

$$P_{DISS} = V_{CC} \times I_{CCSW}$$

For capacitive loads, use the following equation to estimate the power dissipation:

$$P_{LOAD} = 2 \times C_{LOAD} \times V_{CC}^2 \times f_{NDRV_}$$

where C_{LOAD} is the capacitive load at NDRV1 and NDRV2, V_{CC} is the supply voltage, and $f_{NDRV_}$ is the MAX5077 NDRV_ switching frequency.

Calculate the total power dissipation (P_T) as follows:

$$P_T = P_{DISS} + P_{LOAD}$$

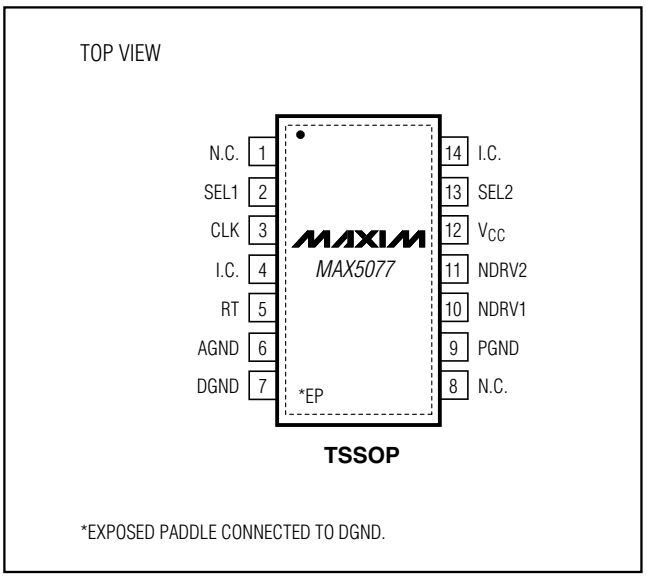
Layout Recommendations

The MAX5077 drivers source and sink large currents that can create very fast rise and fall edges at the gate of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5077:

- Place one or more 0.1µF decoupling ceramic capacitors from V_{CC} to PGND as close to the device as possible. Connect V_{CC} and all ground pins to large copper areas. Place one bulk capacitor of 10µF on the PC board with a low-impedance path to the V_{CC} input and PGND of the MAX5077.
- Two AC current loops form between the device and the gates of the driven MOSFETs. The MOSFET looks like a large capacitance from gate to source when the gate pulls low. The current loop is from the MOSFET gate to NDRV1/NDRV2 of the MAX5077, to PGND, and to the source of the MOSFETs. When the gate of the MOSFET is pulled high, the current is from the V_{CC} terminal of the decoupling capacitor, to V_{CC} of the MAX5077, to NDRV1/NDRV2, to the MOSFET gate and source. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.

Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1335

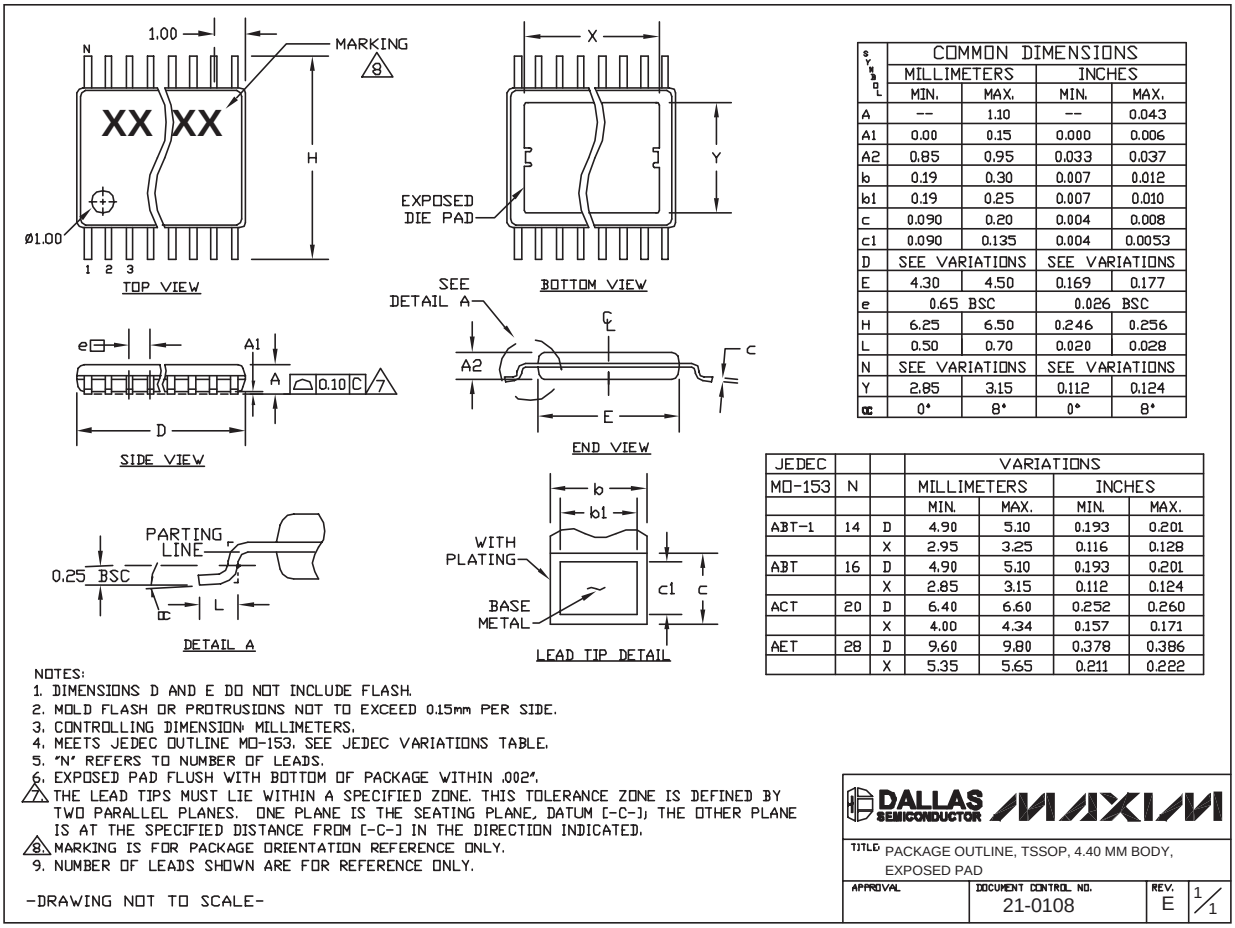
PROCESS: BiCMOS

Push-Pull FET Driver with Integrated Oscillator and Programmable Clock Output

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	E	1/1

Revision History

Pages changed at Rev 1: 1, 2, 5, 6, 9

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