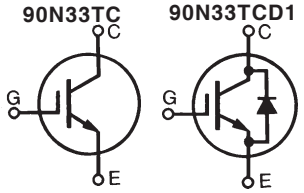
IXYS

Trench Gate, High Speed, IGBTs

IXGA90N33TC
IXGQ90N33TC
IXGQ90N33TCD1

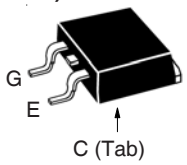
V_{CES} = 330V
I_{CP} = 360A
$V_{CE(sat)}$ ≤ 1.80V

For PDP Applications

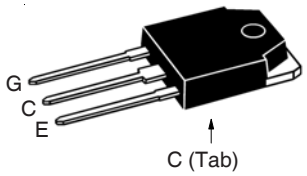


Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	330	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C= 25°C (Chip Capability)	90	A
$I_{C(RMS)}$	Lead Current Limit	75	A
I_{C110}	T_C = 110°C	38	A
I_{CP}	T_C ≤ 150°C, tp ≤ 10µs	60	A
I_{CP}	T_C ≤ 150°C, tp ≤ 10µs, Duty cycle ≤ 1%	360	A
P_C	T_C = 25°C	200	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque (TO-3P)	1.13/10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-3P	5.5	g

TO-263 AA (IXGA)



TO-3P (IXGQ)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250µA, V_{GE} = 0V	330			V
$V_{GE(th)}$	I_C = 250µA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			1	µA
	T_J = 125°C			200	µA
I_{GES}	V_{CE} = 0V, V_{GE} = ±20V			±200	nA
$V_{CE(sat)}$	V_{GE} = 15V, I_C = 20A, Note 1			1.40	V
	I_C = 45A		1.54	1.80	V
	T_J = 125°C		1.54		V
	I_C = 90A		1.82		V
	T_J = 125°C		1.95		V

Features

- Low $V_{CE(sat)}$
  - for minimum On-State Conduction Losses
- Fast Switching

Applications

- PDP Screen Drivers

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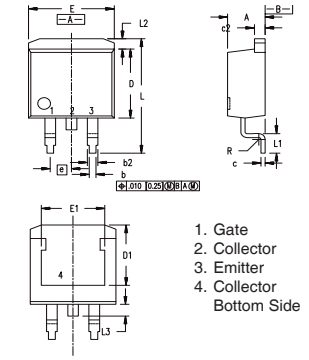
Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 45A, V_{CE} = 10V, Note 1	40	65		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		2320		pF
C_{oes}			180		pF
C_{res}			21		pF
Q_g	I_C = 45A, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		69		nC
Q_{ge}			15		nC
Q_{gc}			13		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		13		ns
t_r	I_C = 45A, V_{GE} = 15V		30		ns
$t_{d(off)}$	V_{CE} = 240V, R_G = 5Ω		38		ns
t_f			49		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		13		ns
t_r	I_C = 45A, V_{GE} = 15V		28		ns
$t_{d(off)}$	V_{CE} = 240V, R_G = 5Ω		50		ns
t_f			74		ns
R_{thJC}				0.62	°C/W
R_{thCS}	TO-3P		0.21		°C/W

Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	I_F = 20A, V_{GE} = 0V, Note 1			2.0	V
R_{thJC}				2.5	°C/W

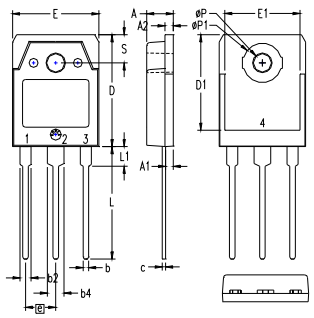
Note: 1. Pulse test, t ≤ 300µs, duty cycle, d ≤ 2%.

TO-263 Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.06	4.83	.160	.190
b	0.51	0.99	.020	.039
b2	1.14	1.40	.045	.055
c	0.40	0.74	.016	.029
c2	1.14	1.40	.045	.055
D	8.64	9.65	.340	.380
D1	8.00	8.89	.280	.320
E	9.65	10.41	.380	.405
E1	6.22	8.13	.270	.320
e	2.54	BSC	.100	BSC
L	14.61	15.88	.575	.625
L1	2.29	2.79	.090	.110
L2	1.02	1.40	.040	.055
L3	1.27	1.78	.050	.070
L4	0	0.13	0	.005

TO-3P Outline



1 = Gate 2,4 = Collector
3 = Emitter

SYM	INCHES MIN	MAX	MILLIMETERS MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
øP	.126	.134	3.20	3.40
øP1	.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25ºC

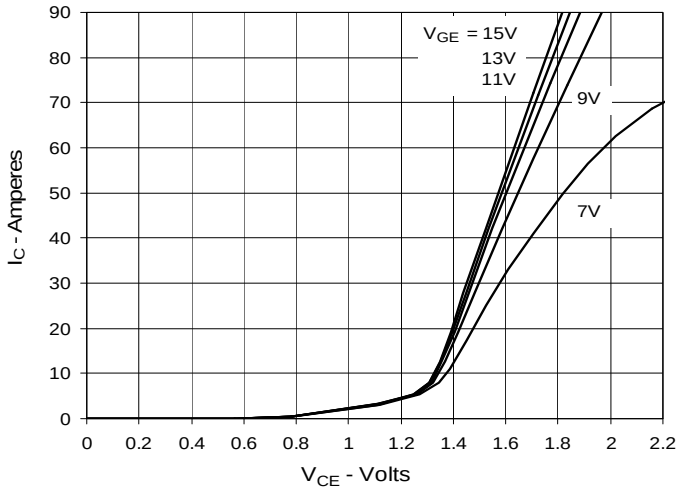


Fig. 2. Extended Output Characteristics @ 25ºC

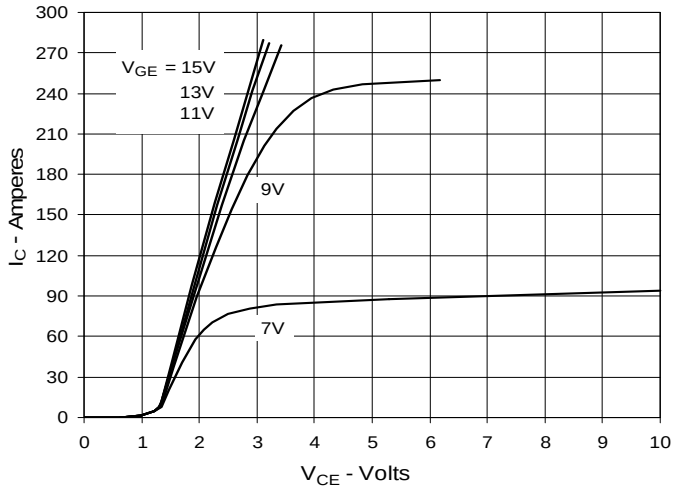


Fig. 3. Output Characteristics @ 125ºC

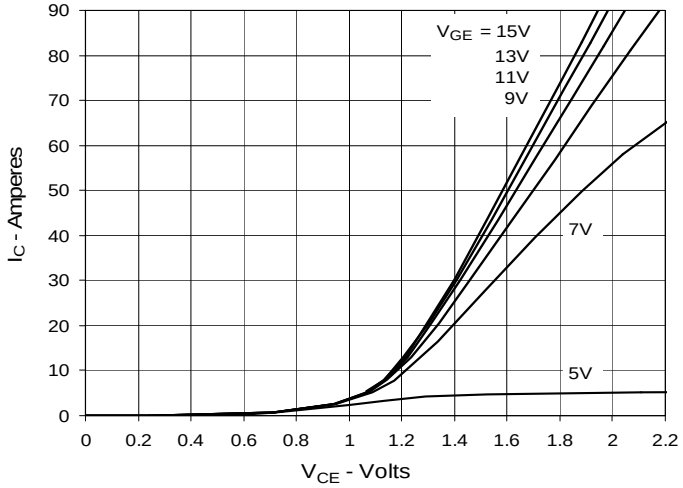


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

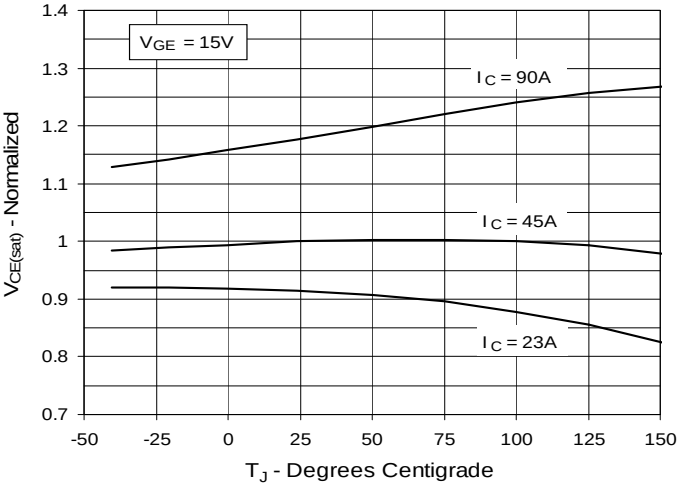


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

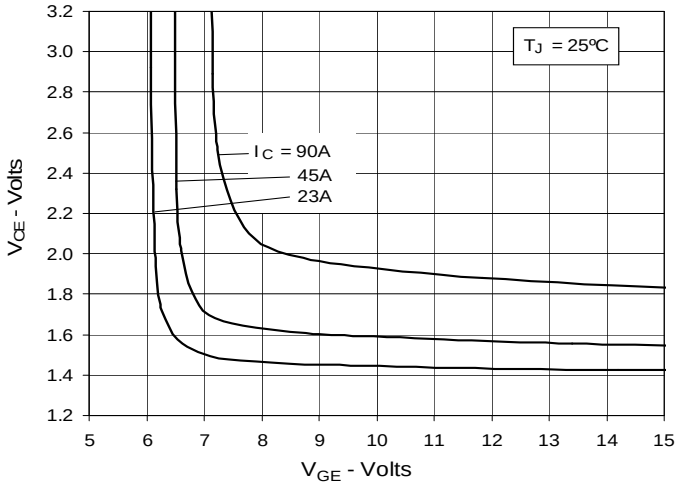
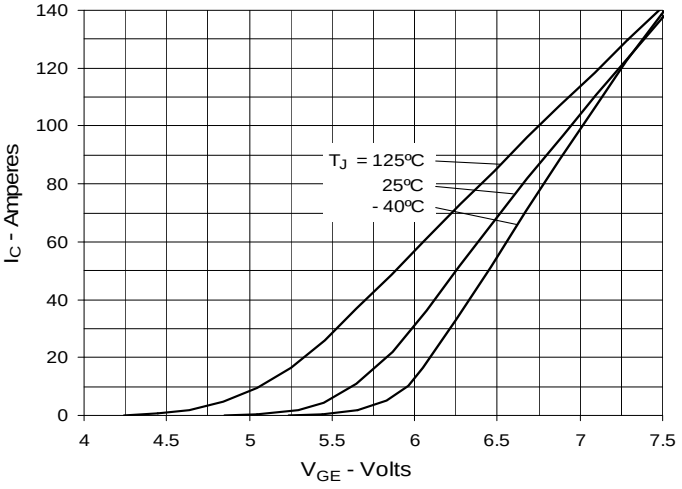


Fig. 6. Input Admittance



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Fig. 7. Transconductance

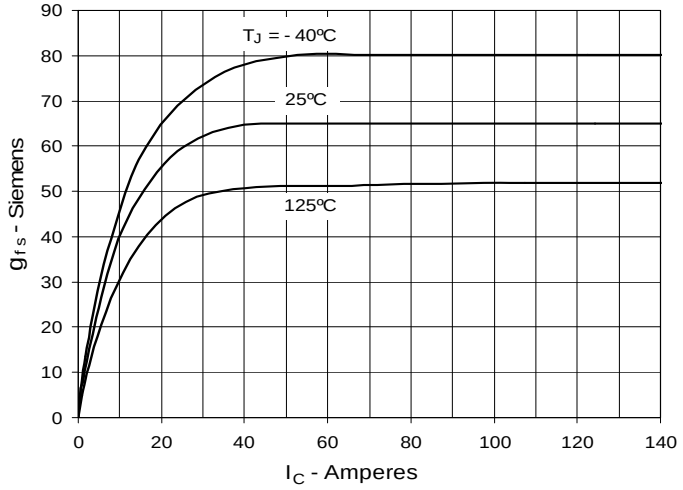


Fig. 8. Gate Charge

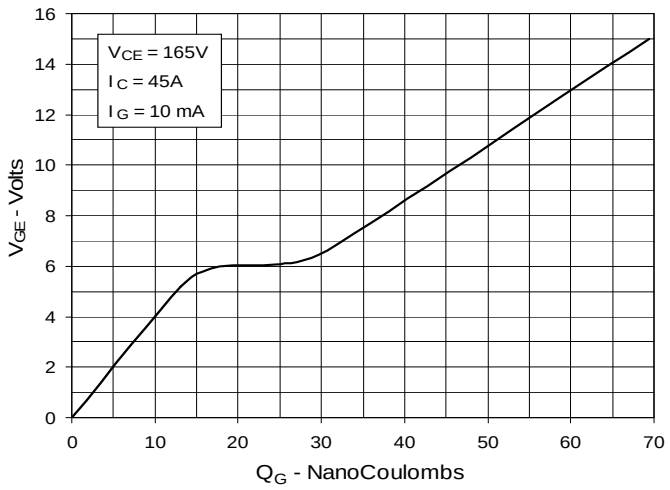


Fig. 9. Reverse-Bias Safe Operating Area

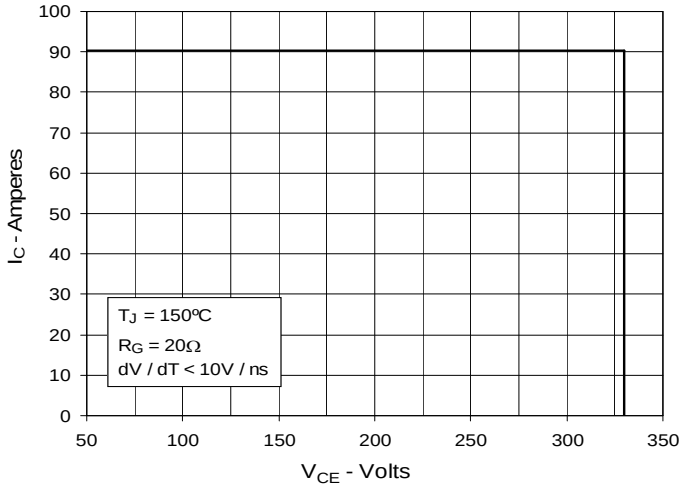


Fig. 10. Capacitance

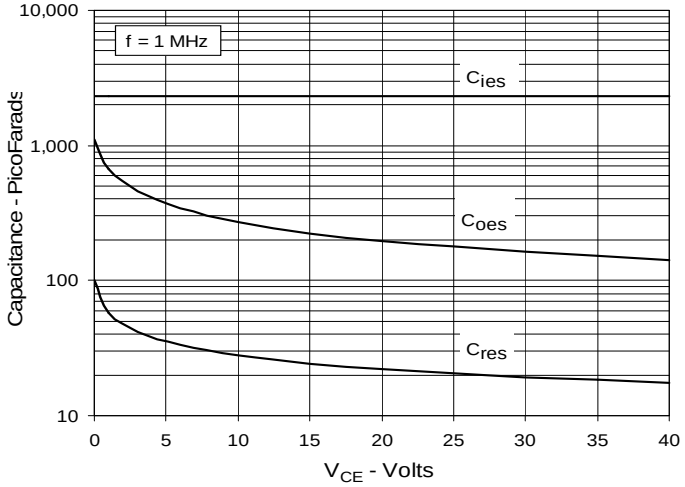


Fig. 11. Forward-Bias Safe Operating Area

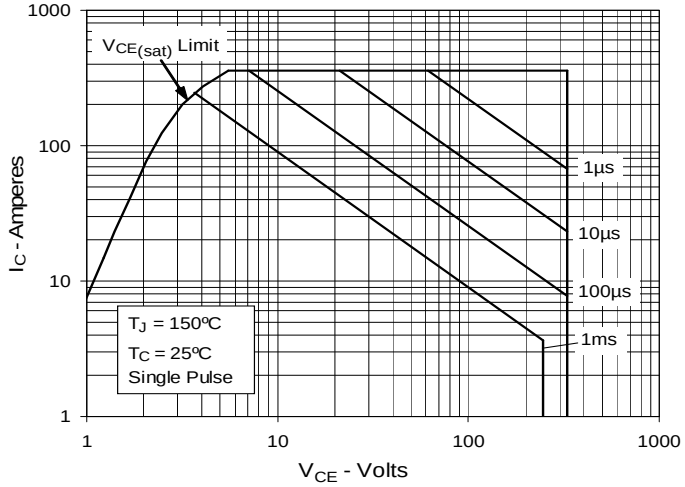


Fig. 12. Maximum Transient Thermal Impedance

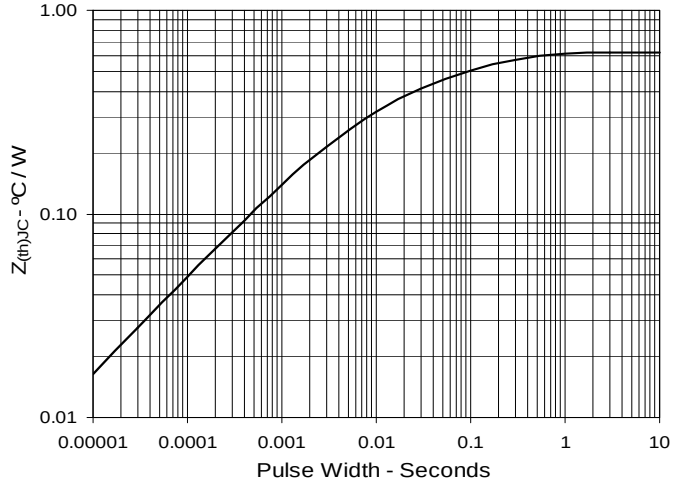


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

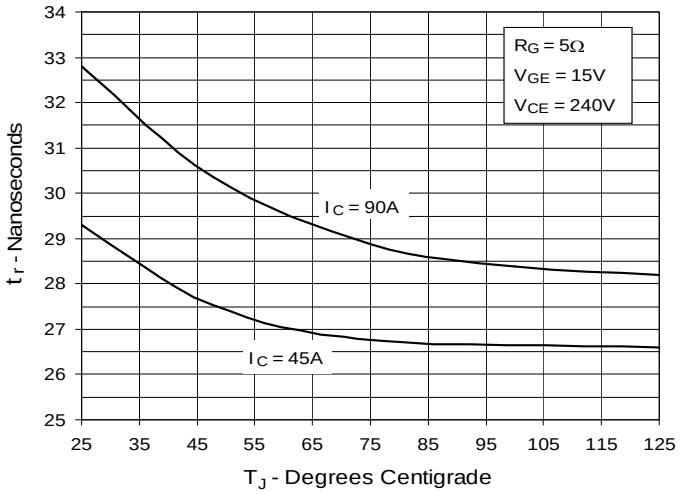


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

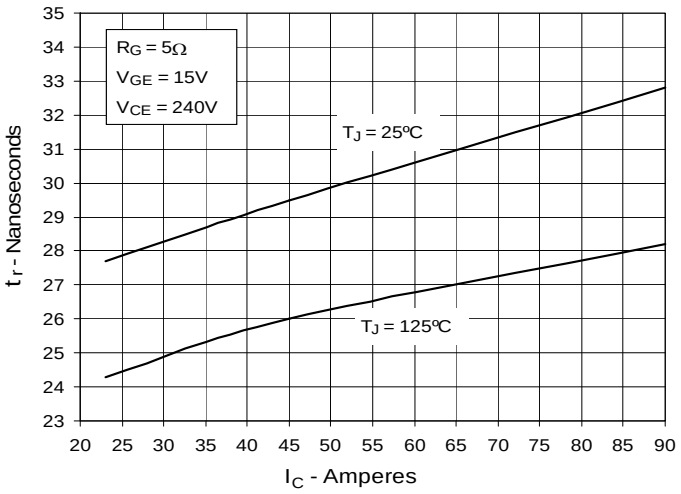


Fig. 16. Resistive Turn-on Switching Times vs. Gate Resistance

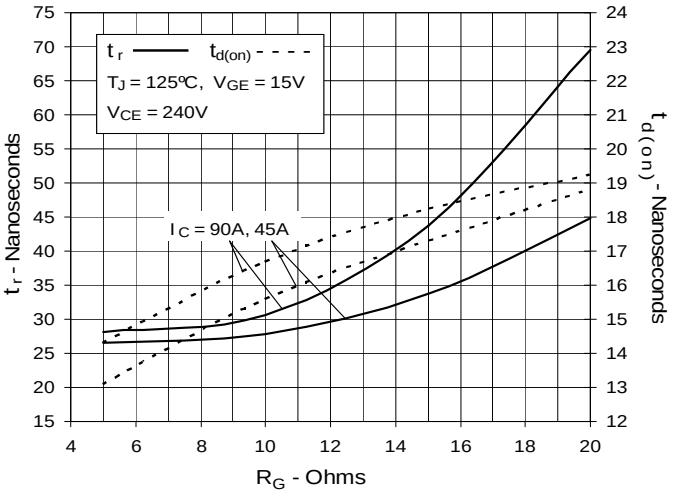


Fig. 17. Resistive Turn-off Switching Times vs. Junction Temperature

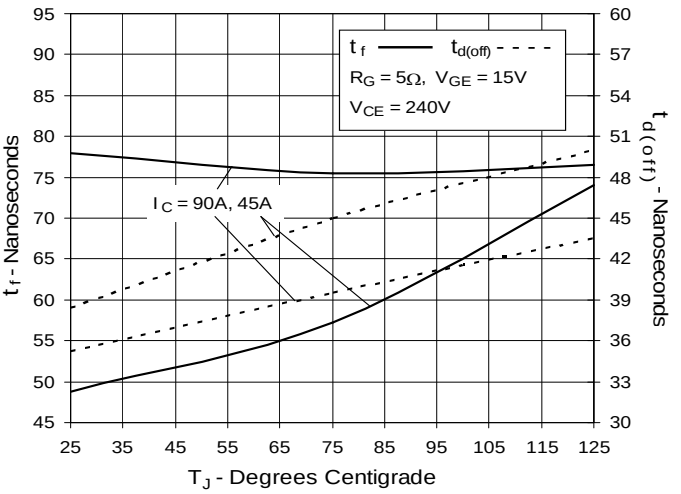


Fig. 18. Resistive Turn-off Switching Times vs. Collector Current

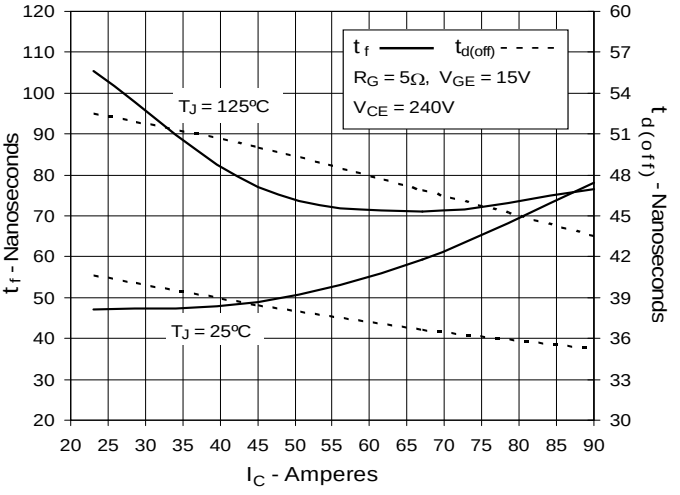
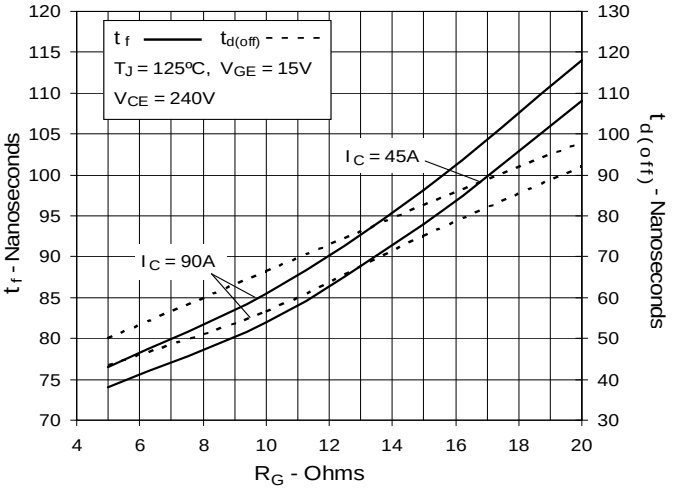


Fig. 19. Resistive Turn-off Switching Times vs. Gate Resistance



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