DP83822 EVM

User's Guide

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DP83822 EVM

This User's Guide details the characteristics, operation, and use of the DP83822 10/100 Mbps Industrial Ethernet PHY. The EVM enables Texas Instruments' customers to quickly design and market systems using the DP83822. This document also includes schematic diagrams, a printed-circuit board layout, board assembly, board marking drawings, and a bill of materials.

Table 1. Terminology

Acronym	Definition
PHY	Physical Layer Transceiver
MAC	Media Access Controller
EEE	Energy Efficient Ethernet
WoL	Wake-on-LAN
SMI	Serial Management Interface
MDIO	Management Data I/O
MDC	Management Data Clock
SFP	Small Form-Factor Pluggable (Fiber Transceiver)
MII	Media Independent Interface
RMII	Reduced Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
SFD	Start-of-Frame Detection
CAT5	Category 5 (cable electrical characteristics)
AVD	Analog Supply Rail
VDDIO	Digital Supply Rail
CT	Center Tap Supply Rail
PD	Pull-Down
PU	Pull-Up

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1 Introduction

The DP83822 EVM supports 10/100 Mbps and is compliant to the IEEE 802.3u standard. This reference design supports MII, RMII and RGMII MAC interfaces.

The DP83822 EVM includes two onboard status LEDs, optional Fiber SFP connector and cage, and onboard supply through a 5-V micro USB connector. The DP83822 EVM is capable of providing a 125-MHz, 50-MHz or 25-MHz reference clock from an onboard 25-MHz crystal. The EVM includes the CDCE925 programmable 2-PLL VCXO clock synthesizer with 1.8-V to 3.3-V LVCMOS outputs. Serial management interface, MDIO/MDC, is supported and can be used to access PHY registers for additional features. There are 4-level straps, which allow for system configurations without the need to directly access PHY registers. External power supplies can be connected to each specified voltage rail for additional system evaluation. The DP83822 supports Wake-on-LAN, Energy Efficient Ethernet (IEEE802.3az), Start-of-Frame Detect IEEE 1588 Time Stamp, and configurable I/O voltages.

Key Features:

- IEEE 802.3u Compliant: 100BASE-FX, 100BASE-TX and 10BASE-Te
- CDCE925 Programmable 2-PLL VCXO Clock Synthesizer with 1.8 V to 3.3 V
- MII, RMII and RGMII MAC interfaces
- SFD IEEE 1588 Time Stamp
- Two status LEDs
  - LED LINK/ACTIVITY
  - LED SPEED
- Low Power Modes
  - Energy Efficient Ethernet (IEEE802.3az)
  - Wake-on-LAN
  - Active Sleep
  - Passive Sleep
  - IEEE Power Down
  - Deep Power Down
- Variable I/O voltage range: 1.8 V, 2.5 V and 3.3 V
- 100BASE-TX error free data transfer over 150 meters on CAT5 cable

The DP83822 EVM has an RJ45 connector (J12) with discrete magnetics and stuffing resistor array for configurable bootstraps. Customers are encouraged to use a design similar to the EVM circuit to expedite their product development.

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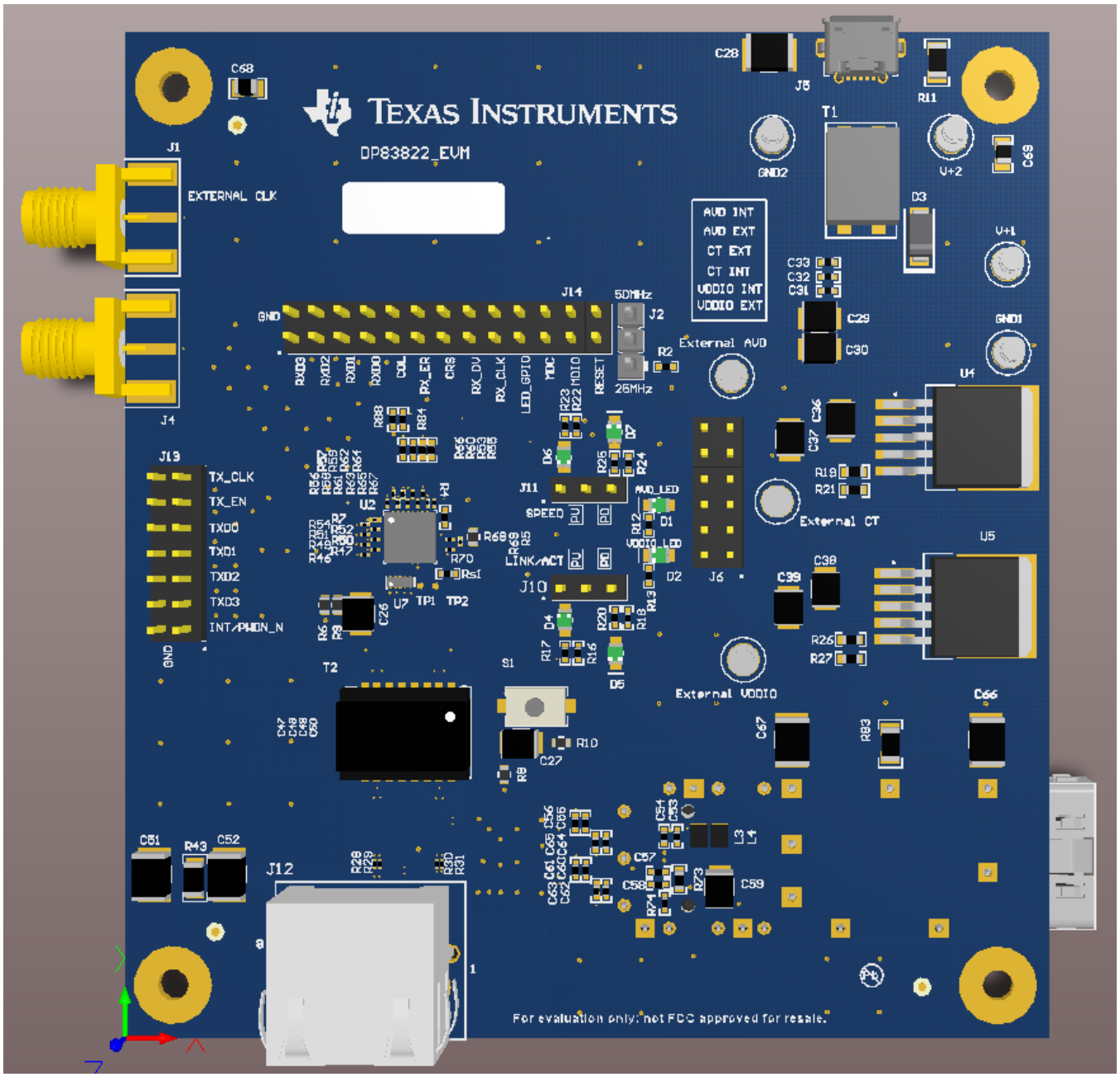


Figure 1. DP83822 EVM – Top Side

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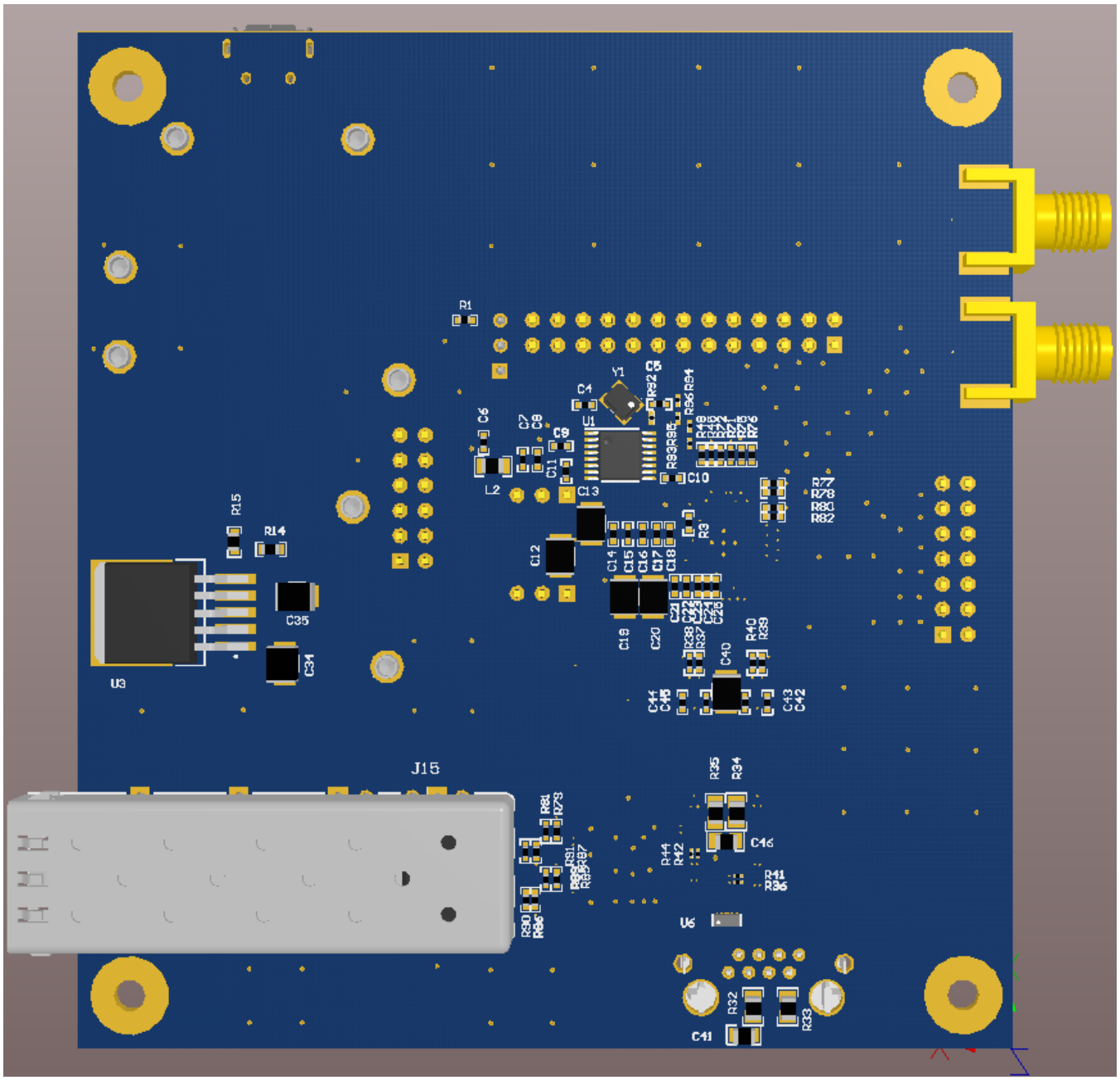


Figure 2. DP83822 EVM - Bottom Side

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1.1 Operation – Quick Setup

1. Select internal supply by populating the following with jumpers (J6):
   (a) Place jumper #1 at 'AVD INT' position
   (b) Place jumper #2 at 'CT INT' position
   (c) Place jumper #3 at 'VDDIO INT' position

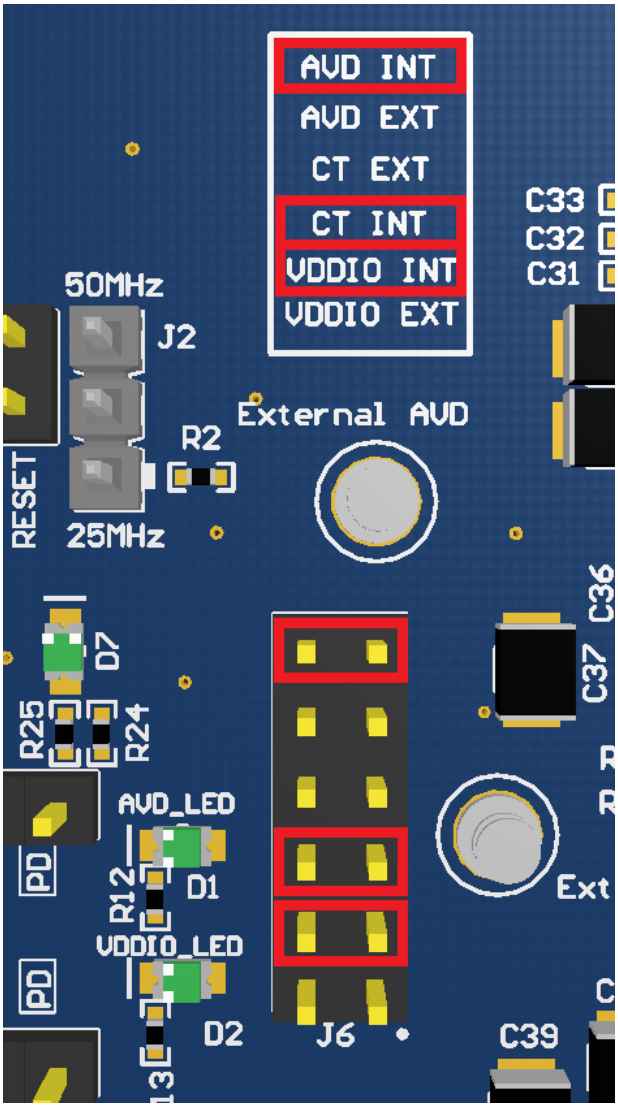


Figure 3. On-Board Power Supply Configuration

2. Select VDDIO voltage level (R26):
   - 4.22 kΩ - 3.3 V operation (Default)
   - 2.56 kΩ - 2.5 V operation
   - 1.20 kΩ - 1.8 V operation
3. Select AVD voltage level (R19):
   - 4.22 kΩ - 3.3 V operation (Default)
   - 1.20 kΩ - 1.8 V operation

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4. Select reference clock frequency (J2):
   - 25 MHz – jumper across pins 1 and 2
   - 50 MHz – jumper across pins 2 and 3

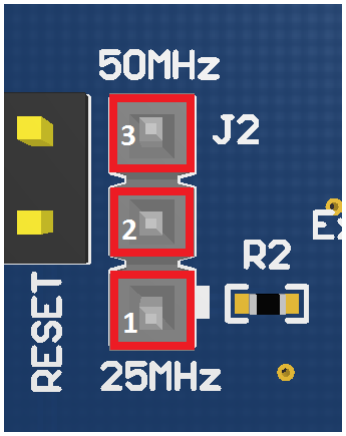


Figure 4. Reference Clock Selection

5. Place a jumper in the 'PU' position for LED LINK/ACT (J10)

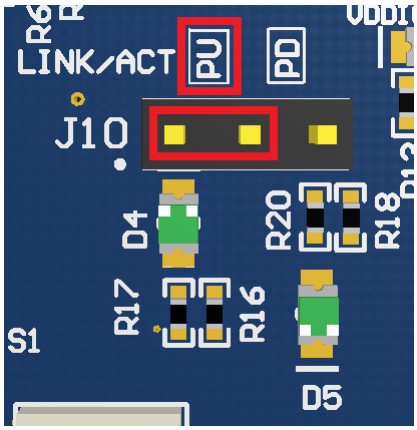


Figure 5. LED LINK/ACT Selection

6. Turn ON the PHY by connecting a 5-V micro USB power supply to J5
7. Plug a CAT5, CAT5E or CAT6 cable into the RJ45 connector (J12)
8. Connect the far-end of the Ethernet cable to a link partner
9. Connect a MAC interface to J13 and J14

- LED Indication
  - The AVD LED (D1) and VDDIO LED (D2) will be illuminated if the 5-V supply is connected
  - Look for the LINK LED (D4) to light up on the DP83822 EVM after the PHY links with a connected partner

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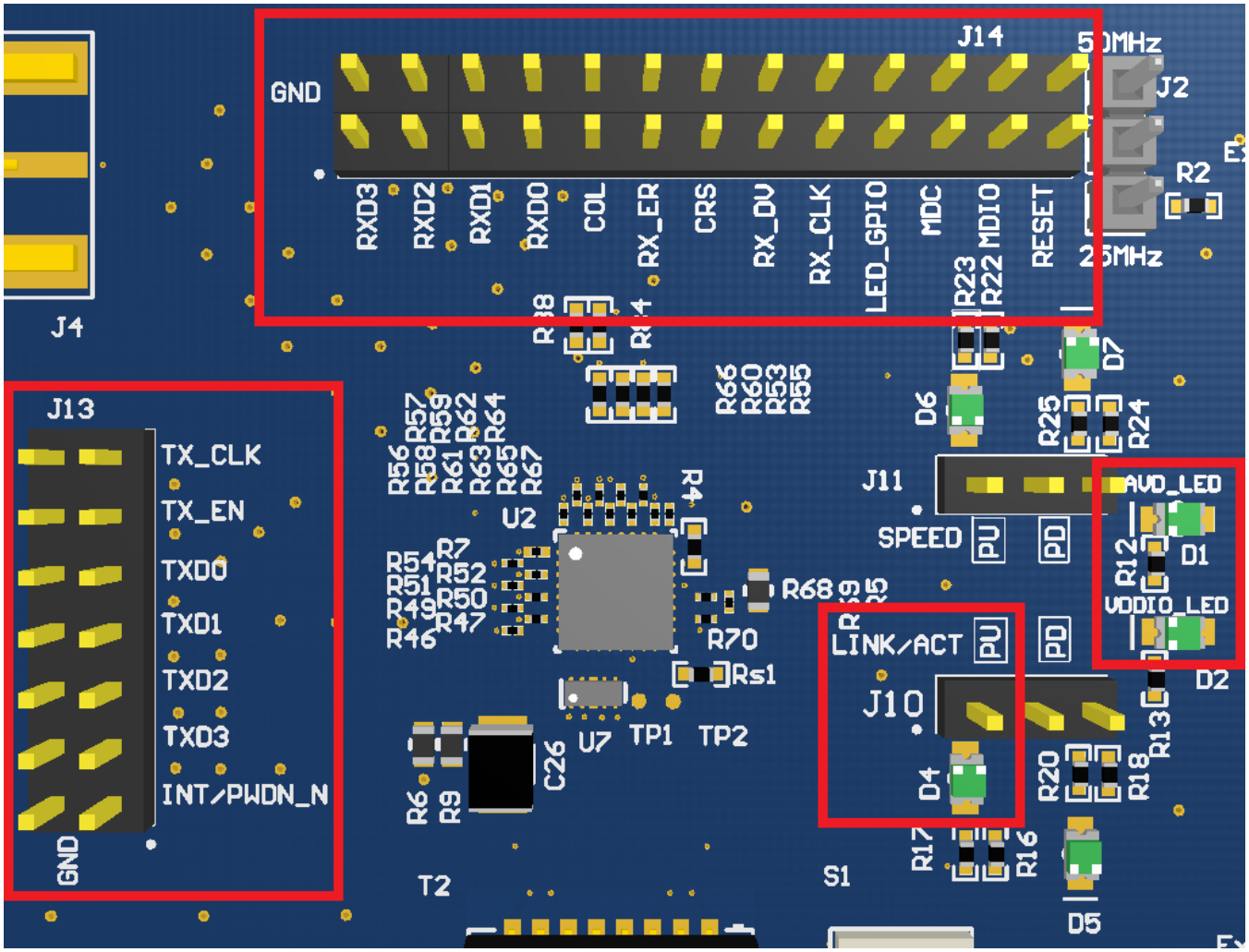


Figure 6. MAC IF Connection and LED Indication

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2 Board Setup Details

2.1 Block Diagram

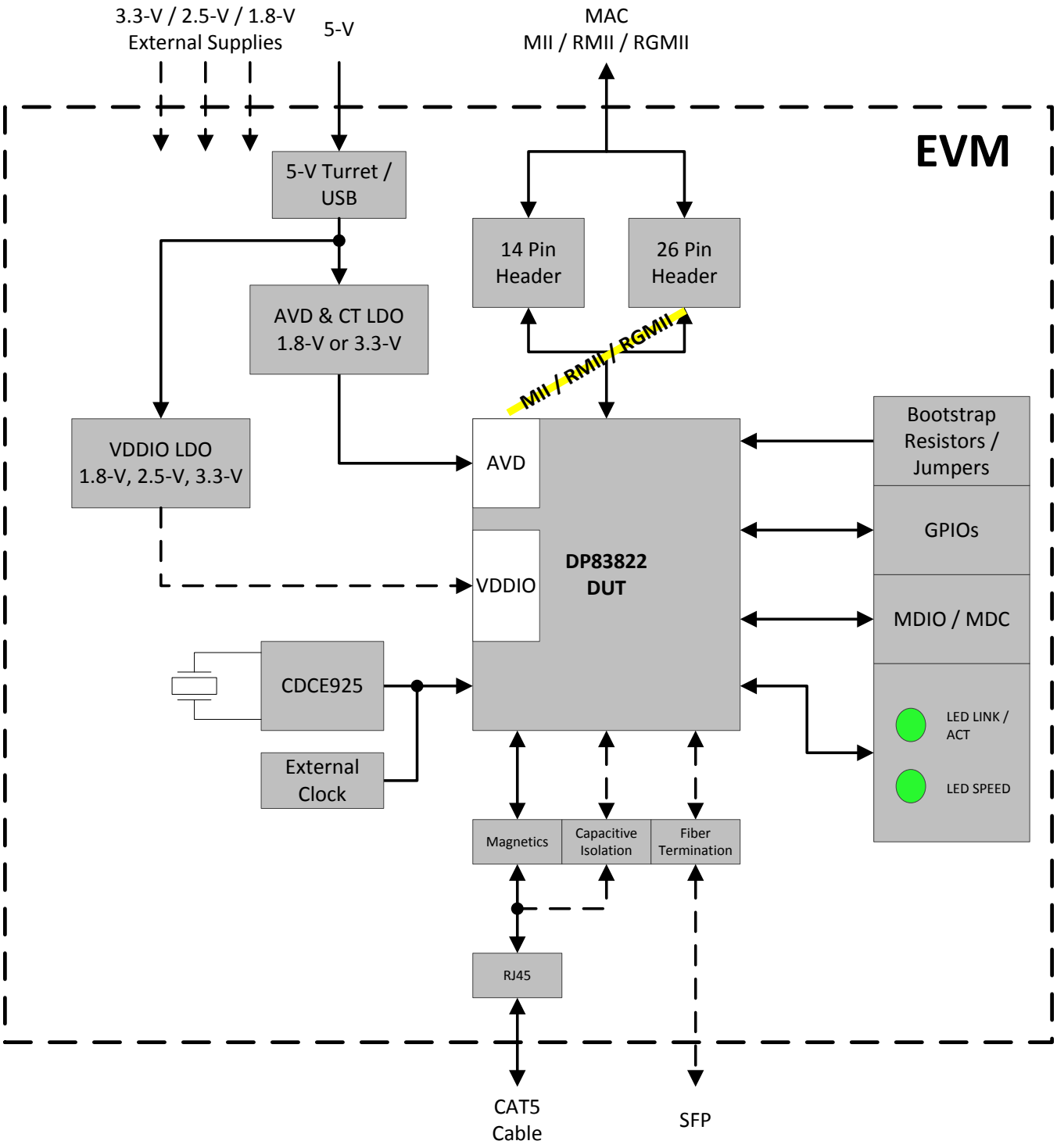


Figure 7. DP83822 EVM Block Diagram

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2.2 Power Supply Options

The DP83822 EVM power is supplied by a single 5-V connection. This option uses onboard LDOs to provide 3.3-V, 2.5-V or 1.8-V rails. Connect 5-V supply to either the USB micro A/B connector (J5) or V+1 turret and populate jumpers on J6 as specified in Section 1.1 for onboard supplies. When using the V+1 turret, GND1 turret should be used as the ground connection.

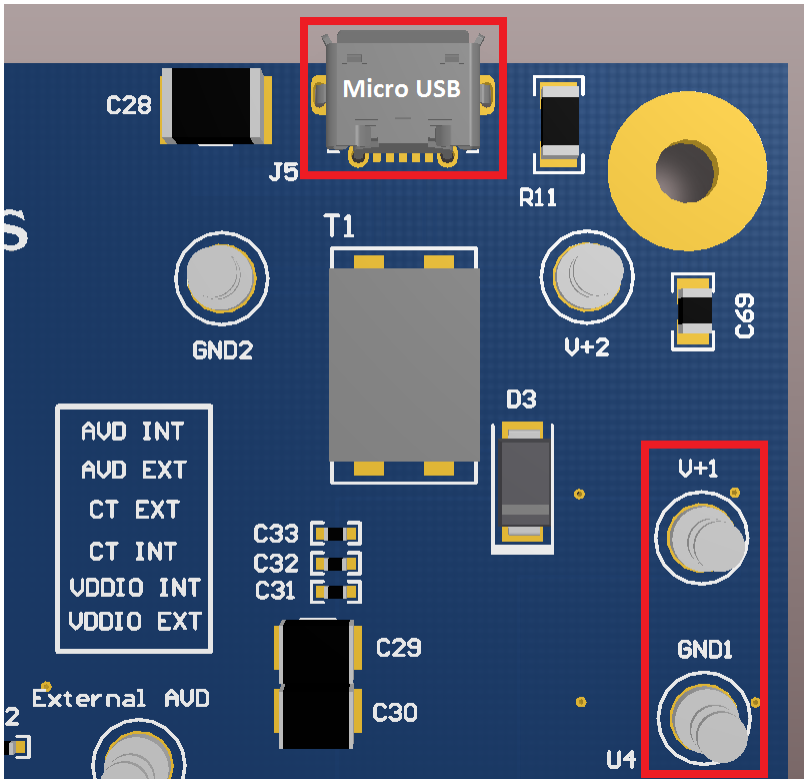


Figure 8. Onboard Supply Connection

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The DP83822 EVM also supports external supply connections. External supply option bypasses the onboard LDOs and allows for direct connections to each supply rail.

To configure the DP83822 EVM for external supply operation, use the following jumper configuration (J6):

- Place jumper #1 at 'AVD EXT' position
- Place jumper #2 at 'CT EXT' position
- Place jumper #3 at 'VDDIO EXT' position

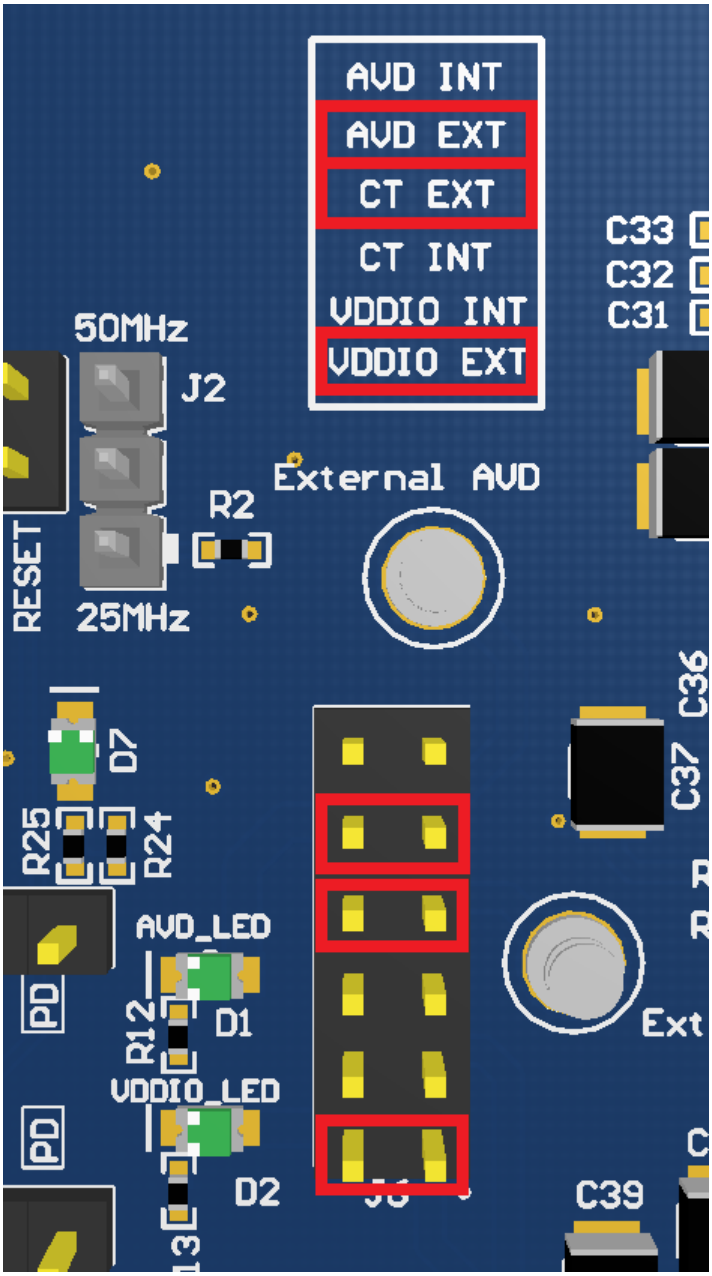


Figure 9. External Supply Configuration

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There are three supply rail turrets for external supply connection. The three turrets are shown in the image below. 'GND1' should be used as the ground connection for each of the three supply rails.

- 'External AVD' – External AVD supply rail
- 'External CT' – External Center Tap supply rail
- 'External VDDIO' – External VDDIO supply rail

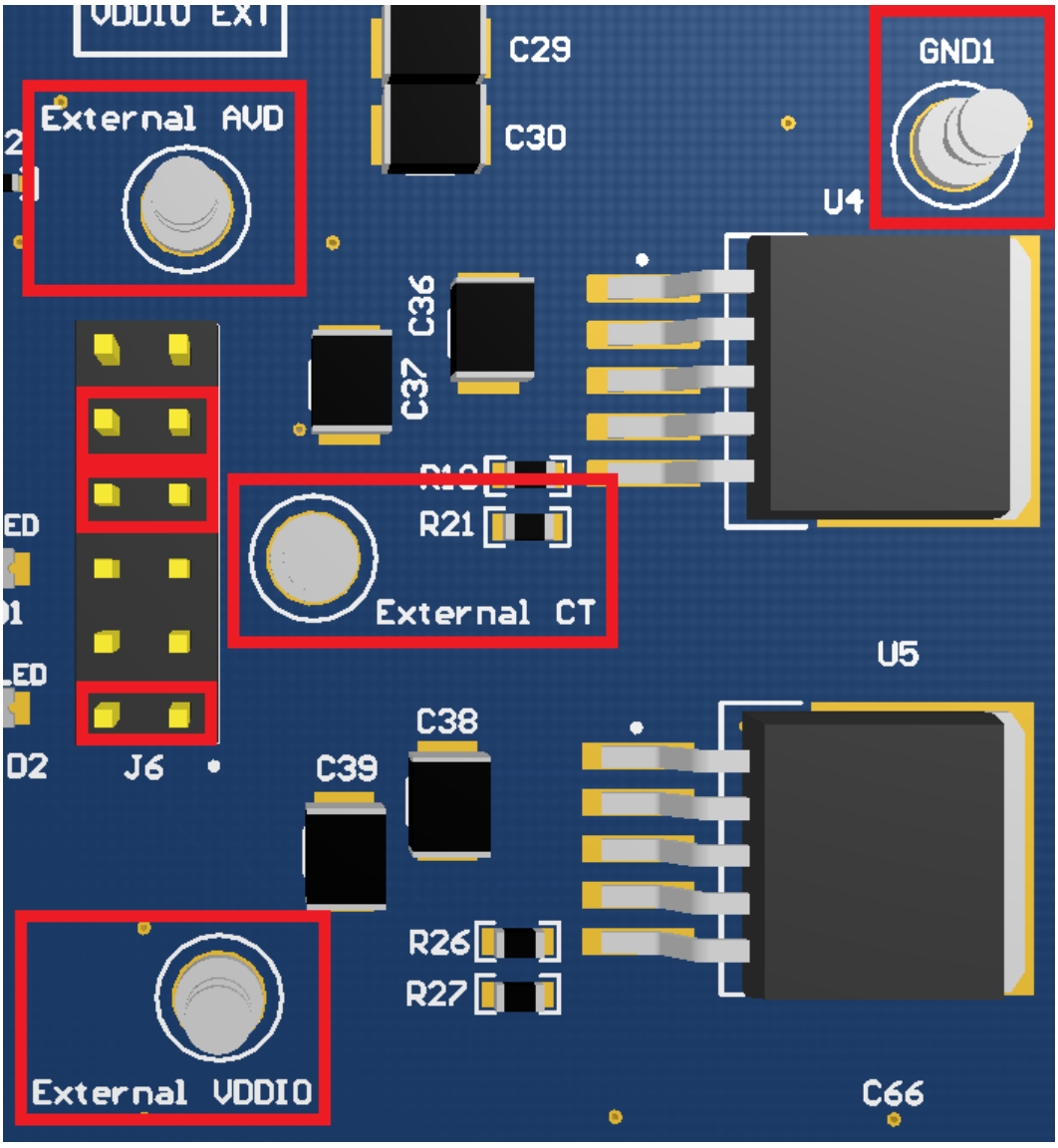


Figure 10. External Turret Connection

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2.3 Serial Management and MAC Interfaces

The DP83822 EVM supports SMI (MDIO/MDC) and MII, RMII and RGMII MAC interfaces. SMI is accessible though J14. MDIO is located at pin 23 and MDC is located at pin 21. Ground connection between the DP83822 EVM and SMI controller is required for proper operation. DP83822 supports both clause 22 and clause 45 in the IEEE 802.3 specification. **For further SMI support please refer to the Ethernet USB2MDIO Application Note for interfacing the MSP430 Launchpad with TI Ethernet PHYs.**

Note: The default PHY_ID is '1'. PHY_ID can be changed via bootstrap options found in the datasheet.

MAC interface pins are located on J13 and J14. MII, RMII and RGMII configurations are located in the datasheet and can be configured by bootstrapping or direct register access through the SMI. Please refer to the DP83822 datasheet for specific pin requirements for each MAC interface.

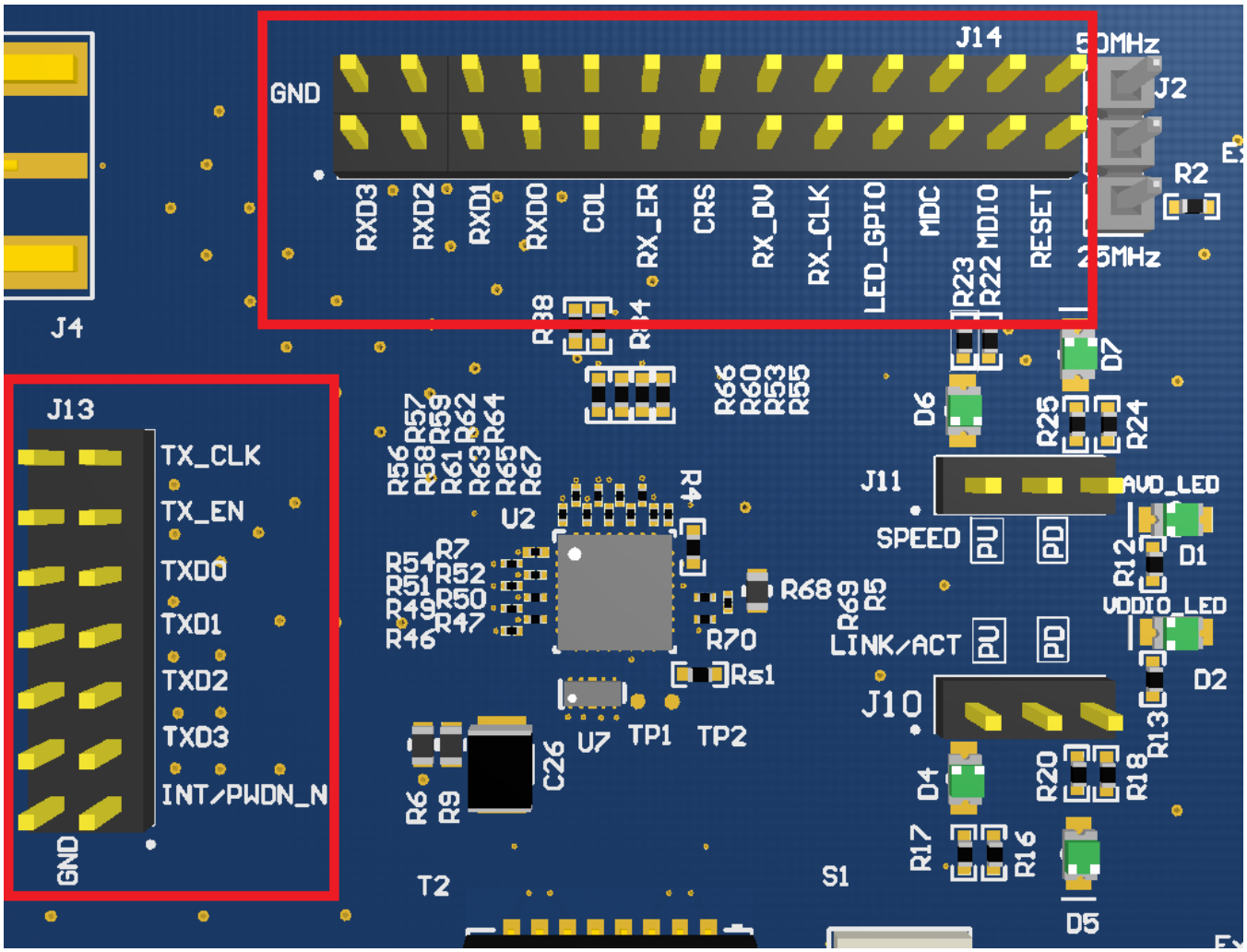


Figure 11. DP83822 EVM MAC IF Connections

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2.4 LED Options

The DP83822 supports up to three configurable LEDs: Link, Speed and MLED. The DP83822 EVM has two onboard LEDs that can be controlled by direct register access using the SMI. LED pins can operate as either current sources (when connected to pull-down) or current sinks (when connected to pull-up).

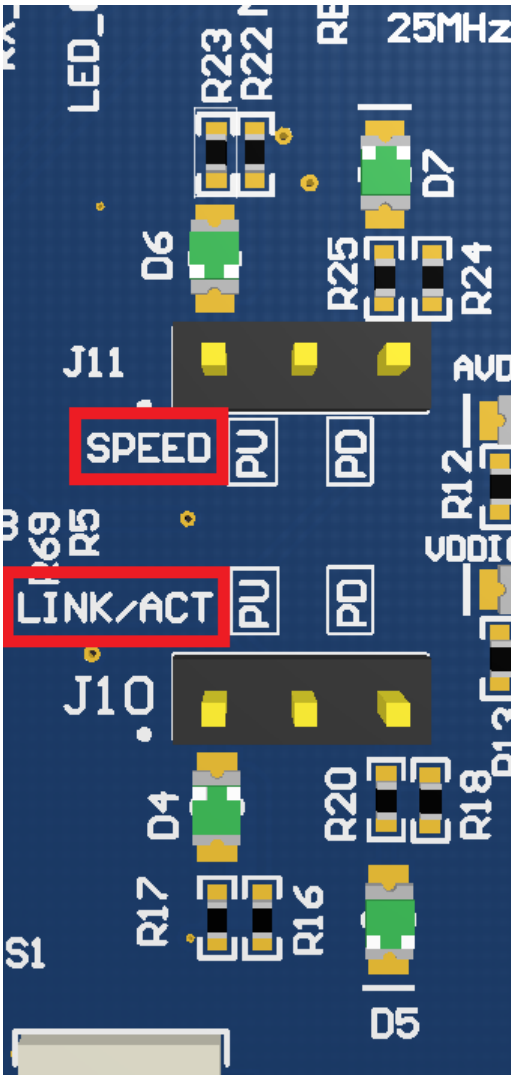


Figure 12. LED Speed and Link

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2.5 Bootstrap Options/Jumpers

Some DP83822 configurations can be done through bootstrap options. Options can be selected with jumpers or resistor population. Please refer to the datasheet for bootstrap options and schematic/layout sections of this User's Guide for resistor locations.

Table 2. Bootstrap Resistor Designation and Suggested Bootstrap Resistor Values

Pin Name	Pin Number	Strap Mode	PU Resistor (kΩ)	PU Resistor Designation	PD Resistor (kΩ)	PD Resistor Designation
COL	29	1	OPEN	R84	1.96	R88
		2	13		1.96	
		3	6.2		1.96	
		4	OPEN		OPEN	
RX_D0	30	1	OPEN	R71	OPEN	R72
		2	10		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_D1	31	1	OPEN	R75	OPEN	R76
		2	10		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_D2	32	1	OPEN	R77	OPEN	R78
		2	10		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_D3	1	1	OPEN	R80	OPEN	R82
		2	10		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
CRS	27	1	OPEN	R53	1.96	R55
		2	13		1.96	
		3	6.2		1.96	
		4	OPEN		OPEN	
RX_ER	28	1	OPEN	R60	1.96	R66
		2	13		1.96	
		3	6.2		1.96	
		4	OPEN		OPEN	
RX_DV	26	1	OPEN	R45	OPEN	R48
		2	10		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	

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2.6 Clock Options

The DP83822 EVM uses the CDCE925 programmable 2-PLL VCXO clock synthesizer. A 25-MHz crystal resonator is connected to the CDCE925, which can then be configured to either a 50-MHz or 25-MHz LVCMOS output in the range of 1.8 V to 3.3 V. The output of the CDCE925 is directly fed into the XI pin of the DP83822.

In order to operate with a 25-MHz reference clock, the following modifications are required:

- Populate R3 with a 0-Ω resistor
- Populate R95 and R96 with 1-kΩ resistors
- Remove R4
- Place a jumper across pin 1 and pin 2 on J2

In order to operate with a 50-MHz reference clock, the following modifications are required:

- Populate R3 with a 0-Ω resistor
- Populate R95 and R96 with 1-kΩ resistors
- Remove R4
- Place a jumper across pin 2 and pin 3 on J2

Table 3. CDCE925 Programmed Clock Setting Selection

S2	S1	S0	Reference Clock Setting
0	0	0	25 MHz
0	0	1	50 MHz

2.6.1 External Configuration

Additionally, the DP83822 EVM has an external reference clock option through an SMA (J1).

The external clock must meet the DP83822 data sheet requirements and to be within 50 MHz or 25 MHz with ±50ppm tolerance.

The following changes are required to route an external clock to the DP83822:

- Populate R4 with a 0-Ω resistor
- Populate an SMA at J1
- Remove R3

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2.7 100BASE-FX Configuration (Fiber)

The DP83822 EVM supports 100BASE-FX by use of an SFP transceiver. The DP83822 can be configured for 100BASE-FX operation through either bootstrap or SMI register configuration.

To configure the DP83822 EVM for 100BASE-FX operation, the following changes are required:

- Remove T2
- Remove R34, R35, R28, R29, R30 and R31
- Populate C47, C48, C49, C50, C53, C54, C57, C58, C59 and C66
- Populate L3 and L4
- Populate J15
- Populate H1
- Populate R36, R41, R42 and R44

Note: It is important to read the termination requirements for the SFP transceiver used. The DP83822 EVM allows for custom termination on both receive and transmit paths to ensure support for most SFP transceivers. Please refer to the schematic/layout for more information regarding the termination network.

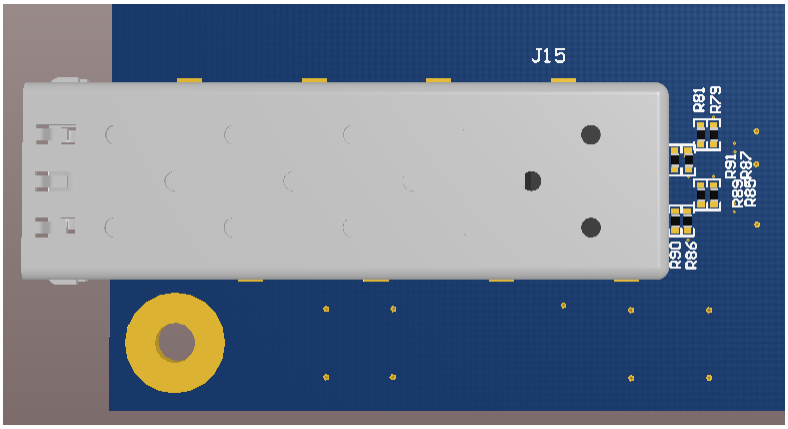


Figure 13. SFP Cage and Termination Network

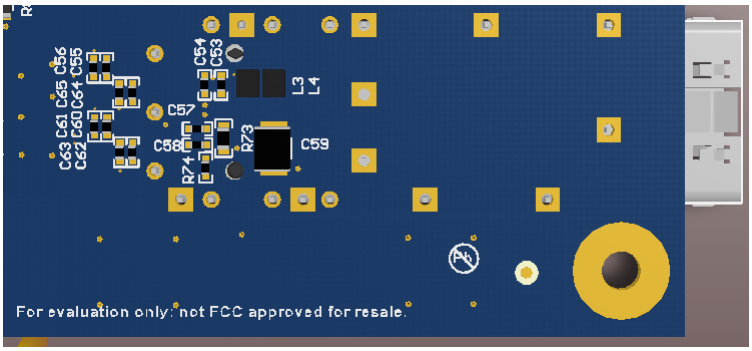
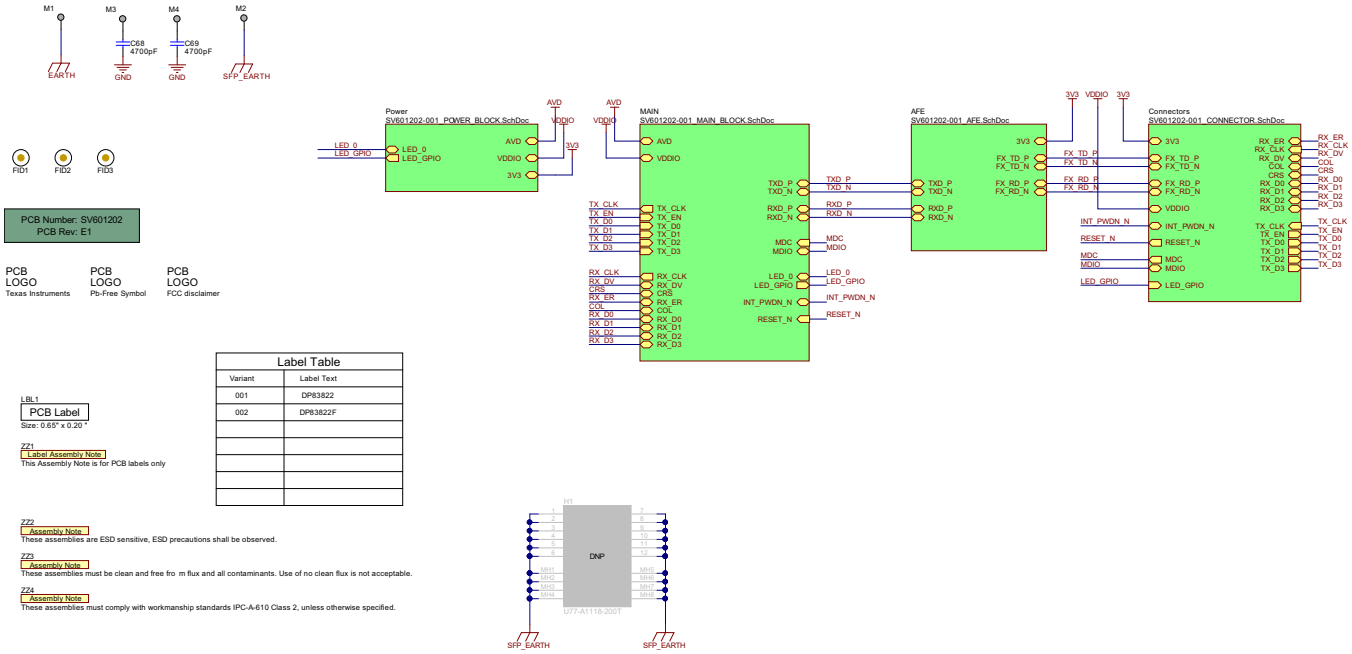


Figure 14. SFP Power Network

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3 Schematic

3.1 Hardware Schematic

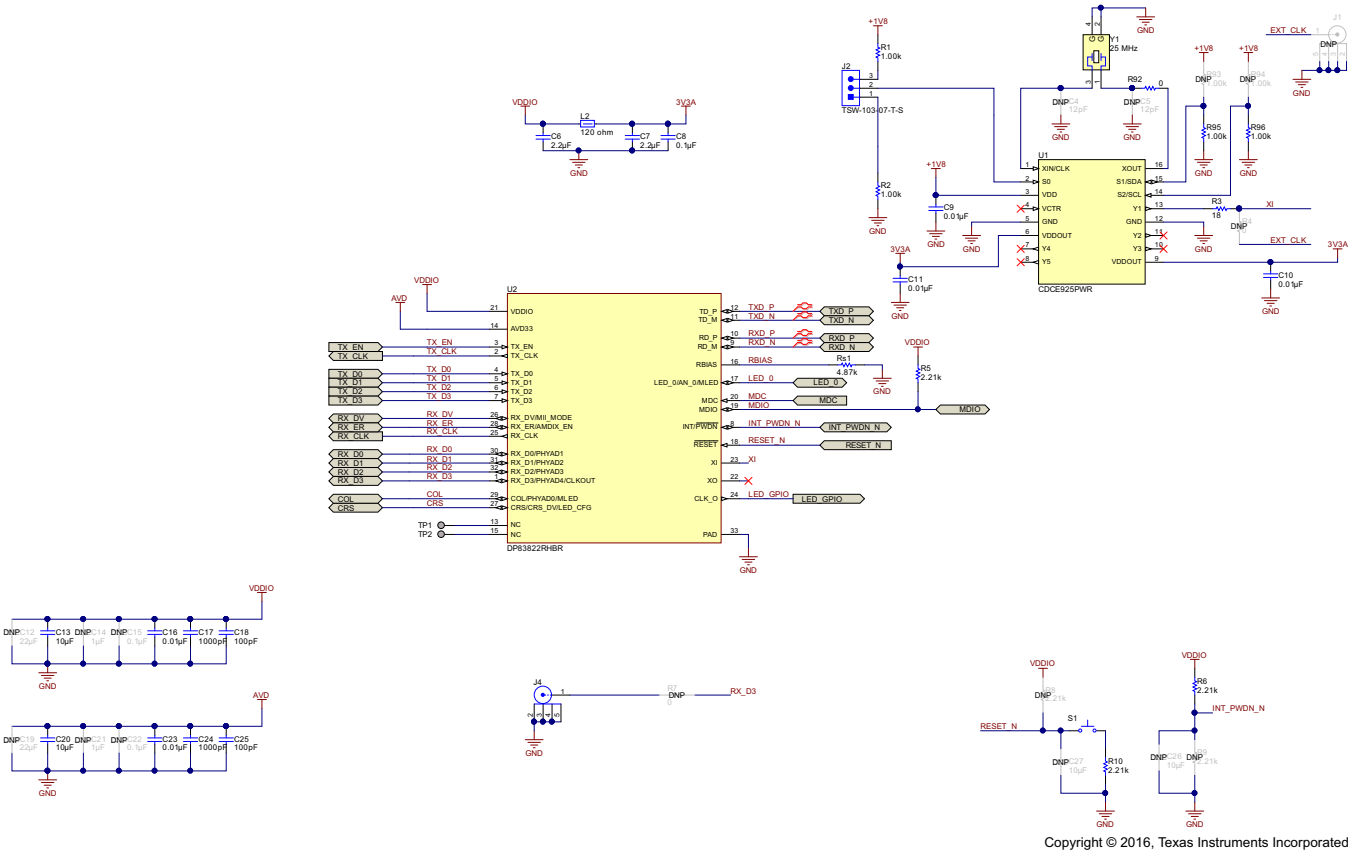


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Figure 15. Hardware Schematic

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3.2 Main Block Schematic

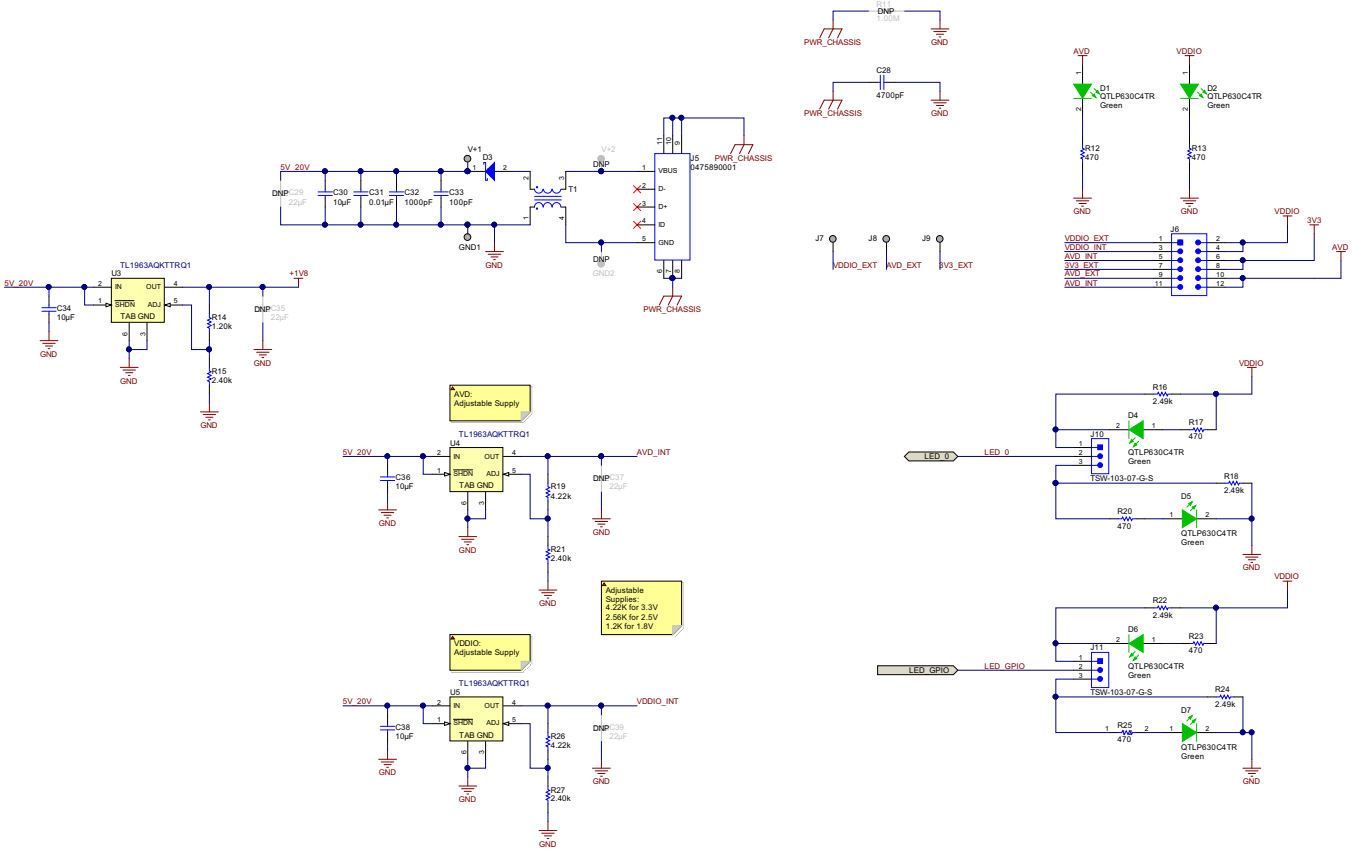


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Figure 16. Main Block Schematic

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3.3 Power Block Schematic

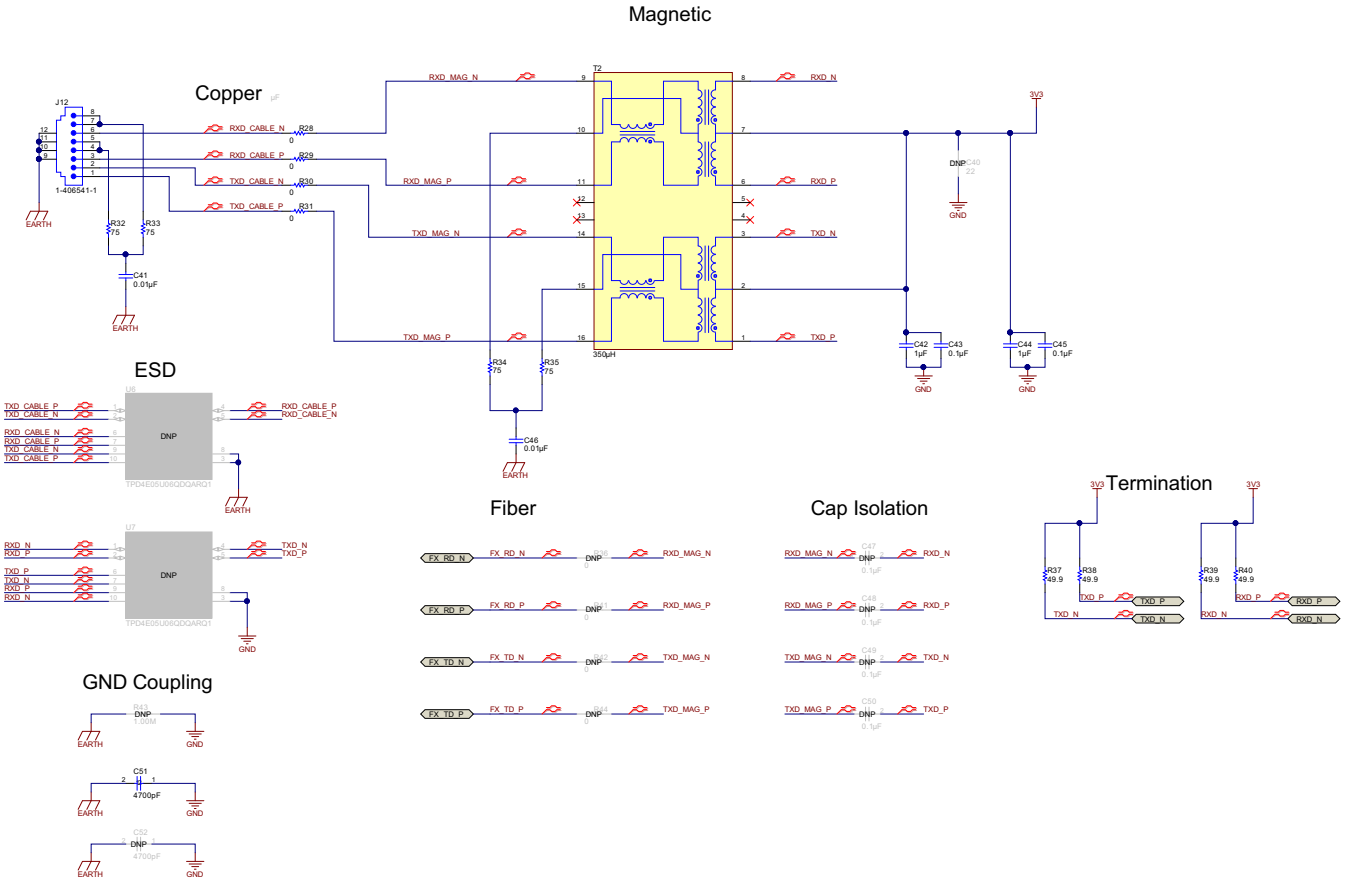


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Figure 17. Power Block Schematic

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3.4 Analog Front-End Schematic

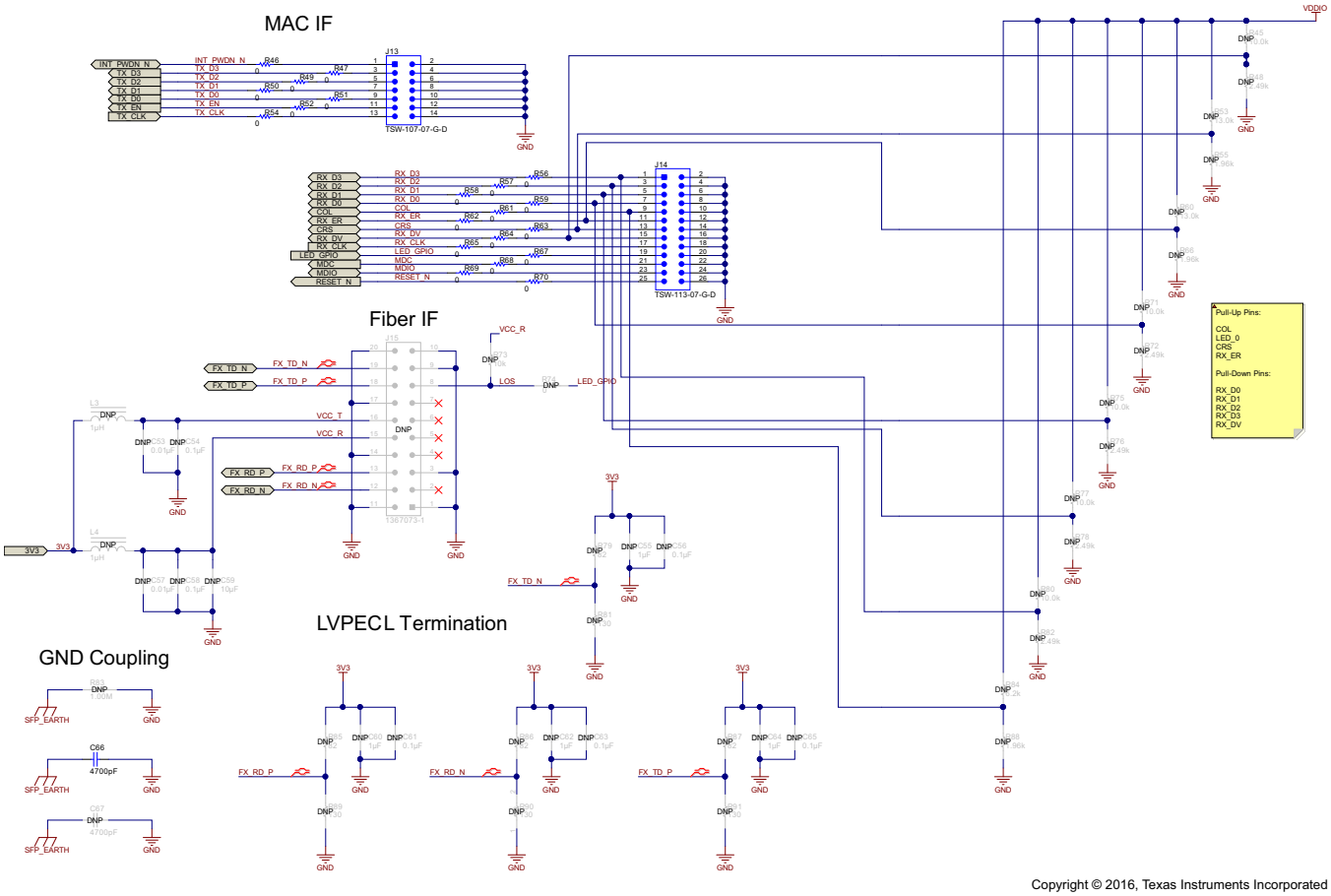


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Figure 18. Analog Front-End Schematic

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3.5 Connector and Bootstrap Schematic



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Figure 19. Connector and Bootstrap Schematic

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4 Layout

4.1 Top Overlay

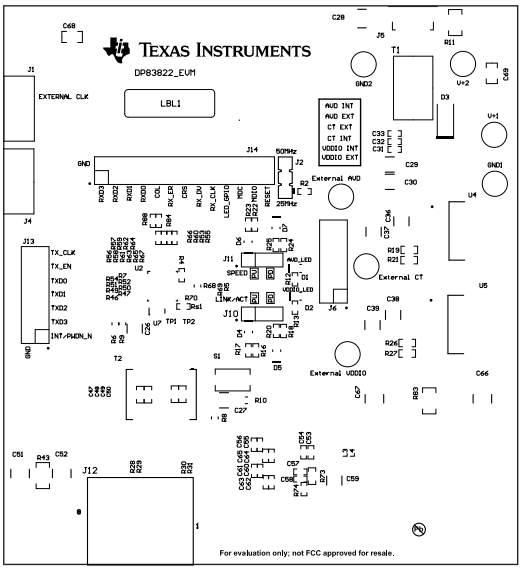


Figure 20. Top Overlay

4.2 Top Layer

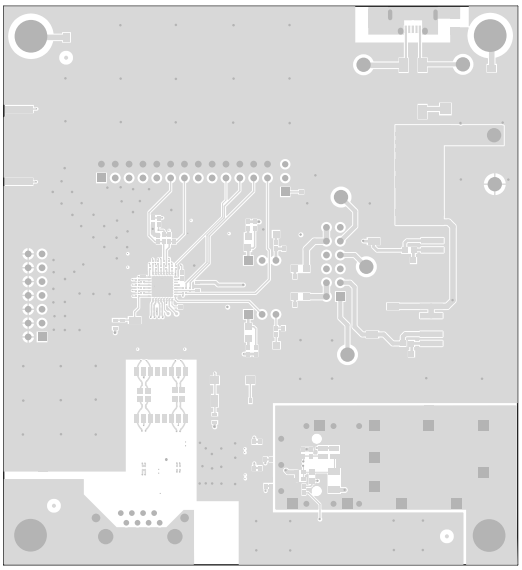


Figure 21. Top Layer

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4.3 Signal Layer 1

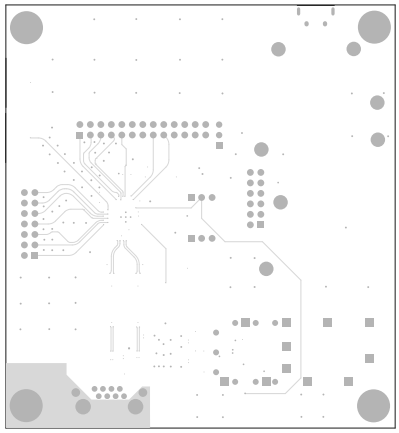


Figure 22. Signal Layer 1

4.4 Signal Layer 2

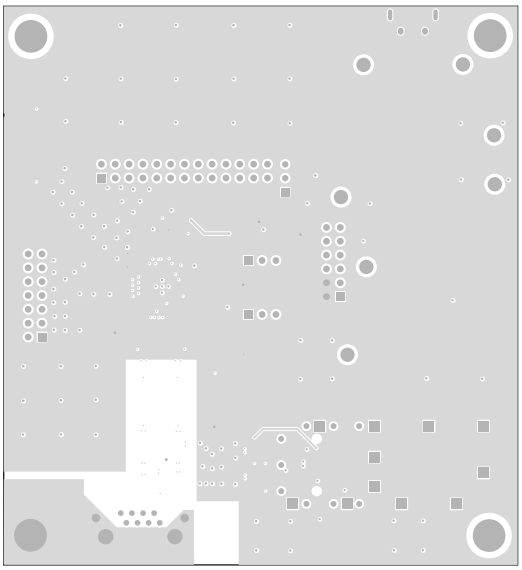


Figure 23. Signal Layer 2

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4.5 Signal Layer 3

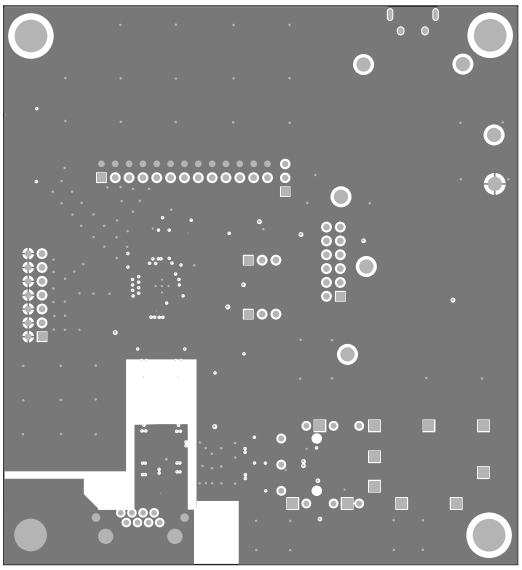


Figure 24. Signal Layer 3

4.6 Signal Layer 4

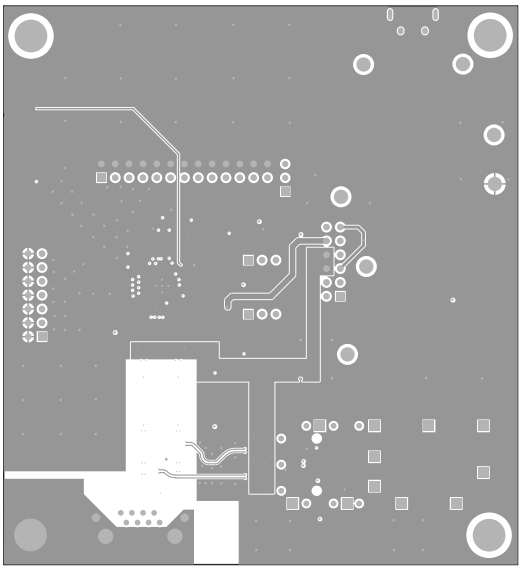


Figure 25. Signal Layer 4

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4.7 Bottom Layer

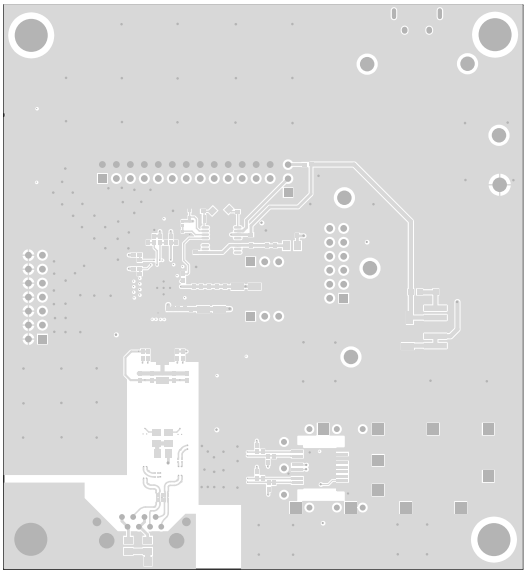


Figure 26. Bottom Layer

4.8 Bottom Overlay

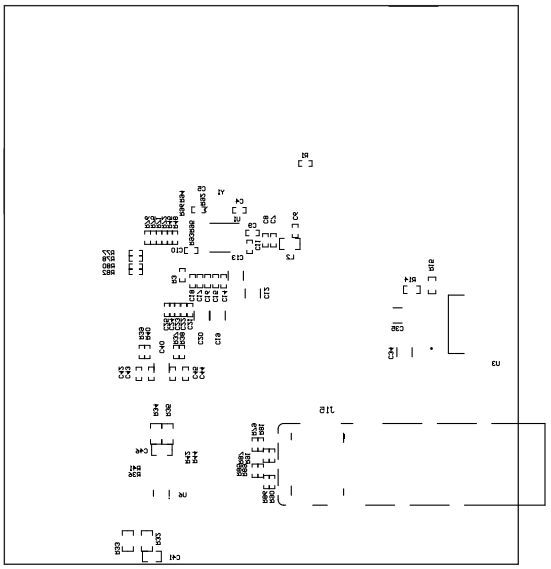


Figure 27. Bottom Overlay

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4.9 Board Assembly

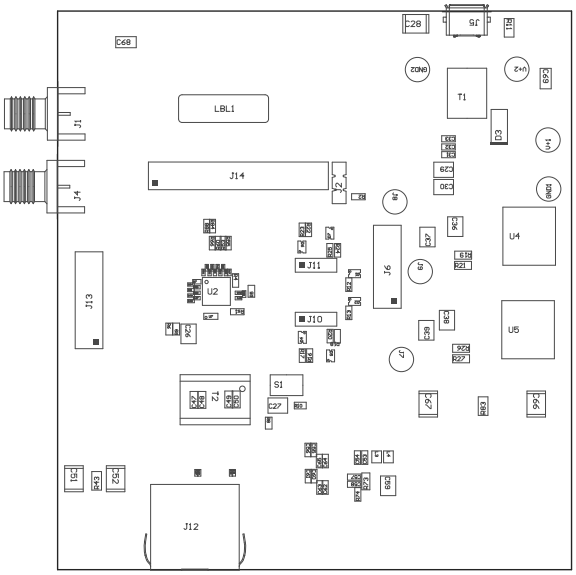


Figure 28. Top Board Assembly

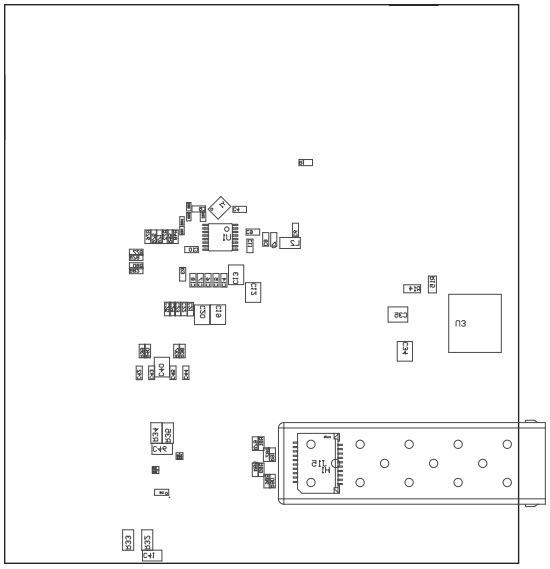


Figure 29. Bottom Board Assembly

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5 Bill of Materials

Table 4. Bill of Materials

Part Number	Component Designation	Description	Qty
C0402C120J3GACAUTO	C4, C5	CAP, CERM, 12 pF, 25 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	2
GRM155R61C225KE11D	C6, C7	CAP, CERM, 2.2 µF, 16 V, ±10%, X5R, 0402	2
GRM155R71C104KA88D	C8, C15, C22, C43, C45, C54, C56, C58, C61, C63, C65	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0402	11
CGA2B3X7R1H103K050BB	C9, C10, C11, C16, C23, C31, C53, C57	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	8
CGA6P1X7R1C226M250AC	C12, C19, C29, C35, C37, C39, C40	CAP, CERM, 22 µF, 16 V, ±20%, X7R, AEC-Q200 Grade 1, 1210	7
CGA6P1X7R1E106M250AC	C13, C20, C26, C27, C30, C34, C36, C38, C59	CAP, CERM, 10 µF, 25 V, ±20%, X7R, AEC-Q200 Grade 1, 1210	9
C1005X7S1A105K050BC	C14, C21, C42, C44, C55, C60, C62, C64	CAP, CERM, 1 µF, 10 V, ±10%, X7S, 0402	8
CGA2B2C0G1H102J050BA	C17, C24, C32	CAP, CERM, 1000 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	3
CGA2B2C0G1H101J050BA	C18, C25, C33	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	3
1812GC472KAT1A	C28, C51, C52, C66, C67	CAP, CERM, 4700 pF, 2000 V, ±10%, X7R, 1812	5
CGA4J3C0G2E103J125AA	C41	CAP, CERM, 0.01 µF, 250 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0805	1
CGA4J3C0G2E103J125AA	C46	CAP, CERM, 0.01 µF, 250 V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0805	1
CGA3E2X8R1E104K080AA	C47, C48, C49, C50	CAP, CERM, 0.1 µF, 25 V, ±10%, X8R, AEC-Q200 Grade 0, 0603	4
08051C472KAT2A	C68, C69	CAP, CERM, 4700 pF, 100 V, ±10%, X7R, 0805	2
QTLP630C4TR	D1, D2, D4, D5, D6, D7	LED, Green, SMD	6
NRVBA160T3G	D3	Diode, Schottky, 60 V, 1 A, AEC-Q101, SMA	1
Fiducial	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	3
1502-2	GND1, GND2, V+1, V+2	Terminal, Turret, TH, Double	4
U77-A1118-200T	H1	SFP Single Cage	1
142-0701-851	J1	Connector, End launch SMA, 50 Ω, SMT	1
TSW-103-07-T-S	J2	Header, 2.54 mm, 3x1, Tin, TH	1
142-0701-851	J4	Connector, End launch SMA, 50 Ω, SMT	1
0475890001	J5	Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	1
TSW-106-07-G-D	J6	Header, 100mil, 6x2, Gold, TH	1
1502-2	J7	Terminal, Turret, TH, Double	1
1502-2	J8	Terminal, Turret, TH, Double	1
1502-2	J9	Terminal, Turret, TH, Double	1
TSW-103-07-G-S	J10, J11	Header, 100mil, 3x1, Gold, TH	2
1-406541-1	J12	RJ-45, No LED, tab up, R/A, TH	1
TSW-107-07-G-D	J13	Header, 100mil, 7x2, Gold, TH	1

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Table 4. Bill of Materials (continued)

Part Number	Component Designation	Description	Qty
TSW-113-07-G-D	J14	Header, 100mil, 13x2, Gold, TH	1
1367073-1	J15	Receptacle, 0.8mm, 10x2, Gold, R/A, SMT	1
BLM21BD121SN1D	L2	Ferrite Bead, 120 Ω at 100 MHz, 0.2 A, 0805	1
IFSC0806AZER1R0M01	L3, L4	Inductor, Shielded, Ferrite, 1 µH, 1.6 A, 0.115 Ω, SMD	2
THT-14-423-10	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	1
CRCW04021K00FKED	R1, R2	RES, 1.00 k, 1%, 0.063 W, 0402	2
CRCW040218R0JNED	R3	RES, 18, 5%, 0.063 W, 0402	1
CRCW04020000Z0ED	R4	RES, 0, 5%, 0.063 W, 0402	1
TNPW06032K21BEEA	R5, R6, R8, R9, R10	RES, 2.21 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	5
ERJ-1GE0R00C	R7	RES, 0, 5%, 0.05 W, 0201	1
CRCW12061M00FKEA	R11, R43, R83	RES, 1.00 M, 1%, 0.25 W, 1206	3
CRCW0402470RJNED	R12, R13, R17, R20, R23, R25	RES, 470, 5%, 0.063 W, 0402	6
RT0603BRD071K2L	R14	RES, 1.20 k, 0.1%, 0.1 W, 0603	1
ERA-3AEB242V	R15, R21, R27	RES, 2.40 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	3
CRCW04022K49FKED	R16, R18, R22, R24, R48, R72, R76, R78, R82	RES, 2.49 k, 1%, 0.063 W, 0402	9
CRCW06034K22FKEA	R19, R26	RES, 4.22 k, 1%, 0.1 W, 0603	2
ERJ-1GE0R00C	R28, R29, R30, R31, R36, R41, R42, R44, R46, R47, R49, R50, R51, R52, R54, R56, R57, R58, R59, R61, R62, R63, R64, R65, R67, R68, R69, R70	RES, 0, 5%, 0.05 W, 0201	28
CRCW080575R0JNEA	R32, R33, R34, R35	RES, 75, 5%, 0.125 W, 0805	4
CRCW040249R9FKED	R37, R38, R39, R40	RES, 49.9, 1%, 0.063 W, 0402	4
CRCW040210K0FKED	R45, R71, R75, R77, R80	RES, 10.0 k, 1%, 0.063 W, 0402	5
CRCW040213K0FKED	R53, R60	RES, 13.0 k, 1%, 0.063 W, 0402	2
CRCW04021K96FKED	R55, R66, R88	RES, 1.96 k, 1%, 0.063 W, 0402	3
RC0603JR-0710KL	R73	RES, 10 k, 5%, 0.1 W, 0603	1
RC0402JR-070RL	R74	RES, 0, 5%, 0.063 W, 0402	1
CRCW040282R0JNED	R79, R85, R86, R87	RES, 82, 5%, 0.063 W, 0402	4
CRCW0402130RJNED	R81, R89, R90, R91	RES, 130, 5%, 0.063 W, 0402	4
CRCW04026K20JNED	R84	RES, 6.2 k, 5%, 0.063 W, 0402	1
ERJ-1GE0R00C	R92	RES, 0, 5%, 0.05 W, 0201	1
CRCW02011K00FKED	R93, R94, R95, R96	RES, 1.00 k, 1%, 0.05 W, 0201	4
CRCW04024K87FKED	Rs1	RES, 4.87 k, 1%, 0.063 W, 0402	1
KSR221GLFS	S1	Switch, Normally open, 2.3N force, 200k operations, SMD	1
ACM9070-701-2PL	T1	Common Mode Filter for Power Line	1
HX1188FNLT	T2	Transformer, 350 uH, SMT	1

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Table 4. Bill of Materials (continued)

Part Number	Component Designation	Description	Qty
CDCE925PWR	U1	PROGRAMMABLE 2-PLL VCXO CLOCK SYNTHESIZER WITH 1.8-V, 2.5-V and 3.3-V LVCMOS OUTPUTS, PW0016A	1
DP83822RHBR	U2	10/100 Ethernet PHY, RHB0032B	1
TL1963AQKTTRQ1	U3, U4, U5	Single Output Fast Transient Response LDO, 1.5 A, Adjustable 1.21 to 20 V Output, 2.1 to 20 V Input, 5-pin DDPAK (KTT), -40 to 125 degC, Green (RoHS & no Sb/Br)	3
TPD4E05U06QDQARQ1	U6, U7	1, 4, 6 CHANNEL PROTECTION SOLUTION FOR SUPER-SPEED (UP TO 6 GBPS) INTERFACE, DQA0010A	2
ABM8AIG-25.000MHZ-12-2Z-T3	Y1	Crystal, 25MHz, 12pF, SMD	1

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