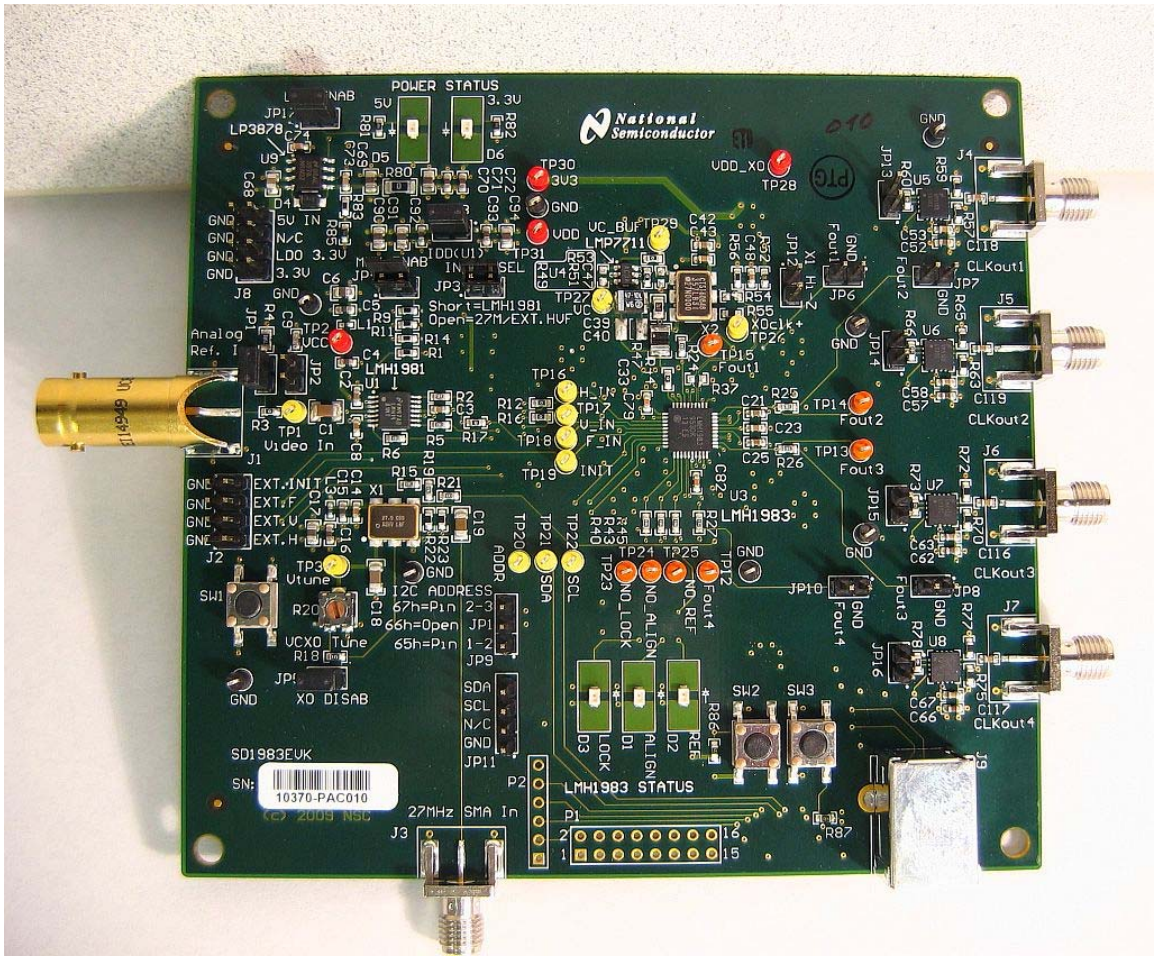
LMH1983 Evaluation Kit Users Guide
Version 1.0
2/4/10



INTRODUCTION

The LMH1983 Evaluation Kit (EVK) allows for the evaluation of the LMH1983 3G/HD/SD Video Clock Generator with Audio Clock. The LMH1983 device is configured and controlled using National Semiconductor's Analog Launch Pad (ALP) software graphical user interface (GUI).

The GUI with the LMH1983 profile runs on Windows PC and can be used to program the device's control registers through the I^2C interface. The Serial Peripheral Adapter (SPA) board included in the kit provides I^2C read/write control via the USB port of the PC with the GUI. For more information about the GUI software and device register descriptions and programming, please refer to the GUI software manual and LMH1983 datasheet.

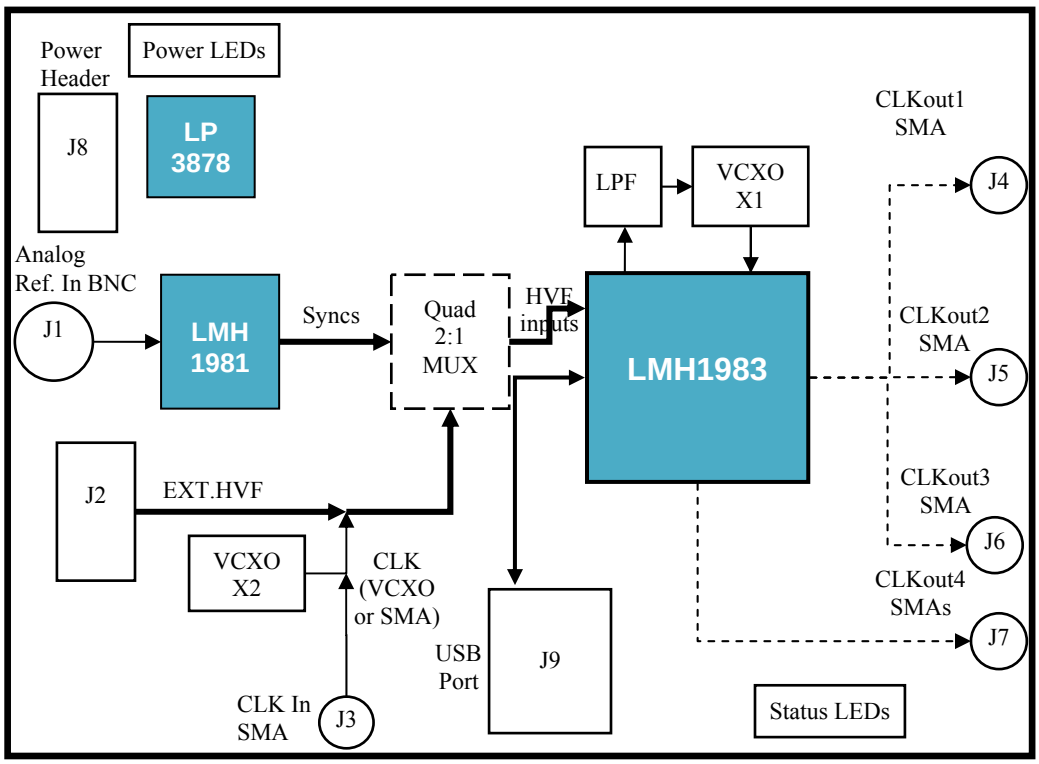
Overview of LMH1983

The LMH1983 clock generator generates four video specific clocks. The device has four PLLs in it.

- PLL1 uses an external 27 MHz VCXO, and always generates a 27MHz reference clock. This clock may be locked to an input reference which can be any of a number of different types of reference – from video specific references to single frequency reference signals.
- PLL2 is dedicated to generating a 148.5 MHz clock (27 MHz * 5.5) , and is locked to PLL1.
- PLL3 is dedicated to generating a clock at 148.35 MHz (27 MHz * 5500/1001)
- PLL4, by default is locked to PLL1, and generates a 24.576MHz clock which can be used as an audio clock. PLL4 has a lot of versatility built in to it and can be used for a broad variety of applications.

LMH1983 EVALUATION BOARD OVERVIEW

The following block diagram shows an overview of the LMH1983 evaluation board and general location of the main features, which will be discussed in the following sections of this manual.



Applying power to the board:

The default configuration to apply power is to apply +5V across the top two pins on J8. With a jumper on JP17, and on board LDO is used to generate the 3.3V rail that powers the circuits on the evaluation board.

Alternately, JP17 may be removed, and a 3.3V rail may be applied directly to the bottom two pins of J8.

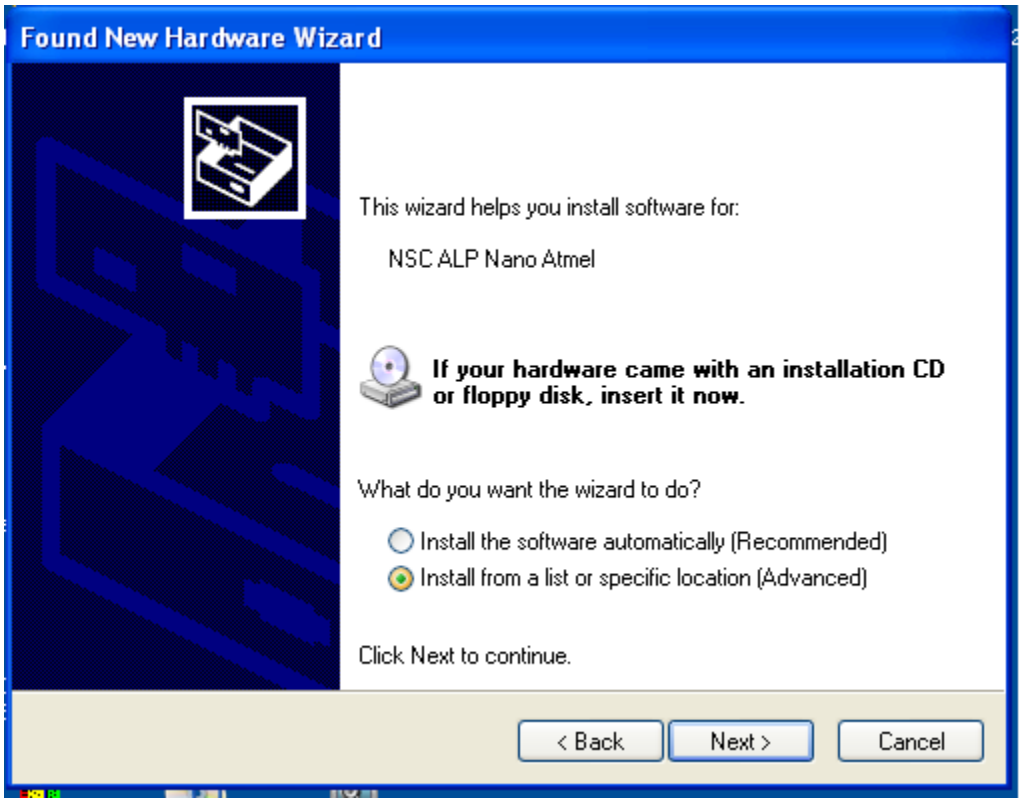
Installing the software:

The evaluation kit contains a CD which has the control software on it. Running the program on the CD will install the software on your computer.

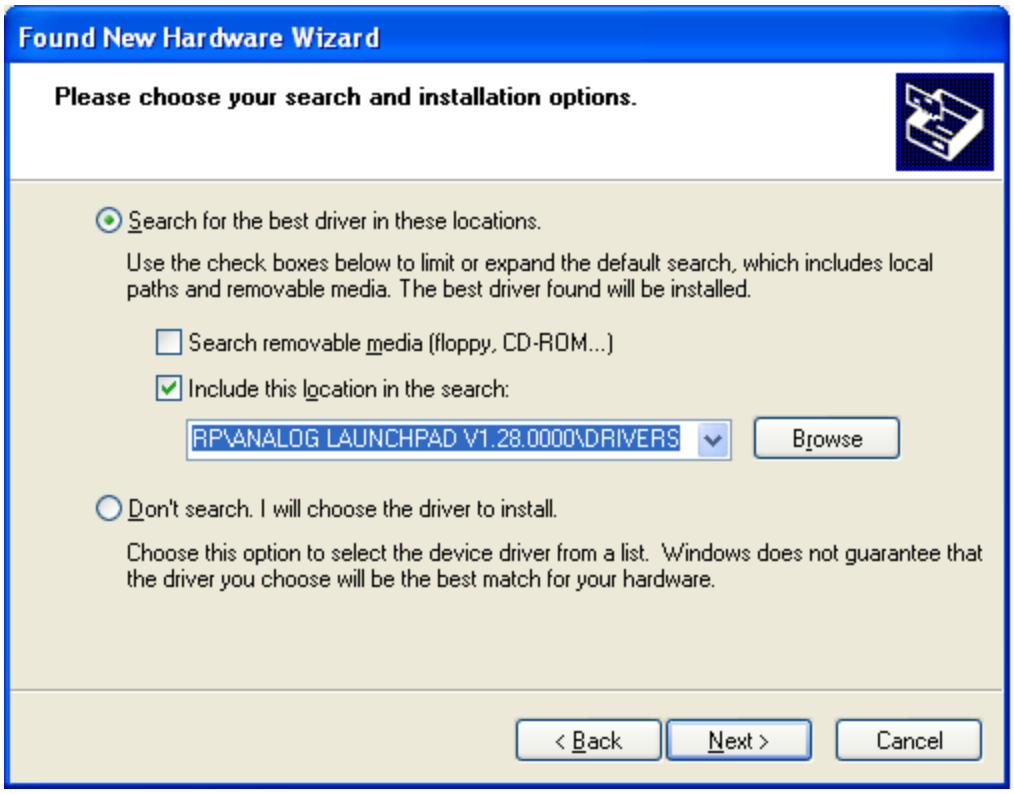
Apply power to the Evaluation Board, and then attach a USB cable between the computer and the board. Windows will recognize the board and pop up the



When this window comes up, select ‘No, not this time’ and ‘Next>’



Select “Install from a list or specific location”

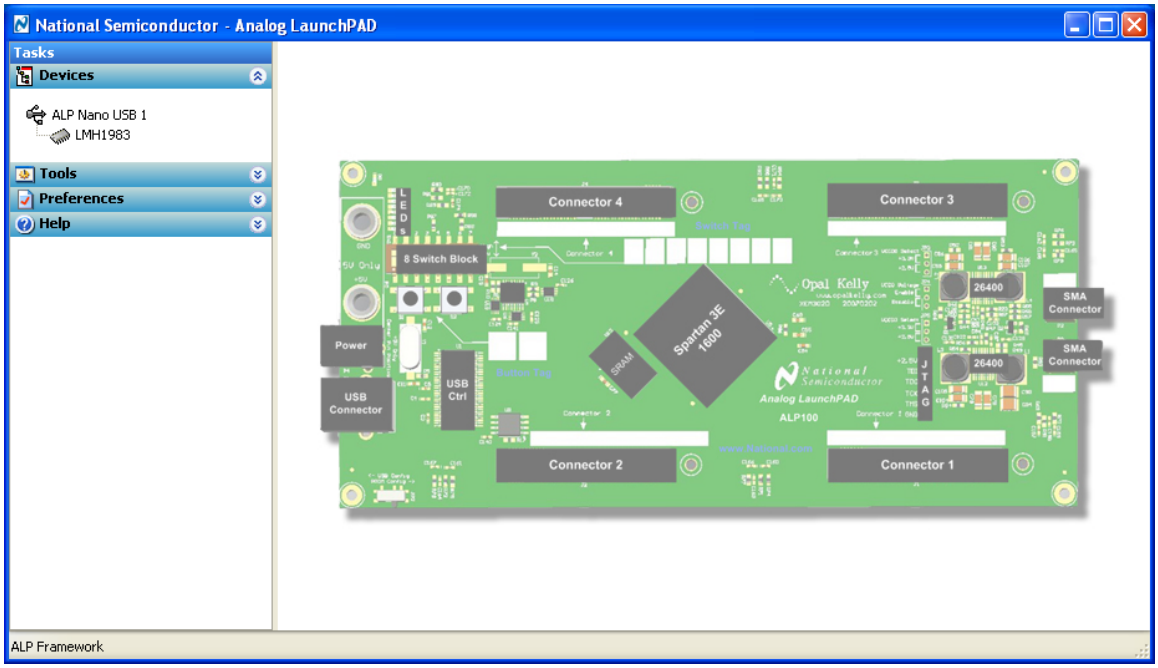

Found New Hardware Wizard
Please choose your search and installation options.
Search for the best driver in these locations.
Use the check boxes below to limit or expand the default search, which includes local paths and removable media. The best driver found will be installed.
Search removable media (floppy, CD-ROM...)
Include this location in the search:
RP\ANALOG LAUNCHPAD V1.28.0000\DRIVERS
Browse
Don't search. I will choose the driver to install.
Choose this option to select the device driver from a list. Windows does not guarantee that the driver you choose will be the best match for your hardware.
< Back
Next >
Cancel

For the location, enter “C:\Program Files\National Semiconductor Corp\Analog Launchpad Vxxx\DRIVERS” This directory was installed on your computer during the ALP software installation.

The computer will warn you that the software has not passed Windows Logo Testing. Go ahead and Continue Anyway.

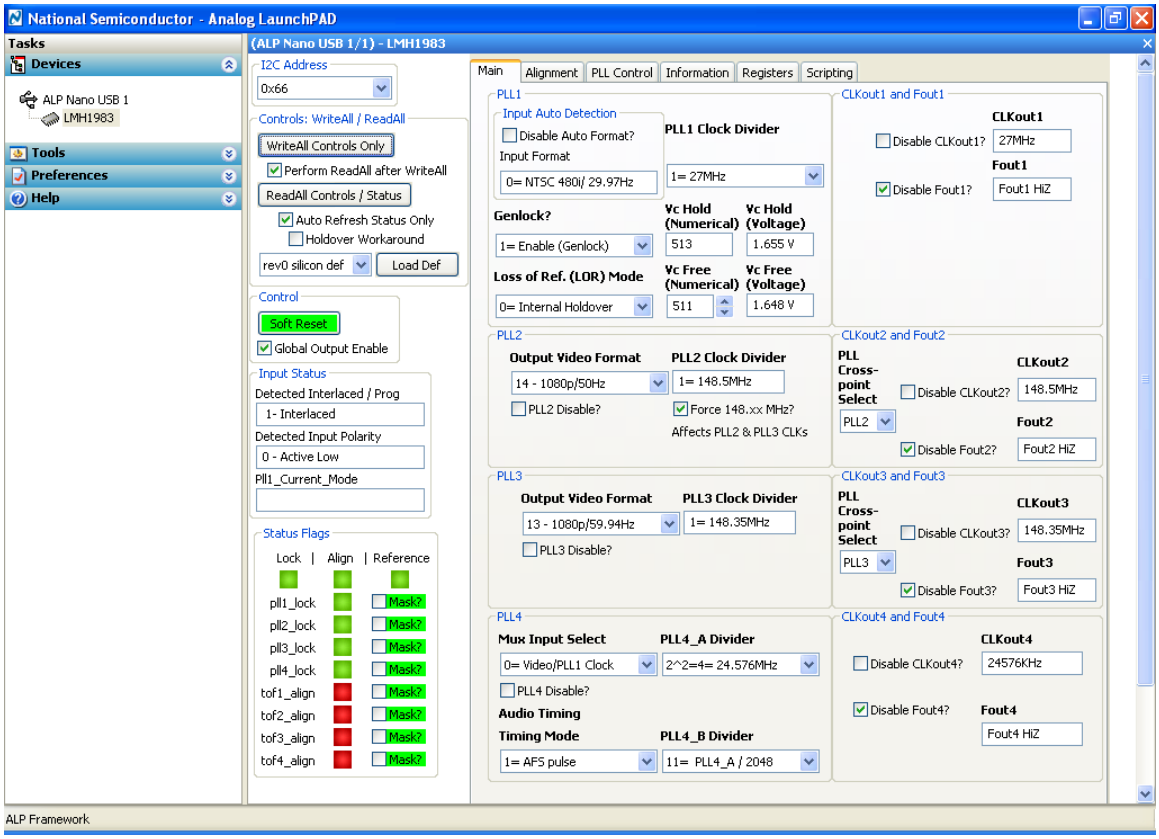
The driver for the LMH1983 evaluation board will now be installed, and you can start the ALP software.

When you start the Analog LaunchPAD software, it should recognize the evaluation board and the screen will look like the figure below.



If the board is not connected properly, or not powered up, the ALP software will start up in a demo mode which will look like the normal mode, but will not control the board.

Once the startup screen appears, click on the LMH1983 icon on the left side of the window, and this will bring up the GUI:



The status indications on the GUI are only updated when the Read Controls/Status button is clicked. To have continuous updates, click the checkbox 'Auto Refresh Status', I also like to check the 'Perform ReadAll after write' box – this will update all of the status controls whenever something is written. In some cases, writing to one register will result in multiple things changing, and checking this button will make sure that everything is kept updated.

There are several panels in the GUI - the first is the main control panel and allows for basic control over the board. Also very useful is the Registers tab, which will allow for detailed manipulation of the various registers in the LMH1983.

I²C SLAVE ADDRESS

The I²C address select jumper JP9 (3-way) can be configured as follows to select one of the three I²C slave addresses offered by the LMH1983. The default for the board, and for the ALP software is address '66h which corresponds to no jumper installed.

Table 1: LMH1983 I²C Slave Address Selection

7-bit I²C Slave Address	JP1 Jumper Setting	LMH1983 Address Input State
65'h (hex)	Short Pins 1-2	Externally tied low
66'h	Open Pins	Internally biased to mid-supply
67'h	Short Pins 2-3	Externally tied high

Observing the Outputs

The LMH1983 generates four clock signals (CLKout1, CLKout2, CLKout3, CLKout4) and four timing signals (TOF1, TOF2, TOF3, TOF4). The LMH1983 outputs are differential outputs, and can be observed directly at JP13, JP14, JP15 and JP16. There are 100Ω termination resistors situated near the connectors (R60,R66, R73 and R78). If the differential signals are to be observed with a high impedance differential scope probe, it can be attached directly to the pins. If it is desired that the differential outputs drive a load, the load resistor should be moved to be adjacent to the final load. In addition to the differential outputs, there are 50Ohm single ended outputs as well. These are provided by using LMH0302 SDI cable drivers. On the initial version of the evaluation board these outputs exhibit some undershoot and ringing at 4GHz which degrades the jitter performance of these outputs.

Configuring the board for operation with an analog video reference signal

The LMH1983 Evaluation board includes an LMH1981 sync separator which is able to extract the timing signals from a broad range of analog sync signals. To use this feature, install a jumper on JP4 (MUX ENABLE), and one on JP3 (Input Select). Supply the reference signal to J1 (analog Ref In), and you can monitor the extracted H, V and F signals at the yellow test points just to the left of the LMH1983.

The GUI will display what format is being detected under the PLL1

The LMH1983 can automatically detect and synchronize to the following reference input formats received at its input pins:

- HVF Sync timing from SMPTE standard video formats
  - 525i/29.97/30
  - 525p/59.94/60

  - 625i/25
  - 625p/50
  - 720p/23.98/24/25/29.97/30/50/59.94/60
  - 1080i/25/29.97/30
  - 1080p/23.98/24/25/29.97/30/50/59.94/60
  - 1080pSf/23.98/24/25/29.97/30
- Audio Word Clock
  - 32 kHz, 48 kHz, 96 kHz, 44.1 kHz
- System Clock
  - 27 MHz
  - 10 MHz

Configuring the board for operation with a digital video reference signal

An external digital reference signal, consisting of H,V and F may be applied to J2, a jumper should installed on JP5, and the jumper on JP3 should be removed.

The GUI will display what format is being detected under the PLL1

For a comprehensive list of formats that can be detected, please refer to the LMH1983 datasheet. To determine format, the device measures the period of the Hsync input by counting 27MHz clock pulses over several Hsync periods. There are some standards where Hsync may be the same, in which case V and F are examined to determine if the reference is an interlaced or progressive format before format detection is complete.

Configuring the board for operation in free-run mode, using the on board reference oscillator

To operate the board in 'stand-alone mode', remove the jumper for JP3, make sure that the jumper is removed from JP5, and in this mode, the frequency can be trimmed via R20 – the trim pot near the lower left corner of the board.

Configuring the board for operation, locked to an external clock oscillator.

To operate the board locked to an external clock, supply the reference signal through the SMA connector 'J3', remove the jumper form JP3 and install a jumper on JP5.
The automatic format detect algorithm in the LMH1983 will recognize reference clocks of 27MHz or 10MHz. Other reference rates can be manually programmed.

PLL1 LOOP FILTER AND VCXO

The LMH1983's primary phase lock loop, PLL1, provides the following key functions:

- Synchronizes the 27 MHz VCXO clock to the reference input
- Attenuates (cleans) input jitter
- Provides a stable, low-jitter 27 MHz clock for PLLs 2, 3, 4

The external loop filter and 27 MHz VCXO are essential to the performance of PLL1, which dominates the overall loop response of the LMH1983. The loop response of PLL1 is influenced by the external loop components and can be characterized by its loop bandwidth and damping factor.

PLL1 is designed for a nominal loop bandwidth of about 3 Hz (min) and damping factor of 0.70 (min). These were calculated using the approximations below, which assume nominal I_{CP1} = 250uA and DIV_N1 = 1716 for the NTSC input format:

Loop Bandwidth (BW) = $R47*I_{CP1}*K_{VCO} / DIV_N1$
Damping Factor (DF) = $0.5*R47*\sqrt{[(C33 \parallel C39)*I_{CP1}*K_{VCO} / DIV_N1]}$

Loop Filter

The loop filter components include R47, C39 || C40, and C33. It's recommended to avoid use of ceramic capacitors in the loop filter since they exhibit piezoelectric properties that can cause electrical noise when the board/component is subjected to vibration or shock. This "shock noise" in the loop filter circuit can result in low-frequency phase modulation on the VCXO output clock and thus on the downstream PLL output clocks. Tantalum and film capacitors are used for the loop filter since they do not exhibit piezo effects.

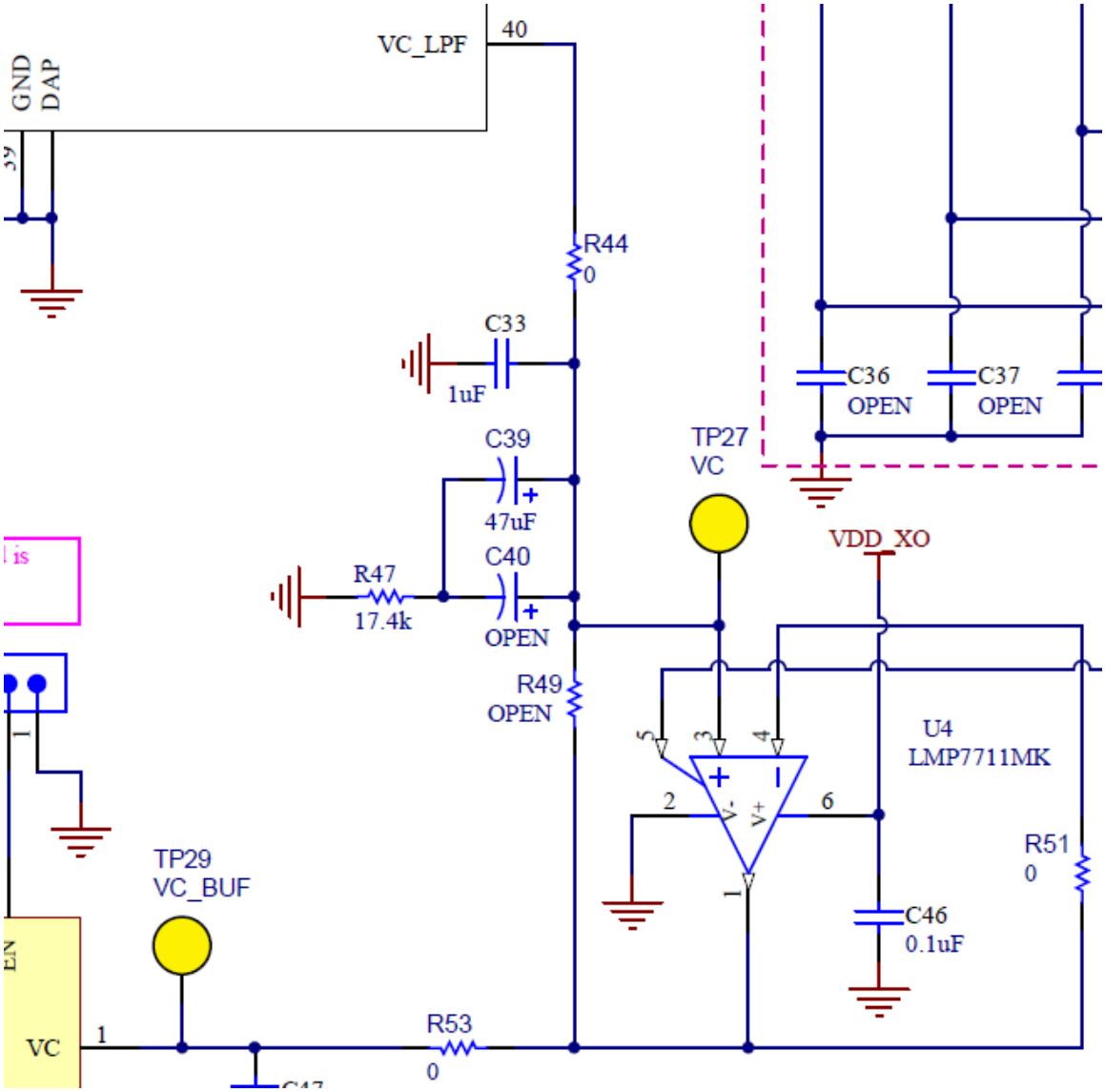


Figure 1: Loop Filter and LMP7711 Buffer Schematic

Op Amp Buffer

The LMP7711 Precision, Low-Noise Op Amp (U4) is used as a buffer to isolate the relatively low input impedance of the VCXO, which would otherwise be the dominant source of leakage current for loop filter circuit. The op amp offers very high input impedance to minimize this leakage current and high slew rate to ensure proper loop operation. The VCXO input control voltage input can be measured at TP29 (VC_BUF).

Note that when the LMH1983 is operating in free run mode, the VC_LPF output set by the user-defined free run voltage control register may be limited by the output voltage range of the LMP7711, as it is not a rail-to-rail op amp.

VCXO

The 27 MHz VCXO (X2) is specified for ±50 ppm APR (min) and ±50 ppm frequency stability. The calculated VCXO gain is 1000 Hz/V (min). The VCXO gain parameter (K_{VCO}) affects the PLL1 loop response, so it must be considered when designing the nominal loop bandwidth and damping factor.

The VCXO's single-ended output clock can be measured at TP26 (XOclk+). The VCXO clock is received at the XOin+ input of the LMH1983. XOin+ (pin 34) and XOin- (pin 33) are differential inputs for the internal op amp that drives the clock signal to the PLL blocks. Because XOin is a differential input, the XOin- pin is biased to about 1.25V using a voltage divider formed by R52 and R56. This input configuration presents a pseudo-differential signal to the XOin pins.

Alternatively, the single-ended VCXO may be replaced with a different 27 MHz VCXO with differential clock outputs (e.g. LVDS); in this case, R52, R56, and C48 should be removed, R54 should be populated with 49.9R to match R55, and R37 should be populated with a 100R differential load. Using a true differential input signal can provide more common-mode rejection and reduce noise/crosstalk, and thus reduce sources of deterministic jitter.

INDEPENDENT AUDIO CLOCK GENERATION

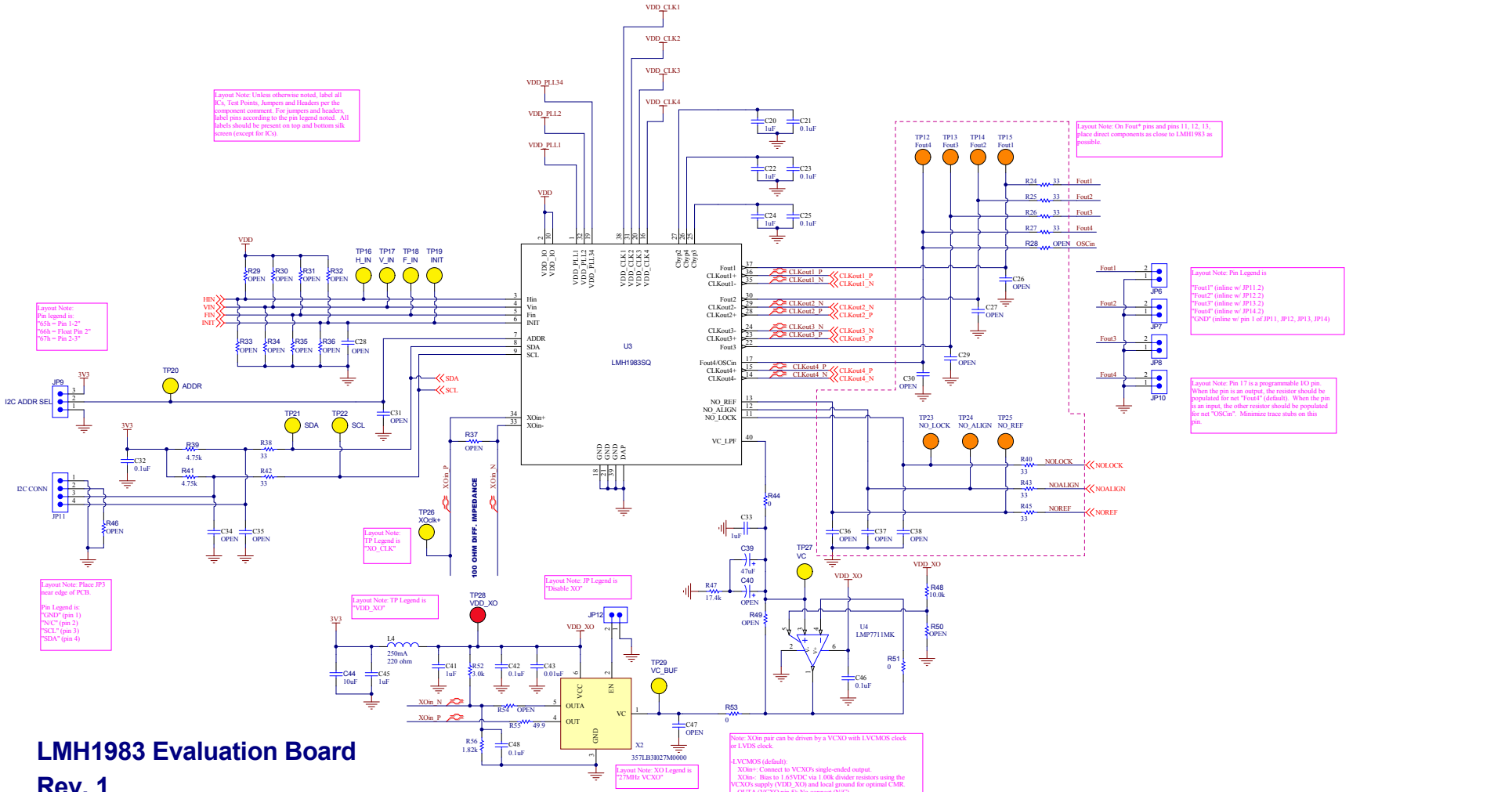
By default, the audio clock generated from PLL4 is phase-locked to the 27 MHz VCXO clock reference from PLL1, and in turn, is synchronized to the reference input.

It is possible to have the audio clock independently generated from an external 27 MHz clock source by changing the PLL4 input mux mode via register programming. Once the PLL4 input mode is properly programmed, pin 17 (normally Fout4) is switched to an input pin (OSCin) and can be driven with an external 27 MHz clock.

There are two options for an independent 27 MHz clock source. The first option is to use an on-board 27 MHz VCXO in the footprint X2. The second option is to receive an external 27 MHz via the SMA clock input, J3. Either one of the options can be used as long as it's not being used to drive the Hin reference of the LMH1983. To make use of this option, populate R21 and R28, then to use the on board oscillator, enable it by removing the jumper on JP5, and to use the external SMA, disable the oscillator with a jumper on JP5 and provide the reference on J3.

Appendix A

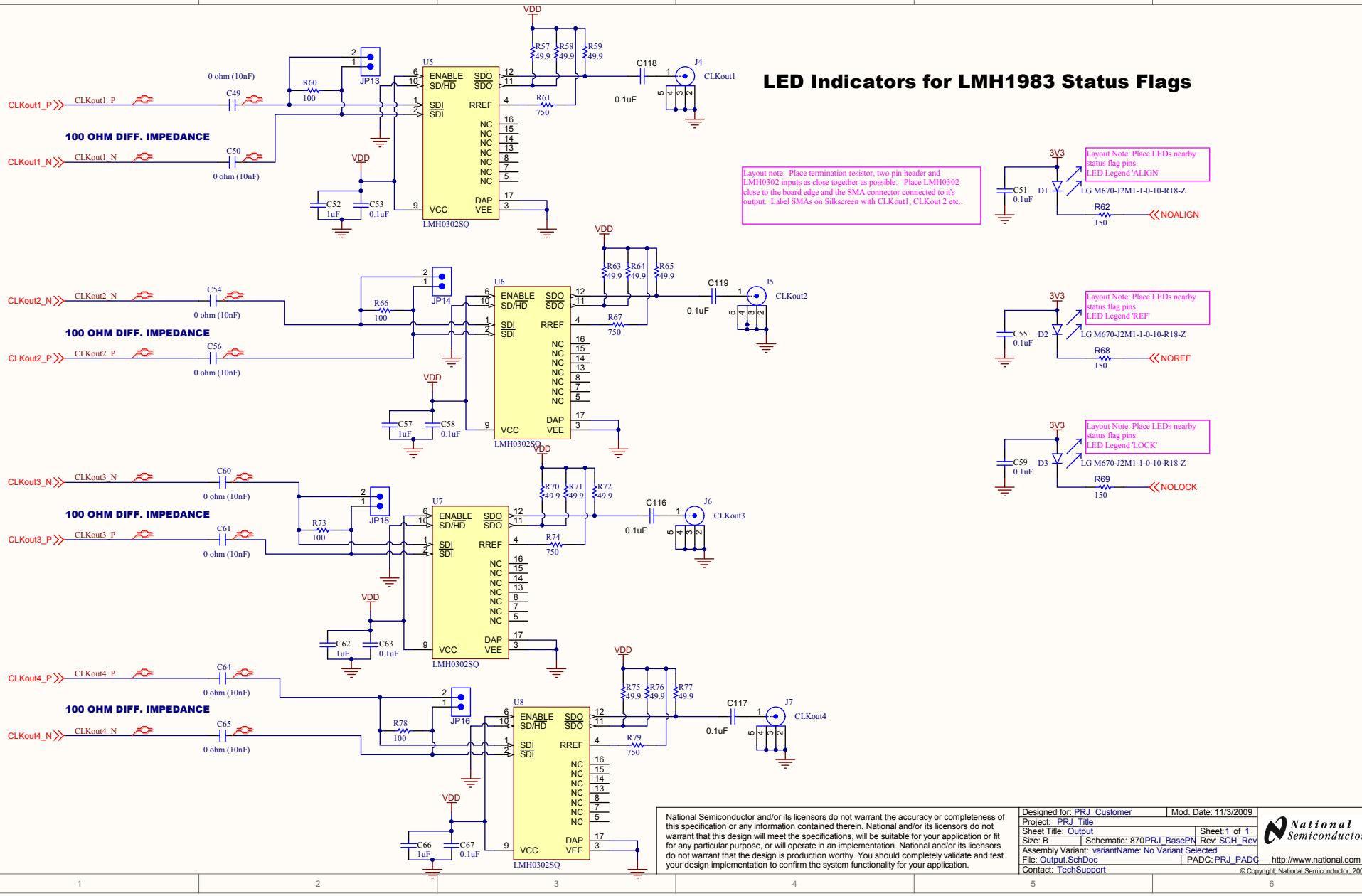
Schematics



LMH1983 Evaluation Board
Rev. 1

PLL1 Loop Filter and VCXO

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Date: 11/3/2009	Sheet 4 of 5	
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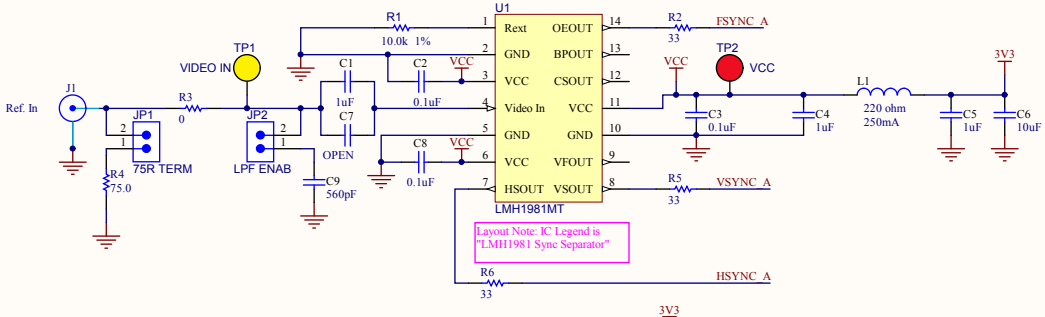
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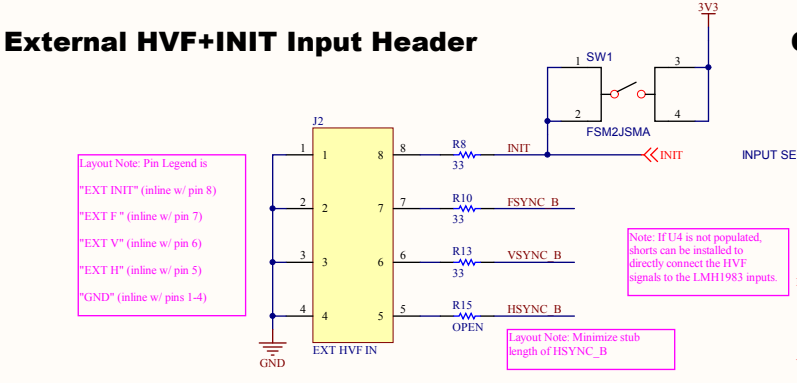
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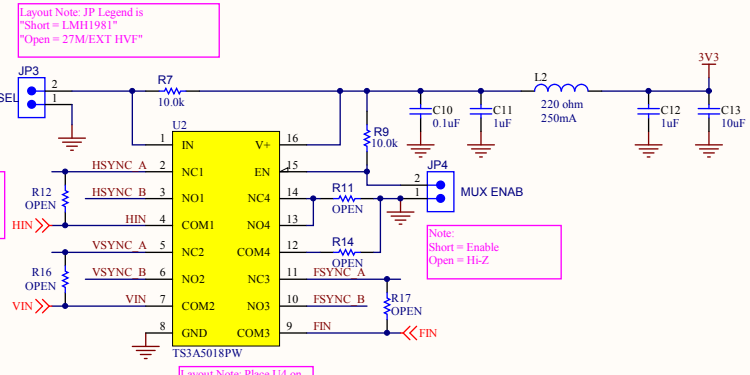
Analog Input and LMH1981 Sync Separator



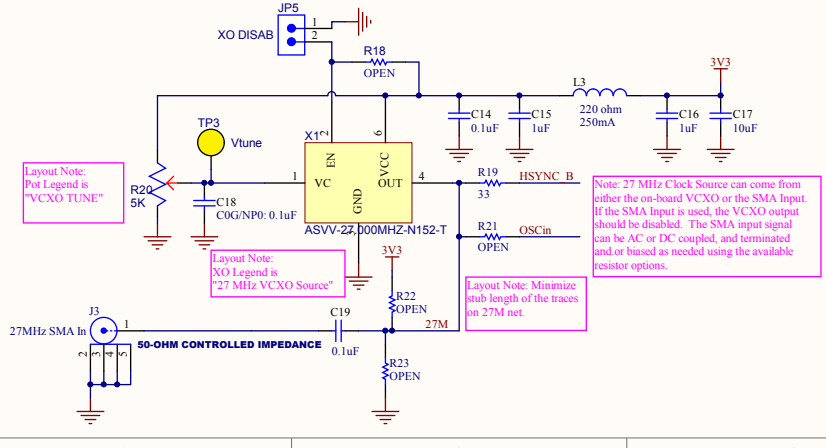
External HVF+INIT Input Header

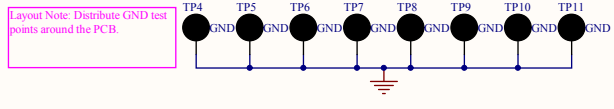


Quad SPDT Input MUX with Output Hi-Z



27 MHz Clock Source from VCXO or SMA Input

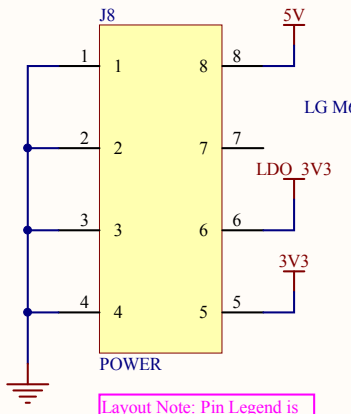




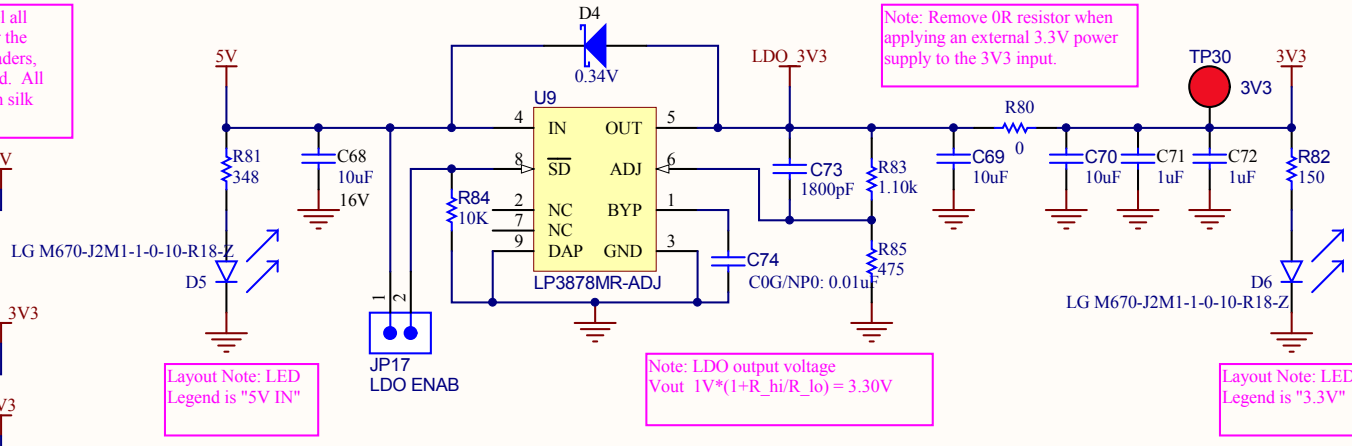
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Date: 11/3/2009		Sheet 4 of 5
File: C:\Projects\..\LMH1981.SchDoc		Drawn By: Sauerwald

Power Supply Input and Low-Noise 3.3V LDO Regulator

Layout Note: Unless otherwise noted, label all ICs, Test Points, Jumpers and Headers per the component comment. For jumpers and headers, label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).



Layout Note: Pin Legend is
"5V IN" (pin 8)
"N/C" (pin 7)
"LDO 3.3V" (pin 6)
"3.3V" (pin 5)
"GND" (pins 1-4)

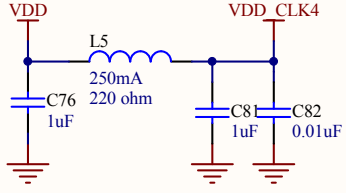


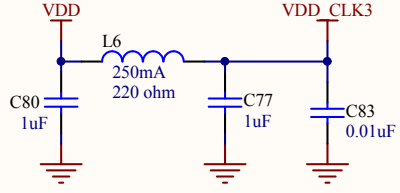
Layout Note: LED Legend is "5V IN"

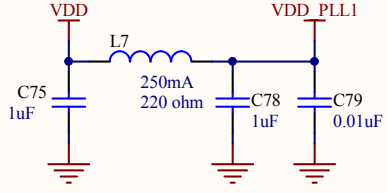
Note: LDO output voltage
Vout 1V*(1+R_hi/R_lo) = 3.30V

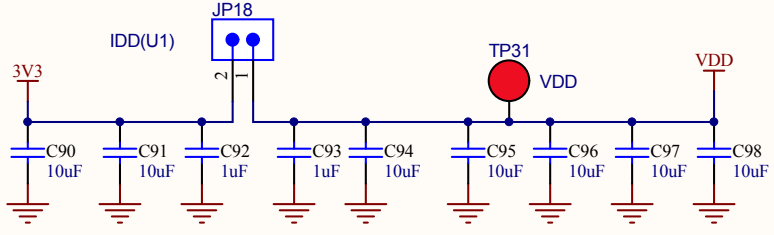
Note: Remove 0R resistor when applying an external 3.3V power supply to the 3V3 input.

Layout Note: LED Legend is "3.3V"

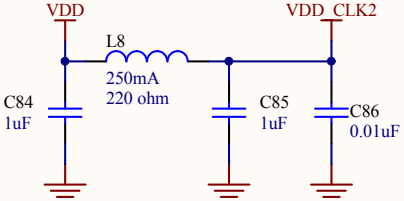


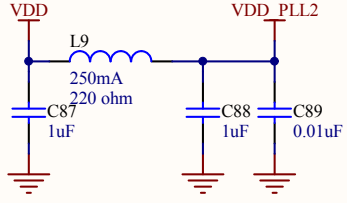


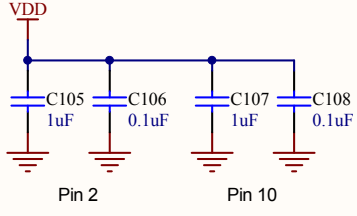


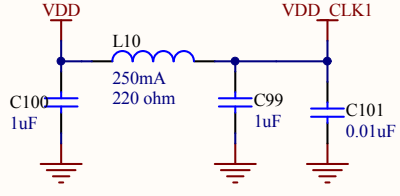


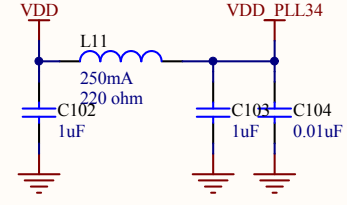
Layout Note: Distribute caps around the 4 sides of LMH1983 for decoupling the VDD power supply plane.



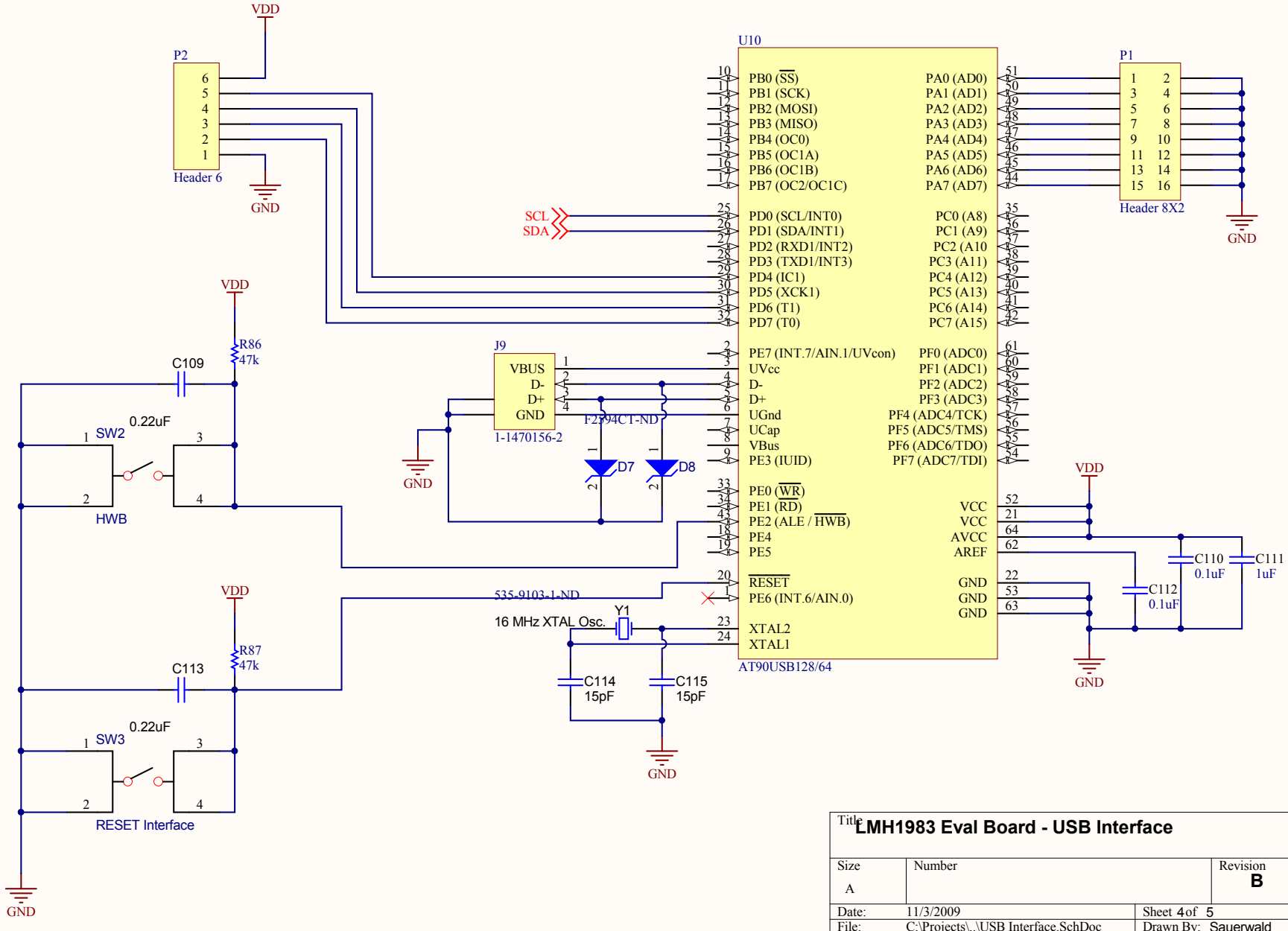




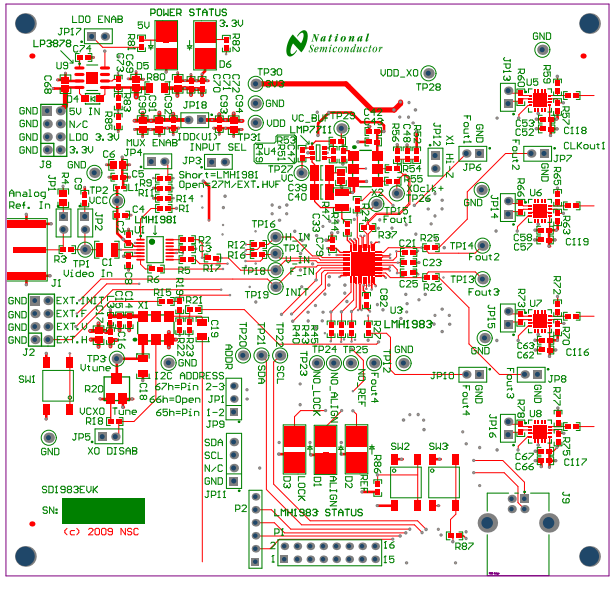




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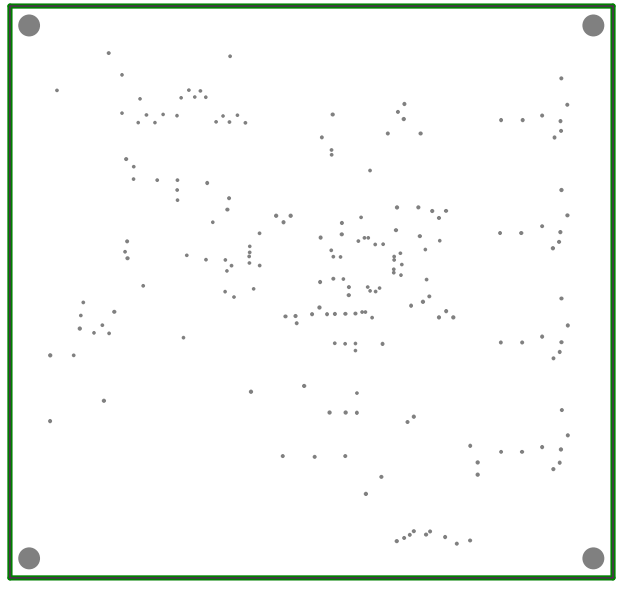


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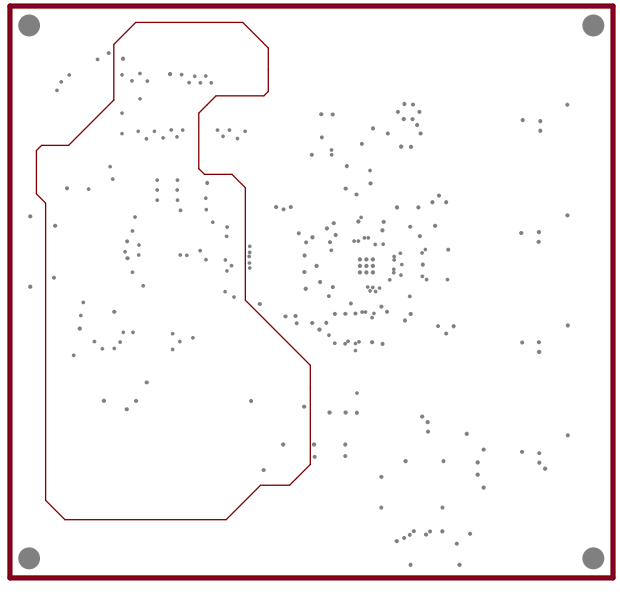


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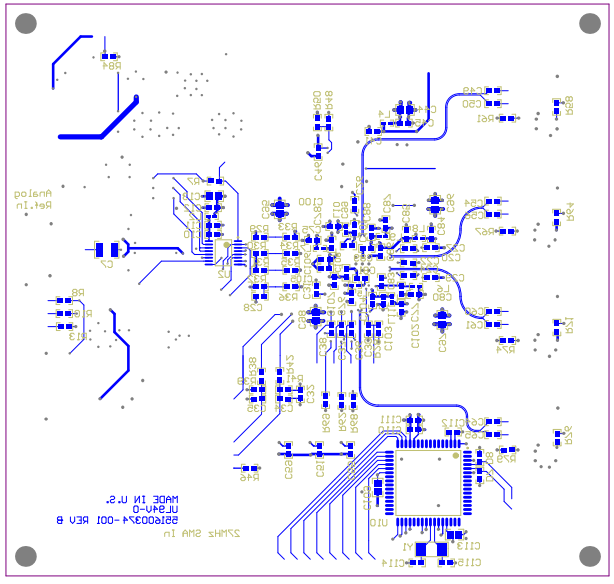
Top Overlay



Layer 2

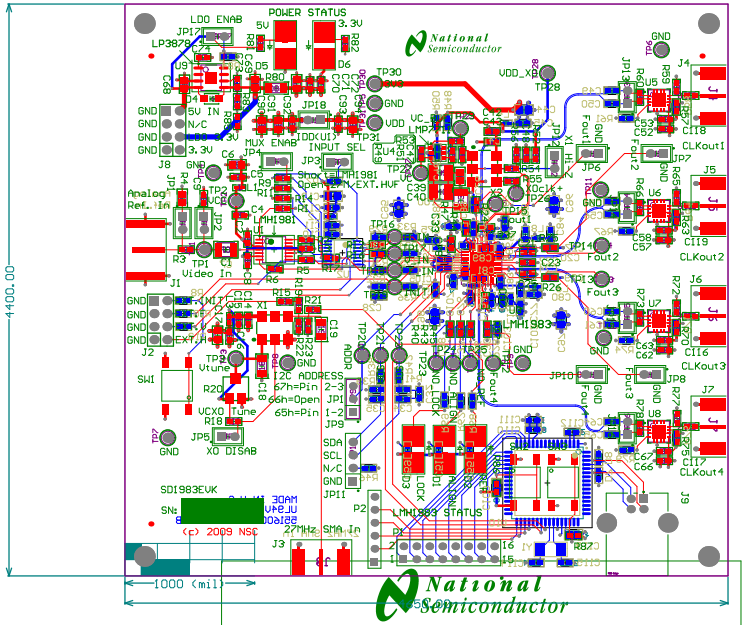


Layer 3



880

Bottom Dagerray



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ALL ARTWORK VIEWED FROM TOP SIDE	
BOARD NAME	LMH1983SQEVAL
ARTWORK #	880600374 -100 REV B
LAYER NAME	Top Overlay, Top Solder, Top, Bottom, Bottom Solder, Bottom
PLOT NAME	Multilayer Composite Print
PRINT DATE	11/3/2009 5:49:29 AM

Update the notes below per your unique requirements.

The Stackup Legend below this statement is for your reference. If you change the stackup, you need to change the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

Layer Name	Gerber Material	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		0.40mil	Solder Resist	3.50	
Plane Layer	(.GP2)	1OZ				
			4.80	FR-4		PREPREG
Plane Layer	(.GP3)	1OZ				
			47.80mil	FR-4	4.80	CORE
Plane Layer	(.GP4)	1OZ				
			4.80	FR-4		PREPREG
Plane Layer	(.GP5)	1OZ				
			0.40mil	Solder Resist	3.50	
Bottom Solder Mask	(.GBS)					

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: PER IPC-4101/21
   - 1A. LAMINATE: HIGH-TEMPERATURE FR-4
   - 1B. COPPER THICKNESS: 1 OZ +/-.0005 INCH OUTER LAYERS, 1 OZ +/-.0005 INCH INNER LAYERS.
   - 1C. ALL CONDUCTOR LAYERS MUST BE SPACED PER DETAIL A.
   - 1D. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER. ANY TIN, TIN/LEAD OR GOLD PLATING, SOLDERMASK AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN FINISHED BOARD THICKNESS.
   - 1E. ALL INNER LAYERS MUST BE OXIDE COATED.
2. ALL CONDUCTOR PATTERNS AND PADS MUST BE REGISTERED WITHIN +/-.005 INCH FROM TRUE POSITION.
3. ETCH TOLERANCES:
   - 3A. ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0015 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
   - 3B. ALL INTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0010 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
4. DRILL TOLERANCES AND HOLE SIZES ARE FOR FINISHED BOARD:
   - ALL PLATED THROUGH HOLES TO .080 INCH ARE +/- .003 INCH.
   - ALL PLATED THROUGH HOLES OVER .081 INCH ARE +/- .005 INCH.
   - ALL NON-PLATED THROUGH HOLES ARE +/- .005 INCH.
5. ALL HOLES MUST BE REGISTERED WITHIN +/-.003 INCH FROM TRUE POSITION.
6. MINIMUM ANNULAR RING MUST BE .002 INCH.
7. PLATING:
   - 7A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0015 INCH MAX. THICK COPPER.
   - 7B. FINISH: ELECTROLESS NICKEL/IMMERSION GOLD (ENIG).
8. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
9. SOLDERMASK: PER IPC-SM-840
   - 9A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
   - 9B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
   - 9C. COLOR GREEN AND SOLVENT FREE.
   - 9D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK MEASURED OVER COPPER PLATING.
10. SILKSCREEN TOP AND BOTTOM SIDES USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON GOLD AREAS, ON PADS OR IN HOLES.
11. ROUTE BOARD OUTLINE, PER DRAWING DIMENSIONS.
12. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE AND ANY OTHER IDENTIFICATION MARKS ON BOTTOM SIDE ETCH (APPROXIMATELY WHERE SHOWN, IF SHOWN)
13. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
14. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC. MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
15. FINISHED BOARD MUST MEET UL94V-0 RATING AND RoHS COMPLIANCE.
16. DOCUMENTATION THAT MUST BE DELIVERED WITH BOARDS:
    - 16A. CROSS SECTION REPORT (SPACING BETWEEN COPPER LAYERS AND COPPER THICKNESS)
    - 16B. ELECTRICAL TEST CERTIFICATION OF COMPLIANCE (ACCORDANCE WITH IPC-ET-652 CLASS II)
    - 16C. RoHS CERTIFICATE OF COMPLIANCE.
    - 16E. IMPEDANCE REPORT (REQUIRED IMPEDANCE TRACES PER NOTE 19)
17. ALL TOP AND BOTTOM SINGLE ENDED MICROSTRIP IMPEDANCE OF .006 INCH TRACES ON LAYERS 1 AND 4 SHALL BE 50 OHMS +/- 10% DIFFERENTIAL IMPEDANCE OF .004 INCH TRACES WITH .006 INCH SPACING BETWEEN TRACES ON LAYERS 1 AND 4 SHALL BE 100 OHM +/-10% TRACE WIDTH AND LAYER SPACING MAY BE CHANGED TO ACCOMMODATE FABRICATION PROCESS BUT PRIOR APPROVAL IS REQUIRED BEFORE TRACE WIDTH OR LAYER SPACING CHANGES ARE MADE.

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	PROJECT TITLE: .PRJ_Title	
REV: -001 REV B / PRINT DATE: 11/3/2009	DESIGNED FOR: .PRJ_Customer	
SCALE: 1.00	PADC NUMBER: .PRJ_PADC	FAB DRAWING NUMBER: 551600374
FILE NAME: LMH1983.PcbDoc		ALTIUM DESIGNER VERSION: 8.3.0.16776

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