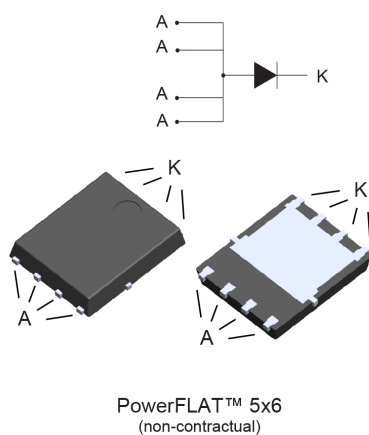


50 V, 20 A field effect rectifier



Features

- ST patented rectifier process
- Stable leakage current over reverse voltage
- Low forward voltage drop
- High frequency operation
- ECOPACK®2 compliant

Applications

- Set-top box
- Battery charger
- DC / DC converter

Description

This single rectifier is based on a proprietary technology, enabling to achieve the best in class V_F/I_R for a given silicon surface.

Packaged in PowerFLAT™ 5x6, the FERD20U50 is optimized for use in rectification and freewheeling operations in switch mode power supplies.

Product status	
FERD20U50	
Product summary	
Symbol	Value
$I_{F(AV)}$	20 A
V_{RRM}	50 V
$T_{j(max.)}$	150 °C
$V_{F(typ.)}$	0.44 V

1 Characteristics

Table 1. Absolute ratings (limiting values at 25 °C, unless otherwise specified, anode terminals short circuited)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		50	V
$I_{F(RMS)}$	Forward rms current		45	A
$I_{F(AV)}$	Average forward current, $\delta = 0.5$ square wave	$T_C = 115\text{ °C}$	20	A
I_{FSM}	Surge non repetitive forward current	$t_p = 10\text{ ms}$ sinusoidal	180	A
T_{stg}	Storage temperature range		-65 to +175	°C
T_j	Maximum operating junction temperature ⁽¹⁾	PowerFlat™ 5x6	+150	°C

1. $(dP_{tot}/dT_j) < (1/R_{th(j-a)})$ condition to avoid thermal runaway for a diode on its own heatsink.

Table 2. Thermal resistance parameter

Symbol	Parameter	Max. value	Unit
$R_{th(j-c)}$	Junction to case	2.6	°C/W

For more information, please refer to the following application note :

- AN5046 : Printed circuit board assembly recommendations for STMicroelectronics PowerFLAT™ packages

Table 3. Static electrical characteristics (anode terminals short circuited)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_R^{(1)}$	Reverse leakage current	$T_j = 25\text{ °C}$	$V_R = V_{RRM}$	-	800	μA
		$T_j = 125\text{ °C}$		-	30	mA
$V_F^{(2)}$	Forward voltage drop	$T_j = 25\text{ °C}$	$I_F = 10\text{ A}$	-	0.37	V
		$T_j = 125\text{ °C}$		-	0.33	
		$T_j = 25\text{ °C}$	$I_F = 20\text{ A}$	-	0.45	
		$T_j = 125\text{ °C}$		-	0.44	

1. Pulse test: $t_p = 5\text{ ms}$, $\delta < 2\%$

2. Pulse test: $t_p = 380\text{ μs}$, $\delta < 2\%$

To evaluate the conduction losses, use the following equation:

$$P = 0.25 \times I_{F(AV)} + 0.011 \times I_{F(RMS)}^2$$

For more information, please refer to the following application notes related to the power losses :

- AN604: Calculation of conduction losses in a power rectifier
- AN4021: Calculation of reverse losses on a power diode

1.1 Characteristics (curves)

Figure 1. Average forward power dissipation versus average forward current (anode terminals short circuited)

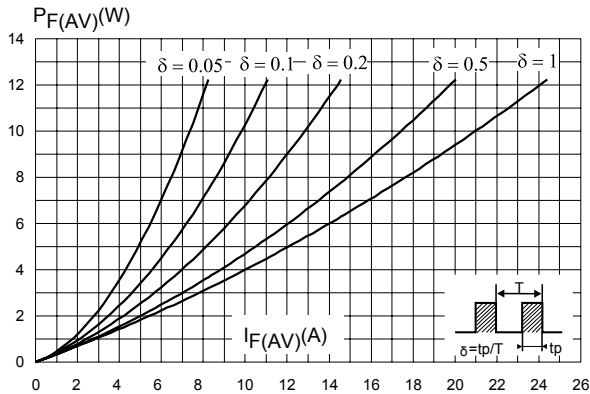


Figure 2. Average forward current versus ambient temperature ($\delta = 0.5$, anode terminals short circuited)

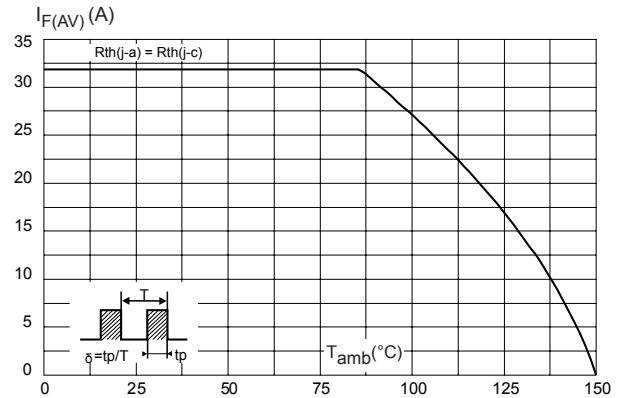


Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

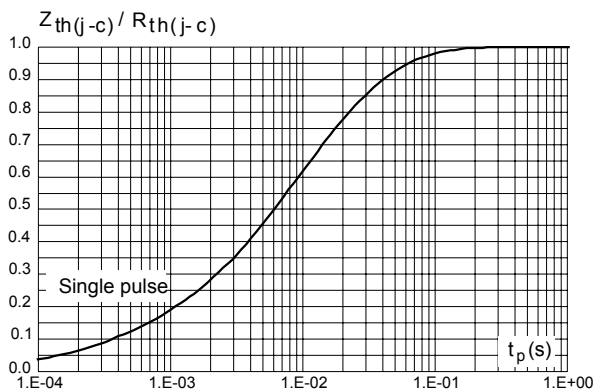


Figure 4. Reverse leakage current versus reverse voltage applied (typical values)

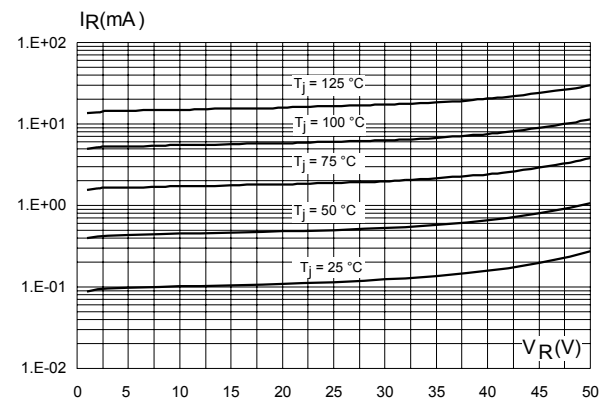


Figure 5. Junction capacitance versus reverse voltage applied (typical values)

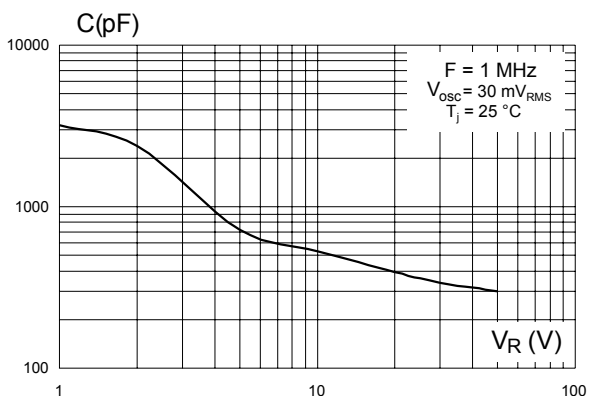


Figure 6. Forward voltage drop versus forward current (typical values, anode terminals short circuited)

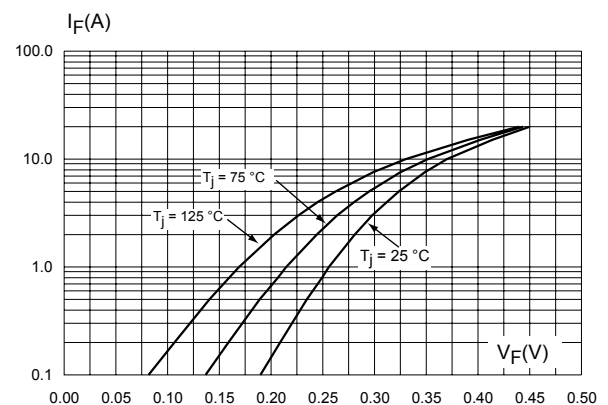
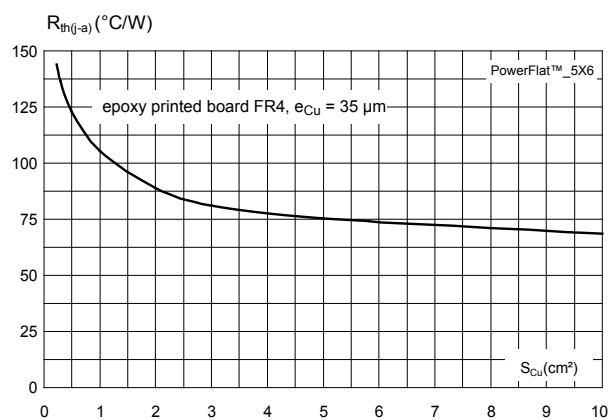


Figure 7. Thermal resistance junction to ambient versus copper surface under tab (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 PowerFLAT™ 5x6 package information

- Epoxy meets UL 94,V0
- Cooling method: by conduction (C)

Figure 8. PowerFLAT™ 5x6 package outline (non-contractual)

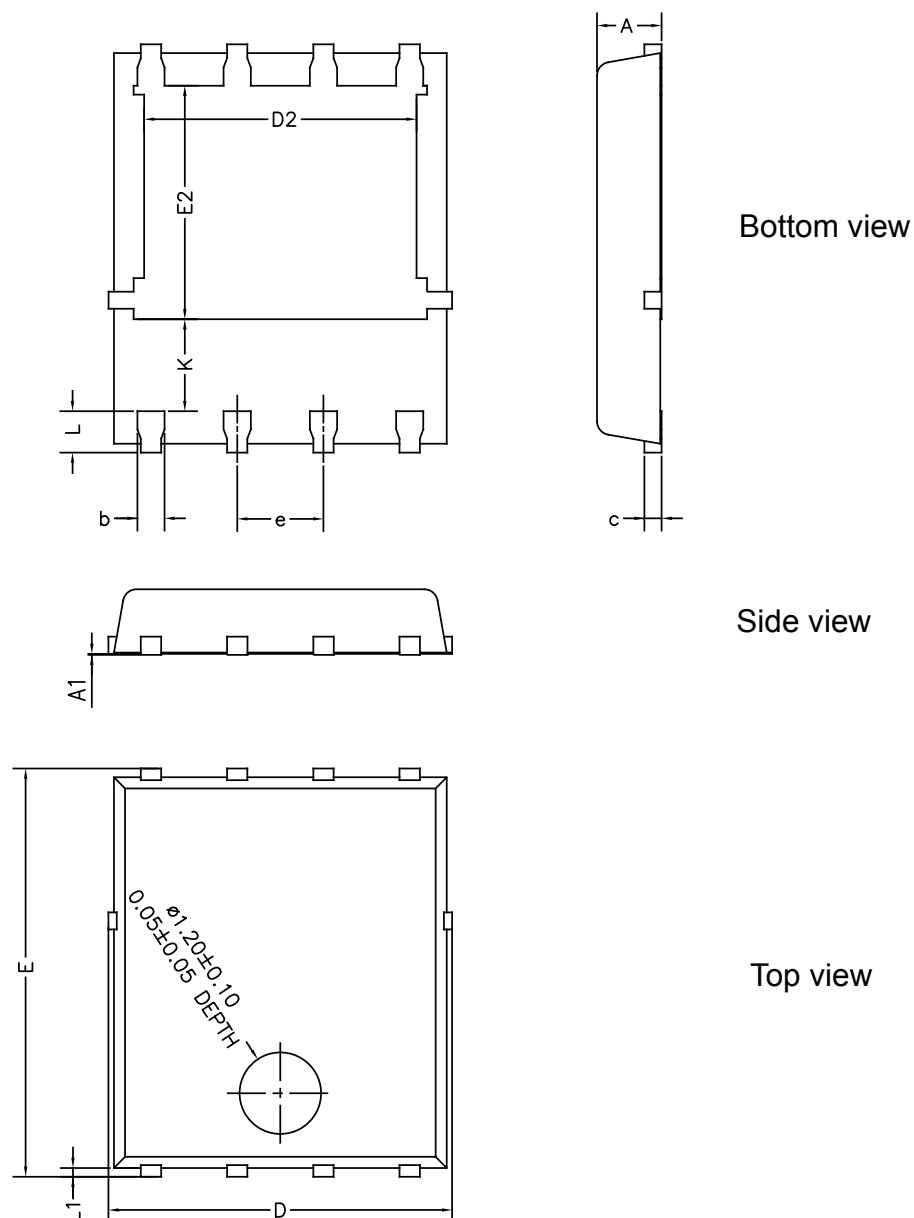
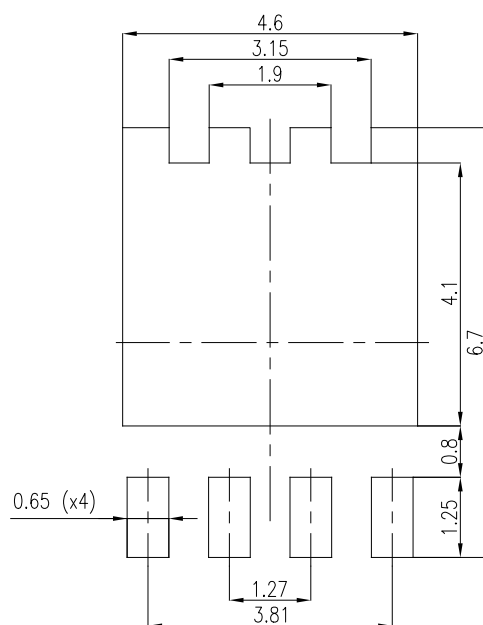


Table 4. PowerFLAT™ 5x6 mechanical data

Ref	Dimensions					
	Millimeters			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0.00		0.05	0.000		0.002
b	0.30		0.50	0.01		0.02
c		0.25			0.010	
D	4.80		5.40	0.189		0.212
D2	3.91		4.45	0.154		0.175
e		1.27			0.050	
E	5.90		6.35	0.232		0.250
E2	3.34		3.70	0.138		0.146
L	0.50		0.80	0.020		0.031
K	1.10		1.575	0.015		0.023
L1	0.05	0.15	0.25	0.002	0.006	0.009

Figure 9. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)


3 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
FERD20U50DJF-TR	FD20 U50	PowerFLAT™ 5x6	95 mg	3000	Tape and reel

Revision history

Table 6. Document revision history

Date	Version	Changes
25-Mar-2014	1	Initial release.
06-Jun-2014	2	Updated RPN
06-Aug-2015	3	Updated Table 2 and reformatted to current standard.
09-Nov-2018	4	Updated Section Cover image and Section 2.1 PowerFLAT™ 5x6 package information . Added Section Applications .
05-Feb-2019	5	Updated Figure 8. PowerFLAT™ 5x6 package outline (non-contractual) and Table 4. PowerFLAT™ 5x6 mechanical data .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved